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Collaborative PCB Design Challenges Tackled by New Cadence Partitioning Technology

Proven Cadence Allegro System Interconnect Design Platform PCB Design Technology
Continues to Extend Capabilities with Team-Based Approach

SAN JOSE, Calif—March 7, 2005—Cadence Design Systems, Inc. today announced new design-partitioning technology for the Allegro PCB Editor, extending the industry-proven technology of the Cadence® Allegro® system interconnect design platform. Cadence design-partitioning technology helps address customer demand for faster time to market and shorter design-cycle times by enabling concurrent collaboration for true team-based printed circuit board (PCB) design.

The pressure to shorten design-cycle times is heightened by the growing deployment of globally dispersed design teams. With Cadence design-partitioning technology, multiple PCB designers working concurrently on a layout share access to a single database, regardless of team proximity. Designers then can partition designs into multiple sections for layout and editing by design-team members. Designers are able to view the partitioned sections and update the design view for monitoring the status and progress of other sections. This can dramatically reduce overall design cycles and accelerate the design process to help meet project schedules.

"Cadence partitioning technology will enable us to make more effective use of our layout resources and design expertise," said Ron Dallas, Design Technology Group, Teradyne, Inc. "Design partitioning allows us to take our PCB layout to the next level to address the pressures and challenges of today's marketplace."

Manual workarounds to address design-partitioning challenges are time consuming, slow and prone to error. The new Cadence Allegro design-partitioning technology provides an automated methodology in its popular PCB Editor software for faster time to market and reduction in layout time.

"The Cadence Allegro platform is the industry-proven leader in the PCB design market," said Charlie Giorgetti, corporate vice president and general manager of the silicon-package-board business unit at Cadence. "Design partitioning eliminates the need for multiple design shifts, helps reduce time to market and design-cycle time, and addresses diverse PCB design technologies. It also bridges independent design departments and manages offsite design partners."

The new Cadence partitioning technology will be available in two new Allegro platform product offerings, Allegro PCB Design 230 and Allegro PCB Design 620. Both help optimize and accelerate high-performance, high-density interconnect PCB design. Design partitioning will be included in the Allegro SPB 15.5 release scheduled for customer shipment in June 2005.

About Cadence

Cadence is the world's largest supplier of electronic design technologies and engineering services. Cadence products and services are used to accelerate and manage the design of semiconductors, computer systems, networking equipment, telecommunications equipment, consumer electronics, and other electronics based products. With approximately 4,900 employees and 2004 revenues of approximately \$1.2 billion, Cadence has sales offices, design centers, and research facilities around the world. The company is headquartered in San Jose, Calif., and trades on both the New York Stock Exchange and Nasdaq under the symbol CDN. More information is available at www.cadence.com.

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