

FEATURES

Design Capture Technology

OrCAD Capture offers a comprehensive solution for entering, modifying, and verifying complex system designs quickly and cost-effectively. Whether used to design a new analog circuit, revise a schematic diagram for an existing PCB, or design a digital block diagram with an HDL module, OrCAD Capture allows designers to enter, modify, and verify the PCB design.

SCHEMATIC EDITING

The full-featured schematic editor enables users to place and connect parts from a comprehensive set of functional libraries. It uniquely packages the parts, ensures design integrity, and creates design netlists for any of the formats supported by Cadence.

PROJECT MANAGEMENT

The project manager enables users to collect and organize all the resources needed for the project throughout the design flow. The expanding tree structure makes it easy to organize and navigate design files, including those generated by PSpice and Cadence Allegro AMS Simulators, Cadence OrCAD Capture CIS, Cadence Allegro Design Entry CIS, and other plugins.

HIERARCHICAL DESIGN AND REUSE

OrCAD Capture boosts schematic editing efficiency by enabling subcircuit reuse—without having to make multiple copies. Using hierarchical blocks, designers simply reference the same subcircuit multiple times. Automatic creation of hierarchical ports eliminates potential design connection errors.

LIBRARIES AND PART EDITING

The library editor is accessed directly from the user interface. Users can create and edit parts in the library or directly from the schematic page without interrupting workflow. Intuitive graphical controls speed schematic part creation and editing. New parts can be created quickly by modifying existing ones.

EASY DATA ENTRY

Designers can access all part, net, pin, and title block properties or any subset and make changes quickly through the spreadsheet property editor.

PCB Editor Technology

FEATURE SUMMARY

Unlimited database	Exposed copper DRC
Netlist/crossplace/crossprobe	Interactive routing/etch editing
Padstack and symbol editor	Automatic silkscreen generation
Customizable/automated drill legend/NC output	Split plane support
Multiple via sizes, blind/buried via support	SKILL runtime, macro, and script support
Autoplace/Quickplace/Floorplanner	Variant assembly drawing creation
Dynamic shapes with real-time plowing and healing	Variant bill-of-materials generation
2-D drafting and dimensioning	IFF import
Gerber 274X, 274D artwork output generation	CAD interfaces – DXF (Ver.14), IDF (Ver. 2 and 3)
Multiple UNDO/REDO	PCB interfaces – OrCAD Layout, PADS (Ver.5), P-CAD (Ver.8)
Valor ODB++, ODB++(X) and universal viewer	Constraint manager (physical, spacing, properties, and DRC)
HTML-based reports	Manual testprep

PCB EDITING ENVIRONMENT

At the heart of the OrCAD PCB Designer Suite is OrCAD PCB Editor—an intuitive, easy-to-use, constraint-driven environment for creating and editing simple to complex PCBs. Its extensive feature set addresses a wide range of today's design and manufacturability challenges. The PCB editor provides a powerful and flexible set of floorplanning tools. Powerful shape-based shove/hug interactive etch creation/editing provides a highly productive interconnect environment. Dynamic shape capability offers real-time copper pour plowing/healing functionality during placement and routing iterations. The PCB editor can also generate a full suite of phototooling, bare-board fabrication and test outputs, including Gerber 274x, NC drill, and bare-board test in a variety of formats.

CONSTRAINT MANAGEMENT

A constraint management system displays physical and spacing rules. Each worksheet provides a spreadsheet interface that enables the user to define, manage, and validate the different rules in a hierarchical fashion. This powerful application allows designers to graphically create, edit, and review constraint sets as graphical topologies that act as electronic blueprints of an ideal implementation strategy. Once the constraints are present in the

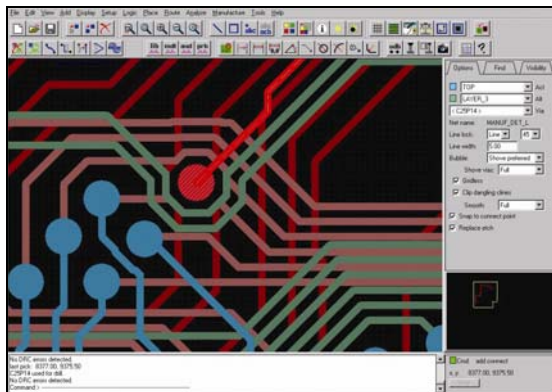
database, they are used to drive the placement and routing processes for constrained signals. The constraint management system is completely integrated with the PCB editor.

FLOORPLANNING AND PLACEMENT

The constraint and rules-driven methodology drives a powerful and flexible set of placement capabilities, including interactive and automatic component placement. The engineer or designer can assign components or subcircuits to specific “rooms” during design entry or floorplanning. Components can be filtered and selected by reference designator, device package/footprint style, associated net name, part number, or the schematic sheet/page number. With thousands of components on today’s boards needing precise management, real-time assembly analysis and feedback increases the designer’s productivity and efficiency by placing components to corporate or EMS guidelines.

INTERACTIVE ETCH EDITING

The interactive routing capability of the PCB editor provides powerful, interactive features that deliver controlled automation to maintain user control, while maximizing routing productivity. Real-time, shape-based, any angle, push/shove routing enables users to choose between “shove-preferred,” “hug-preferred,” or “hug-only” modes. Shove-preferred mode allows users to construct the optimum interconnect path while the real-time, shape-based router takes care of dynamically pushing obstacles. Routes will automatically jump over obstacles such as pins or vias. The hug-preferred mode is the perfect solution when a databus needs to be constructed. In hug-preferred mode, the router contour follows other interconnect as a priority and only pushes aside or jumps obstacles when there is no other option. The hug-only option performs like the hug-preferred mode, but without the push-and-shove aggression on other etch objects. The real-time, embedded, shape-based routing engine optimizes the route by either pushing obstacles or contour-following obstacles while dynamically jumping vias or component pins.



Dynamic push-and-shove capabilities make interactive editing easy

DYNAMIC SHAPES

Dynamic shape technology offers real-time copper pour plowing/healing functionality. Shape parameters can be applied at three different levels. Parameters are structured into global, shape instance, and object-level hierarchies. Traces, vias, and components added to a dynamic shape will automatically plow and void through the shape. When items are removed, the shape will automatically fill back in. Dynamic shapes do not require batch autovoicing or other post-processing steps after edits are made.

PCB MANUFACTURING

A full suite of photo-tooling, bare-board fabrication and test outputs, including Gerber 274x, NC drill, and bare-board test in a variety of formats can be generated. More importantly, OrCAD PCB Editor supports the industry initiative towards Gerber-less manufacturing through its Valor ODB++ interface that also includes the Valor Universal Viewer. The ODB++ data format creates accurate and reliable manufacturing data for high-quality, Gerber-less manufacturing.

PCB Autorouter Technology

FEATURE SUMMARY

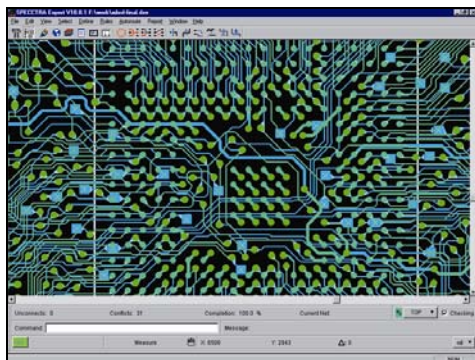
6 signal layer limit	Interactive via search
Shape-based or gridded autorouting	Interactive routing with shoving and plowing
SMD fanout	Interactive floorplanning
Trace width by net and net classes	Online design rule checking
Staggered pin support	Flip, rotate, align, push, and move components
45-degree ECO routing	Placement density analysis
Memory pattern routing (SMD or through-hole)	

AUTOMATED INTERCONNECT ENVIRONMENT

Increased design complexity, density, and high-speed routing constraints make manual routing of PCBs difficult as well as time-consuming. SPECCTRA for OrCAD solves the challenges of complex interconnect routing with powerful, automated technology. This robust, production-proven autorouter includes a batch routing mode with extensive user-defined routing strategy control as well as built-in automatic strategy capability. An interactive routing environment—that features real-time interactive trace pushing and shoving—aims in making quick edits to traces. An interactive placement environment with extensive floorplanning functionality and complete component placement features eliminates the need to switch applications to make placement changes to optimize routing. By using the auto-interactive floorplanning and placement capability, designers can improve routing quality and productivity, which are directly related to component placement. In addition, an extensive rule set allows designers to control a wide range of constraints from default board-level rules to rules by net/net class, and regions rules.

AUTOROUTING

SPECCTRA for OrCAD provides powerful, shape-based autorouting with fast, high completion rates. Its routing algorithms are designed to handle a wide range of PCB interconnect challenges—from simple to complex, low density to high density—as well as the demands of high-speed constraints. These powerful algorithms make the most efficient use of the routing area. To find the best routing solution for each case, the router uses a multi-pass, cost-based, conflict resolution algorithms. An extensive rule set provides the capability for physical and electrical constraint control. The extensive rule set has the flexibility to handle specific rules on various routing elements in a design. Users can define rules required to meet common physical/spacing net rules and class rules.



Advanced autorouting technology effectively handles dense, highly constrained designs

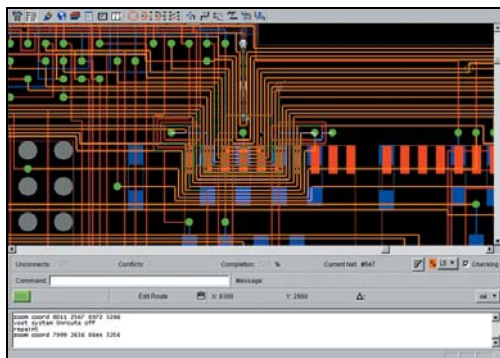
INTERACTIVE ROUTE EDITING

The SPECCTRA for OrCAD route editor simplifies and streamlines the etch editing process. As new conductors are routed, the plowing feature automatically pushes aside existing conductors and routes around pins. Using the shoving feature, designers can move conductor segments or vias against existing traces and push ahead over other pins and vias if necessary. A ghosting feature makes it easy to evaluate “what if” scenarios. As a conductor segment or via is moved under cursor control, the surrounding conductor is shoved and displayed dynamically so the adjusted routing can be evaluated before accepting a final configuration.

The route editor is ideal for dense, multilayer boards where legal via sites can be difficult to find. Vias are positioned by simply clicking twice at a chosen location. If possible, the chosen site is made available by shoving conductors aside on layers as needed. If not, the route editor displays a design rule violation and shows the legal via sites nearby. In addition, the copyroute feature, which allows an existing route to be copied to complete unrouted bus connections, simplifies bus construction.

PLACEMENT EDITING

The placement editor allows designers to quickly place components while simultaneously evaluating space, logic flow, and congestion before beginning the route or as needed during the routing process. The *Move* mode allows components to be flipped, rotated, aligned, pushed, and moved either as individual components or as a group. The location can be accepted or rejected by the user. Components can be placed by directly entering their X-Y locations. This capability is particularly useful for placing connectors and components with fixed locations. Density analysis graphically displays circuit congestion by overlaying the PCB with a color map showing a range of areas—from highly congested areas to lightly congested. This helps determine where placement adjustments could be made to relieve congestion and improve routing completion.



Placement editor allows you to evaluate space, logic flow, and congestion at all stages of the routing process

PCB EDITOR INTEGRATION

The PCB routing technologies are tightly integrated with the PCB editor. Through the PCB editor interface, all design information and constraints are automatically passed to the router. Once the route is completed, all route information is automatically passed back to the PCB editor.

Optional Advanced Simulation Technology

PSpice A/D is a full-featured analog simulator with support for digital elements to help solve virtually any design challenge—from high-frequency systems to low-power IC designs. The powerful simulation engine integrates easily with Cadence PCB schematic entry solutions, improving time to market and keeping operating costs in check. An interactive, easy-to-use graphical user interface provides complete control over the design process. Availability of resources such as models from many vendors, built-in mathematical functions, and behavioral modeling techniques make for an efficient design process.

FEATURE SUMMARY

Design entry and editing	Model editing
Stimulus creation	Behavioral modeling
Circuit simulation	Magnetic parts editor
Mixed analog/digital simulation	Encryption
Graphical results and data display	SLPS integration (optional)
Model library	Checkpoint restart

SYSTEM REQUIREMENTS

- Pentium 4 (32-bit) equivalent or faster
- Windows XP Professional, Vista Enterprise
- Minimum 512MB (1G or more recommended for XP and Vista Enterprise requirements)
- 300MB swap space (or more)
- CD-ROM drive
- 65,000 color Windows display with minimum 1024 x 768 (1280 x 1024 recommended)

SALES, TECHNICAL SUPPORT, PRICING AND TRAINING

The OrCAD product line is owned by Cadence Design Systems, Inc. and supported by a worldwide network of Cadence Channel Partners.

For sales, technical support, pricing, or training information contact EMA, a Cadence Channel Partner:

EMA Design Automation • 225 Tech Park Drive, Rochester NY 14623
Tel: 877.362.3321 • eMail: info@ema-eda.com • web: www.ema-eda.com