



## **CADENCE PRODUCTIVITY FOR NEXT-GENERATION PCB DESIGN WITH NEW ALLEGRO PLATFORM**

### **Allegro Delivers Advanced Constraint-Driven PCB Flow and Global Routing To Improve Ease-of-Use, Productivity, Collaboration, Scalability, and Accuracy**

**SAN JOSE, Calif., May 15, 2007**

Cadence Design Systems, Inc. (NASDAQ: CDNS), the leader in global electronic-design innovation, today announced new product and technology enhancements within the Cadence® Allegro® system interconnect design platform for printed-circuit board (PCB) design. The enhanced platform, which includes Global Route Environment technology, establishes a unique paradigm for PCB designers, offering significant new capabilities for constraint-driven design, as well as new technology and enhancements to improve usability, productivity and collaboration among design teams in the IC, package, and board domains.

"As supply voltages go down and current needs increase, package and IC characteristics must be considered while designing Power Delivery Networks on PCB systems," said Xiangzhong Jiang, SI manager at Huawei Technologies. "With the enhancements in Allegro PCB PI technology, we are able to plug in package models, on-die current profile, and die capacitance - improving our accuracy without sacrificing simulation performance."

Today, engineering teams face unprecedented challenges in designing and managing the overall system interconnects of today's complex electronic designs. As the average PCB size decreases, the number of device pin counts, the frequencies of designs, and the complexity of design constraints increase. This ongoing challenge is making traditional approaches to PCB design obsolete. Building on Cadence PCB market segment leadership, the new Allegro platform offers a new paradigm in PCB design by offering a flow and methodology that adapts to and overcomes these increasing complexities.

"The new Allegro platform release introduces many new productivity features that will prove advantageous for designers like me," said Vincent Di Lello, senior PCB designer, Kaleidescape Canada, Inc. "Features like physical and spacing constraints, noun-verb function selection mode, expanded RMB functions, open GL, and numerous visual enhancements will greatly increase a designer's output and provide a much more user-friendly design environment."

The Cadence Allegro platform is the leading physical and electrical constraint-driven PCB layout and interconnect design system. It has been updated to include the most advanced routing technology and a new methodology for physical and spacing constraints using the Cadence Constraint Management System, a common cockpit which provides constraint management throughout the entire PCB flow. Other updates include support for algorithmic modeling for advanced serial-link design, improved circuit simulation, seamless scalability with Cadence OrCAD® products, enhanced collaboration, and a new user-interface for improved

productivity and usability. This release of the Allegro platform also offers significant new functionality for signal integrity (SI) and power integrity (PI).

“Being our most significant PCB release in many years, we have worked with many customers to meet their requirements so they can solve their most challenging design problems,” said Charlie Giorgetti, corporate vice president, product marketing at Cadence. “Our ability to develop and deliver innovation for our customers clearly is a visible commitment to the PCB market segment.”

### **Next-Generation PCB Design Flow**

The new release of the Cadence Allegro platform features new technologies for hierarchical planning and global routing, and improved capabilities for advanced constraint-driven design. The platform also offers greater usability through a new use-model. Allegro and OrCAD PCB design suites include new PCB editing technologies to improve designer efficiency, as well as productivity.

### **Improved Design Creation and Simulation**

This release of the Allegro platform allows hardware designers to shorten development time to create designs with a large number of differential signals by 60 percent using the latest version of Allegro System Architect. Cadence further enhances analog simulation by adding substantial improvements in performance and convergence to Cadence PSpice® technology.

### **Advanced Constraint-Driven Design**

The Allegro platform’s constraint-management system offers an advanced new capability to reduce creation time for designs with advanced I/O interfaces, such as PCI Express, DDR2, SATA, and others. The system gives designers the power to create and specify constraints using formulas that reference other objects. The constraint-management system includes a component workbook, in addition to physical and spacing constraints, providing one location for design constraints, design-rule checks, and properties.

### **Improved Productivity and Simulation Accuracy**

This release of the Allegro platform offers significant new functionality in Allegro PCB SI and PCB PI. Both options offer new functionalities that shorten interconnect design time and improve product performance and reliability. These capabilities include significant improvements for serial-link design, allowing users to accurately predict bit-error ratio for channels with algorithmic transceivers above 6Gbps. Additionally, channel compliance with statistical analysis allows users to evaluate legacy channels for possible use with high-data-rate transceivers.

The Allegro PCB PI option consumes package parasitics, die capacitance, and switching currents from IC and IC package design tools to accurately model a complete power-delivery system. In conjunction with Static IR Drop analysis, Allegro PCB PI users can quickly determine if power-distribution systems can maintain reference voltages within specification.

**Availability**

The latest version of the Allegro platform is scheduled for release in June 2007. The Global Route Environment, showcased at PCB West, is included in the Allegro PCB Design GXL product.

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**About Cadence**

Cadence enables global electronic-design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence software and hardware, methodologies, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. Cadence reported 2006 revenues of approximately \$1.5 billion, and has approximately 5,200 employees. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services is available at [www.cadence.com](http://www.cadence.com).

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