



INSIDE CONTACTLESS ADOPTS CADENCE VIRTUOSO MULTI-MODE SIMULATION TO SPEED SOC DESIGN VERIFICATION

Virtuoso UltraSim Full-Chip Simulator, with High-Performance Digital Solver and Flexible Licensing, Saves INSIDE Contactless 20 Percent in Development Time

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Cadence Design Systems, Inc. (NASDAQ: CDNS), the leader in global electronic-design innovation, announced today that INSIDE Contactless adopted the Cadence® [Virtuoso® UltraSim Full-Chip Simulator](#), a component of [Virtuoso Multi-Mode Simulation](#) with a high-performance digital-solver technology, for the verification of its current and next-generation contactless and Near Field Communication (NFC) system-on-chip (SoC) designs. INSIDE Contactless, a fabless company and leader in contactless technology providing high-performance chipsets for secure, fast and reliable transactions with electronic identification, has saved 20 percent in development time since adopting this new technology.

The high-performance digital-solver technology in Virtuoso UltraSim is an innovation from Cadence that provides unparalleled accuracy for full-chip verification of SoC designs with large custom digital blocks. Fast and accurate design verification is a critical success factor for INSIDE Contactless. To stay competitive, the company must develop contactless and NFC SoC designs within narrow time-to-market windows.

INSIDE Contactless benefited from the fully integrated custom IC flow within the Cadence Virtuoso custom design platform, as well as the platform's flexible Virtuoso Multi-Mode Simulation token licensing model. This model offers users a choice among best-in-class Virtuoso Multi-Mode Simulation technologies: [Virtuoso Spectre® Circuit Simulator](#), [Virtuoso Spectre RF Simulation Option](#), Virtuoso UltraSim Full-Chip Simulator, and [Virtuoso AMS Designer](#). As a result, INSIDE Contactless can address all of its simulation needs as designs move from block-level to full-chip verification.

"Using the Virtuoso UltraSim Simulator with high-performance digital-solver technology ensured that we were able to complete full-chip verification, helping us cut the time to market for our Near Field Communication and Contactless SoC designs," said Michel Martin, IC design manager at INSIDE Contactless. "This success, the tight integration into [Virtuoso Analog Design Environment](#) and the Virtuoso Multi-Mode Simulation token-based licensing model made our decision to adopt the Cadence Virtuoso UltraSim Simulator very easy."

"More than 100 of our customers currently deploy Cadence Virtuoso UltraSim for full-chip verification of their complex analog, mixed-signal and custom digital designs. With high-performance digital-solver technology, Virtuoso UltraSim now performs 10 times faster than ever before," said Charlie Giorgetti, corporate vice president, Product Marketing, at Cadence. "This performance improvement enables customers, like INSIDE Contactless, to reduce full-chip SoC verification times and accelerate their time to market. With the latest Virtuoso Multi-

Mode Simulation technology, the Virtuoso platform provides the industry's only front-to-back custom design solution."

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About Cadence

Cadence enables global electronic-design innovation and plays an essential role in the creation of today's integrated circuits and electronics. Customers use Cadence software and hardware, methodologies, and services to design and verify advanced semiconductors, consumer electronics, networking and telecommunications equipment, and computer systems. Cadence reported 2006 revenues of approximately \$1.5 billion, and has approximately 5,200 employees. The company is headquartered in San Jose, Calif., with sales offices, design centers, and research facilities around the world to serve the global electronics industry. More information about the company, its products, and services is available at www.cadence.com.

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