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## **EMA Announces TimingDesigner 9.2 with New Interface to Cadence Allegro PCB SI Technology**

Rochester, NY (August 18, 2009) – EMA Design Automation™ ([www.ema-eda.com](http://www.ema-eda.com)), one of the world's largest Electronic Design Automation Value Added Resellers, today announced the availability of EMA TimingDesigner® 9.2, which interfaces with the Cadence® Allegro® PCB Signal Integrity (SI) technology providing users with a complete SI and timing design environment. The TimingDesigner integration with Allegro PCB SI allows customers to do a full signal integrity and timing analysis early in the design phase, with best in class timing reporting technology to quickly and accurately manage timing paths. Engineers can then move their boards to manufacturing with the confidence that the design will operate as expected.

“This new release of TimingDesigner brings our static timing analysis technology into the Cadence signal integrity design flow ensuring correct results while creating an automated, reusable design process,” said Manny Marcano, President and CEO of EMA Design Automation. “This is especially important as timing windows shrink and SI effects increasingly consume timing margins.”

With today's high speed designs, short timing margins, and tight project schedules, the pressure is on for first pass success. Engineering teams have

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come to depend on upfront analysis and simulation to provide an early and accurate picture of design behavior when the cost of change is the lowest. “Merging simulator-derived interconnect delay data into timing tools has previously been a manual and error-prone operation,” said Brad Griffin, Product Marketing Director at Cadence. “With this integrated environment, engineers can now combine the accuracy of simulation with an interactive, comprehensive timing diagram solution to quickly determine if today’s shrinking timing margins are in spec.”

The TimingDesigner graphical interface makes developing and performing analysis on complex timing relationships easy, while enabling review of the entire signal path. Timing can be analyzed across traditional design domains (chip, package, board) allowing timing optimization at the system level. In addition, TimingDesigner 9.2 includes many new features and enhancements. For ASIC and FPGA design customers, this new version includes enhanced support for SDC generation, 65nm and below support for Altera® FPGAs, and a new interface to the Actel® Libero® development environment.

“Incorporating SI simulated delays into our timing analysis is an absolute must for us,” said Bryn Holmes, Principal Design Engineer - Hardware Engineering, Fujitsu Telecommunications Europe Ltd. “The new TimingDesigner interface allows me to accomplish in 20 minutes what used to take 3 days. Because of this, I have my entire team using TimingDesigner.”

EMA TimingDesigner 9.2 will be available late August with pricing starting at \$2,640 for a 1 year license. For more information about TimingDesigner 9.2, visit [www.ema-eda.com/TimingDesigner](http://www.ema-eda.com/TimingDesigner) or call 800-813-7494.

### **About EMA Design Automation, Inc.**

EMA Design Automation offers leading product development solutions including electrical CAD tools, mechanical CAD tools, a complete range of product lifecycle

management systems, consulting services, training, and technical support. EMA is a Cadence® Channel Partner serving all of North America, and an Autodesk® authorized value added reseller. EMA manufactures the Component Information Portal™, TimingDesigner®, and CircuitSpace™, and all are distributed through a worldwide network of value added resellers. EMA is a privately held corporation headquartered in Rochester, New York. Visit EMA at [www.ema-eda.com](http://www.ema-eda.com) for more information.

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