

Cadence OrCAD Signal Explorer

For pre- and post-layout signal integrity analysis

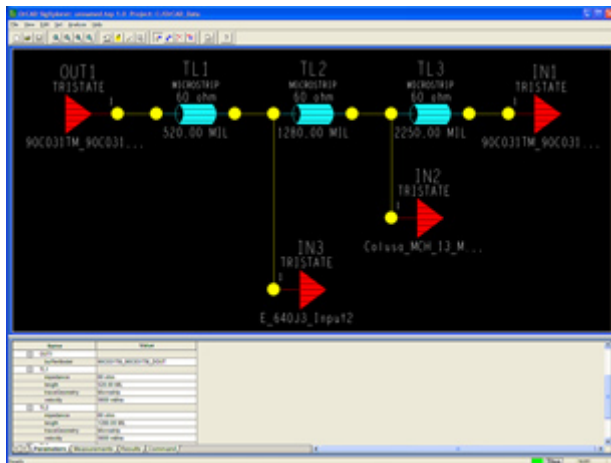
Cadence® OrCAD® Signal Explorer provides a scalable, cost-effective pre- and post-layout system interconnect design and analysis environment. Signal Explorer is tightly integrated with Cadence OrCAD PCB Editor and is a component of the Cadence OrCAD PCB Designer suites. As your level of signal integrity challenges and sophistication grows, Signal Explorer provides an easy upgrade path to the advanced Cadence Allegro PSB SI technologies.

Signal Explorer addresses the challenges created as a result of increasing design density, complexity, and faster edge rates by enabling designers to address signal integrity (SI) issues throughout the design process. This approach allows design teams to eliminate time-consuming simulate-fix-simulate iterations at the back-end of a design process. It also enables designers to maximize electrical performance while minimizing cost of the overall product by exploring topologies and models with manufacturing tolerances.

Signal Explorer allows users to weigh the trade-offs involved in routing choices (rules) that affect cost relative to electrical performance and reliability. Once developed, these optimum constraints then drive the physical layout and routing of the PCB. The integrated design and analysis environment eliminates the need to translate design databases to run simulations.

BENEFITS

- Provides cost-effective, scalable, pre- and post-layout system interconnect design and analysis
- Improves circuit performance
- Increases circuit reliability
- Eliminates the need to translate designs databases to run simulations
- Saves time via a virtual prototyping environment that is seamlessly integrated with OrCAD PCB Editor



Signal Explorer provides pre- and post-route signal integrity analysis

FEATURES

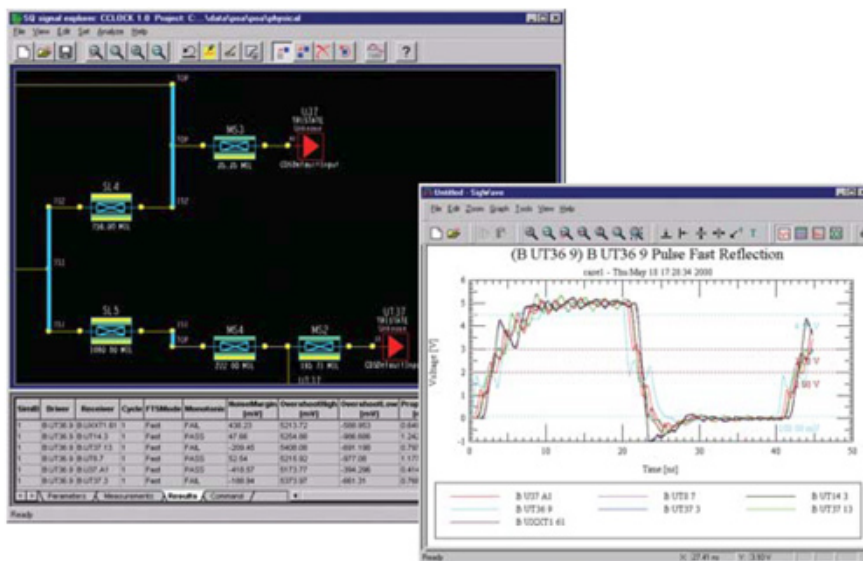
FEATURE SUMMARY

Macro modeling support (DML)	Graphical topology editor
IBIS 4.2 support	Lossy transmission lines
IBIS ICM model support	Coupled (3 net) simulation
Spectre-to-DML conversion	Differential pair exploration and simulation
HSPICE-to-IBIS conversion	

SIGXPLORESR MODULE

Signal Explorer contains a module for pre-route topology design and analysis even before a schematic is created (the SigXplorer module). This type of analysis is common at the earliest stages of the design cycle when designers assess the impact of using a new device technology or of increasing bus transfer rate. SigXplorer can be used to build and validate detailed electrical topology models and prove the viability of a new technology—before the detailed design process begins. SigXplorer is a graphical topology design environment that allows design engineers to prototype critical signals, understand sensitivity, and use “what-if” scenarios to develop optimum constraints. By performing this type of analysis at the earliest stages of the design cycle, designers can assess the impact of using a new device technology or of increasing edge rates.

Using the SigXplorer module, users can extract a net from OrCAD PCB Editor that provides an electrical view of a physical topology, including vias and changes in interconnect that affect impedance or velocity. This allows the design engineer to perform “what-if” investigations of electrical behavior without having to edit the PCB design. The engineer can investigate the effects of changing parameter values and develop an acceptable solution without disrupting the PCB design process. This ability is available at any stage of the PCB design process, from schematics, from PCB with placement through to a fully routed board.



Signal Explorer analyzes and validates topologies and interconnects to help minimize potential SI-related issues for fewer re-spins and shorter lab debug time

SIMULATION ENVIRONMENT

Signal Explorer provides a SPICE-based simulation environment for PCB SI analysis. It consists of the Tlsim simulation engine, the SigWave waveform display, the Device Modeling Language (DML), translators from other modeling formats, and a library model editing/management subsystem.

The Tlsim simulation engine combines the advantages of traditional SPICE-based structural modeling with the speed of behavioral analysis. It includes an IBIS-style behavioral driver element that models I/O behavior based on the V-I and V-T data provided by behavioral modeling techniques. By combining both structural and behavioral modeling techniques, Tlsim enables accurate and efficient modeling of complex device behavior. It includes a lossy, frequency-dependent transmission line model that accurately predicts the distributed behavior of PCB traces up to several GHz. An integrated electrical field solver is used to determine the electrical characteristics of routed etch and to create electrical models of PCB vias.

The SigWave module provides capabilities to import waveform data both directly from various standard test equipment formats as well as from the output formats of popular SI analysis tools. The SigWave waveform viewer can present simulation results in multiple formats.

- *Oscilloscope mode* allows users to turn the display of individual waveforms on and off, provides markers for use in making on-screen measurements, and allows notes to be added to the display

- *Logic-analyzer mode* presents waveforms alongside each other so that logic behavior and bus transactions are easier to observe
- *Spectrum analyzer mode* displays signal behavior in the frequency domain using one of several different FFT techniques
- *Eye-diagram mode* is useful for viewing patterns in long simulation sequences

MODEL DEVELOPMENT AND VERIFICATION

Signal Explorer includes a model integrity module that allows designers to create, manipulate, and validate models quickly in an easy-to use editing environment. Device model formats supported include:

- IBIS 4.2 External Model support for Verilog®-A, Cadence Spectre®, HSPICE, Cadence eSpice models
- IBIS ICM package and connector models
- SPICE device models
- Cadence Device Modeling Language (DML)
- Mentor/Quad XTK

A Spectre-to-DML conversion module assists in creating DML models from Spectre simulation runs. With the output of the Spectre simulation run, buffer options file, users can quickly create DML models. Model integrity identifies V-I and V-T tables for typical, maximum, and minimum corner cases from the Spectre run file. A proven, intelligent best-curve-fitting algorithm provides an accurate DML model. An HSPICE-to-IBIS conversion module allows users to create IBIS models from HSPICE simulation runs.

SYSTEM REQUIREMENTS

- Pentium 4 (32-bit) equivalent or faster
- Windows XP Professional, Vista Enterprise
- Minimum 512MB (1G or more recommended for XP and Vista Enterprise requirements)
- 300MB swap space (or more)
- CD-ROM drive
- 65,000 color Windows display with minimum 1024 x 768 (1280 x 1024 recommended)

SALES, TECHNICAL SUPPORT, PRICING AND TRAINING

The OrCAD product line is owned by Cadence Design Systems, Inc. and supported by a worldwide network of Cadence Channel Partners.

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