

# Newsletter

## TimingDesigner 9.0 Includes New Design Kits

TimingDesigner® 9.0 introduces Design Kits—pre-assembled diagrams and libraries for commonly used parts and interface protocol standards—as well as many underlying changes which give the tool a whole new look and feel.

“Since acquiring TimingDesigner a short time ago, our design team has been working diligently to add value to benefit our customers,” said Manny Marciano, President and CEO of EMA.

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### 16.0 Intro Seminars

Complimentary Seminars Coming to a City Near You [Page 3 >](#)

### New Products

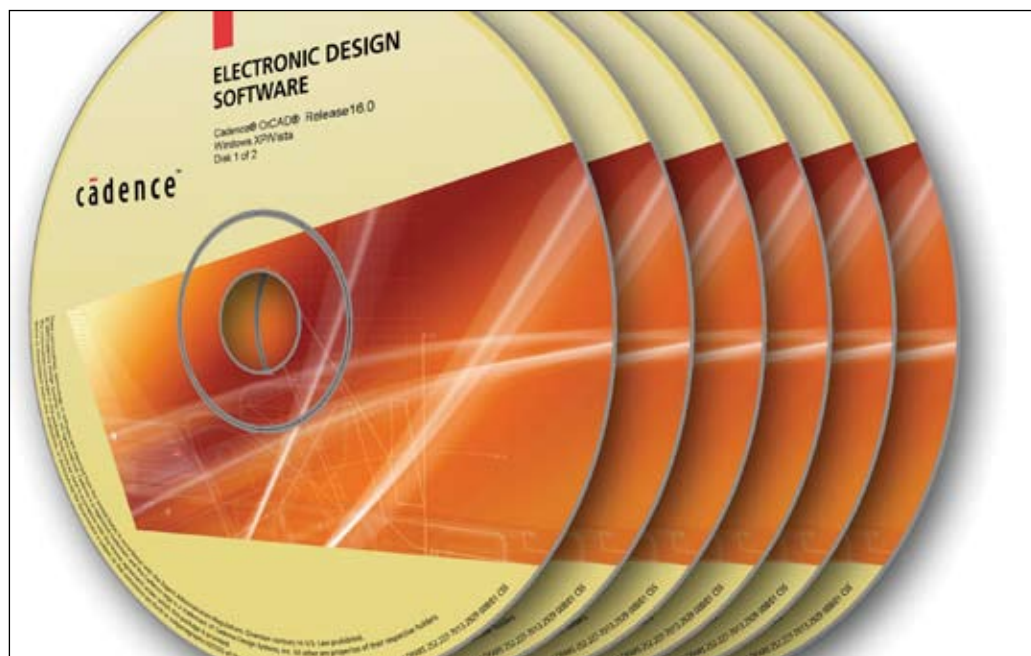
**CircuitSpace:** Automates PCB Component Placement [Page 6 >](#)

**MakeCAP:** Property Editor for Cadence OrCAD Capture [Page 7 >](#)

### White Paper

How to Effectively Manage Timing of FPGA Design Flows [Page 10 >](#)

**...and Lots More!**



## Cadence Allegro and OrCAD 16.0 Shipping in June

### Allegro 16.0 Platform

*Next-generation PCB design*

The Cadence® Allegro® platform has been significantly enhanced to improve design efficiency and designer productivity.

“Being our most significant PCB release in many years, we have worked with many customers to meet their requirements so they can solve their most challenging design problems,” said Charlie Giorgetti, corporate vice president, product marketing at Cadence. “Our ability to develop and deliver innovation for our customers clearly is a visible commitment to the PCB market segment.” [Pages 4-5 >](#)

### OrCAD 16.0 Products

*A flexible, scalable solution that adapts to your needs*

Cadence OrCAD® personal productivity tools (including Cadence PSpice®) have a long history of addressing the demands of today's competitive marketplace. Now more than ever, the affordable, high performance OrCAD product line is easily scalable with the full complement of Allegro PCB design technologies. The 16.0 release includes enhancements to Cadence OrCAD Capture, PSpice, Cadence OrCAD PCB Editor, and more.

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## OrCAD and PSpice Classroom Training

Learn the latest OrCAD and PSpice techniques from professional instructors! Reserved seating only; advance registration required. Learn more at <http://www.ema-eda.com/training/orcadtraining.aspx> >

### Salt Lake City, UT

June 4 - June 15

*OrCAD Capture, Analog Simulation with PSpice, OrCAD PCB Editor (based on Allegro Technology)*

### Detroit, MI

June 4 - June 8

*OrCAD Capture, Cadence OrCAD Layout*

### San Jose, CA

July 9 - July 20

*OrCAD Capture, OrCAD Layout, Advanced OrCAD Layout, Analog Simulation with PSpice*

### Austin, TX

August 2 - August 24

*OrCAD Capture, OrCAD Layout, Advanced OrCAD Layout, Analog Simulation with PSpice, OrCAD PCB Editor (based on Allegro Technology)*

### Albuquerque, NM

September 10 - September 28

*OrCAD Capture, OrCAD Layout, Advanced OrCAD Layout, Analog Simulation with PSpice, OrCAD PCB Editor (based on Allegro Technology)*

### Reston, VA

September 17 - October 5

*OrCAD Capture, OrCAD Layout, Advanced OrCAD Layout, Analog Simulation with PSpice, OrCAD PCB Editor (based on Allegro Technology)*

## New OrCAD 16.0 Products Provide a Flexible and Scalable Solution

To stay competitive in today's market, engineers must take a design from engineering through manufacturing with shorter design cycles and faster time to market. To be successful, you need a set of powerful, intuitive, and integrated tools that work seamlessly from start to finish.

OrCAD personal productivity tools (including PSpice) have a long history of addressing these demands. Designed to boost productivity for smaller design teams and individual PCB designers, OrCAD PCB design suites grow with your needs and technology challenges. The powerful, tightly integrated PCB design suites include design capture, librarian tools, a PCB editor, an auto/interactive router, and optional analog and mixed-signal simulator. The affordable, high-performance OrCAD product line is easily scalable with the full complement of Allegro PCB design technologies.

All OrCAD 16.0 products are now supported in Windows Vista™ Enterprise.

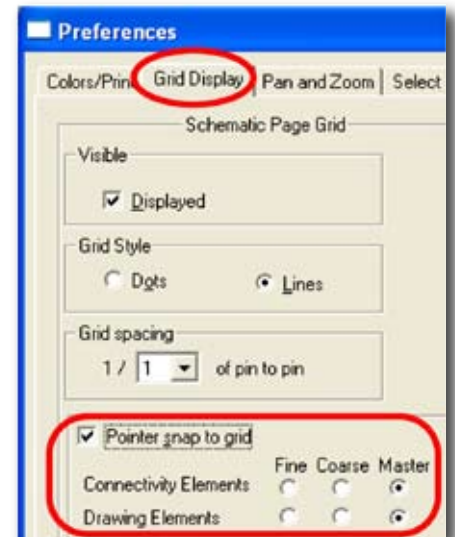
### New OrCAD and PSpice Bundle! Cadence OrCAD EE Designer Plus

Cadence OrCAD EE Designer Plus provides powerful schematic entry and simulation in one premium package. This competitively priced, complete front-end design solution includes:

- OrCAD Capture schematic entry, the world's leading schematic capture tool
- PSpice A/D for analog and mixed-signal simulation
- PSpice advanced analysis capabilities—sensitivity analysis, optimization, Smoke (component derating analysis), and Monte Carlo (yield analysis)—to automatically maximize the performance of circuits

### OrCAD Capture

- Improved support for complex hierarchical designs, including better support for occurrence properties and externally referenced designs
- Support for placing and moving text and drawing objects on fine grid independent of connectivity objects (as shown at right)
- Enhancements to archiving adds an option to include PSpice models in the archive libraries which improves the performance of archived simulation profiles
- Improved error messages and DRC engine
- Cadence Help Online Documentation System replaces CDSDoc, providing faster invocation time, advanced search capabilities, and built-in viewing window
- Usability enhancements and implementation of over 100 CCRs for improved quality and performance



Placing and moving text and drawing objects

### OrCAD Capture CIS Option

- Support for mechanical parts and assemblies in standard component information system (CIS) Bill of Materials (BOM)
- Better support for Japanese characters in CIS
- Better BOM generation for non-English operating systems

### PSpice A/D

- Improved speed for power electronics designs, especially those using ABM if-then expressions, which will simulate up to 50x faster
- CheckPoint Restart feature allows you to save the state of a transient simulation at specific times as CheckPoints. Prior to restarting, you can change component values, so if you're not getting the results you want, you can tune your circuit without having to restart from the beginning. This is particularly useful for circuits that have a long startup time like a switch mode power supply. You can simulate once to reach steady state, tune the circuit to get the final result you want, and then simulate from the beginning to verify the full simulation. In this situation, CheckPoint Restart can be a significant time saver

[More on Page 3 >](#)

## OrCAD 16.0 Products (Continued from Page 2)



Cadence Help Online Documentation System provides faster invocation time, advanced search capabilities

- Autoconvergence feature allows PSpice to automatically modify convergence options as necessary. This reduces the need for user interaction for problem circuits
- Improved transient convergence. Adaptive iteration, improvements in the step time algorithm, and an improved switch model allow PSpice to converge on certain types of problem circuits
- Run in resume mode accessible from graphical user interface (GUI)
- Minimum step size recalculation
- Usability enhancements
  - Tasks such as adding a trace, adding a plot, zooming the view, or adding a text label are now available using the right mouse button to display a context-sensitive menu in the Probe window
  - Probe window cursors now display X and Y coordinates on the status bar of the Probe window
- Improved simulation speed for E and G device-based circuits
- PSpice libraries have 120 new power devices. Updated vendor libraries include 290 new LED models
- Cadence Help Online Documentation System replaces CDSDoc, providing faster invocation time, advanced search capabilities, and built-in viewing window

### Cadence PSpice Advanced Analysis

- PSpice Advanced Analysis support for legacy PSpice models. Traditional tolerance specifications can now be used by the Monte Carlo and Sensitivity tools. This includes the use of PDF custom distributions and device and lot tolerances

### OrCAD PCB Designer (including OrCAD PCB Editor)

- OrCAD Layout translator user interface opens from within OrCAD PCB Editor
- Cadence Help Online Documentation System replaces CDSDoc, providing faster invocation time, advanced search capabilities, and built-in viewing window
- Usability enhancements made within the display canvas and to the command structure
- Redesigned color / visibility GUI
- Enhancements made to the underlying graphics system, based on OpenGL graphics engine
- Physical and spacing constraints incorporated in the Allegro constraint management system
- Interactive and automatic controls for component fanout (pin escaping)
- Context-sensitive editing paradigm built on selecting database objects first, followed by action command

### OrCAD Layout

- Cadence Help Online Documentation System replaces CDSDoc, providing faster invocation time, advanced search capabilities, and built-in viewing window
- Support for GerbTool Version 15.0
- Implementation of numerous CCRs for improved quality and performance

Please note: The OrCAD 16.0 upgrade will be provided without charge to all current OrCAD customers with active maintenance contracts. If you haven't received your updated license file and CD by July 23, 2007, or if you have additional questions, please visit: <http://support.ema-eda.com/update>

## 16.0 Seminars Feature Live Demos

See the Latest Advances in Cadence  
PCB Design Technology

DATE	LOCATION
June 20	Westford, MA
June 27	Toronto, ON
July 11	Ottawa, ON
July 12	Cleveland, OH
July 17	Austin, TX
July 18	Dallas, TX
July 19	Louisville, CO
July 24	Bellevue, WA
July 26	Albuquerque, NM
August 7	Tempe, AZ

For additional dates and locations, visit <http://www.ema-eda.com/training/seminars.aspx> >

Register now to attend this complimentary one-day seminar, coming soon to major cities across the USA. You will see live demonstrations of the newest Cadence 16.0 technologies for schematic design entry, circuit simulation, PCB design, high-speed PCB design and analysis, and global routing.

Discover how the Allegro platform improves design efficiency and designer productivity by dramatically shortening the learning curve in the adoption of new solutions and enhancing ease-of-use.

#### WHO SHOULD ATTEND

- Allegro, OrCAD, and PSpice users
- Hardware designers
- Cadence Allegro PCB SI users
- Manufacturing engineers
- CAD application engineers
- PCB designers
- Cadence OrCAD Signal Explorer users
- SI engineers
- Electrical engineers
- System designers
- Engineering managers

For more information, agendas and online registration, visit <http://www.ema-eda.com/training/seminars.aspx> >

## Cadence Schedules New Allegro 16.0 Platform Webinars

Come see the latest enhancements to the Allegro system interconnect design platform. This webinar series focuses on the new products, technology, and feature enhancements that are now part of the constraint-driven Allegro PCB design flow—and how they can improve ease of use, productivity, scalability, collaboration, and accuracy.

Discover how the Allegro platform improves design efficiency and designer productivity by dramatically shortening the learning curve in the adoption of new solutions.

### DESIGN CREATION

- Cadence Allegro System Architect GXL Improvements  
*June 28, 2007 / 10:00 a.m. PDT*
- Cadence Allegro Design Publisher Improvements  
*July 19, 2007 / 10:00 a.m. PDT*

### PCB LAYOUT AND ROUTING

- Cadence Allegro PCB Editor Improvements  
*June 12, 2007 / 10:00 a.m. PDT*
- Improvements in Constraint Manager  
*July 12, 2007 / 10:00 a.m. PDT*

### PCB SIGNAL / POWER INTEGRITY

- Cadence Allegro PCB SI Improvements  
*June 14, 2007 / 10:00 a.m. PDT*
- PCB Power Delivery System Design Improvements  
*June 20, 2007 / 10:00 a.m. PDT*

For more information, please visit [http://www.cadence.com/webinars/webinars.aspx?xml=allegro\\_16\\_0\\_webinar\\_series&CMP=NLC-MJ7055940997](http://www.cadence.com/webinars/webinars.aspx?xml=allegro_16_0_webinar_series&CMP=NLC-MJ7055940997) > or send an email to [events@cadence.com](mailto:events@cadence.com) >

## Allegro 16.0 Platform: Enabling Technology for Next-Generation PCB Design

The Allegro platform is the leading physical and electrical constraint-driven PCB layout and interconnect system. Now, it has been updated to include a new methodology for physical and spacing constraints using the Allegro constraint management system, a common cockpit throughout the entire design flow. Other updates include support for algorithmic modeling and package parasitic, improved circuit simulation and statistical analysis, seamless scalability with OrCAD products, enhanced collaboration, and a new user interface for improved productivity and usability.

The enhanced platform, which includes Global Route Environment technology, establishes a unique paradigm for PCB designers, offering significant new capabilities for constraint-driven design, as well as new technology and enhancements to improve usability, productivity and collaboration among design teams in the IC, package, and board domains.

“Being our most significant PCB release in many years, we have worked with many customers to meet their requirements so they can solve their most challenging design problems,” said Charlie Giorgetti, corporate vice president, product marketing at Cadence. “Our ability to develop and deliver innovation for our customers clearly is a visible commitment to the PCB market segment.”

The Allegro 16.0 platform is now supported in Windows Vista Enterprise.

Discover how the Allegro platform improves design efficiency and designer productivity by dramatically shortening the learning curve in the adoption of new solutions and enhancing ease-of-use.

### Allegro PCB Editor

- Usability enhancements within the display canvas and to the command structure
- Redesigned color/visibility GUI with global and shape transparency controls
- Improved visibility, additional color support, smoother panning and zooming
- Enhancements made to the underlying graphics system, based on OpenGL engine
- Context-sensitive editing paradigm built on selecting database objects first, followed by command
- Interactive and automatic controls for component fanout (pin escaping)
- Physical and spacing constraints incorporated in the Allegro constraint management system
- Mouse wheel support actions supported will be zoom in, zoom out, and change active subclass of TOP to BOTTOM
- *Design Parameter* Editor to setup, access, change and review most often used parameters
- Application modes which automatically selects actions based on the object selected

### Allegro PCB SI

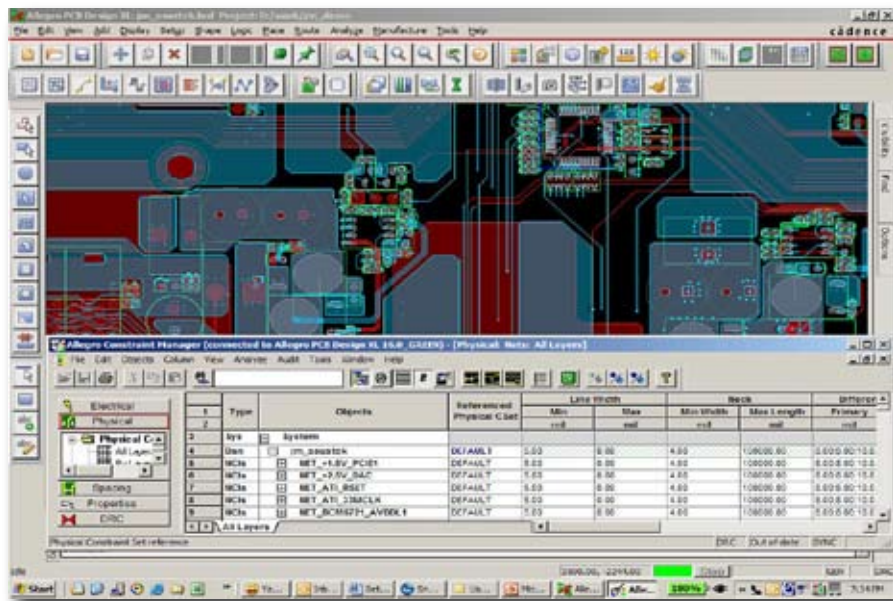
- Serial link design improvements (BER prediction, bathtub curve profiles, channel compliance through statistical analysis)
- S-Parameter DC extrapolation improvements
- Support for analytical coupled via model during topology extraction
- Improvements for post-layout analysis of source synchronous signals (usability, comprehensive simulation, slew-rate measurements, de-rating tables)
- Estimated crosstalk table generation enhancements
- Incorporating package and IC parasitics to improve accuracy without sacrificing performance

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*Interactive component fanout commands*

## Allegro 16.0 Platform (Continued from Page 4)



The Allegro 16.0 platform offers significant new capabilities for constraint-driven design

- Static IR drop analysis
- Support for IBIS ICM models and support for AC, DC threshold markers
- Improvements to Sigwave (angled markers, basic drawing functions, waveform filtering, eye-diagram preferences per waveform)

### Advanced constraints in constraint management system

- Advanced constraints for managing advanced I/O interfaces, such as PCI Express, DDR2, and SATA, using formulas, user-defined constraints, and custom measurements
- Component workbook in the Allegro constraint management system
- Custom stimulus integration

### Cadence Allegro System Architect GXL

- Accelerated design of differential connectivity (connectivity, DRCs)
- Enhanced schematic generation (cross-reference generated schematics, routing preserve, block flattening)
- Pin properties in connectivity pane

### Allegro Design Publisher

- Option of true color or B/W content rich PDF files
- Integrated attribute form to view net and component attributes
- Optimization for Adobe Reader 8.0
- Ability to view in design colors, but print in B/W

### Allegro Design Entry HDL

- Improved design navigation using *Sheet Names*
- Controlled deployment using directive locking
- Physical and spacing classes support in *Constraint Manager*
- View physical *Net* names on canvas for plotting

### Documentation

- Cadence Help Online Documentation System replaces CSDoc, providing faster invocation time, advanced search capabilities, and built-in viewing window

Note: The Cadence Allegro 16.0 upgrade is scheduled for release in June 2007 to all current Allegro customers with active maintenance contracts. To request your updated software license file go to the Cadence SourceLink<sup>SM</sup> web site, visit <http://sourcelink.cadence.com?CMP=NLC-PC2079203350> >

## CDNLive! Returns To Silicon Valley

September 10-12, 2007  
San Jose Marriott  
and San Jose Convention Center  
San Jose, CA

CDNLive! Silicon Valley 2007 is a unique opportunity to network with industry experts and other power users of Cadence technologies. At this annual event, participants exchange ideas and best practices for boosting design productivity, eliminating risk, and developing differentiated products.



### Conference Highlights

**PAPERS:** Choose from more than 80 papers addressing all aspects of logic design, verification, implementation, custom design, package design, and PCB design.

**TECHTORIALS:** Participate in a variety of interactive and hands-on techtorials to get a more in-depth look at specific Cadence products, new solutions, and feature enhancements.

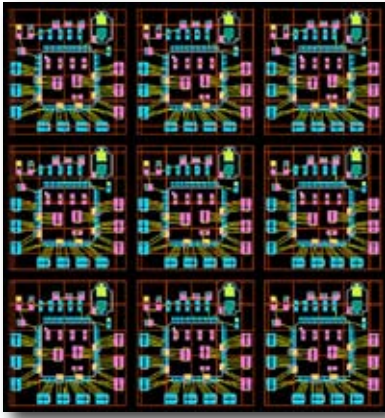
**PANELS AND FORUMS:** Find out how other designers and leading customers plan to solve their design and verification challenges and what technologies they are deploying.

**CADENCE TECHNOLOGY NIGHT:** See demonstrations of the latest Cadence products, flows, and methodologies. Talk directly with the Cadence people who develop the solutions you rely on to create innovative designs

**KEYNOTE SPEAKERS:** Hear from industry leaders who influence change and drive innovation in the global electronics marketplace.

**DESIGNER EXPO:** Explore new solutions from a variety of exhibitors, including EMA, and learn about the solutions they have developed jointly with Cadence.

Learn more about CDNLive! at <http://www.cadence.com/cdnlive/na> >



## New! Automate PCB Component Placement With CircuitSpace

Component placement is time consuming and has traditionally proven to be difficult to automate. With component counts on the rise and 10,000 part boards becoming commonplace, managing placement is a difficult task and can take months to complete.

Through a patented approach, CircuitSpace™ from DesignAdvance breaks down the current “click and drag” placement tedium and accelerates the whole design process. This unique product seamlessly integrates with Allegro PCB Design or OrCAD PCB Designer (or the PCB Editor in Allegro PCB Design and OrCAD PCB Designer) and allows users to achieve board layouts in a fraction of the time it would take to complete by hand.

CircuitSpace implements a hierarchical approach to printed circuit board design through enhanced autoclustering™ and replication technologies. It also expedites the design process through the use of template generation for global library usage across divisions, template usage with and without etch, automated layout reference designator propagation and automated change report between layout designs.

CircuitSpace improves communication between EE and layout designers; shortens design cycle timeline by weeks; and works seamlessly within existing design methodologies. Learn more at <http://www.ema-eda.com/products/other/circuitspace.aspx> >

## Tech Tips OrCAD Capture CIS

- ◆ **How can I have alternate symbols and footprints for one part in my database?**  
Enter multiple symbol and footprint names separated by a comma in the database field, and these will be displayed as a drop down list in OrCAD Capture CIS.
- ◆ **I imported my MS Access database into SQL Server. Why does OrCAD Capture CIS throw an exception when I try to place parts?**  
When an MS Access database is imported into SQL Server, the default datatype `<nvarchar>` is assigned to all fields. This needs to be changed to `<varchar>` for OrCAD Capture CIS to function properly. Database field names with special characters such as apostrophes (for example, *Manufacturer's Part Number*) are not allowed.
- ◆ **How do I deal with mechanical parts?**  
Create a page that only has your mechanical parts on it. Create an extra schematic folder in your design that is not hierarchically connected. When you wish to netlist the design, move the page to the unconnected schematic folder. This is where the page would be most of the time. When you wish to make an OrCAD Capture CIS BOM, move that page into one of the folders that are electrically connected. The OrCAD Capture CIS BOM will see the page when it is connected, while the Allegro netlist does not see the parts without pins. In Capture CIS 16.0 release you can use the *Standard CIS Bill of Materials* dialog box to generate a BOM that lists all the mechanical parts and assemblies associated with an electrical part in your design.
- ◆ **What are BOM variants in OrCAD Capture CIS?**  
Using design variants, you can manage unlimited board assembly variations without having to maintain duplicate schematics or hand-edit bills of materials. This works with complex hierarchical designs as well.
- ◆ **What actions are performed within OrCAD Capture CIS during an *Update Part Status*?**
  - 1) During an *Update Part Status*, OrCAD Capture CIS finds the part number property assigned to a schematic symbol
  - 2) OrCAD Capture CIS passes a query using the part number through the ODBC
  - 3) The ODBC returns the properties associated with that part number from the database
  - 4) The properties that are set as *Transfer to Design* in the *CIS Database Configuration .dbc* file are then compared with properties of the same name in the schematic symbol
  - 5) If a discrepancy is found, OrCAD Capture CIS alerts the user with the *Update Part* dialog box which displays the schematic properties and database properties side by side, highlighting the discrepancies in red
- ◆ **While configuring a new .dbc file, only tables are displayed in the list. Why not queries?**  
Create a .dbc file using any one table in the list. After configuring the file, click on *Setup* in the *CIS Configuration File* dialog, and all tables and queries are displayed here for further configuration.

## Tech Tips Active Parts

- ◆ **I can't find the symbols I need in the OrCAD default libraries or in my company's database. What do I do?**  
ActiveParts is an online electronic component information system available for OrCAD users. ActiveParts contains more than 2 million OrCAD Capture symbols at <http://www.activeparts.com> with the OrCAD Capture CIS *Internet Component Assistant*. By configuring your existing .dbc file using the instructions on ActiveParts you can download symbols and save them in your local library folder and database. [More Tech Tips on Page 7 >](#)

## Tech Tips OrCAD PCB Editor

### ◆ How do I translate OrCAD Layout .max files into OrCAD PCB Editor .brd files?

The translator is located in *File – Import – OrCAD Layout*. It will allow you to translate OrCAD Layout .max files to OrCAD PCB Editor .brd files. Note that OrCAD Layout padstacks are translated with internal pads differently sized than surface pads.

### ◆ How do I import a netlist from OrCAD Capture?

- 1) The Allegro .cfg file is located in the install directory. This file lists the default properties that can be passed from OrCAD Capture to OrCAD PCB Editor. Custom properties can be added to this file and passed to OrCAD PCB Editor
- 2) A *PCB\_footprint* name is required. Filter by *Cadence - Allegro Properties* in the *Properties* menu for verification
- 3) Logical and physical pin counts and pin numbers must match for a netlist to import into OrCAD PCB Editor successfully
- 4) Warnings and error messages are written to *netrev.lst* file located in the *Board* file directory during netlist import
- 5) Netlist files are written to */allegro* directory by default. The three files created are *pstchip.dat*, *pstxnet.dat*, and *pstxprt.dat*. Do not relocate these files after importing the netlist into OrCAD PCB Editor. These files need to stay in the original location for a successful backannotation

## New! Cadence Hands-On Workshops Help Accelerate the Design Cycle

Today, engineering teams in the electronics industry face unprecedented challenges in product development characterized by shorter design cycles, stringent cost constraints, new feature requirements, and smaller geometries—in order to help you accelerate through these challenges EMA is offering a variety of technology workshops.

EMA's complimentary "hands-on" technical workshops are designed to assist customers who are evaluating Cadence technology. Through a combination of lecture, live demonstration, and hands-on labs, customers can "test drive" a product and get a firsthand user-experience of the full range of the technology's capabilities.

The workshops are delivered by one of our technology Application Engineers, and each workshop is typically given in a small group of no more than 12 people. This optimizes the hands-on experience and interactive environment that workshops are intended to provide. An average workshop session is approximately four hours in length. For your convenience, our workshops are hosted onsite at your facilities. EMA supplies the computers, manuals, software, and licenses for use during the workshop.

EMA currently offers the following hands-on workshops:

- Introduction to Cadence Allegro PCB Signal Integrity Workshop
- Front to Back PCB Design Flow with Cadence Allegro Design Entry HDL Workshop
- Cadence Allegro PCB SI GXL Multi-gigahertz Design Workshop
- Cadence Encounter® Conformal® Equivalence Checker Workshop
- Cadence Virtuoso® Custom Design Platform Workshop (release IC 6.1)
- Cadence Virtuoso Digital Implementation Option Workshop (6 hour workshop)
- Cadence Virtuoso Accelerated Layout Workshop

For detailed information, please visit <http://www.ema-eda.com/training/workshops.aspx>

NEW workshops are added to the list regularly—check with your local EMA Field Sales Representative for a current list.

For more information, please contact your local EMA Field Sales Representative or contact us at [info@ema-eda.com](mailto:info@ema-eda.com).

Type	Objects	Prop Delay	
		Min	Max
Net	AD0		
PPr	AD:AR	1500 mil	3000 mil
Net	AD1		
PPr	AD:AR	1500 mil	3000 mil
Net	AD2		
PPr	AD:AR	1500 mil	3000 mil
Net	AD3		
PPr	AD:AR	1500 mil	3000 mil
Net	AD4		
PPr	AD:AR	1500 mil	3000 mil

## New! MakeCAP Property Editor for OrCAD Capture

View Properties in Constraint Manager-like Collections

MakeCAP is an easy-to-use tool for populating the OrCAD Capture Property Editor. It allows engineers working within the OrCAD Capture schematic to easily embed the high-speed properties needed to drive the Cadence Allegro constraint driven flow:

- Work from your schematic database to select nets and parts for adding properties
- Apply new properties to multiple nets and parts; edit existing properties
- Define values and objects with perfect syntax
- Organize properties for the Allegro Constraint Manager and high-speed flow
- View properties in both Schematic and Constraint Manager-style views
- Compare properties between schematic versions
- Define differential pairs and rules
- Cross-probe from MakeCAP to an open schematic in OrCAD Capture

MakeCAP is powered by the MakeGOOD AllegroCentric Constraints Engine.

Learn more about MakeCAP at <http://www.ema-eda.com/products/other/makecap.aspx> >

## EMA Trade Show Schedule Update

### Freescale Technology Forum

Orlando, FL • June 25-28, 2007

The Freescale™ Technology Forum (FTF) will feature visionary keynote speakers, hundreds of hours of in-depth technical sessions, hands-on demonstrations in an interactive Technology Lab, endless networking opportunities, and a good bit of fun. For more information and online registration, visit <https://getregisterednow.com/FTF/Register/Login.asp> >

### CDNLive!

San Jose, CA • September 10-12, 2007

CDNLive! Silicon Valley 2007 is a unique opportunity to network with industry experts and other power users of Cadence technologies. At this annual event, participants exchange ideas and best practices for boosting design productivity, eliminating risk, and developing differentiated products. For more information, visit <http://www.cadence.com/cdnlive/na> >

### SMTA International Conference

Orlando, FL • October 9-10, 2007

Lead-free, SMT, RFID, Process Control, Flip Chip, Chip Scale, BGA, RoHS Compliance, Automotive, and more...at SMTA International 2007 in Orlando, FL, you'll find the electronic interconnection solutions you need, because this event is dedicated to surface mount, advanced packaging, and related technologies. For more information and online registration, visit: <http://www.smta.org/smtai/> >

### PCB Design Conference East

Durham, NC • October 23-24, 2007 •

Visit EMA in Booth #200

PCB Design Conference East will showcase emerging technologies used in the design and manufacture of PCBs, programmables, MCMs, HDI, flex and related technologies. PCB East is also the premier conference dedicated exclusively to the educational needs of PCB engineering, design and manufacture professionals, featuring dozens of in-depth technical courses taught by industry experts. For more information, visit <http://www.pcbeast.com/> >

## TimingDesigner 9.0 to Ship in July with Flexible New Design Kits

TimingDesigner is the interactive timing analysis tool users trust to deliver fast and accurate results for timing critical designs. TimingDesigner is ideal for high-speed, multi-frequency designs where it is essential to accurately model and analyze signal relationships between devices on a board or between embedded functions on an ASIC or FPGA. It can evaluate comprehensive sets of timing alternatives and provide direction to the most complex of timing challenges, enabling designers to manage and monitor timing margins through the design process.

TimingDesigner 9.0 will ship in July with many underlying changes to accommodate the latest features of the newest operating systems as well as giving the tool a whole new look and feel. In addition, this release will introduce Design Kits: pre-assembled diagrams and libraries for commonly used parts and interface protocol standards. "Since acquiring TimingDesigner a short time ago, our design team has been working diligently to add value to benefit our customers," said Manny Marciano, President and CEO of EMA.

The TimingDesigner design kits are pre-assembled component diagrams complete with all specified libraries for speed and voltage ratings, and are intended to provide designers with a time saving head start for timing analysis of their designs. Each kit consists of all documented timing protocols associated with one or more design components, and are assembled for easy importation into TimingDesigner's Manager Window allowing quick assembly of any timing project.

These components are parameterized where applicable so that configuration options that affect timing relationships are accurately represented. Also included are the manufacturers' data sheets, assembly notes, and any other pertinent documentation.

### Design Kits Offer Flexibility

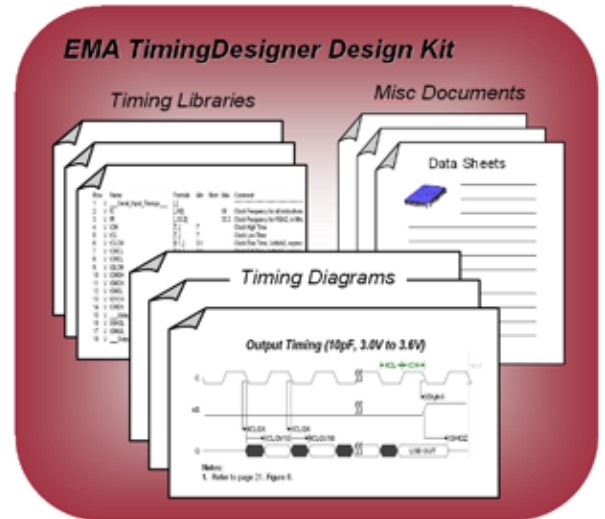
- Choose from a comprehensive list of today's most popular design components, interface specifications, and frequently requested parts
- Complete "importation" into the currently opened timing project
- Parameterized diagrams for easy adjustment of clock frequencies, configuration modes, speed ratings, and voltage varieties
- Contains manufacturers data sheet from which it was built, and other documents where applicable

TimingDesigner 9.0 offers Design Kits for processors from companies such as Intel®, Freescale™, Analog Devices and Texas Instruments. Kits are available for memory styles such as DDR, DDR2, QDR, and QDR2; Flash, SRAM, and DRAM. Interface specifications include PCI (33 and 66 MHz) PCI-Express and USB.

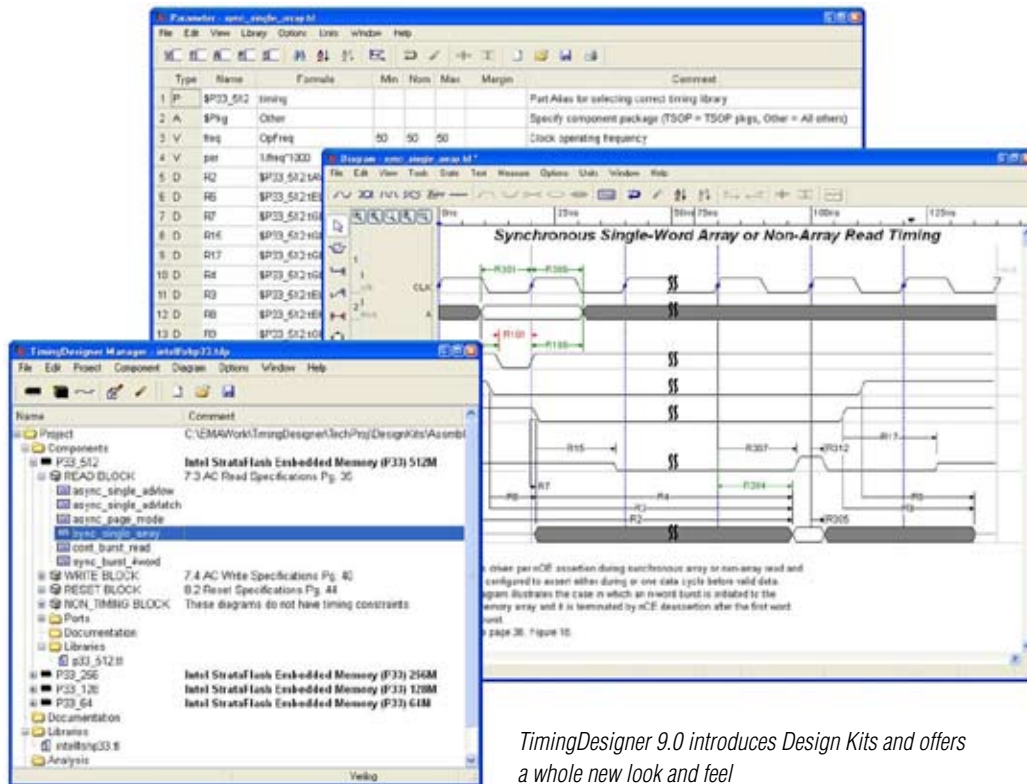
### 9.0 Improvements Include New Look and Feel

The TimingDesigner 9.0 release offers a new look and feel as well as improvements in performance and capabilities:

- New *Parameter/Library* spreadsheets that operate more like popular dedicated spreadsheet applications [More on Page 9](#) >



TimingDesigner 9.0 (Continued from Page 8)



TimingDesigner 9.0 introduces Design Kits and offers a whole new look and feel

- New *Manager Window* features
  - Libraries are now present and editable from *Manager Window*
  - Allows non-TimingDesigner documents (Adobe®, Microsoft® Word, PowerPoint®, Excel®)
  - All objects now have *Comments* field
  - *Properties* field for *Components*
- New and improved online help system
- Selectable Windows styles on Unix
- New *Toolbar* control characteristics
- *Parameter SS* variables can now be added through the *Parameter Browser*
- Resizable dialog boxes, for long signal names and text comments
- New *Notes* dialog window for selectable display of *Diagram Notes*
- Drag and drop of TDML files
- PDF export capability
- New keyboard shortcuts
- Various new environment control settings and improvements
  - New reference cursor
  - *Open Last Diagram* on startup option
  - Show zero margin constraints as violations...or not
  - *Show/hide full path names* in title bar
  - Allow *DSig* and *Bus* waveforms placement w/o attributes
  - *Settings* dialog available via *Parameter* and *Library* Windows

TimingDesigner excels in using an intuitive timing diagram approach for developing specifications to drive the design process, analyzing timing to answer critical design questions, and documenting results to clearly illustrate and communicate the design implementation.

TimingDesigner 9.0 will be shipped starting July 1, 2007 without charge to all customers with current maintenance contracts. For additional information, visit <http://www.ema-eda.com/products/other/timingdesigner.aspx> or call EMA at 800-813-7494.

## Need Help? Try Our Online Resource Center

EMA Design Automation is committed to providing unsurpassed customer service and support. The EMA Resource Center (ERC) at <http://support.ema-eda.com> provides 24/7 technical assistance for OrCAD, Allegro, Cadence Concept®, and TimingDesigner products.

The ERC provides a wide range of information to help you maximize your productivity:

- **Product Downloads**  
Access current and archived product downloads, service packs, patches, utilities, translators, and more
- **Knowledge database**  
Search application notes, FAQs, known problems and solutions, and product documentation for answers to your technical questions
- **Training information**  
Links to our webinar listings, classroom training schedule and course descriptions
- **Frequently asked questions**  
Covering a variety of topics including installation, license files and product usage
- **EMA Solutions Guide**  
Useful information for OrCAD 16.0 product installation and usage

Registered users can also submit priority Service Requests to our technical support staff, and verify their contact and product information to ensure that future shipments are 100% accurate.

Unlimited access to the ERC is provided at no charge to registered users. Register today at <http://support.ema-eda.com/register.asp> >

## Cadence Global Route Environment Technology Sets New Standards for PCB Design

*First Global Routing and Hierarchical Planning Architecture Brings Intelligent Automation to PCB Design, Reduces Manual Work and Shortens Design Time*

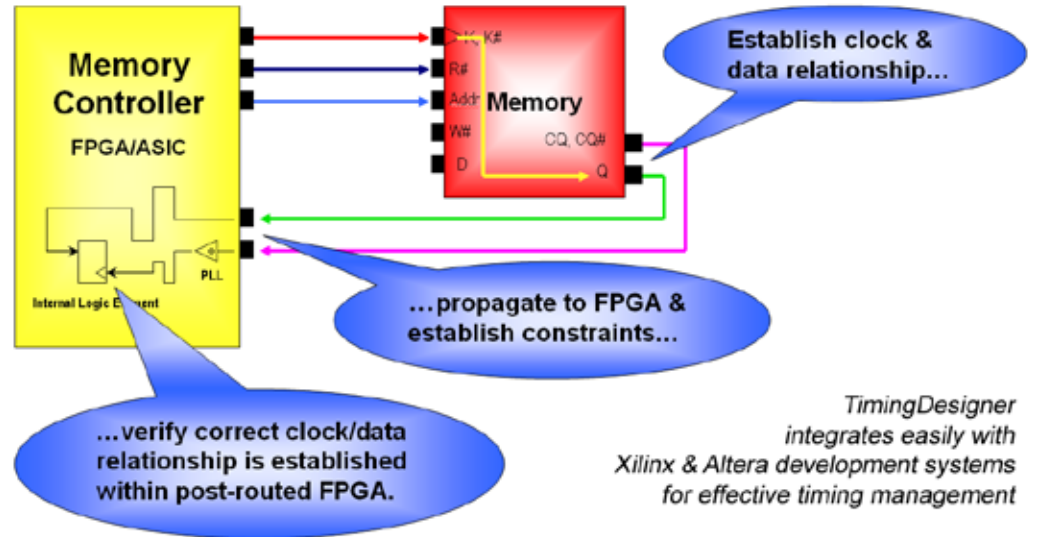
Cadence Design Systems, Inc., the leader in global electronic-design innovation, has announced the Global Route Environment technology for Cadence Allegro PCB design. This revolutionary technology combines a graphical interconnect flow-planning architecture and a hierarchically-aware global routing engine to provide PCB designers with an automated, intelligent planning and routing environment. As the first solution of its kind to bring intelligent automation where no automation was previously available, Global Route Environment technology represents a significant leap forward and establishes a new PCB design paradigm.

Prior to this technology, PCB designers spent weeks or months manually routing complex, high-speed designs with many interconnected buses and multiple high pin-count devices. This resulted in prolonged and unpredictable design-cycle time, impacting project schedules and budgets. Cadence worked with several early adopter partners to help define the problem as well as drive and validate this unique solution.

"Our early adopter customers have been critical in helping us understand product design requirements and then validate our unique solution," said Charlie Giorgetti, corporate vice president, Product Marketing, Cadence. "The Global Route Environment technology for Allegro PCB design helps customers quickly solve the interconnect challenges that previously would have taken weeks or even months of laborious work, threatening project schedules and budgets." Read full press release at [http://www.ema-eda.com/documents/PR\\_Cadence\\_GRE\\_3-26-07.pdf](http://www.ema-eda.com/documents/PR_Cadence_GRE_3-26-07.pdf) >

## How to Effectively Manage Timing of FPGA Design Flows

*Integrating EMA TimingDesigner with Xilinx and Altera Development Systems*



### ABSTRACT

When combined with advances in FPGA technologies for interface design efforts, EMA TimingDesigner can simplify design issues and provide advanced accurate control of virtually any interface. From simple SRAM interface protocols to high-speed source synchronous interface protocols, TimingDesigner allows designers to identify potential timing problems early in the design process and thereby providing the greatest opportunity to get the timing right the first time.

Detecting timing problems early in the design process not only saves time but also permits much easier implementation of design alternatives. TimingDesigner, from EMA Design Automation, allows you to create interactive timing diagrams for capturing interface specifications, analyze component interface timing characteristics, and communicate design requirements among project engineering teams. In addition, TimingDesigner contains features that allow exchange of critical timing data with Xilinx ISE™ and Altera Quartus® II tool sets, throughout the design process. TimingDesigner can communicate place-and-route constraints that reference design specific timing measurements, and allows direct use of post place-and-route timing information to provide visual verification of the interface signal relationships required for desired FPGA interface operation. Integration with other FPGA tool sets such as ispLEVER™ from Lattice®,

Designer from Actel®, and QuickWorks® from QuickLogic® is also planned with future releases of TimingDesigner.

### INTRODUCTION

Designing FPGAs with the high-speed interface technologies available today helps you meet market demands, but it also presents some interesting design challenges. To ensure accurate data transfer for memory interfaces that operate at 200 MHz and beyond, timing analysis needs to play a more prominent role in the identification and resolution of system operation issues. At these frequencies, the margins for setup and hold times are tight, leaving minimal room to secure an accurate data capture and presentation window. Faster edge rates also magnify physical design effects, which cause signal integrity issues that require additional settling time, shrinking timing margins further.

FPGA devices now include advanced features that directly support Double Data Rate (DDR) interface technology within the I/O blocks, and on-board phase locked loop (PLL) networks for accurate clock control. These advances in FPGA technology help reduce the interface design effort by providing advanced building blocks that are explicitly designed for these advanced interfaces, and when combined with the unique capabilities of TimingDesigner, [More on Page 11 >](#)

## How to Effectively Manage Timing of FPGA Design Flows (Continued from Page 10)

provide a powerful solution that can provide that most accurate solution in the least amount of time. This white paper explores a technique for determining necessary clock skew for balanced read data capture margins with DDR type memory interface designs.

### DDR/QDR MEMORY INTERFACE DESIGN PROBLEM

DDR and/or Quad Data Rate™(QDR™) memory devices provide and accept source-synchronous data at twice the rate of the device's clock frequency. This means that data is transferred on the rising and falling edges of the capture clock. In addition, these devices require capture clock skew adjustments to ensure proper clock/data relationships. As noted earlier, several FPGA devices now include DDR interface technology support within I/O blocks and on-board PLL networks. In using these advanced building blocks, you need to conform to memory design requirements. This means that you must have a way to manipulate the blocks accurately and reliably. To illustrate this point, let's take a look at a design requirement for a read operation with a QDR II SRAM source-synchronous interface.

In synchronous memory systems such as QDR SRAM, data is presented coincident with a provided clock, so clock derivatives must be created that are shifted by 90 degrees in order to safely latch memory data. This phase shifting is commonly referred to as center-alignment of the clock within the data valid window and

is an important QDR design characteristic for accurate data capture (see Figure 2 on page 10). To shift the clock for a center-alignment, we can simply delay the clock signal by phase shifting using the PLL network on board the FPGA.

### Capturing Read Data

Delaying the clock signal to achieve center-alignment ensures that various temperature changes and other similar effects the design may encounter won't cause an excessive amount of shift in clock/data position and therefore violate the setup or hold time requirements of the receiving register. In theory, a center-aligned clock edge will maximize the setup and hold times for most devices, allowing sufficient safety margins for drift. However, unless the setup requirement is equal to the hold requirement, center-alignment of the clock signal will provide more margin for one than the other.

The ideal solution is to provide a maximum safety margin for both setup and hold requirements of the device, which translates to balancing the margins, providing equal amounts of safety for both. To balance the margins, we determine the minimum data valid window for the receiving device, and center that window within the actual data valid window provided from the memory device given our design parameters. [More on Page 12 >](#)

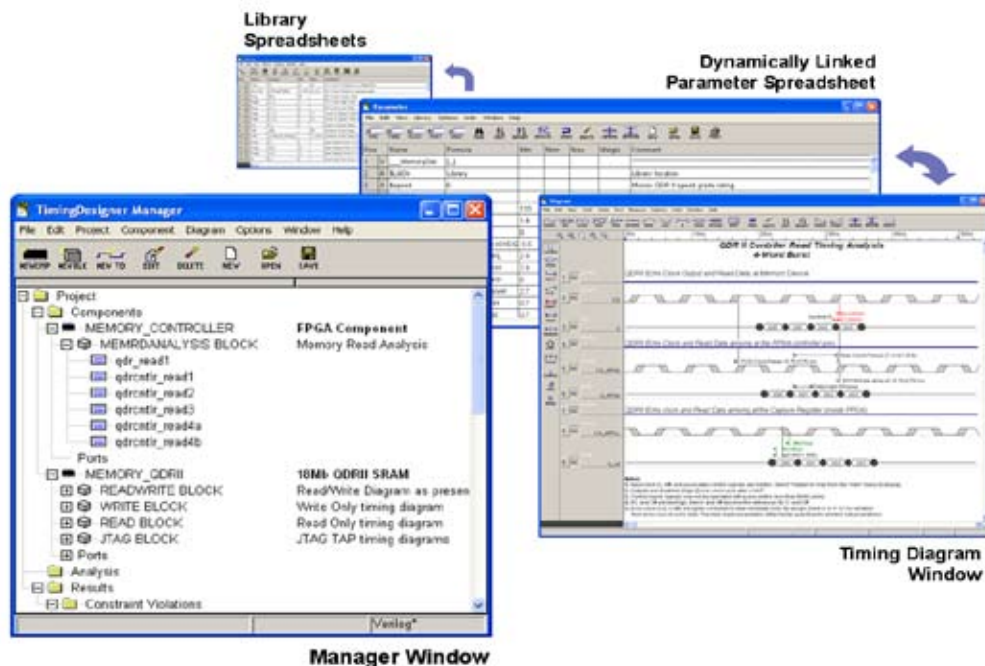


Figure 1 - TimingDesigner's GUI windows allow easy capture of design interface characteristics

## Test Your PCB Design Knowledge!

One of the most interesting aspects of EMA's recently re-launched iTrain Online website is the new "Test Your Knowledge" section. For each eLearning course offered, a series of multiple-choice questions are presented, allowing our on-line students to evaluate their progress.

Test your PCB design knowledge with these sample questions from the iTrain "Test Your Knowledge" section. The correct answers are printed on [Page 12 >](#).

### 1. OrCAD Capture

What command do you use to place a *Net Name* on a wire?

- Place *Wire*
- Place *Text*
- Place *Net Alias*

### 2. OrCAD Layout Basics

Which setting in the *Design Rules Check* allows you to accept a previously marked error?

- Select Next*
- Pad Exit Violations*
- Mark As Good DRC*

### 3. PSpice A/D

What does transient analysis simulate?

- AC Sources
- Time Domain Effects
- Parametric Effects

### 4. OrCAD PCB Designer

A PCB footprint (package name) is limited to how many characters?

- 27
- 30
- 128

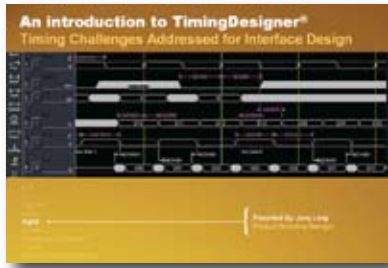
### 5. CADENCE SPECCTRA® for OrCAD

What indicates a protected net visually?

- Highlighted
- White Center Line
- Dashed Line

Learn more about our iTrain Online eLearning options at [http://education.ema-eda.com >](http://education.ema-eda.com)

# TimingDesigner Video Demos Now Available



A variety of TimingDesigner video presentations are now available for online viewing at <http://www.ema-eda.com/resources/movies/movies.aspx>. EMA recently added three new titles:

“License Options” covers purchased and evaluation licenses, installing port drivers, FLEXid keys and floating licenses.

“Node-locked and Floating Licenses” reviews usage of FLEXid keys, loading port drivers, floating license setup and more.

“Evaluation - Configuring the License Manager” covers how to start and navigate through the License Manager tools utility.

## Answers for Test Your PCB Design Knowledge!

1. Place Net Alias=
2. Mark As Good DRC
3. Time Domain Effects
4. 27
5. White Center Line

Questions on [Page 11 >](#)



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### How to Effectively Manage Timing of FPGA Design Flows (Continued from Page 11)

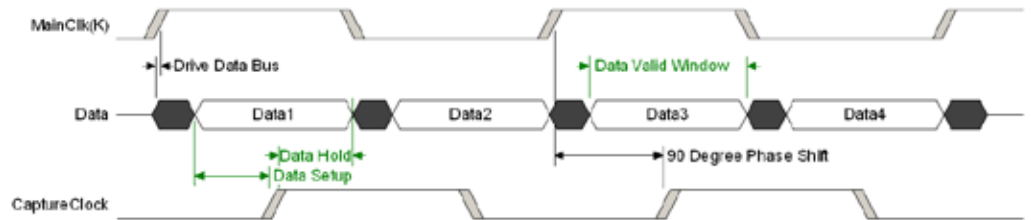


Figure 2 – Illustration of center-aligned clock/data relationship

Using the minimum setup and hold characteristics of our receiving device, we determine a minimum “safe” data valid window with the following formula:

$$\text{Minimum Setup} + \text{Minimum Hold} = \text{Minimum Data Valid Window}$$

The resulting data valid window is centered within the actual data valid window provided by the memory device, as shown in Figure 3. To ensure data capture, the data bus must transition within the indicated “safe” regions outside of the receiver’s minimum data valid window. With this clock/data relationship, we ensure the maximum possible safety margin for read data capture when the design experiences signal drift in either direction.

#### Achieving Proper Clock Skew

Skewing the source-synchronous clock will effectively shift the minimum data valid window of the receiving registers in the memory controller, and will therefore serve as the mechanism for balancing the data valid window. Clock skew adjustments are made with one of the PLL components inside the FPGA device. To determine the skew value, we must take into account routing delays and any external

delay mechanisms that will affect the signal relationships.

We start by using TimingDesigner to create a diagram for the read operation of the QDR SRAM directly from the memory datasheet (Figure 4). We use this diagram to determine the clock and data signal timing relationships as they appear at the pins of the memory device as well as the data valid window characteristics of the design. The objective is to begin at a point where the signal relationship is well defined (the memory device), and propagate that relationship across the PCB to the FPGA where the unknowns begin to have an impact.

Figure 4 shows how the PCB propagation delay is accounted for in the clock (CQ\_FPGA) and the data (Q\_FPGA) signals as they appear at the pins of the FPGA. Using separate variables in TimingDesigner’s dynamically linked parameter spreadsheet allows easy variation of PCB delay values while showing the effect on the associated signals. We can now fit the design into the FPGA device to obtain the internal routing delays and determine the correct phase shift necessary for the capture clock.

[Read complete white paper at http://www.timingdesigner.com >](http://www.timingdesigner.com)

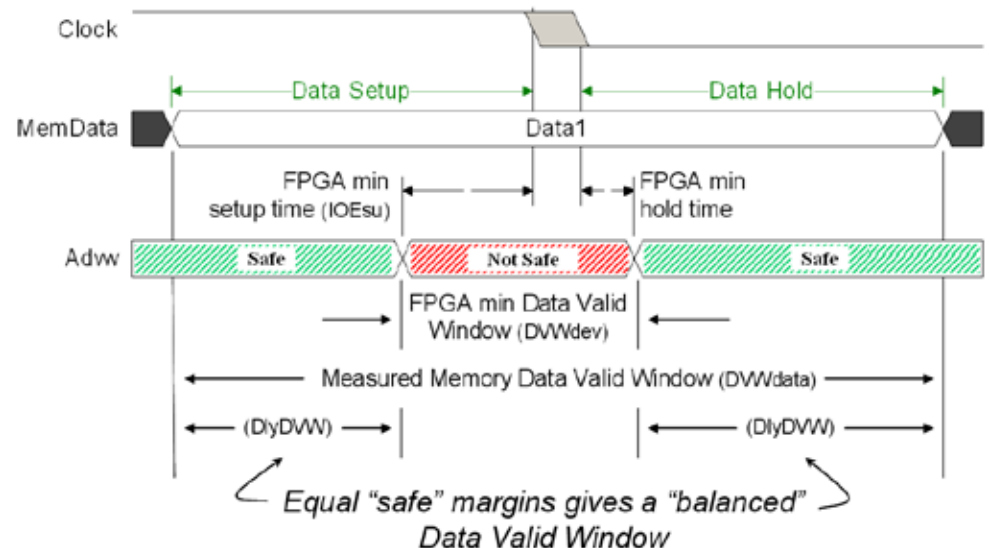


Figure 3 – Balancing the minimum Data Valid Window within actual Data Valid Window