

## JDSU AND CADENCE

JDSU turns to Cadence Allegro technology for more automation, shorter design cycle, and lower project cost

“With Allegro FPGA System Planner, we finalized the pin assignment after the first pass, with only one or two pin swaps. In the front-end design process alone, we realized a 30% to 40% time savings. In addition, we realized a 50% time reduction in routing high-speed signals.”

**Bogdan Petrisor**, *Hardware Design Engineer, JDSU*

### BUSINESS CHALLENGES

- Meet an aggressive project timeline
- Reduce the number of PCB layers to accommodate design complexity and manufacturing requirements

### DESIGN CHALLENGES

- Pin assignment for multiple FPGAs on a new optical network tester board
- High-density, multi-port design with 5,500 components and stringent communications requirements
- 4,596 high-speed nets with constraints

### CADENCE SOLUTIONS

- Cadence® Allegro® FPGA System Planner
- Cadence Allegro Global Route Environment

### RESULTS

- A “first-time-right” board
- Routed in the fixed number of layers in half the time
- 30–40% time savings in the front-end design process
- 50% shorter back-end design cycle compared to previous interactive approaches

## THE CUSTOMER

JDSU is the leading provider of communications test and measurement solutions and optical products for a wide range of industries. One area of focus for the company’s Communications Test and Measurement Group is developing instruments, systems, and software for broadband communication service providers, equipment manufacturers, and major communication users.

Putting a large, complex field programmable gate array (FPGA) on a printed circuit board (PCB) can invite a host of challenges—from unworkable pin assignments in the board layout to problems with signal integrity. So when JDSU embarked upon a new optical network tester board project with complex requirements and a tight timeline, it turned to Cadence for FPGA/PCB co-design and global routing technologies.

“Allegro Global Route Environment helped us successfully reduce PCB place-and-route design time... In the end we were able to shorten the cycle by 50% compared to previous interactive approaches.”

— Dejan Banic, Hardware Design Engineer, JDSU

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## THE CHALLENGE

JDSU’s Communications Test and Measurement Group knew its next-generation optical network tester board would be challenging for several reasons. The board would include a high-density, multi-port design with more than 5,500 components covering both sides of a compact 11x11-inch design, as well as stringent communications requirements. The design had 4,596 high-speed nets that included DDR3, PCI Express, and other advanced high-speed interfaces. In addition, the project schedule was very aggressive.

“Given the complexity of the design and the aggressive schedule, we knew our current process would be inadequate and would delay the project,” says Dejan Banic, Hardware Design Engineer, JDSU. “On the board layout side, we knew that routing some of the high-speed interfaces would take a long time and possibly add layers if we didn’t have time to do it right the first time.”

## THE SOLUTION

This JDSU design team had a long history of using Cadence OrCAD® and Allegro tools with good results, so the team decided to look into two robust Cadence Allegro solutions: FPGA System Planner and Global Route Environment.

## ALLEGRO FPGA SYSTEM PLANNER

Allegro FPGA System Planner provided JDSU with a complete, scalable technology for FPGA-PCB co-design. It enabled the design team to complete the project in a shorter, more predictable manner—with a first-pass success on the board.

Bogdan Petrisor, Hardware Design Engineer at JDSU, told his manager that in order to adhere to the aggressive project schedule, the team would need Allegro FPGA System Planner.

“With this Cadence technology we were able to automatically synthesize FPGA pin assignment based on user-specified, interface-based connectivity, FPGA device pin assignment rules, and placement of FPGAs on the PCB,” Petrisor says. “With automatic pin assignment synthesis, we avoided internal custom-made tools and error-prone processes while shortening the design cycle time.”

Allegro FPGA System Planner provided JDSU with a floorplan view to place components in the FPGA system. Through interface definitions, the design team was able to specify connectivity between components within the FPGA sub-system at a higher level.

The JDSU team shortened its time for optimum initial pin assignment, accelerating the design schedule. It also eliminated unnecessary design iterations during the layout process and reduced the PCB layer count through placement-aware pin assignment.

## ALLEGRO GLOBAL ROUTE ENVIRONMENT

For the back end of the design process, the JDSU team relied on Allegro Global Route Environment—which provides interconnect planning and routing technology for PCB design. This technology provided JDSU with automation for various stages of interconnect planning and routing where no automation was previously available.

“Our first reaction was, ‘This tool will leave the PCB designers without much work to do,’ Banic jokes. “We used Allegro Global Route Environment to create our high-level routing strategy. We used the Interconnect Feasibility capability to check on available space for each of the flows and modify our routing strategy accordingly.”

The Allegro Global Route Environment built upon this feasibility analysis, including all of the engineers’ input, and automatically completed the routing.

“This approach was very effective for our high-speed memory interfaces, with their stringent high-speed design constraints,” Banic says. “Allegro Global Route Environment helped us successfully reduce PCB place-and-route design time. There was a short learning curve, but Cadence support addressed our issues quickly—often within 24 hours. In the end we were able to shorten the cycle by 50% compared to previous interactive approaches.”

## LESSONS LEARNED

This JDSU design group plans to continue using their new Allegro technologies on upcoming projects—and recommend them to other teams at JDSU—to improve boards, reduce design cycle times, speed time to market, and reduce cost.

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