

# PCB DESIGN SOLUTIONS COMPARISON GRID

## OrCAD, ALLEGRO L, ALLEGRO XL, ALLEGRO GXL SERIES (SPB 16.0)

| PCB EDITOR FEATURE SUMMARY                                       | OrCAD PCB DESIGNER/BASICS | ALLEGRO PCB DESIGN L   | ALLEGRO PCB DESIGN XL | ALLEGRO PCB DESIGN GXL |
|--|---------------------------|------------------------|-----------------------|------------------------|
| Limited database (layers, components, connections)               | Basics                    | n/a                    | n/a                   | n/a                    |
| Unlimited database   | Designer                  | •                      | •                     | •                      |
| Netlist/crossplace/crossprobe                                    | •                         | •                      | •                     | •                      |
| Padstack and symbol editor                                       | •                         | •                      | •                     | •                      |
| Customizable/automated drill legend/NC output                    | •                         | •                      | •                     | •                      |
| Multiple via sizes, blind/buried via support                     | •                         | •                      | •                     | •                      |
| Autoplacement/Quickplace/Floorplanner                            | •                         | •                      | •                     | •                      |
| Dynamic shapes with real-time plowing and healing                | •                         | •                      | •                     | •                      |
| 2-D drafting and dimensioning                                    | •                         | •                      | •                     | •                      |
| Gerber 274X, 274D artwork output generation                      | •                         | •                      | •                     | •                      |
| Multiple UNDO/REDO   | •                         | •                      | •                     | •                      |
| Valor ODB++, ODB++(X) and universal viewer                       | •                         | •                      | •                     | •                      |
| HTML-based reports   | •                         | •                      | •                     | •                      |
| Exposed copper DRC   | •                         | •                      | •                     | •                      |
| Interactive routing/etch editing                                 | •                         | •                      | •                     | •                      |
| Automatic silkscreen generation                                  | •                         | •                      | •                     | •                      |
| Split plane support  | •                         | •                      | •                     | •                      |
| SKILL runtime, macro, and script support                         | •                         | •                      | •                     | •                      |
| Variant Editor (Design Entry HDL)                                | n/a                       | •                      | •                     | •                      |
| Variant assembly drawing creation                                | •                         | •                      | •                     | •                      |
| Variant bill-of-materials generation                             | •                         | •                      | •                     | •                      |
| IFF import   | •                         | •                      | •                     | •                      |
| CAD interfaces – DXF (Ver.14), IDF (Ver. 2 and 3)                | •                         | •                      | •                     | •                      |
| PCB interfaces – PADS (Ver.5), P-CAD (Ver.8), OrCAD Layout       | •                         | •                      | •                     | •                      |
| Constraint manager (physical, spacing, properties, and DRC)      | •                         | •                      | •                     | •                      |
| Manual testprep  | •                         | •                      | •                     | •                      |
| Length, parallelism, and differential pairs rule support         |                           | PCB Performance Option | •                     | •                      |
| Pin-pair multi/matched nested group support                      |                           | PCB Performance Option | •                     | •                      |
| Real-time DRC and routing of differential pairs and length rules |                           | PCB Performance Option | •                     | •                      |
| Interactive delay tuning   |                           | PCB Performance Option | •                     | •                      |
| Complex physical design rule checking (no electrical)            |                           | PCB Performance Option | •                     | •                      |
| Group routing  |                           | PCB Performance Option | •                     | •                      |
| Measure parasitic  |                           | PCB Performance Option | •                     | •                      |
| Advanced trace glossing  |                           | PCB Performance Option | •                     | •                      |
| Database-driven design reuse modules                             |                           | PCB Performance Option | •                     | •                      |
| Technology files   |                           | PCB Performance Option | •                     | •                      |
| Design-for-assembly rule checking                                |                           | PCB Performance Option | •                     | •                      |

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|--|---------------------------|--------------------------|-------------------------|-------------------------|
| Automatic testprep   |                           | PCB Performance Option   | •                       | •                       |
| Constraint manager (physical, spacing, electrical (routing), properties and DRC) |                           | PCB Performance Option   | •                       | •                       |
| Allegro PCB Router high-speed routing alignment (6U)                             |                           | PCB Performance Option   | •                       | •                       |
| Real-time DRC of delay and crosstalk rules                                       |                           | PCB Performance Option   | •                       | •                       |
| Constraint regions and technology file support                                   |                           | PCB Performance Option   | •                       | •                       |
| Automatic line width adjustment for impedance rules                              |                           | PCB Performance Option   | •                       | •                       |
| eXtended net support (x-nets)  |                           | PCB Performance Option   | •                       | •                       |
| Layer set rules and routing support  |                           | PCB Performance Option   | •                       | •                       |
| Via array/shielding  |                           | PCB Performance Option   | •                       | •                       |
| SKILL development  |                           | PCB Performance Option   | •                       | •                       |
| Delay, crosstalk, and impedance routing support                                  |                           |                          | •                       | •                       |
| Constraint manager (physical, spacing, electrical (all), properties and DRC)     |                           |                          | •                       | •                       |
| Z-axis delay support   |                           |                          | •                       | •                       |
| Extended timing path support   |                           |                          | •                       | •                       |
| Group routing (space control)  |                           |                          | •                       | •                       |
| Dynamic phase control for differential pairs                                     |                           |                          | •                       | •                       |
| Dynamic design-for-assembly analysis (real-time feedback)                        |                           |                          | •                       | •                       |
| Display and spread segments over voids   |                           |                          | •                       | •                       |
| Back-drilling support  |                           |                          | •                       | •                       |
| Hierarchical flow planning   |                           |                          |                         | •                       |
| Interconnect data abstraction  |                           |                          |                         | •                       |
| Global route engine  |                           |                          |                         | •                       |
| PCB design partitioning technology   |                           | PCB Partitioning Option* | PCB Partitioning Option | PCB Partitioning Option |
| Bi-directional IFF interface   |                           |                          | PCB RF Option           | PCB RF Option           |
| RF geometry and circuit creation/editing   |                           |                          | PCB RF Option           | PCB RF Option           |

## PCB DESIGN SOLUTIONS COMPARISON GRID OrCAD, ALLEGRO L, ALLEGRO XL, ALLEGRO GXL SERIES (SPB 16.0)

| PCB ROUTER FEATURE SUMMARY         | OrCAD PCB DESIGNER/BASICS*** | ALLEGRO PCB DESIGN L           | ALLEGRO PCB DESIGN XL | ALLEGRO PCB DESIGN GXL |
|------------------------------------|------------------------------|--------------------------------|-----------------------|------------------------|
| 6 signal layer limit               | •                            | •                              | n/a                   | n/a                    |
| 256 signal layer limit             | n/a                          | Router Auto/Interactive Option | •                     | •                      |
| Shape-based or gridded autorouting | •                            | •                              | •                     | •                      |
| SMD fanout                         | •                            | •                              | •                     | •                      |
| Trace width by net and net classes | •                            | •                              | •                     | •                      |

\*PCB Performance Option required

\*\*\* No PCB Router technology is included in the OrCAD PCB Designer Basics suite

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|--|-------------------------------|-----------------------------|-----------------------|------------------------|
| Staggered pin support                            | •                             | •                           | •                     | •                      |
| 45-degree ECO routing                            | •                             | •                           | •                     | •                      |
| Memory pattern routing (SMD or through-hole)     | •                             | •                           | •                     | •                      |
| Interactive via search                           | •                             | •                           | •                     | •                      |
| Interactive routing with shoving and plowing     | •                             | •                           | •                     | •                      |
| Interactive floorplanning                        | •                             | •                           | •                     | •                      |
| Autoplacement                                    | n/a                           | n/a                         | •                     | •                      |
| Online design rule checking                      | •                             | •                           | •                     | •                      |
| Flip, rotate, align, push, and move components   | •                             | •                           | •                     | •                      |
| Placement density analysis                       | •                             | •                           | •                     | •                      |
| Router support for PCB design partitioning files | n/a                           | •                           | •                     | •                      |
| <b>Allegro PCB Router ADV 6U or 256U</b>         |                               | Router Performance Option** | •                     | •                      |
| Layer set rules and routing support              |                               | Router Performance Option** | •                     | •                      |
| Signals on specific layers                       |                               | Router Performance Option** | •                     | •                      |
| Width and clearance rules by layer               |                               | Router Performance Option** | •                     | •                      |
| Via rules by net and/or net class                |                               | Router Performance Option** | •                     | •                      |
| Net and/or net class rules by layer              |                               | Router Performance Option** | •                     | •                      |
| Crosstalk violation report                       |                               | Router Performance Option** | •                     | •                      |
| Trace length violation report                    |                               | Router Performance Option** | •                     | •                      |
| Blind and buried via support                     |                               | Router Performance Option** | •                     | •                      |
| Via under SMD pad checking                       |                               | Router Performance Option** | •                     | •                      |
| Automatic wire bonding                           |                               | Router Performance Option** | •                     | •                      |
| Plural vias                                      |                               | Router Performance Option** | •                     | •                      |
| Stacked vias                                     |                               | Router Performance Option** | •                     | •                      |
| Enhanced via fanout                              |                               | Router Performance Option** | •                     | •                      |
| <b>Allegro PCB Router DFM 6U or 256U</b>         |                               | Router Performance Option** | •                     | •                      |
| Automatic trace spreading                        |                               | Router Performance Option** | •                     | •                      |
| Automatic via reduction                          |                               | Router Performance Option** | •                     | •                      |
| Automatic miter 90 to 45                         |                               | Router Performance Option** | •                     | •                      |
| Automatic test point generation                  |                               | Router Performance Option** | •                     | •                      |
| Test point specific clearance rules              |                               | Router Performance Option** | •                     | •                      |

\*PCB Performance Option required

\*\* Router Auto/Interactive Required

\*\*\* No PCB Router technology is included in the OrCAD PCB Designer Basics suite

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|--|------------------------------|------------------------|-----------------------|------------------------|
| <b>Allegro PCB Router HP 6U or 256U</b>                              |                              | PCB Performance Option | •                     | •                      |
| Minimum, maximum, and matched length rules                           |                              | PCB Performance Option | •                     | •                      |
| Crosstalk controls on same and adjacent layers                       |                              | PCB Performance Option | •                     | •                      |
| Virtual pins, which can be moved during autorouting                  |                              | PCB Performance Option | •                     | •                      |
| Parallelism controlled by length and gap                             |                              | PCB Performance Option | •                     | •                      |
| Differential pair routing  |                              | PCB Performance Option | •                     | •                      |
| Automatic net shielding  |                              | PCB Performance Option | •                     | •                      |
| Design rules by area   |                              | PCB Performance Option | •                     | •                      |
| Online display of length tolerance                                   |                              | PCB Performance Option | •                     | •                      |
| Global violation indicator   |                              | PCB Performance Option | •                     | •                      |
| Dynamic display of available length                                  |                              | PCB Performance Option | •                     | •                      |
| Automatic single net routing   |                              | PCB Performance Option | •                     | •                      |
| Multiple net/bus routing   |                              | PCB Performance Option | •                     | •                      |
| Relative delay rules   |                              | PCB Performance Option | •                     | •                      |
| Z-Axis delay support (PCB Editor integration)                        |                              | PCB Performance Option | •                     | •                      |
| Extended timing path support (PCB Editor integration)                |                              | PCB Performance Option | •                     | •                      |
| Pin-pair multi/matched nested group support (PCB Editor integration) |                              | PCB Performance Option | •                     | •                      |

## PCB DESIGN SOLUTIONS COMPARISON GRID OrCAD, ALLEGRO L, ALLEGRO XL, ALLEGRO GXL SERIES (SPB 16.0)

| FRONT-END OPTIONS SUMMARY                            | OrCAD PCB DESIGNER/BASICS | ALLEGRO PCB DESIGN L | ALLEGRO PCB DESIGN XL | ALLEGRO PCB DESIGN GXL |
|--|---------------------------|----------------------|-----------------------|------------------------|
| Allegro Design Entry HDL-or-Allegro Design Entry CIS | OrCAD Capture             | •                    | •                     | •                      |
| Constraint Manager (Allegro Design Entry HDL only)   | n/a                       | n/a                  | •                     | •                      |
| Part Developer/Component Management                  | CIS Option                | •                    | •                     | •                      |
| Allegro Design Entry HDL Rules Checker               | n/a                       | n/a                  | •                     | •                      |

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