

## ISL6740 Voltage Mode PWM Controller

### 1.0 Scope

This document contains the SPICE models, application circuit, and model description for the Intersil ISL6740 voltage mode PWM controller. The ISL6740 features protection circuitry which is not used in normal operation, to minimize simulation time a basic version of the SPICE model is included which omits the protection circuitry. The models are built up from the sections described in the Table below listing their position in the circuit hierarchy.

ISL6740 PWM Controller			
Function	Implementation	Hierarchy	Basic
Oscillator	subcircuit	Top level	Ö
PWM comparator		Top level	Ö
PWM latch		Top level	Ö
PWM toggle		Top level	Ö
Latch - dominant	subcircuit	All levels	Ö
Latch	subcircuit	All levels	Ö
Soft-start	subcircuit	Top level	
Short circuit detector	subcircuit	Top level	
Counter	subcircuit	Short circuit detector	
Fault		Top level	

### 2.0 Assumptions

- Behavior is based on typical values given in the specification sheet for operation at 25 °C.
- Thermal shutdown is not modeled.

### 3.0 A simulation note

The latches used in this model have an initialization input that is driven from the reference voltage. The reference voltage is established once the supply pin reaches its'

threshold voltage. For the initialization to work correctly the supply must be stepped or ramped up from zero during the transient analysis.

## 4.0 Functional Description

The ISL6740 is well described by the block diagram, figure 2, in the data sheet.

The heart of the device is the oscillator (ramp generator). The oscillator can be a slave or a master when synchronizing with other oscillators.

The oscillator ramp waveform is compared with the incoming voltage error signal,  $V_{error}$ , in the PWM comparator. When the rising ramp level exceeds the error signal the PWM latch is set, the latch is then reset during the ramp discharge time. The PWM latch output is ORed with the oscillator reset pulse to drive the PWM toggle latch.

The PWM toggle latch alternates the drive between OUTA and OUTB. Gating on the drive outputs makes the drive active from the end of the oscillator reset pulse until the ramp level exceeds  $V_{error}$ .

Soft-start is achieved through charging up a capacitor to 4.5 volts, the input signal to the PWM comparator is made the lesser of  $V_{error}$  and the voltage on the soft start capacitor.

Additional circuitry provides over-current and short circuit protection; either condition will initiate a new soft start cycle.

Comparators are provided for external thermal protection and under voltage sensing. These together with the other protection mechanisms provide a fault indication output.

#### **4.1 The Oscillator**

The oscillator subcircuit contains the oscillator, Vref generator, and external synch circuitry.

The oscillator has three external components, a timing capacitor and two resistors that set the charge and discharge currents. Sources V2 and V3 sense the current flows from EB2 ( $0.4 * V_{ref}$ ) through the external resistors.

EB3 and GB4 switch these currents into the base of charge transistor Q1 and discharge transistor Q2, respectively. The transistors have BF set to give the correct current scaling.

Control of the charge/discharge currents is from the outputs of latch X1 which is toggled by comparators EB5 and EB6. EB6 signals the end of the discharge period at 0.8 volts while the charge period terminates at 2.8 volts or on receipt of an external synch signal.

The external synch pin may act as output for master control or as input for slave operation. For output operation, MOSFET M1 pulls the synch pin high during the reset period of the oscillator. For input operation, latches X2, X3 & X4, together with comparator EB7, allow any synch signal duty cycle to be used while preventing charging times of less than 71% of the free running time occurring.

Comparator EB1 provides power on control of Vref. Vref is established when the supply voltage exceeds 7.25 volts.

#### **4.2 The PWM toggle**

Sources EB1, EB2 & EB3 form the toggle. EB1 takes its' input from EB2 when the clock is high and EB3 when the clock is low. EB1 is the inverse of EB3 when the clock is low and holds its' own value when the clock is high. The result is that the “q”

output toggles every time the clock transitions from low to high. Sources EB4, EB5, & EB6 add the output gating and fault inhibit functions.

### **4.3 The latches**

Two types of latch are used in the model, a normal set-reset type and a set dominant type. (Note: the set dominant is also used as reset dominant).

Vref is used in both types of latch to force the state of the latch at power up to avoid convergence problems.

### **4.4 Soft-start**

The soft-start circuit includes parts of the over-current and short circuit detection features.

The soft-start timing capacitor is an external component connected to the SS pin. This is charged and discharged by Q1 and Q2 in a similar way to the oscillator described in section 4.1. MOSFET M1 provides rapid discharge from the fault latch.

In normal operation once Vref becomes available the soft-start capacitor will charge towards Vref. The expression used in GB3 will limit the charging voltage to a little over 4.5 Volts.

CS is the current sense pin; this is pulled to ground during the oscillator reset period implemented by the “clk” input, EB8 and M2. If the CS input goes above 0.6 volts during the charge period it trips the OC comparator, EB1. EB1, EB5, & EB6 with associated components form a retriggerable monostable with 50 usec period.

X3 is the OC latch. This is set if the OC comparator is tripped and the SS voltage is greater than 4.5 volts (EB2). When set the OC latch will turn off the soft-start charging current and the capacitor will start to discharge. If the monostable times out before the SS voltage drops to 4.25 volts, EB7), then the OC latch will be reset and normal operation

resumed. If the SS voltage drops below 4.25 volts discharge will continue to 0.27 volts when EB4 will reset the OC latch.

X1 is the SC latch. This is set if the short circuit detection is triggered, (see section 4.5). This latch also disables the SS charging current but is not cleared until the “sslow” condition is reached via comparator EB9.

X2 is the fault latch set by the UV or OTS inputs. This latch drives the fast discharge MOSFET M1 and is reset when the “sslow” condition is reached.

#### **4.5 The short circuit detector**

The SC-detect subcircuit looks for cycles where the OC comparator is triggered before a set point on the ramp is reached. The set point is determined by the SCSET input. These events are detected by EB1 while the SS voltage is greater than 4.25 volts, “sshi”.

X1 and X2 are two counter subcircuits, they have a modulo input set to 32 for X1 and 8 for X2. X1 counts oscillator reset pulses and clears X2 from its’ carry output. The carry output of X2 will go true if more than 8 SC events have occurred in 32 oscillator cycles, this is the SC condition.

#### **4.6 The counter**

It is based on a charge pump. The “clk” input charges/discharges C4 with a short pulse. Diodes D1 and D2 direct these pulses into C1 or to ground according to their polarity. Since C1 and C4 are equal the voltage on C1 increments by the clk level (1 volt) each positive clk edge.

EB3 compares the count value with the modulo input. The output from EB3 is ORed with the clear input to set the clear latch, X1. The clear latch output drives the discharge current source GB5. The latch is reset when the count is close to zero.

GB5 with D3 and associated components stretch and form the clear pulse to form the carry output.

#### **4.7 The basic ISL6740**

The basic ISL6740 subcircuit contains the essential elements for normal operation with simplified soft-start input.

The oscillator subcircuit provides the ramp waveform and reset pulses plus Vref.

EB3 is the PWM comparator; this compares the ramp waveform with the lesser of the “error” input and “ss”, the soft start input. The lesser is obtained through the three-diode circuit driven by EB1 and EB2.

The PWM latch, X3, is set by the PWM comparator and reset by the oscillator during the discharge period.

The oscillator reset pulse and the PWM latch output are ORed to drive the toggle subcircuit. If the ramp voltage does not reach the error voltage then the toggle produces output drive pulses at the maximum duty cycle determined by the oscillator charge/discharge times. As the error voltage falls the PWM latch is set earlier in the cycle and extends the output off times.

#### **4.8 The full ISL6740 model**

The full ISL6740 model contains the basic model described in section 4.7 plus the soft start and SC detect subcircuits. Circuitry for the FAULT output is also added.

The SC-circuit and soft-start work as described above and link to the output disables in the toggle circuit.

EB7 is a comparator that checks that the soft-start voltage is greater than the error voltage. This condition sets a latch, X6, that enables the tri-state FAULT output, GB8 & EB9.

## 5.0 Application test circuit

### 5.1 Basic model

The application test circuit is the 48V input DC transformer circuit given in the data sheet. The SPICE schematic is shown in figure 10. The current sensing connection is not used in the basic model. The soft start voltage is applied from an external voltage source.

Simulation results for 48V input with 1.5 ohm load are shown in figure 11. The graphs show how the soft start holds the duty cycle at zero until the SS voltage is sufficient to exceed the minimum ramp voltage.

### 5.2 Full model

Figure 12 shows the same application test circuit but using the full model.

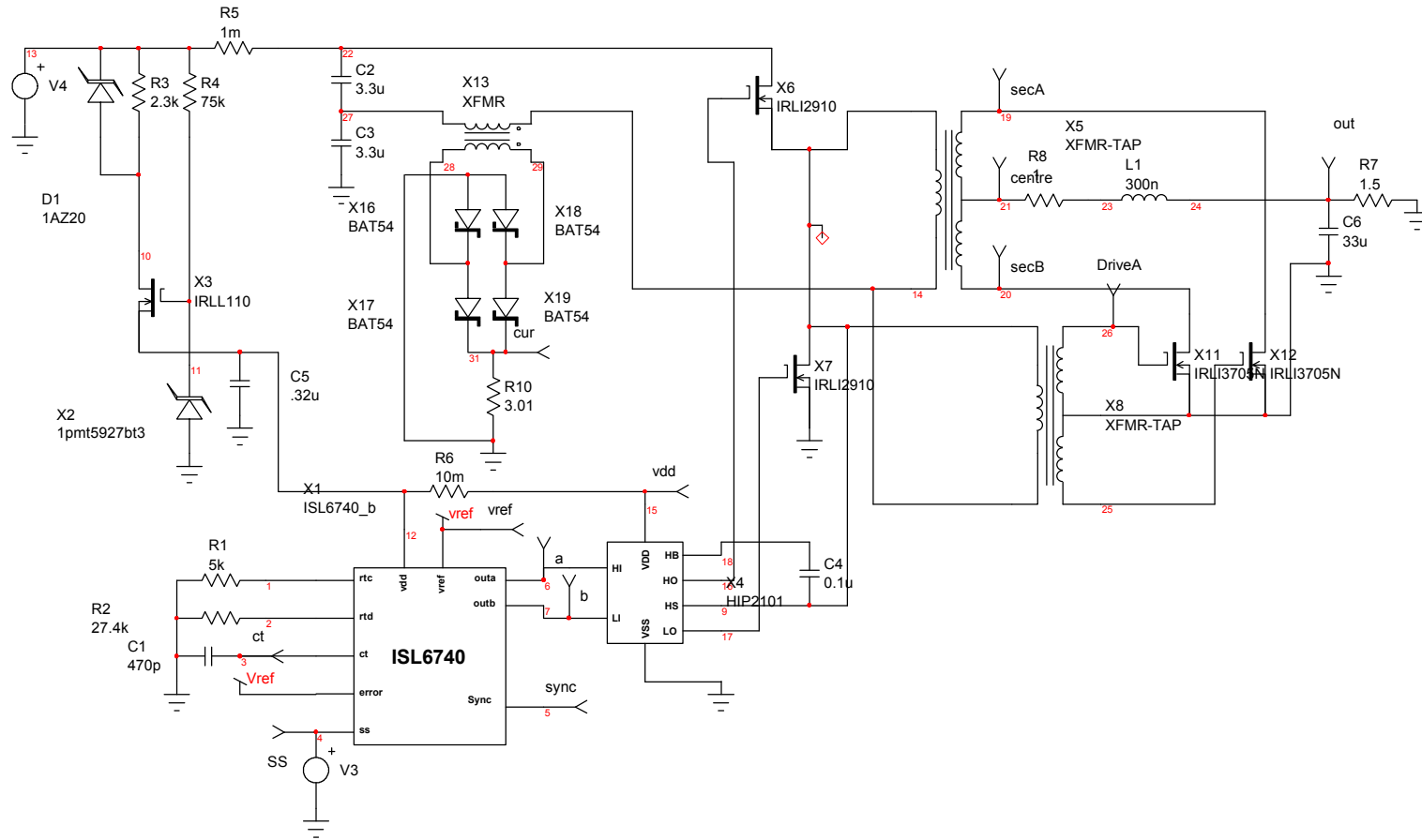
The operation of the over-current detector for a transient overload is shown in figure 13. The soft-start voltage can be seen to discharge following the fault but to recover after the 50 usec monostable timeout since the soft start voltage is still greater than 4.25 Volts.

The effect of a longer overload is shown in figure 14, here the over-current persists for more than 8 oscillator cycles which activates the SC detect circuit and asserts a fault condition. The drive outputs are inhibited while SS drops to its' minimum level before clearing the fault latch and initiating a soft start cycle. Figure 15 zooms in on the fault to show the fault flag raised after 8 over-current occurrences have been counted. The upper trace is the fault flag, the center trace is the counter within the SC subcircuit, and the lower trace is the current sense input, CS.

## 6.0 Conclusions

The basic ISL6740 model performs as expected in the application circuit for normal operation while the full model demonstrates the protection features of the ISL6740 at the expense of simulation time.

**NOTE: Subcircuit schematic figures have been removed.**



**Figure 10 – Application test circuit using basic model**

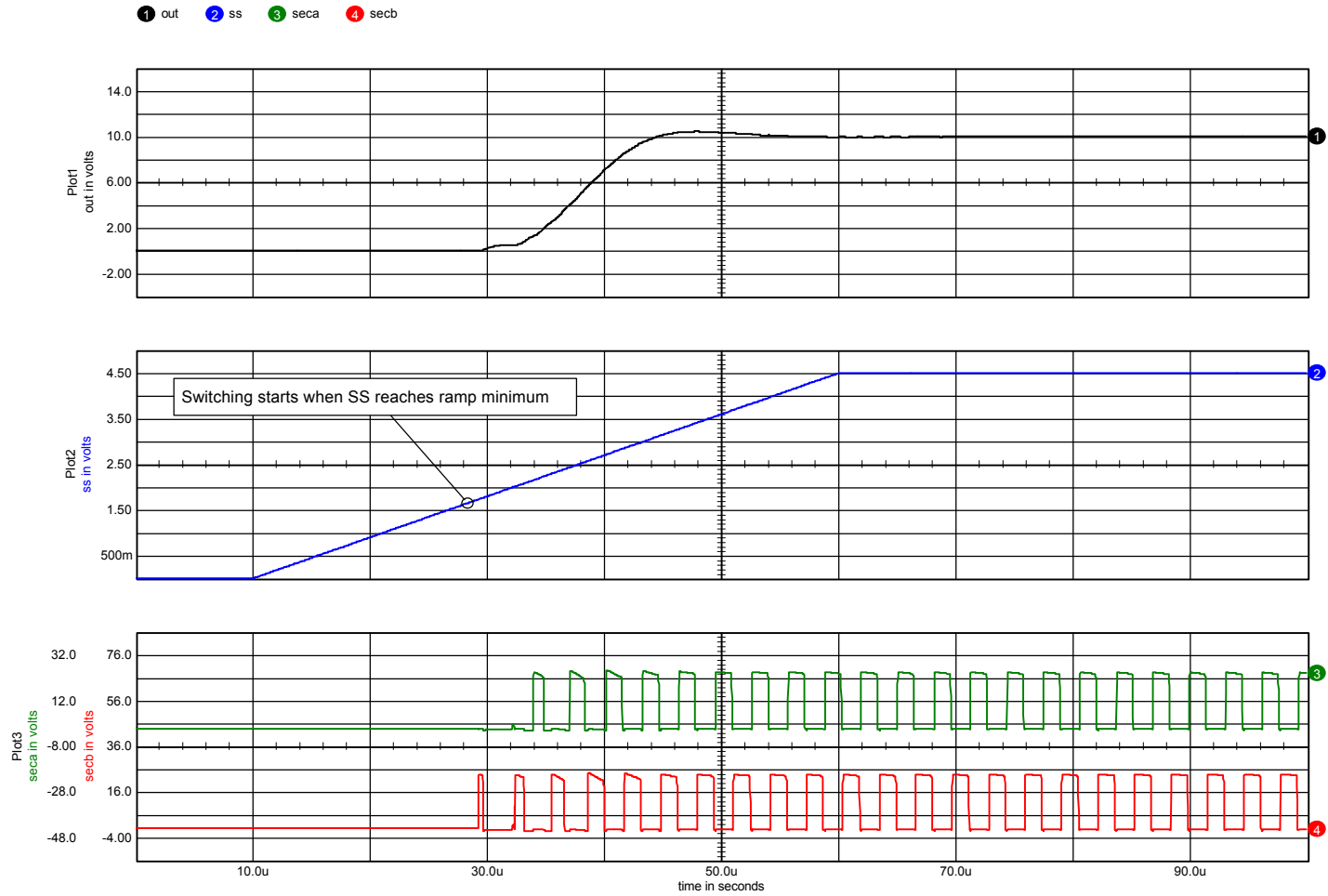


Figure 11 – Application test circuit results for basic model

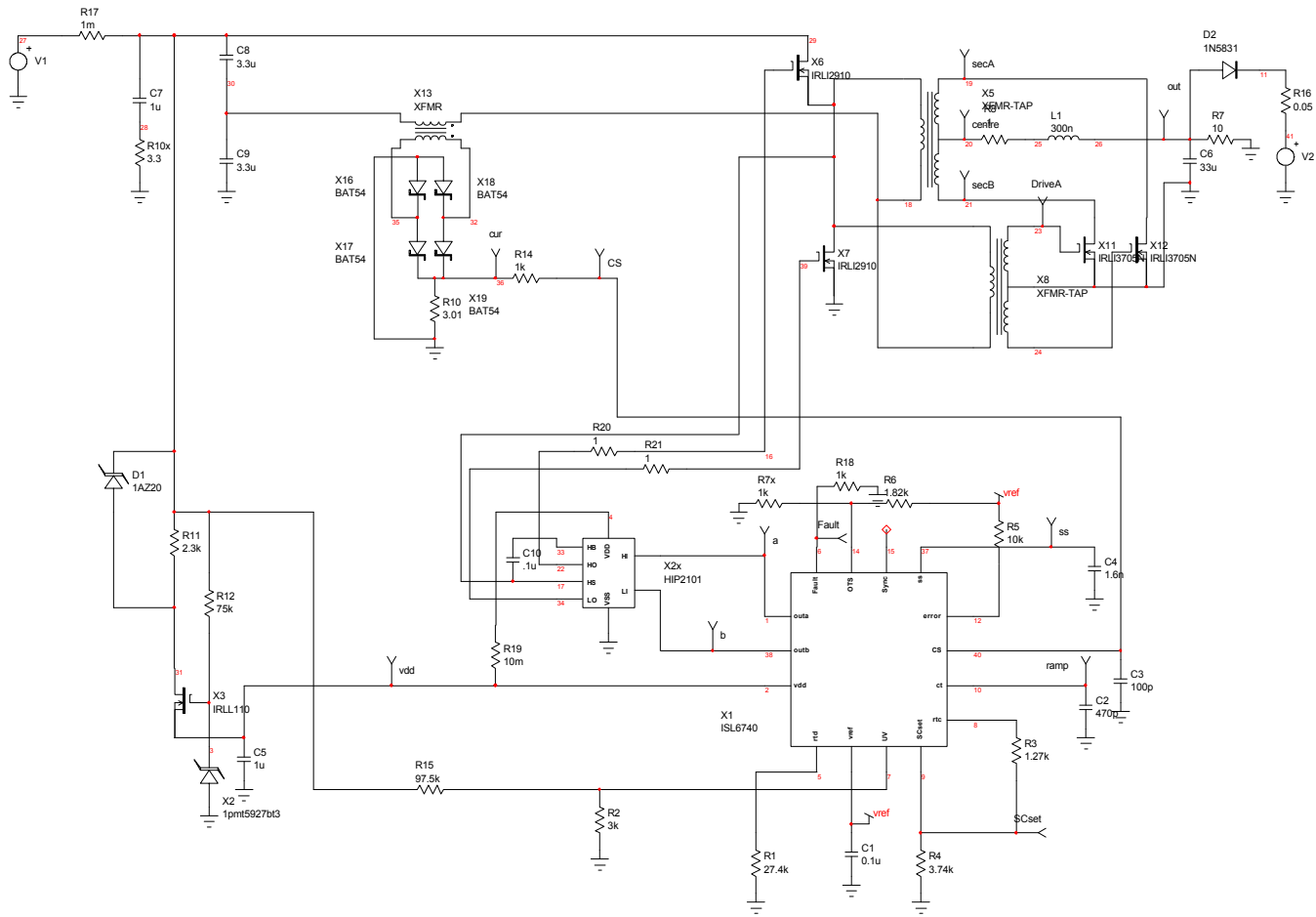


Figure 12 – Application test circuit for the full model

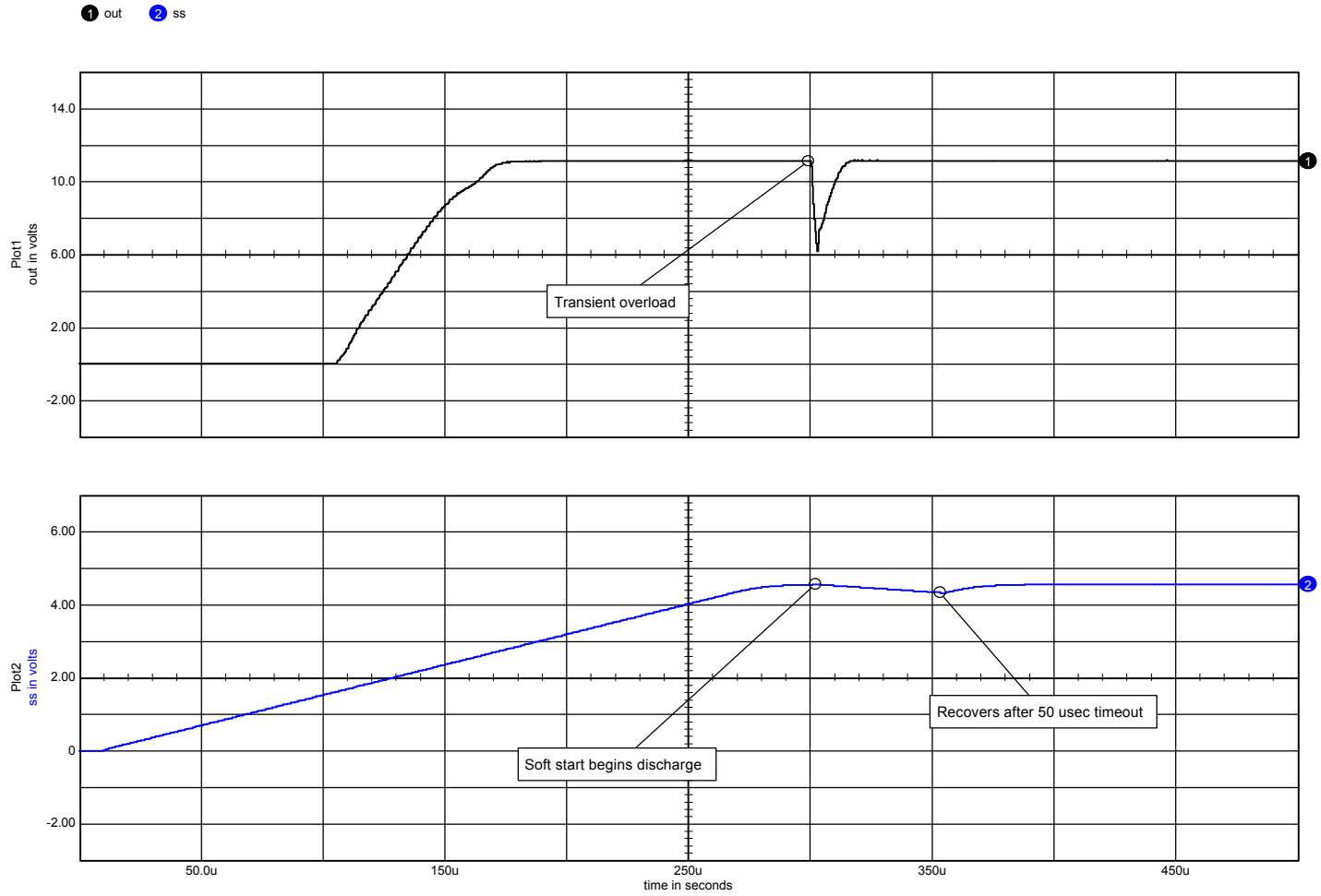


Figure 13 – Test results for the full model with transient overload

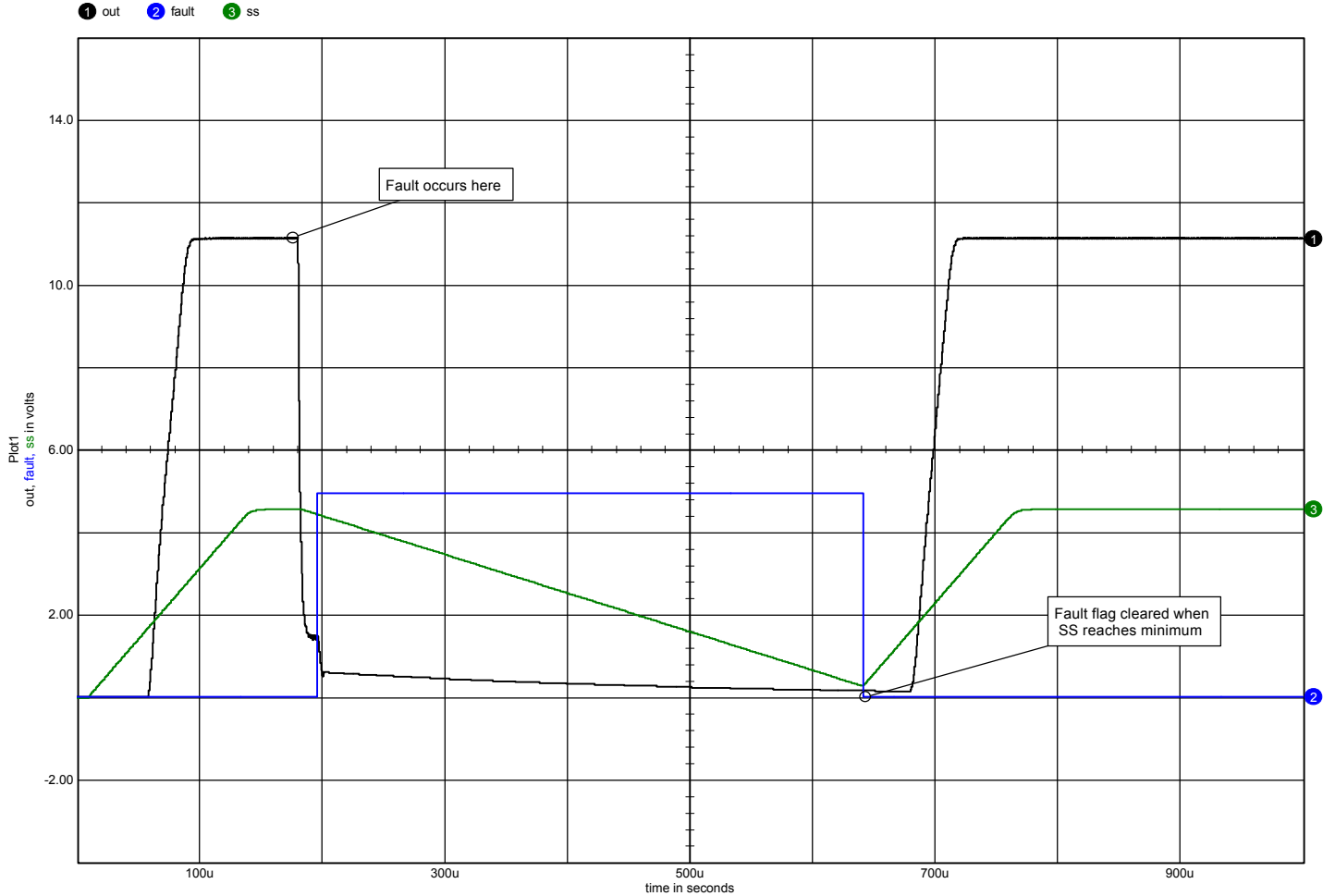


Figure 14 – Full model test circuit showing longer term overload and SS recycling

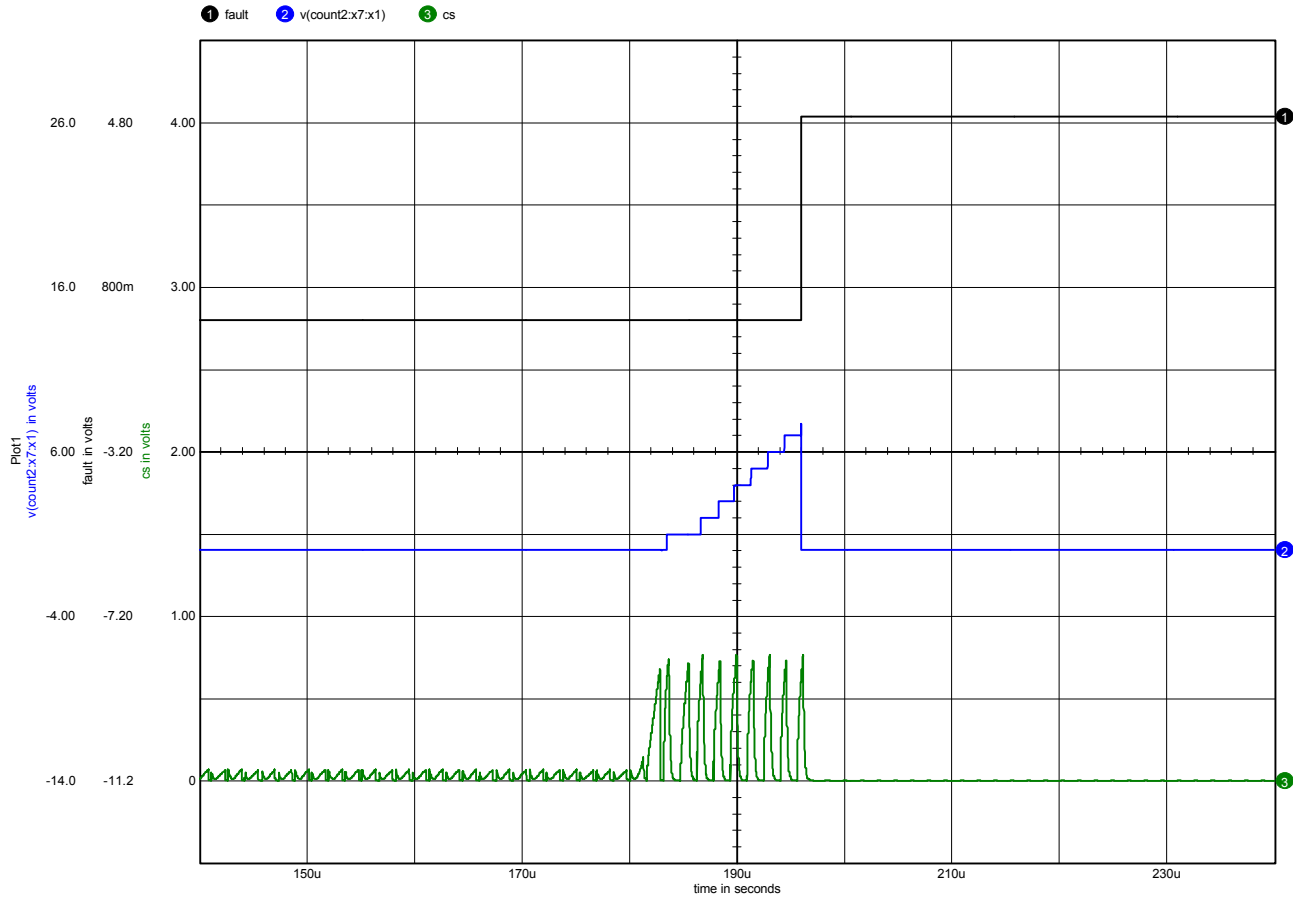


Figure 15 – Full model test results showing over current event counting