

AEi Systems
Power IC Model Library™
for PSpice®

Model Documentation

Version 1.1a, March, 2005

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Chapter 1 - Overview

Welcome

Thank you for purchasing the AEi Systems Power IC Model Library for PSpice.

SMPS applications today are much more demanding than ever. Today's designs require increases in switching frequency, higher efficiency and lower standby current. State space based models simply do not reveal many important nonlinear factors that influence these performance characteristics. To address the needs of today's power supply designer, AEi Systems introduced the Power IC Model Library for PSpice. This library represents a major breakthrough for SMPS designers who use PSpice.

AEi Systems has spent years developing accurate and robust models for the components that are used in power designs. We test our models thoroughly so you can have confidence in the model's operation and results. Useful examples are also provided for most of the models.

The library incorporates a comprehensive set of large signal hyper-accurate cycle-by-cycle simulation models for Pulse Width Modulation (PWM), Switching Regulators, Phase Shift Controllers and other Power ICs. You can perform high-speed, cycle-by-cycle simulation to show true large-signal performance, simulate current-mode control using the latest accurate modeling techniques, run CCM and DCM converter simulations, analyze control systems including loop gain, input filter design and analysis, and measure power stage loss and stress analysis for all major components. In summary, you can simulate your entire power system.

Nonlinear characteristics such as propagation delay, switching speed, drive capability and maximum duty cycle/current limits, startup phenomena are all accurately modeled. You can

directly compare the performance of components from different vendors and analyze the effects of different implementations such as peak current mode control, hysteric current control, low voltage, and low operating current, to name just a few.

Summary of Benefits:

- Analyze large signal effects like start-up transients, power stage semiconductor stress, and step-load response
- Explore different approaches to transformer, converter, filter, and control structures
- Compute component stresses and test for excessive power dissipation
- Compare circuit characteristics with linear and nonlinear magnetics
- Analyze in both time and frequency domains
- Simulate and analyze your entire power supply without ANY limitations.

The models utilize analog behavioral elements, special Boolean logic elements and other specially designed function blocks. Together they greatly reduce the model's simulation runtime, while maintaining "better than data sheet max/min" accuracy, an important factor in SMPS analysis.

Components are normally modeled to match "Typical" part performance at room temperature. Some temperature performance variations are also taken into account.

What's Included – Getting Started

The Power IC Model Library includes over 150 PSpice syntax compatible models in multiple model library files (See Chapter 4, Library Listings). Example schematics in native format and symbols for both OrCAD Capture and Microsim Schematics are included.

Files Included and Location on the Distribution CD:

PowerLib Folder

Library Folder - Models and Symbols

- PSpice Model Libraries Files for both Capture and Schematics (.LIB)
- Symbol Files for both Capture and Schematics (.OLB, .OLJ, .SLB)

Examples Folder – OrCAD Capture Schematics

Various Folders (by manufacturer)

- Capture schematic files (.OPJ, .DSN, .SCH)

Microsim Folder - Microsim Schematics Files

Various Folders (by manufacturer)

- Schematics Files (.SCH, .NET, .ALS, etc.)

Documentation Folder - Manual and Model Reference Documentation

Installing Schematic, Library, or Symbol Files

Please see the relevant portions of your OrCAD, Microsim, or other Schematic Entry tool User's Guide for details on how to incorporate new models and/or symbols into the design environment.

The example OrCAD schematic files may be copied from the distribution CD to any directory, for example, **C:\PowerLib\Examples**.

The library and symbols files may be copied from the distribution CD to a directory on your hard disk, for example, **C:\PowerLib\Libraries**.

Symbol and model libraries generally use the name of the IC manufacturer whose parts are modeled in the library. The models in a .LIB file have corresponding symbols in the same named symbol file. Please see Chapter 4, Library Listings, for information on where specific models/symbols are located.

Master Library File

The **Power_EMA_AEI.LIB** file contains a list of all of the library files and may be used to include all of the models in the Power IC Model Libraries in a manner similar to the NOM.LIB file (Nom.Lib is distributed with PSpice).

The library names in the Power_EMA_AEI.LIB file have a path that may need editing depending on where you place the library files. For example, the path (in quotes) in the line

```
.lib "c:\PowerLib\Libraries\ADI_Linear.LIB" ; Analog Devices
```

should be changed to the path corresponding to whatever folder you place the libraries files into. Other .lib lines should be changed likewise.

In some cases, common sub-blocks called by a subcircuit in one library might be located in another library. That's why it is best to use the Power_EMA_AEI.LIB master library file to incorporate models into your simulations and schematic environment.

Important Note: It is recommended that Power IC Model Library files and symbols NOT be placed in the same directory as the OrCAD delivered files in order to avoid any naming conflicts that may arise in the future.

Microsim Schematics

While the Microsim Schematics files are included in the relevant OrCAD schematics folders a separate folder set is included for Microsim Schematics users that only includes the relevant *.SCH file, without any OrCAD Capture related files.

You may have to edit the Library Settings... using the Editor Configuration... function in the Options menu in order to get Microsim Schematics to recognize the .SLB symbol files.

Uninstalling Files

There is no special uninstall utility or procedure.

Model Documentation and Support

Each model in the AEi Systems Power IC library is tested under various conditions using multiple test circuits for specific functions and then again in one or more full application test circuits. The results are compared to data sheet performance and in most cases actual bench measurements.

AEi Systems strives to produce models that meet all key performance metrics and exhibit “typical” performance as specified in the data sheet or performance that is within given Max-Min specifications.

Adobe Acrobat .PDF files containing documentation for various models in the library are included in the Documentation folder on the distribution CD.

The documentation discusses the model development and architecture and contains the results of the testing and verification process.

The support section of AEi Systems web site, <http://www.aeng.com/support.asp>, contains additional model documentation and various white papers on simulation and modeling.

Documentation for other models that are not on the distribution CD may or may not be available. Please inquire with AEi Systems directly at info@aeng.com.

Chapter 2 - Model Discussions

Model Usage

The majority of the models in the Power IC Model Libraries are transient time-domain models. That includes the FET Drivers and majority of the controller models (parts without an “s” extension in the model name).

The controller models are normally pin-for-pin compatible with the actual physical part. All key functions of the actual chip are modeled with the exception of variations with temperature. This includes startup nonlinearities and other transient phenomenon. Smoke alarm parameters are not currently implemented. While over-current and other protection functions are modeled, stimulus or supply voltages that exceed the data sheet minimums or maximums may produce unreliable results.

The models are characterized for typical operation at room temperature.

The transient models can be used in all types of simulations including startup, line transient, load transient, and steady state, provided that the external circuit and stimulus are properly adjusted.

The transformer and semiconductor models can be used in either transient or frequency domain simulations.

For switching circuit simulations linearized models are required in order to perform frequency domain simulations. The switching based transient controller models can not be used in frequency domain simulations. Models that are linearized fall into the classification of “state space” models. While a variety of state space models are available on the Internet,

the Power IC Model Library includes Boost, Buck, Forward, and Flyback “PWM” blocks. See references 1 and 2 for more information on these blocks.

Frequency domain versions of various PWM controllers are included in the Power IC Model Library. They have an “s” appended to their model name as in the LT1242s and UC1845As. Several example .AC simulations are included (UC1842STATESPACE.DSN, UC1843ASTEST.DSN, NCP1000AVGTEST.DSN, etc.).

Using the Models with Other Simulators

In order to produce models that are accurate but run in a reasonable time frame, AEl Systems uses a combination of actual semiconductors and behavioral modeling constructs to model power ICs. Two constructs are utilized frequently; the switch with hysteresis and If-Then-Else expressions.

Not all versions of PSpice support a switch with hysteresis. While the S_ST Short-Transition switch model, which emulates the Berkeley SPICE 3 S element, is now available, older versions of PSpice did not support the hysteresis effect. A subcircuit, shown below, is utilized in order to provide compatibility with all versions of PSpice without compromising performance.

```
.subckt SWhyste NodeMinus NodePlus Plus Minus PARAMS: RON=1 ROFF=100MEG
VT=1.5 VH=.5
S5 NodePlus NodeMinus 8 0 smoothSW
EBctrl 8 0 Value = { IF ( V(plus)-V(minus) > V(ref), 1, 0 ) }
EBref ref1 0 Value = { IF ( V(8) > 0.5, {VT-VH}, {VT+VH} ) }
Rdel ref1 ref 70
Cdel ref 0 100p IC={VT+VH}
Rconv1 8 0 10Meg
Rconv2 plus 0 10Meg
Rconv3 minus 0 10Meg
.model smoothSW VSWITCH (RON={RON} ROFF={ROFF} VON=1 VOFF=0)
.ends SWhyste
```

If-Then-Else expressions in the E and G elements are also used for various logic and controlling functions. In them, mathematical equations using Boolean combinations of node voltages and branch currents are utilized.

For example,

```
GB1 33 2 Value= { IF ( V(5) > 2.5 & V(11) > 4.3 , -.014 , 0 ) }
EB19 44 0 Value= { IF ( V(22)<1 , 2 , IF ( V(30)<1 & V(42)<1 , 2 , V(30) ) ) }
```

If you are trying to use the models with other SPICE based simulators you will have to make

sure that the simulator supports these extensions to the basic SPICE primitive set. If you need one or more of the models translated to another SPICE syntax (Saber, HSpice, etc.) please contact AEi Systems.

Chapter 3 - Using the Power IC Model Schematic Examples

Schematic Examples

The Power IC Model Library for PSpice includes a number of application test circuit examples. Some are simple; others are fairly complicated and mimic the actual applications circuit found in the data sheet. All should run in a few minutes or less on most computers.

The example schematic designs can be found in two folders on the distribution CD. Under the PowerLib folder is an Examples folder. That contains the schematics for the OrCAD Capture system. The Microsim folder contains approximately the same set of examples for the Microsim Schematics environment.

A master library file has been created called Power_EMA_AEI.lib. It is in the Libraries folder along with the rest of the model libraries. You can refer to this file in the in order to include all of the models in the parts database for either OrCAD Capture Library Configuration or the Microsim Schematics Library and Include Files... function (Analysis menu)

The Microsim Schematics editor may not be able to find the symbol library files depending on where you choose to install them. You can correct this problem by pointing to the symbol library file on your hard disk using the Editor Configuration... function in the Options menu.

Most parts have an equivalent test circuit matched to their name. In some cases, where there is a family of parts there may be fewer test circuits than parts, but the parts are normally

interchangeable, in so far as the test circuit is concerned, allowing the same test circuit to serve the part family.

The test circuits will allow you to explore the basic functionality of the model, if not its entire range of features.

Types of Simulations

Simulation Run Times

The time it takes to run a switch mode power supply simulation is directly related to a number of factors:

- Complexity of the model and external circuitry
- Length of the simulation
- Time step of the simulator

The last item is driven by a number of factors including the stimulus and loading, soft-start and compensation components, the simulator .OPTION tolerances, the TMAX timestep setting, and the overall frequency content of the circuit (edge speeds).

It is not uncommon for SMPS simulations to take 15-60 minutes each. However, most of the example simulations run in just a few minutes.

Startup Simulations

Startup simulations can take a long time to run depending on the conditions and compensation settings. You can recognize these simulations in the examples because they normally don't use the UIC (use initial conditions) transient directive and use VCC/stimulus settings that start at zero and are pulsed on to their terminal voltage. In addition, initial conditions on input, output or compensation capacitors are not utilized.

Steady State, Line, Load Transient Simulations

In order to speed up the simulation of these types of analyses it is best to try to set initial conditions on key storage elements. This helps to get the circuit running at or near steady state almost immediately. This is as opposed to running a startup type simulation and delaying the data taking interval until steady is achieved. To do this, the UIC option is used and IC= directives are inserted, especially on input output, and compensation capacitors.

Correct initial conditions can allow a circuit that would normally take several milliseconds of time to start to get to steady state in a few hundred microseconds.

Incorrect initial conditions, whether they are set by the .NODESET, .IC, or IC= directives can cause the PSpice simulation to take much longer than if it were started from a zero

voltage state due to transient residues or can cause convergence problems. In some circuits the initial conditions on compensation components can be very sensitive with respect to simulation settling time, with a few tenths of a volt making a huge difference in settling/runtime.

Except in cases where the compensation is internal, the models in the Power IC Model Library are setup to allow you to achieve steady state by setting initial conditions on elements external to the part.

Simulation Convergence – Quick Fix

If you encounter a convergence problem change the .OPTIONS settings you are using to the following:

- **Abstol = 0.01u**
- **Vntol = 10u**
- **Reltol = 0.01**
- **ITL4 = 500**

This should cure most simulation convergence problems unless there is an error in your circuit description.

Switching simulations refer to simulations which have a significant number of repetitive cycles, such as those found in SMPS simulations. Most of the simulation you perform with the Power IC Models will be of this type.

SMPS simulations can experience a large number of rejected timepoints. Rejected timepoints are due to the fact that PSpice has a dynamically varying timestep which is controlled by constant tolerance values (Reltol, Abstol, Vntol). An event that occurs during each cycle, such as the switching of a power semiconductor, can trigger a reduction in the timestep value. This is caused by the fact that PSpice attempts to maintain a specific accuracy, and adjusts the timestep in order to accomplish this task. The timestep is increased after the event, until the next cycle, when it is again reduced. This timestep hysteresis can cause an excessive number of unnecessary calculations. To correct this problem, we can regress to a SPICE 2 methodology and force the simulator to have a fixed timestep value.

To force the timestep to be a fixed value, set the Trtol value to 25, i.e. .OPTIONS TRTOL=25. The default value is 7. The Trtol parameter controls how far ahead in time SPICE tries to jump. The value of 25 causes PSpice to try to jump far ahead. Then set the Tmax value (maximum allowed timestep) in the .TRAN statement to a value which is between 1/10 and 1/100 of the switching cycle period. This has the opposite effect; it forces

the timestep to be limited. Together, they effectively lock the simulator timestep to a value which is between 1/10 and 1/100 of the switching cycle period, and eliminate virtually all of the rejected timepoints. These settings can result in over a 100% increase in speed!

Note: In order to verify the number of accepted and rejected timepoints, you may issue the .OPTIONS ACCT parameter and view the data at the end of the output file.

If this does not help the simulation converge proceed to the next section which has more details.

Simulation Convergence

The answer to a nonlinear problem, such as those in the SPICE DC and Transient analyses, is found via an iterative solution. For example, PSpice makes an initial guess at the circuit's node voltages and then, using the circuit conductances, calculates the mesh currents. The currents are then used to recalculate the node voltages, and the cycle begins again. This continues until all of the node voltages settle to values which are within specific tolerance limits. These limits can be altered using various .Options parameters such as Reltol, Vntol, and Abstol.

If the node voltages do not settle down within a certain number of iterations, the DC analysis will issue an error message such as “No convergence in DC analysis”, “Singular Matrix”, or “Source Stepping Failed”. PSpice will then halt the run because both the AC and transient analyses require an initial stable operating point in order to proceed. During the transient analysis, this iterative process is repeated for each individual time step. If the node voltages do not settle down, the time step is reduced and PSpice tries again to determine the node voltages. If the time step is reduced beyond a specific fraction of the total analysis time, the transient analysis will issue the error message, “Time step too small,” and the analysis will be halted.

Convergence problems come in all shapes, sizes, and disguises, but they are usually related to one of the following:

- Circuit Topology
- Device Modeling
- Simulator Setup

The DC analysis may fail to converge because of incorrect initial voltage estimates, model discontinuities, unstable/bistable operation, or unrealistic circuit impedances. Transient analysis failures are usually due to model discontinuities or unrealistic circuit, source, or parasitic modeling. In general, you will have problems if the impedances, or impedance changes, do not remain reasonable. Convergence problems will result if the impedances in

your circuit are too high or too low.

The various solutions to convergence problems fall under one of two types. Some are simply band-aids which merely attempt to fix the symptom by adjusting the simulator options. Other solutions actually affect the true cause of the convergence problems.

The following techniques can be used to solve a large number of convergence problems. When a convergence problem is encountered, you should start at solution 0 and proceed with the subsequent suggestions until convergence is achieved. The sequence of the suggestions is structured so that they can be incrementally added to the simulation. The sequence is also defined so that the initial suggestions will be of the most benefit. Note that suggestions which involve simulation options may simply mask the underlying circuit instabilities. Invariably, you will find that once the circuit is properly modeled, many of the “options” fixes will no longer be required!

General Discussion

Many power electronics convergence problems can be solved with the .OPTIONS Gmin parameter. Gmin is the minimum conductance across all semiconductor junctions. The conductance is used to keep the matrix well conditioned. Its default value is 1E-12mhos. Setting Gmin to a value between 1n and 10n will often solve convergence problems. Setting Gmin to a value which is greater than 10n may cause convergence problems.

PSpice does not always converge when relaxed tolerances are used. One of the most common problems is the incorrect use of the .Options parameters. For example, setting the tolerance option, Reltol, to a value which is greater than .01 will often cause convergence problems.

Setting the value of Abstol to 1u will help in the case of circuits that have currents which are larger than several amps. Again, do not overdo this setting. Setting Abstol to a value which is greater than 1u may cause more convergence problems than it will solve.

After you've performed a number of simulations, you will discover the options which work best for your circuit. Very often various options will be needed as the circuit topology is developed. Invariably, you will find that after you have debugged your circuit representation, and if your components are well modeled, most of the options can be removed.

If all else fails, you can almost always get a circuit to simulate in a transient simulation if you begin with a zero voltage/zero current state. This makes sense if you consider the fact that the simulation always starts with the assumption that all voltages and currents are zero. The simulator can almost always track the nodes from a zero condition. Running the simulation will often help uncover the cause of the convergence failure.

The above recommendation is only true if your circuit is constructed properly. Most of the time, minor mistakes are the cause of convergence problems. Error messages will help you track down the problems, however, a good technique is to scan each line of the netlist and look for anomalies. It may be tedious, but it's a proven way to weed out mistakes.

Not all convergence failures are a result of the PSpice software! Convergence failures may identify many circuit problems. Check your circuits carefully, and don't be too quick to blame the software.

DC Convergence Solutions

2. Check the circuit topology and connectivity.

Common mistakes and problems:

- Make sure that all of the circuit connections are valid. Also, verify component polarity.
- Check for syntax mistakes. Make sure that you used the correct SPICE units (i.e. MEG instead of M(milli) for 1E6).
- Make sure that there is a DC path from every node to ground.
- Make sure that voltage/current generators use realistic values, especially for rise and fall time
- Make sure that dependent source gains are correct, and that E/G element expressions are reasonable. If you are using division in an expression, verify that division by zero cannot occur or protect against it with a small offset in the denominator.

1. Increase ITL1 to 400 in the .OPTIONS statement.

Example: `.OPTIONS ITL1=400`

This increases the number of DC iterations that PSpice will perform before it gives up. In all but the most complex circuits, further increases in ITL1 won't typically aid convergence.

2. Add .NODESETs

Example: `.NODESET V(6)=0`

View the node voltage/branch current table in the output file. PSpice produces one even if the circuit does not converge. Add `.NODESET` values for the top level circuit nodes (not the subcircuit nodes) that have unrealistic values. You do not need to nodeset every node. Use a `.NODESET` value of 0V if you do not have a better estimation of the proper DC voltage. Caution is warranted, however, for an inaccurate Nodeset value may cause undesirable results.

3. Add resistors and use the OFF keyword.

Example: `D1 1 2 DMOD OFF`
`RD1 1 2 100MEG`

Add resistors across diodes in order to simulate leakage. Add resistors across MOSFET drain-to-source connections to simulate realistic channel impedances. This will make the

impedances reasonable so that they will be neither too high nor too low. Add ohmic resistances (RC, RB, RE) to transistors. Use the .Options statement to reduce Gmin by an order of magnitude.

Next, you can also add the OFF keyword to semiconductors (especially diodes) that may be causing convergence problems. The OFF keyword tells PSpice to first solve the operating point with the device turned off. Then the device is turned on, and the previous operating point is used as a starting condition for the final operating point calculation.

4. Use PULSE statements to turn on DC power supplies.

Example: `VCC 1 0 15 DC`
becomes `VCC 1 0 PULSE 0 15`

This allows the user to selectively turn on specific power supplies. This is sometimes known as the “Pseudo-Transient” start-up method. Use a reasonable rise time in the PULSE statement to simulate realistic turn on. For example,

`V1 1 0 PULSE 0 5 0 1U`

will provide a 5 volt supply with a turn on time of 1 μ s. The first value after the 5 (in this case, 0) is the turn-on delay, which can be used to allow the circuit to stabilize before the power supply is applied.

5. Add UIC (Use Initial Conditions) to the .TRAN statement.

Example: `.TRAN .1N 100N UIC`

Insert the UIC keyword in the .TRAN statement. Use Initial Conditions (UIC) will cause PSpice to completely bypass the DC analysis. You should add any applicable .IC and IC= initial conditions statements to assist in the initial stages of the transient analysis. Be careful when you set initial conditions, for a poor setting may cause convergence difficulties.

AC Analysis Note: Solutions 4 and 5 should be used only as a last resort, because they will not produce a valid DC operating point for the circuit (all supplies may not be turned on and circuit may not be properly biased). Therefore, you cannot use solutions 4 and 5 if you want to perform an AC analysis, because the AC analysis must be preceded by a valid operating point solution. However, if your goal is to proceed to the transient analysis, then solutions 4 and 5 may help you and may possibly uncover the hidden problems which plague the DC analysis.

Transient Convergence Solutions

0. Check circuit topology and connectivity.

This item is the same as item 0 in the DC analysis.

1. Set RELTOL=0.01 or 0.005 in the .OPTIONS statement.

Example: `.OPTIONS RELTOL=0.01`

This option is encouraged for most simulations, since the reduction of Reltol can increase

the simulation speed by 10 to 50%. Only a minor loss in accuracy usually results. A useful recommendation is to set Reltol to 0.01 for initial simulations, and then reset it to its default value of .001 when you have the simulation running the way you like it and a more accurate answer is required. Setting Reltol to a value less than .001 is generally not required.

2. Set I TTL4=500 in the .OPTIONS statement.

Example: .OPTIONS I TTL4=500

This increases the number of transient iterations that SPICE will attempt at each time point before it gives up. Values which are greater than 500 or 1000 won't usually bring convergence.

3. Reduce the accuracy of ABSTOL/VNTOL if current/voltage levels allow it.

Example: .OPTION ABSTOL=1N VNTOL=1M

Abstol and Vntol should be set to about 8 orders of magnitude below the level of the maximum voltage and current. The default values are Abstol=1p and Vntol=1u. These values are generally associated with IC designs.

4. Realistically Model Your Circuit; add parasitics, especially stray/junction capacitance.

The idea here is to smooth any strong nonlinearities or discontinuities. This may be accomplished via the addition of capacitance to various nodes and verifying that all semiconductor junctions have capacitance. Other tips include:

- Use RC snubbers around diodes.
- Add capacitance for all semiconductor junctions (3pF for diodes, 5pF for BJTs if no specific value is known).
- Add realistic circuit and element parasitics.
- Watch the real-time waveform display and look for waveforms that transition vertically (up or down) at the point during which the analysis halts. These are the key nodes which you should examine for problems.
- If the .Model definition for the part doesn't reflect the behavior of the device, use a subcircuit representation. This is especially important for RF and power devices such as RF BJTs and power MOSFETs. Many model vendors cheat and try to "force fit" the SPICE .MODEL statement in order to represent a device's behavior. This is a sure sign that the vendor has skimped on quality in favor of quantity. Primitive level 1 or 3 .MODEL statements CAN NOT be used to model most devices above 200MEGhz because of the effect of package parasitics. And .MODEL statements CAN NOT be used to model most power devices because of their extreme nonlinear behavior. In particular, if your vendor uses a .MODEL statement to model a power MOSFET, throw away the model. It's almost certainly useless for transient analysis.

5. Reduce the rise/fall times of the PULSE sources.

Example: VCC 1 0 PULSE 0 1 0 0 0
becomes VCC 1 0 PULSE 0 1 0 1U 1U

Again, we are trying to smooth strong nonlinearities. The pulse times should be realistic, not ideal. If no rise or fall time values are given, or if 0 is specified, the rise and fall times will be set to the TSTEP value in the .TRAN statement.

6. Add UIC (Use Initial Conditions) to the .TRAN line.

Example: .TRAN .1N 100N UIC

If you are having trouble getting the transient analysis to start because the DC operating point can't be calculated, insert the UIC keyword in the .TRAN statement (skip initial transient solution). UIC will cause PSpice to completely bypass the DC analysis. You should add any applicable .IC and IC= initial conditions statements to assist in the initial stages of the transient analysis. Be careful when you set initial conditions, for a poor setting may cause convergence difficulties.

Modeling Tips

Device modeling is one of the hardest steps encountered in the circuit simulation process. It requires not only an understanding of the device's physical and electrical properties, but also a detailed knowledge of the particular circuit application. Nevertheless, the problems of device modeling are not insurmountable. A good first-cut model can be obtained from data sheet information and quick calculations, so the designer can have an accurate device model for a wide range of applications.

Data sheet information is generally very conservative, yet it provides a good first-cut of a device model. In order to obtain the best results for circuit modeling, follow the rule: "Use the simplest model possible". In general, the SPICE component models have default values that produce reasonable first order results. Here are some helpful tips:

- Don't make your models any more complicated than they need to be. Overcomplicating a model will only cause it to run more slowly, and will increase the likelihood of an error.
- Remember: modeling is a compromise.
- Don't be afraid to pull apart your circuit and test individual sections or even models, especially the ones you did not create.
- Create subcircuits which can be run and debugged independently. Simulation is just like being at the bench. If the simulation of the entire circuit fails, you should break it apart and use simple test circuits to verify the operation of each component or section.
- Document the models as you create them. If you don't use a model often, you might forget how to use it.
- Be careful when you models which have been produced by hardware vendors. Many have limitations on the operating point bounds for which they can be used.

- Semiconductor models should always include junction capacitance and the transit time (AC charge storage) parameters.
- If the .Model definition for a large geometry device doesn't reflect the behavior of the device, use a subcircuit representation.
- Be careful when using behavioral models for power devices. Many models are not thoroughly tested and work at one operating point but are highly inaccurate at other operating points.
- And lastly, there is no substitute for knowing what you're doing!!

Chapter 4 - Library Listings

Power FET Drivers

Power MOS/IGBT D	Vendor	Library	Description
IR2110	IR	IR_Driver	Hi and Lo Side Drivers
IR2110S	IR	IR_Driver	Hi and Lo Side Drivers
RIC7113	IR	IR_Driver	Hi and Lo Side Drivers
Si4724CY	Vishay	Vishay	N-Channel Synchronous MOSFETs with Break-Before-Make, See Si4724CY.pdf
Si4768CY	Vishay	Vishay	N-Channel Synchronous MOSFETs with Break-Before-Make
Si4770CY	Vishay	Vishay	N-Channel Synchronous MOSFETs with Break-Before-Make
HIP2100	Intersil	Intersil	100VDC – 2A Half Bridge Driver
HIP2101	Intersil	Intersil	100V Half Bridge N-Channel
HIP6601B	Intersil	Intersil	MOSFET Driver, Dual N-Channel
HIP6602B	Intersil	Intersil	Synchronous Rectified Buck MOSFET
UCC37324DGN	TI	TI_Driver	Dual 4 A Peak High Speed Low-Side Power MOSFET Drivers
MIC4421	Micrel	Micrel	9A-Peak Low-Side MOSFET Driver
MIC4422	Micrel	Micrel	9A-Peak Low-Side MOSFET Driver
MIC4427	Micrel	Micrel	Dual 1.5A-Peak Low-Side MOSFET Driver

Linear ICs

Linear	Vendor	Library	Description
AD524S	AD	ADI_Linear	Analog Multiplier, See AD524S.pdf
AD534	AD	ADI_Linear	Instrumentation Amp, See AD534T.pdf
AD8099	AD	ADI_Linear	Op-amp, See AD8099.pdf

Power ICs

Power IC Models	Vendor	Library	Description
ML4863	Microlineai	Microlinear	Boost Regulators for Battery Powered Applications
LT1242	Linear Tec	LT_Power	High Speed Current Mode Pulse Width Modulators
LT1242S	Linear Tec	LT_Power	State space average model
LT1243	Linear Tec	LT_Power	High Speed Current Mode Pulse Width Modulators
LT1243S	Linear Tec	LT_Power	State space average model
LT1244	Linear Tec	LT_Power	High Speed Current Mode Pulse Width Modulators
LT1244S	Linear Tec	LT_Power	State space average model
LT1245	Linear Tec	LT_Power	High Speed Current Mode Pulse Width Modulators
LT1245S	Linear Tec	LT_Power	State space average model
UC1637	TI	TI_Power	Switched Mode Controller for DC Motor Drive
UC1823	TI	TI_Power	High Speed PWM Controller
UC1824	TI	TI_Power	High Speed PWM Controller
UC1825	TI	TI_Power	High Speed PWM Controller
UC1842	TI	TI_Power	Current Mode PWM Controller
UC1842A	TI	TI_Power	Current Mode PWM Controller
UC3842B	On Semi	TI_Power	Current Mode, See UC384x.pdf
UC1842S	TI	TI_Power	State Space Average Model
UC1842AS	TI	TI_Power	State Space Average Model
UC1843	TI	TI_Power	Current Mode PWM Controller
UC1843A	TI	TI_Power	Current Mode PWM Controller
UC3843B	On Semi	TI_Power	Current Mode, See UC384x.pdf
UC1843S	TI	TI_Power	State Space Average Model
UC1843AS	TI	TI_Power	State Space Average Model
UC1844	TI	TI_Power	Current Mode PWM Controller
UC1844A	TI	TI_Power	Current Mode PWM Controller
UC3844B	On Semi	TI_Power	Current Mode, See UC384x.pdf
UC1844S	TI	TI_Power	State Space Average Model
UC1844AS	TI	TI_Power	State Space Average Model
UC1845	TI	TI_Power	Current Mode PWM Controller
UC1845A	TI	TI_Power	Current Mode PWM Controller
UC3845B	On Semi	TI_Power	Current Mode, See UC384x.pdf
UC1845S	TI	TI_Power	State Space Average Model
UC1845AS	TI	TI_Power	State Space Average Model
UC1846	TI	TI_Power	Current Mode PWM Controller
UC3854	TI	TI_Power	Enhanced High Power Factor Preregulator
UC3854B	TI	TI_Power	Enhanced High Power Factor Preregulator
UC1871	TI	TI_Power	Resonant Fluorescent Lamp Driver
UC1872	TI	TI_Power	Resonant Fluorescent Lamp Ballast Controller
UC1875	TI	TI_Power	Phase Shift Resonant Controller
UC1876	TI	TI_Power	Phase Shift Resonant Controller
UCC1806	TI	TI_Power	Low Power, Dual Output, Current Mode PWM Controller
UCC2808	TI	TI_Power	Current Mode Push-Pull PWM With Programmable Slope Compensation
UCC3895	TI	TI_Power	BiCMOS Advanced Phase Shift PWM Controller
UA723	TI	TI_Power	Precision Voltage Regulator

Power IC Models	Vendor	Library	Description
CS322	On Semi	ON_Power	High Speed PWM Controller
CS324	On Semi	ON_Power	High Speed PWM Controller
CS51220	On Semi	ON_Power	Feed Forward Voltage Mode PWM Controller with Programmable Synchronization
CS51411	On Semi	ON_Power	1.5A, 260kHz Low Voltage Buck Regulators
CS5155	On Semi	ON_Power	CPU 5-Bit Synchronous Buck Controller
CS5156	On Semi	ON_Power	CPU 5-Bit Nonsynchronous Buck Controller
CS5171	On Semi	ON_Power	1.5 A 280kHz Boost Positive Feedback Regulators
CS5172	On Semi	ON_Power	1.5 A 280kHz Boost Negative Feedback Regulators
CS5173	On Semi	ON_Power	1.5 A 560kHz Boost Positive Feedback Regulators
CS5174	On Semi	ON_Power	1.5 A 560kHz Negative Feedback Boost Regulators
CS5307	On Semi	ON_Power	Four-Phase VRM 9.0 Buck Controller
CS5308	On Semi	ON_Power	Two-Phase PWM Controller with Integrated Gate Drivers for VRM 8.5
CS5322	On Semi	ON_Power	Two-Phase Buck Controller with Integrated Gate Drivers and 5-Bit DAC
CS5323	On Semi	ON_Power	Three-Phase Buck Controller with 5-Bit DAC
MC33063	On Semi	ON_Power	1.5A, Step-Up/Down/Inverting Switching Regulator
MC33064	On Semi	ON_Power	1.5A, Step-Up/Down/Inverting Switching Regulator
MC33161	On Semi	ON_Power	Universal Voltage Monitor
MC34163	On Semi	ON_Power	3.4A, Step-Up/Down/Inverting Switching Regulator
MC33262	On Semi	ON_Power	Power Factor Controller
NCP100	On Semi	ON_Power	Adjustable 0.9-6V \pm 1.7% Output Voltage 0.1-20mA Shunt Regulator
NCP1000	On Semi	ON_Power	Fixed-100kHz Switching Regulator with 700V / 0.5A Switch
NCP1000A	On Semi	ON_Power	Fixed-100kHz Switching Regulator with 700V / 0.5A Switch, average model, See NCP1000 SSA Model.pdf
NCP1001	On Semi	ON_Power	Fixed-100kHz Switching Regulator with 700V / 1A Switch
NCP1002	On Semi	ON_Power	Fixed-100kHz Switching Regulator with 700V / 1.5A Switch
NCP1203P40	On Semi	ON_Power	40kHz PWM Current-Mode Controller for Universal Off-Line Supplies
NCP1203P60	On Semi	ON_Power	60kHz PWM Current-Mode Controller for Universal Off-Line Supplies
NCP1203P100	On Semi	ON_Power	100kHz PWM Current-Mode Controller for Universal Off-Line Supplies
NCP1203AV	On Semi	ON_Power	PWM Current-Mode Controller average model
NCP1400ASN19T1	On Semi	ON_Power	Up to 100mA, 1.9V, 180kHz Boost PWM Switching Regulator with Enable
NCP1400ASN30T1	On Semi	ON_Power	Up to 100mA, 3.0V, 180kHz Boost PWM Switching Regulator with Enable
NCP1400ASN50T1	On Semi	ON_Power	Up to 100mA, 5.0V, 180kHz Boost PWM Switching Regulator with Enable
NCP1570	On Semi	ON_Power	Low Voltage Synchronous Buck Controller
NCP1571	On Semi	ON_Power	Low Voltage Synchronous Buck Controller
TL431	On Semi	ON_Power	Adjustable 2.5-36V \pm 1% Tolerance 1-100mA Shunt Regulator
TLV431A	On Semi	ON_Power	Low Voltage Precision Adjustable Shunt Regulator
MC33201	On Semi	ON_Power	Low Voltage, Rail-to-Rail, Single Operational Amplifier
MC33202	On Semi	ON_Power	Low Voltage, Rail-to-Rail, Single Operational Amplifier
MC33204	On Semi	ON_Power	1V, Rail-to-Rail, Single Operational Amplifier
MC33501	On Semi	ON_Power	1V, Rail-to-Rail, Single Operational Amplifier
MC33502	On Semi	ON_Power	1V, Rail-to-Rail, Single Operational Amplifier
MC33503	On Semi	ON_Power	1V, Rail-to-Rail, Single Operational Amplifier
ISL6225	Intersil	Intersil	PWM Controller, Dual, Regulated Output Voltage 0.9V-5.5V
ISL6520a	Intersil	Intersil	PWM Controller, +5V Input, VOUT 0.8V Min @ 1.5%, 300kHz
ISL6520Assa	Intersil	Intersil	Average model
ISL6721	Intersil	Intersil	Single-Ended Current Mode PWM controller
ISL6721Av	Intersil	Intersil	Single-Ended Current Mode PWM controller , Average model
ISL6740	Intersil	Intersil	PWM controller for half bridge and bus converter, See ISL6740switching.pdf
ISL6740av	Intersil	Intersil	Average model, See ISL6740average.pdf
ISL6741av	Intersil	Intersil	PWM controller for hard-switched full bridge and push-pull applications, Average model
HA16163	Renesas	Renesas	Synchronous Phase Shift Full-Bridge Control IC, 480 kHz, See Application Circuit.pdf
LM78S40	National	Nat_Power	Universal Switching Regulator Subsystem
LP2953	National	National_LDO	Adjustable Micropower Low-Dropout Voltage Regulator, See LP2953A.pdf
TNY256	PI	PI_Power	TinySwitch with line under-voltage lockout, auto-restart

Semiconductors

Semiconductors	Vendor	Library	Description
57034, 57130, 57230	IR	IR_Semi	Power Mosfets
CMPD2004, CMPD3003, CMPD6001, CMDSH2-3, CMDSH-3, CMPD6263, CMHSH5-4, CMHSH5-2L, CMSH1-40M, CMSH1-60M, CMSH5-40, CMSH5-60, CMSH2-40M, CMSH2-60M, CSDH10-45L	CS	CS_Diodes	Diodes
CCL0035, CCL0130, CCL0300, CCL0500, CCL0750, CCL1000, CCL1500, CCL2000, CCL2700, CCL3500, CCL4500, CCL5750, CCLH080, CCLH100, CCLH120, CCLH150	CS	CS_Current_Dio	JFET Current Regulators
CMPTA44, CMPTA94, CMPT404A	CS	CS_BJTs	BJTs
Mi1020T	Marlow	Misc	Thermal-Electro Cooler, See TEC.Doc
53259, 53111, 53124, 53253, 53250	Micropac	Micropac_Relays	Solid-State Switches, See 53111.doc & 53250.doc
8CLJQ045, 8CLJQ045_Sub	IR	IR_Semi	Power Schottky, See 8CLJQ045.doc
SSR8045P	SSDI	Misc	Power Schottky
SFH615A-1, SFH615A-2, SFH615A-3, SFH615A-4	Vishay	Vishay	Optocoupler, Hi-Rel 5300Vrms
SFH610A-1, SFH610A-2, SFH610A-3, SFH610A-4	Vishay	Vishay	Optocoupler, Hi-Rel 5300Vrms
MOC8101, MOC8102, MOC8103, MOC8104, MOC8105, MOC8106, MOC8107, MOC8108	Fairchild	Fairchild	Optocoupler, Hi-Rel 5300Vrms
CNY17F-1, CNY17F-2, CNY17F-3, CNY17F-4	Fairchild	Fairchild	Optocoupler, Hi-Rel 5300Vrms

Generic Model Templates

Generic Models	Vendor	Library	Description	Parameters
Flyback	Generic	PowerSS	State Space average model for Flyback converters.	L=Primary inductance in Henries NC=Current transformer turns ratio NP=Power transformer turns ratio F=Switching frequency in Hz EFF=Efficiency RB=Current transformer burden resistor in ohms TS=Propagation delay time in the current loop in secs
Forward	Generic	PowerSS	State Space average model for Forward converters.	L=Primary inductance in Henries NC=Current transformer turns ratio NP=Power transformer turns ratio F=Switching frequency in Hz EFF=Efficiency RB=Current transformer burden resistor in ohms TS=Propagation delay time in the current loop in secs
Boost	Generic	PowerSS	State Space average model for Boost converters.	L=Primary inductance in Henries F=Switching frequency in Hz NC=Current transformer turns ratio NP=Power transformer turns ratio EFF=Efficiency RB=Current transformer burden resistor in ohms TS=Propagation delay time in the current loop in secs
MPP	Generic	Mags	MPP Core model. MPP55 Series	N= # of turns U= Permeability AL= Inductance reference of the core mHy/1000T ² LM=Magnetizing Inductance in Henries DCR=Series resistance in ohms IC=Initial Conditions
MPP2	Generic	Mags	MPP Core model. MPP58 Series	N= # of turns U= Permeability AL= Inductance reference of the core mHy/1000T ² LM=Magnetizing Inductance DCR=Series resistance in Ohms
Transformers	Generic	Mags	Transformers, Various topologies	Series resistance and turns ratio
CPWR	Generic	Misc	Constant Power Load	VKnee=Load is resistive below knee and then constant power for all voltages above that Power=Constant Power
SWhyste	Generic	Misc	Switch with hysteresis	Ron=On Resistance Roff=Off resistance VT=Threshold voltage (On/Off @ VT+VH, VT-VH) VH=Hysteresis voltage
CAT5	Generic	Misc	Category 5 Cable	L=Length in meters C= capacitance ESR1K= ESR at 1kHz ESL=Series Inductance RLEAK=Leakage Resistance IC=Initial Conditions
Tant, TANTwIC	Generic	TantCap	Tantulum Capacitor Model with and w/o Initial Conditions, See Capacitor.pdf	

Chapter 5 - References

General

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3. “Power Specialist's App Note Book, Papers on Simulation, Modeling and More”, Edited by Charles Hymowitz, <http://www.intusoft.com/lit/psbook.zip>
4. “Inline equations offer hysteresis switch in PSpice”, Christophe Basso, On Semiconductor, EDN, August 16, 2001