

SI4724CY N-Channel Synchronous MOSFETs

1.0 Scope

This document contains a description of the SPICE model and test and application circuits for the Vishay Si4724CY N-Channel Synchronous MOSFETs with Break-Before-Make.

Analysis:	FET Driver
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Last Rev Date:	6/3/2003
Publication Number:	SI4724CY.DOC
SPICE File	Vishay.Lib

2.0 Functional Description

The SI4724CY is a high speed driver designed to operate in high frequency dc-dc switch mode power supplies. It is designed to be used with any single output PWM IC or ASIC to produce a highly efficient synchronous rectifier converter. Under-voltage protection is provided for the Vdd power supply. The device includes a bootstrap diode, integrated Schottky diode, and fast switching times.

3.0 Model Description

The driver circuit was decomposed into elemental blocks, and then modeled accordingly as per the data sheet and specific topological IC information provided to AEi Systems by Vishay's engineers.

PSpice models for the output MOSFETs, bootstrap PNP diode, and the Schottky diode, Si4830ADY, were provided and used in the modeling of the SI4724CY. No efforts were made to improve the models although they were reviewed and comments are shown below.

Using SPICE a model of the driver was then created using the modules and a corresponding schematic and netlist was generated.

The model includes the following functionality and features:

- Proper transient response including variations with external components.
- Proper connectivity as per the real-life part
- Output rise and fall times for varying loads
- Under voltage lockout & hysteresis
- Switching times (turn off and propagation delays)
- Schottky behavior
- Bootstrap voltage and diode characteristics
- Logic input voltage thresholds
- Break-before-make reference

Note: The variation of the Vref and logic input voltage levels with Vdd are not modeled.

3.1 Assumptions

- Behavior is based on typical values given in the specification sheet for operation at 27 °C.
- Some thermal variations are modeled including some FET related parameters and the propagation delay and are represented in the subcircuit.

4.0 Model Verification

The test circuit described in the data sheet as Figure 4 was created, and shown in figure 4.1. The model was tested as per the manufacturer’s datasheet using component values provided by Vishay.

The results of the simulation performance for various model aspects are shown in the following figures.

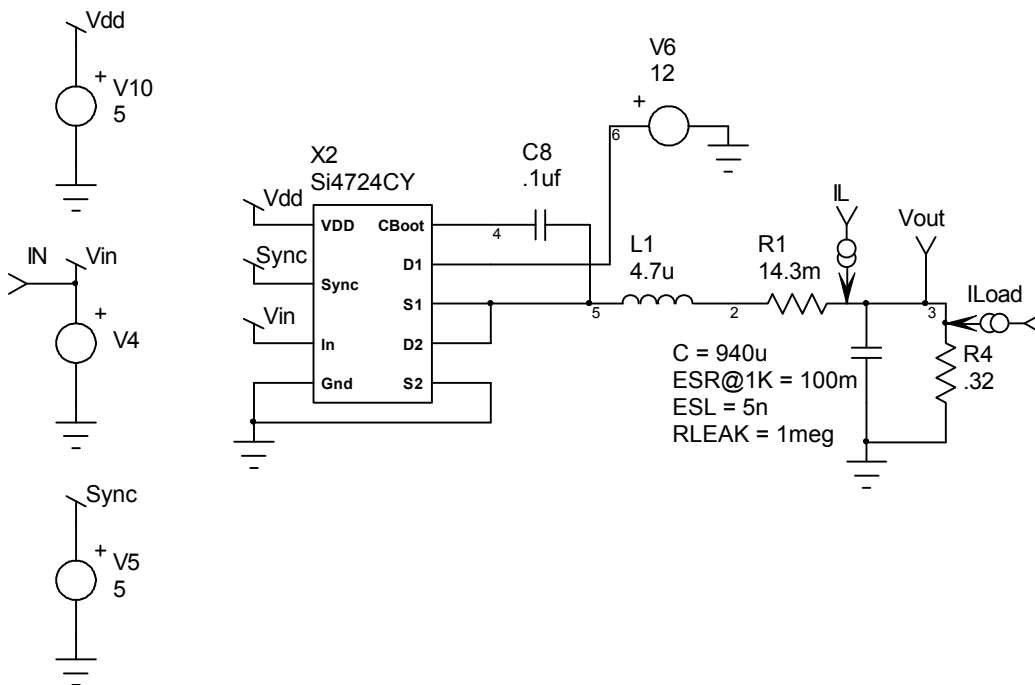


Figure 4.1: SPICE schematic diagram of the SI4724CY switching test circuit. The configuration in Figure 3.1 and this schematic were used for propagation delay, delay matching, and rise/fall time tests. Capacitor ESR/ESL and leakage were estimated.

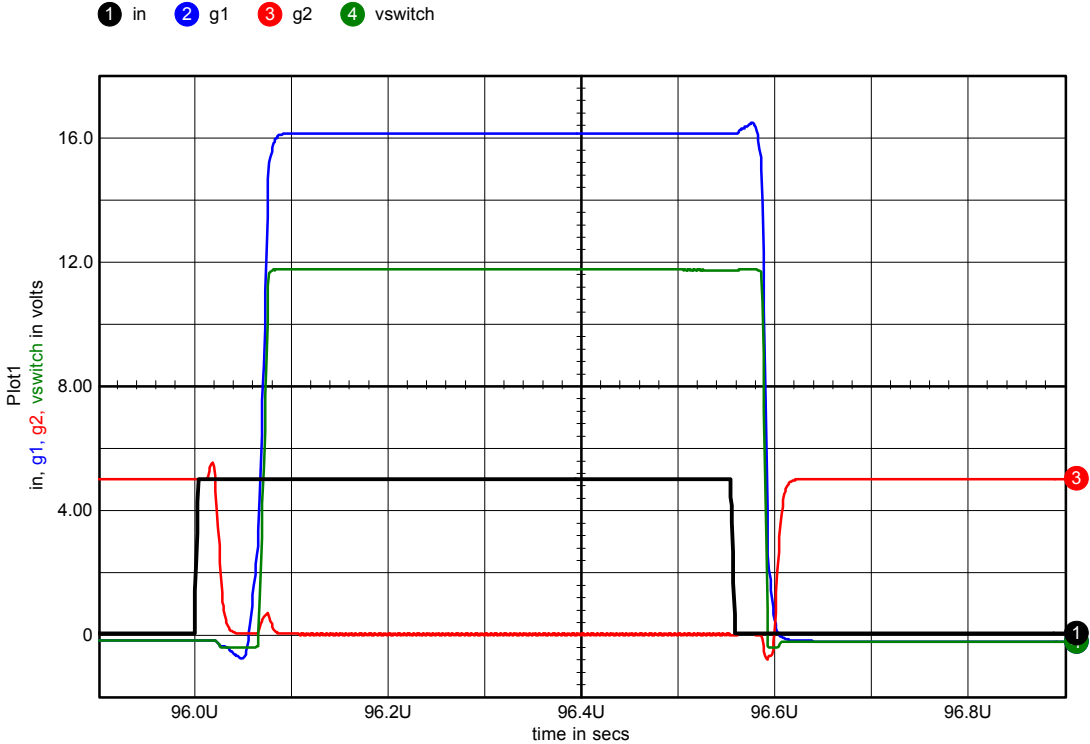


Figure 4.2: Single input pulse simulation results. Note the dip in Vswitch (green waveform).

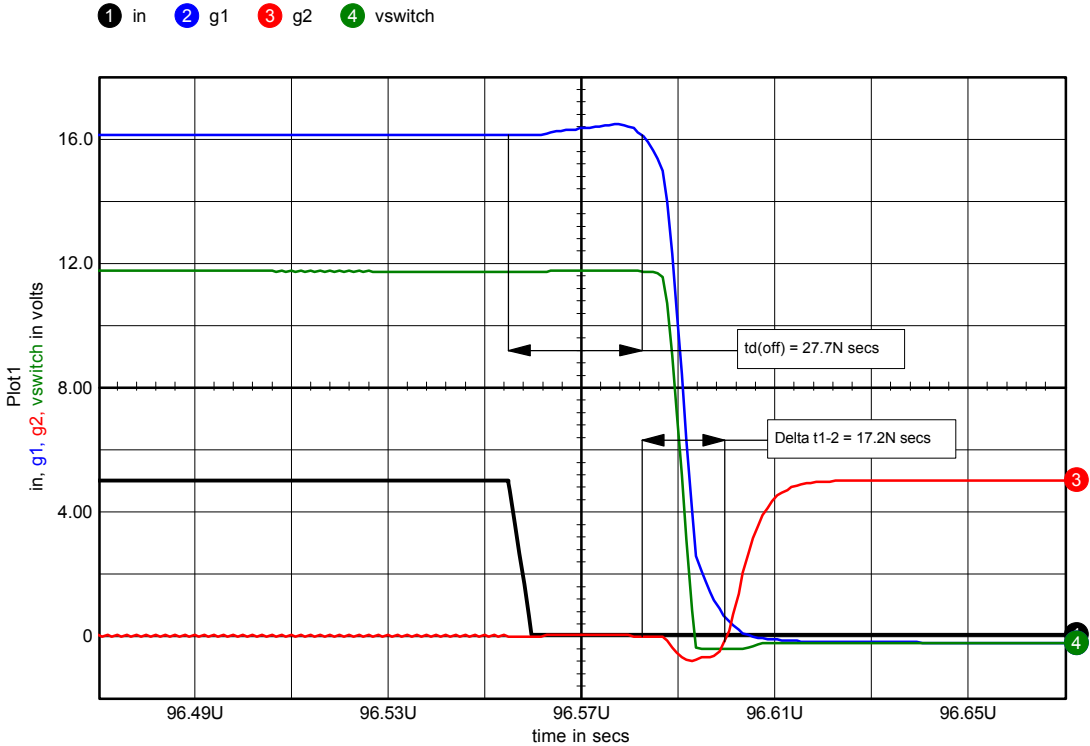


Figure 4.3: Delta t1-2 Propagation delay simulation results (falling edge of IN).

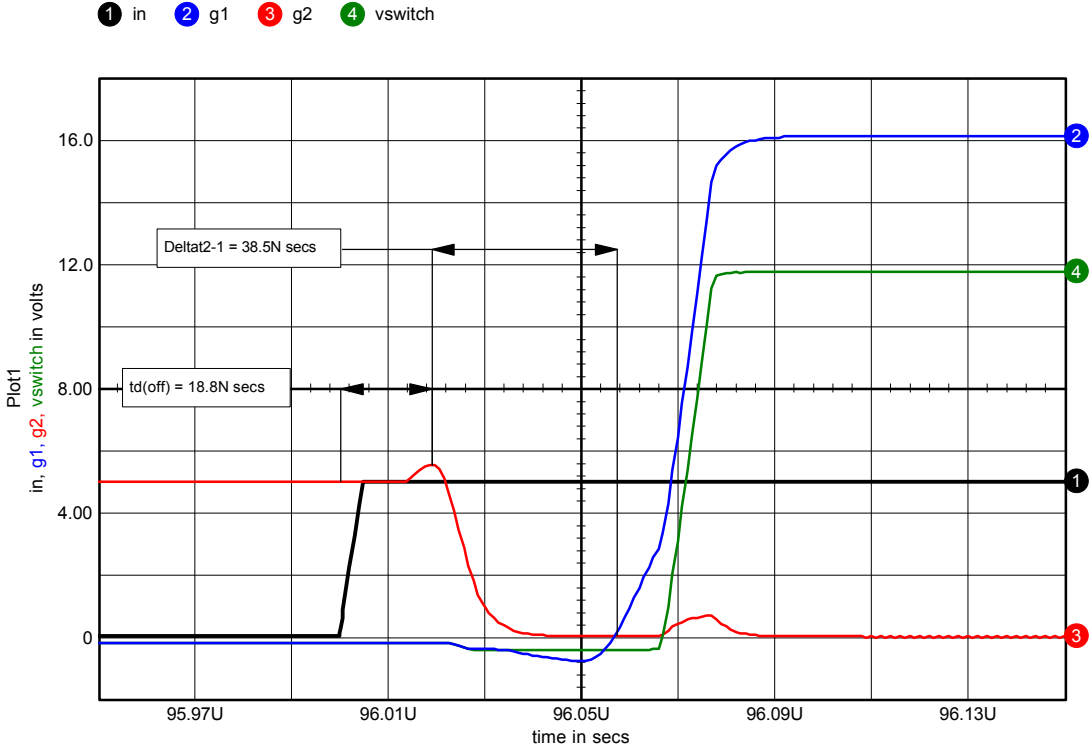


Figure 4.4: Delta t2-1 Propagation delay simulation results (rising edge of IN).

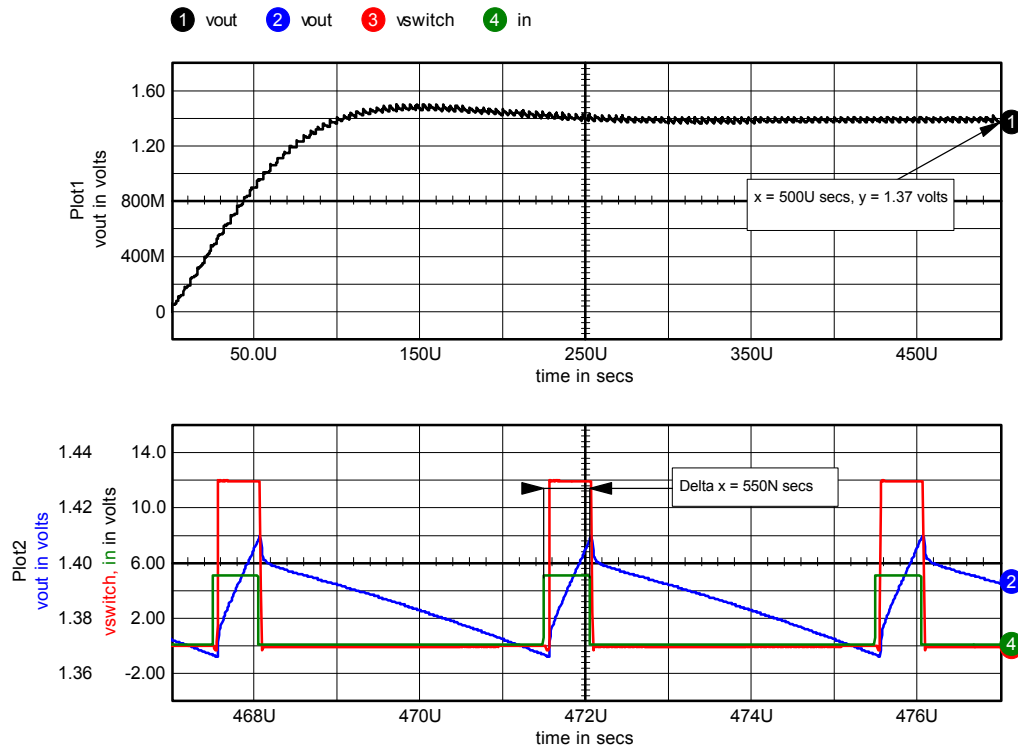


Figure 4.5: Startup simulation shows VOUT (top graph) and Vout, Vswitch (S1/D1), and IN (bottom graph).

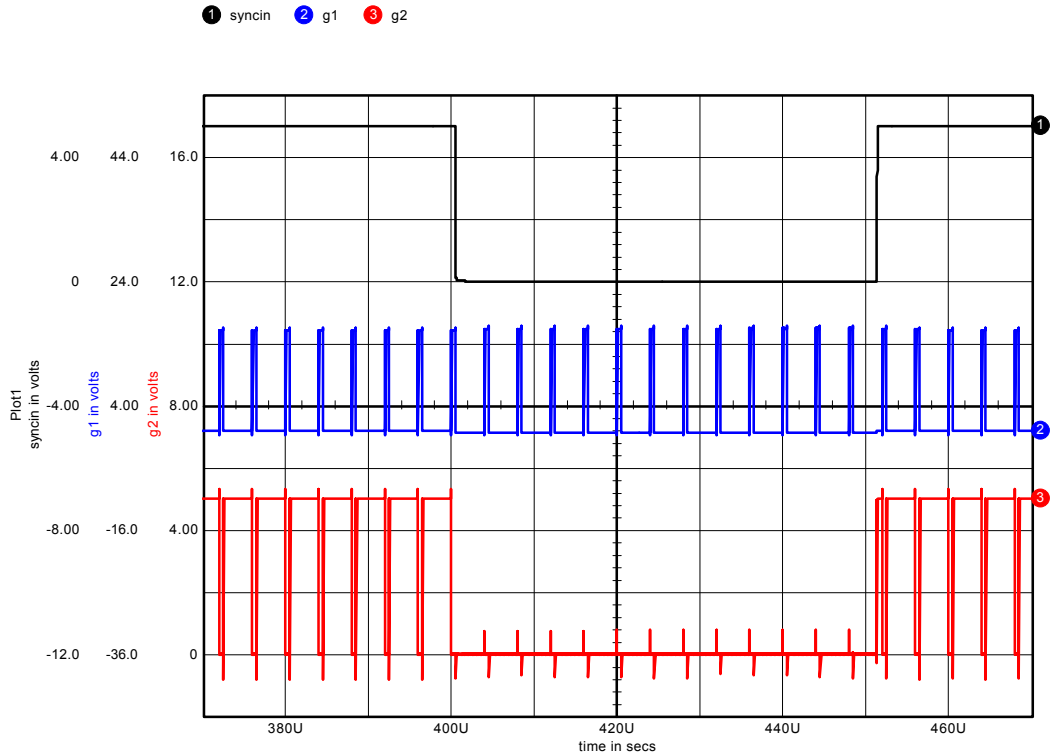


Figure 4.6 Response of the G1 and G2 signals for Sync pulse.

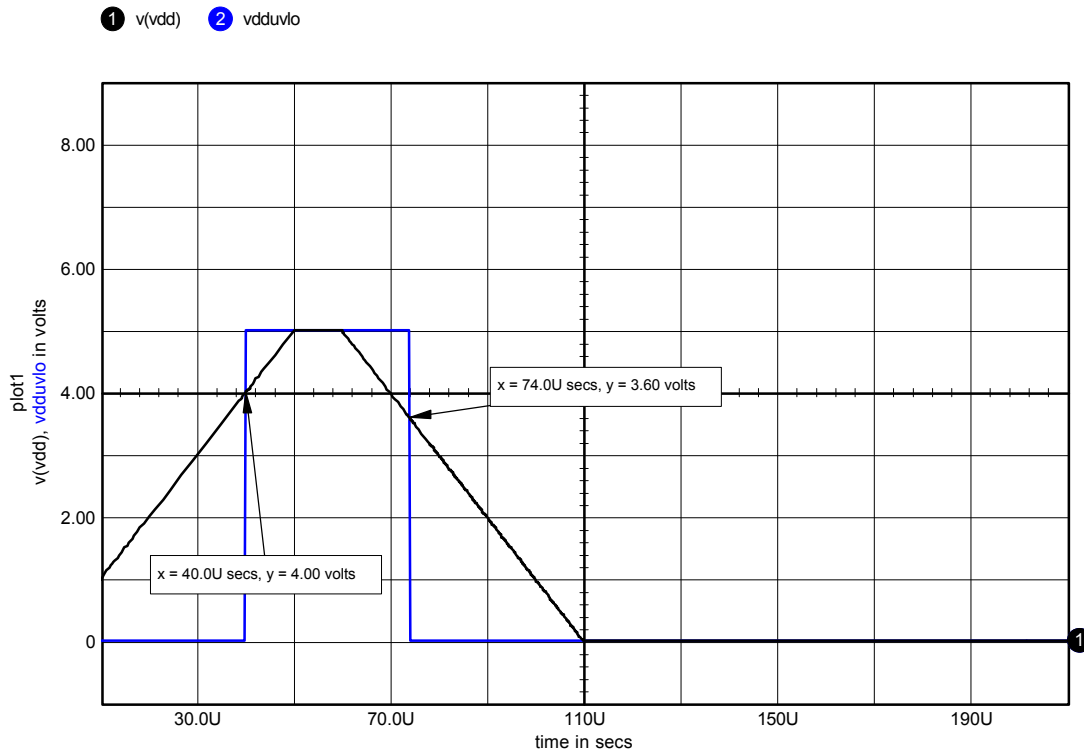


Figure 4.7 Turn-on/Turn-off and hysteresis for VDD.

4.1 Model Comments

The Schottky model provided by Vishay had a value of 0.9 for EG, energy gap and 0.50 for the XTI, saturation temperature exponent, model parameters. Normally, Schottky diodes have an EG value of 0.69 and XTI=2. Any other parameters should be experimentally verified. The series resistance, RS, has also been set to zero, an unrealistic value.

The Power MOSFET model is somewhat less sophisticated than AEi developed models and models contained in the Intusoft package. It is not clear how some key power MOSFET effects are modeled using the provided topology. Convergence problems have been experienced with this structure and other simplified Power MOSFET structures in certain types of simulation.

The reader is referred to three references on this topic.

- 1) "Power Requirements for Power MOSFET Models", I Budihardjo, Peter Lauritzen, A. Mantooh, IEEE Transactions on Power Electronics, Vol 12, No. 1, Jan 1997
- 2) "An Improved Mosfet Spice Model, Supports the development of Low Dropout Voltage Regulators", Steven M. Sandler, EDATools Café & Internal AEi White Paper, www.edatoolscafe.com/DACafe/TECHNICAL/Papers/Mosfet_paper.htm
- 3) "SPICE Model for TMOS", C.E. Cordonnier, Motorola Application Note, AN1043, 1989.

5.0 Conclusions

The model of the SI4724CY driver correlates very well with the manufacturer's datasheet and meets all of the items listed in the Statement of Work (SOW). This data should be verified against actual hardware for further confirmation.

The output voltage (1.4V) is somewhat less than the 1.6V that should be achieved with an input pulse width of 545us (0.545u/4u). The reason for this is unknown.

The variation of the Vref and logic input voltage levels with Vdd are not modeled but could be added.