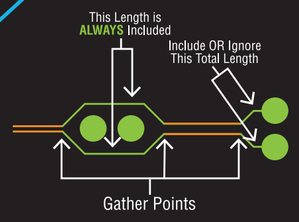
The Anatomy of a Differential Pair

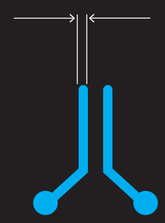
Design Guidelines to Keep in Mind When Working with Differential Pairs

PIN PITCH



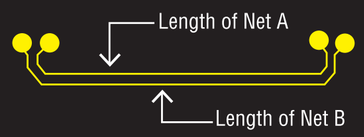
- Choose whether to **Include** or **Ignore**
- If included, the etch gap or from etch gather point) is needed when calculating the max uncoupled length.

MIN LINE WIDTH



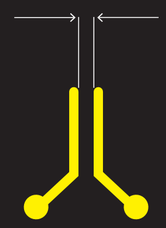
- The trace width that should be used to route the differential pair nets the majority of the time
- The width you prefer your differential pairs to be routed

PHASE TOLERANCE



- Allowable difference in length between the differential pair nets
- Phase tolerance is the timing (Flight Time) of the signal leaving the drive and getting to the receiver in phase (together)

PRIMARY GAP



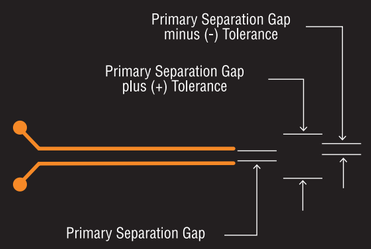
- The spacing, edge-to-edge, that should be used to route the differential pair nets the majority of the time
- The rule you prefer your differential pairs to follow
- This only applies to the two differential pair nets. Other net spacing to the differential pair nets is controlled by the Spacing Rule set Line to Line clearance

Note: The stackup of the board drives the line width and gap, so be sure to check in with your fabricators

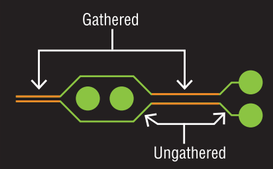
SEPARATION GAP TOLERANCE

Coupled Tolerance (+)/(-)

- Provides a coupling range based on the primary Separation Gap
- Summing Primary Separation Gap and Coupled Tolerance (+) provides the maximum coupled gap
- Subtracting Primary Separation Gap and Coupled Tolerance (-) provides the minimum coupled gap
- Values above or below these become an uncoupling event



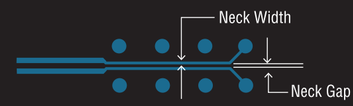
MAX UNCOUPLED LENGTH



- The trace width that should be used to route the differential pair nets the majority of the time.
- The width you prefer your differential pairs to be routed

NECK WIDTH & NECK GAP

- Rules to be applied when the traces must “squeeze” down to be routed between pins/vias (for example, in BGA areas)
- Neck Gap is the new spacing, edge to edge, that should be used to route the differential pair
- Neck width is the new trace width that should be used to route the differential pairs



These differential pair design guidelines are just a few of the many items engineers must verify in their attempt to prevent sending a bad design to production. With the number of constraints and managed nets continuing to increase, keeping track of rules becomes an arduous task. Implementing a constraint-aware CAD environment allows design teams to embed their design intent directly into their CAD data at both the schematic and PCB stage. This ensures everyone stays in-sync throughout the design process. Simply put, a constraint-driven environment helps design teams reduce errors due to miscommunication and achieve production-ready designs faster.

For more information about a Constraint-Driven PCB Design Environment, visit:

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