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Cadence Sigrity Technology

Sigrity™ technology integrates seamlessly with Cadence® Allegro® PCB and IC packaging design solutions to deliver a complete power-aware design and signal integrity analysis solution. These production-proven tools enable power delivery system analyses across chip-package-board; system-level signal integrity analysis of high-speed signal transmissions; and, advanced physical design for single- and multi-chip packages, state-of-the-art 3D packages, and systems-in-package.

Power Integrity

Cadence Power Integrity (PI) solutions, originally developed by Sigrity, provide signoff-level accuracy for AC and DC power analysis of printed circuit boards (PCBs) and integrated circuit (IC) packages:

Sigrity PowerSI®: An advanced signal integrity, PI, and design-stage electromagnetic interference (EMI) solution. Supports S-parameter model extraction and provides robust frequency domain simulation for entire IC package and PCB designs.

Sigrity PowerDC™: An efficient DC signoff solution for IC package and PCB designs, with electrical/thermal co-simulation to maximize accuracy. Quickly pinpoints IR drop and current hotspots. Automatically finds best remote sense locations.

Sigrity OptimizePI™: A highly automated board and IC package AC frequency analysis solution. Supports pre-and post-layout decap studies, identifies impedance issues, and suggests placement locations for EMI decaps. Decap implementations are optimized for performance and cost.

Power-Aware SI

Cadence Power-Aware Signal Integrity (SI) tools, originally developed by Sigrity, provide signoff-level-accurate SI analysis for PCBs and IC packages. These tools are critical to signoff-level SI accuracy of signals with frequencies higher than 1GHz, which must consider the signals and the power/ground network that enables the current return path.

Sigrity SPEED2000™: A complete PCB/package layout-based time domain EM simulation tool for SI, PI, and design-stage EMI analysis. Supports advanced layout checking for design signoff and debug.

Sigrity SystemSI™: A comprehensive and automated SI environment for the accurate assessment of high-speed chip-to-chip system designs. Ensures robust parallel bus and serial link interface implementations.

Sigrity Broadband SPICE®: A combination of S-parameter checking, tuning, and extraction capability to convert N-port network parameters to efficient SPICE-compatible circuits that can be used in time domain simulations.

Sigrity Transistor-to-Behavioral (T2B™) Model Conversion: T2B model conversion is an efficient way to create accurate models for SSO and other simulations. These models run an order of magnitude faster than the original transistor models.

Package Design and Assessment

Cadence Package Design and Assessment tools, originally developed by Sigrity, provide IC package design, analysis, and model extraction capability—and can exchange data with Cadence System-in-Package (SiP) Layout and Allegro Package Designer. Assessment capabilities allow you to quickly spot potential SI and PI issues. Model extraction capabilities provide unique full package model extraction with accuracy into the multi-GHz frequency range.

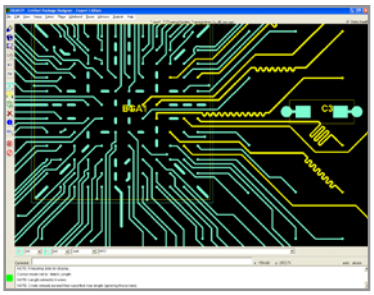

Figure 1: Sigrity Unified Package Designer

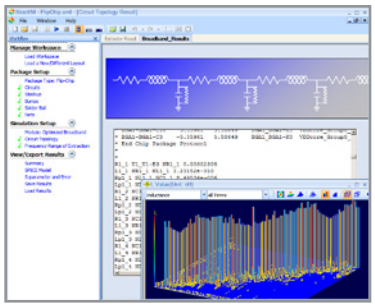

Figure 2: Sigrity XtractIM

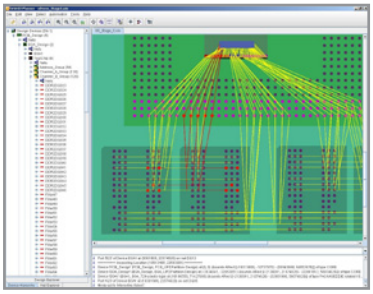

Figure 3: Sigrity OrbitIO Planner

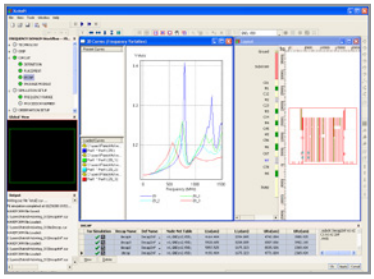

Figure 4: Sigrity XcitePI

Sigrity Unified Package Designer™ (UPD): A versatile, analysis-driven package design environment. Supports a broad range of wirebond, flip-chip, and leadframe packages including single-die BGAs and SiP implementations.

Sigrity XtractIM™: A fast IC package RLC extraction and assessment solution with an option to generate highly accurate broadband models. Supports a broad range of package types including BGA, SiP, and leadframe.

Co-Design

Sigrity Co-Design products complement the Cadence SiP Co-Design solution by providing early system prototyping and co-analysis capability. They enable coordinated chip-package-board planning for system optimization, resulting in shorter cycle times and maximum performance. The results and output of these products serve as a starting point for physical implementation.

Sigrity OrbitIO™: A co-design solution for rapid system prototyping and pad ring planning in single/multi-die package configurations. Supports flip-chip, wirebond, and RDL feasibility using industry-standard data from IC, package, and PCB tools.

Sigrity XcitePI™: A full-chip PI solution targeting chip/system co-simulation applications. Supports early chip power planning, I/O and core power model extraction, and simulation in both time and frequency domains.

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Cadence is transforming the global electronics industry through a vision called EDA360. With an application-driven approach to design, our software, hardware, IP, and services help customers realize silicon, SoCs, and complete systems efficiently and profitably. www.cadence.com