SUCCESS STORY

CADENCE AND BAYSIDE DESIGN, INC.

Cadence Allegro Platform Enables Low-Cost, High-Density Build-Up Package For 6.5G SerDes IC

"If we had been using a multivendor design solution on this project, I don't think we would have been able to meet the schedule. The superior performance and integration of the design tools in the Allegro platform gave us the confidence that we could deliver quality results on a very tight deadline."

Kevin Roselle, *Chief Technical Officer, Bayside Design, Inc.*

CORPORATE PROFILE

• Bayside Design specializes in high-speed interconnect engineering design services

DESIGN CHALLENGE

• Develop a complete evaluation system for 6.5-Gbps SerDes design, including package, board, FPGA, and software for debug

• Complete project in eight weeks

CADENCE SOLUTION

• Upgraded design environment with Cadence Allegro® system interconnect design platform

CADENCE PRODUCTS AND SERVICES

• Cadence Allegro Package Designer/Allegro Package SI

• Cadence Allegro PCB SI

• Cadence Allegro Design Entry HDL

COLLABORATING ON A STATE-OF-THE-ART PACKAGE

Cadence Engineering Services was developing a next-generation 6.5G SerDes macro to put in their IP Gallery. To prove commercial viability, the team decided to develop a test chip using a low-cost organic substrate 3-2-3 High Density Build-Up (HDBU) flipchip package.

The Cadence team designed and fabricated the chip, but needed a partner to complete the IC package and testboard. They found Bayside Design, Inc. to be the best equipped to take on such a complex, high-speed design challenge. Using the Cadence® Allegro® design platform together with Bayside expertise, the team developed a working, state-of-the-art organic HDBU package costing only half as much as a ceramic substrate package.

ADDRESSING PACKAGING COST AND PERFORMANCE

As packaging costs continue to rise, semiconductor manufacturers are facing a significant challenge. How can they deliver high-performance chips without moving to more expensive substrates? Signaling speeds of 3.125 Gbps are common, and new designs have high-speed serial interfaces of 6 to 10 Gbps and higher. Using a traditional, lower-cost package presents significant challenges for high-performance chips, especially for those with high-speed serial channels. Success requires careful attention to design of the complete signal interface, from die bumps to PCB contacts.

Headquartered in Milpitas, CA, Bayside Design is a high-performance interconnect design and analysis company focusing on the challenge of highspeed design. They design signal integrity (SI) compliant packages, working with engineering teams to create the minimum layer count

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to enable desired performance. This expertise was critical for the Cadence IP project. The Cadence 6.5-Gbps chip contained 16 SerDes, each with a differential, bi-directional link. Because IP customers are concerned about both cost and performance, the goal was to achieve maximum performance using a low-cost, organic substrate. Other vendors indicated that they might be able to achieve the desired speed on four lanes. Only Bayside demonstrated the expertise to address the challenge for all 32 lanes required by the design.

HIGH-SPEED SERIAL I/O CHALLENGES DESIGN

The Cadence team had already designed and fabricated the SerDes test chip along with the supporting logic functions. "One of the most important decisions for this project was choosing a package that could handle the high-speed performance requirements of the design without escalating the cost of the chip," said Kevin Roselle, Chief Technical Officer at Bayside Design. The Bayside team chose a 3-2-3 HDBU substrate (three top layers, a core with two metal layer cladding, and three bottom layers with the same buildup as the top layers).

At high speed, the signal can get distorted for a variety of reasons, including impedance mismatch, skin effect, dielectric losses, etc. Since the SerDes chip needed to be debugged at speed, there was a need to feed data on a continuous basis in full-duplex mode and also flag errors.

ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM SPEEDS PROCESS

To keep the SerDes project on schedule, Bayside would have to deliver the new package to Cadence by the time the chip came back from manufacture—in only eight weeks. But the project involved much more than just the package. The complete evaluation system included a package, a board, an FPGA, and debug software.

To accomplish this task, the Bayside team needed to augment their design flow with a more robust system interconnect solution—one capable of implementing high-speed constraints system-wide and controlling interconnect across the package and the board. The Cadence Allegro platform was the only solution that could deliver this capability. "The features in the Allegro platform are very powerful, and the tools work well in our design flow," continued Roselle. "We were able to enter constraints and check for violations. In addition, we were able to readily access reports and easily generate manufacturing data."

SUPERIOR DESIGN TOOL INTEGRATION ENABLES PROJECT SUCCESS

The tight integration of the tools in the Allegro platform reduced design time and allowed Bayside to deliver on schedule. They were able to define and capture constraints and have violations flagged in real time, eliminating time-consuming rework. In addition, the tight integration of extraction and simulation provided a major productivity boost.

"If we had been using a multi-vendor design solution on this project, I don't think we would have been able to meet the schedule," said Roselle. "The superior integration of the design tools in the Allegro platform gave us the confidence that we could deliver quality results on a very tight deadline."

"This project is a great example of how, with the right skills and design tools, you can deliver very advanced IP using conventional technology."

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