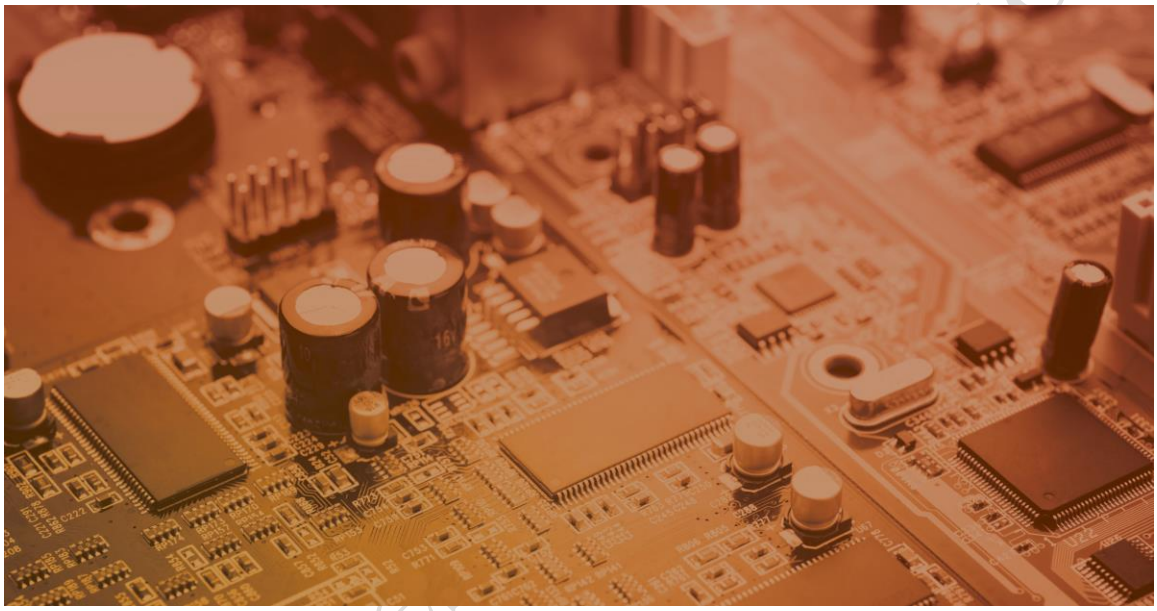
EMA Design Automation™



PCB Editor Essentials

Version 17.4

EMA Education Services

Classroom, on-site, and eLearning

OrCAD PCB Designer 17.4-2019 S004 (2/4/2020)

Version 1 March 12, 2020

Table of Contents

How to Use This Manual 10
Course Agenda 10
Appendices 10
Other Related Courses 11
Formatting Conventions 11
Lesson 1: PCB Editor User Interface 13
Learning Objectives 13
Version 17.4 Notations 13
Course Directory Structure 14
Primary PCB Editor Programs 15
PCB Editor Tools 16
Setting and Changing Your Working Directory 17
PCB Editor Workspace 17
PCB Editor Menu Restructuring 18
Status Bar 19
Control Panel Selections and Workspace Windows 20
Database Check Tool – DB Doctor 21
Lab 24
Lab 1-1: PCB Editor Tour 25
Mouse Buttons 29
Controlling the Window Display – Zoom Options 30
Controlling the Window Display – View Options 31
Navigating Using the View Window 32
Default Aliases for Function and Control Keys 33
Controlling the Toolbars 33
Toolbar Icons 34
Design Parameters Editor 35
Display Tab 36
Design Tab – Command Parameters Section 38
Design Tab – Line Lock and Symbol Section 39
Text Tab 40
User Preferences 41
Lab 43
Lab 1-2: Navigating the PCB Editor User Interface 44
Lesson 2: Managing the PCB Editor Work Environment 49
Learning Objectives 49
Categories, Classes and Subclasses 49
Controlling Color and Visibility 50
Coloring Nets in the Color Dialog 52
Controlling Etch Visibility 53
Transparency Options 54
Graphics Dimming or Shadow Mode 55
Export and Import Design Parameters 56

Lab 57
Lab 2-1: Controlling Visibility and Color 58
Find Tab - Selectable Objects List 63
Using the Find by Name Section 64
Using Find by Name – Property Selection 65
The Super Filter 66
Application Modes 67
Pre-selection Mode 68
Right-Mouse-Button Command Use 69
Right-Mouse-Button Common Area Commands 70
Coloring Elements 71
Highlight Elements 72
Highlighting Fixed Objects 73
Using the Show Element Command 74
Using the Measure Command 75
Change Origin Command 76
Using the Flip Design Command 77
Using the 3D View Command 77
Labs 78
Lab 2-2: Using the Find Filter and Pre-Selection Mode 79
Lab 2-3: Using the Find Filter with the Show Element Command 80
Lab 2-4: Changing the Drawing Origin 83
Lab 2-5: Using the Flip Design and 3D View Commands 84
Lesson 3: Padstacks 87
Learning Objectives 87
Anatomy of a Padstack 87
Padstack Geometry Details 88
What Does the Padstack Editor Do? 89
Padstack Editor 90
Pad Editor - Title Bar and Tabs 91
Padstack Editor – Start Tab 91
Pad Editor – Drill Tab 92
Pad Editor – Secondary Drill Tab 93
Pad Editor – Drill Symbol Tab 93
Pad – Drill Offset Tab 94
Pad Editor – Design Layers Tab 94
Pad Editor – Mask Layers Tab 95
Pad Editor – Options Tab 96
Pad Editor – Summary Tab 96
Labs 97
Lab 3-1: Creating a Padstack for a Through- Hole Pin 98
Lab 3-2: Creating a Padstack for a Surface Mounted Device 104
Lesson 4: Component Symbols 107
Learning Objectives 107
PCB Editor Symbol Types 107
Package Symbol Wizard 108

Package Symbol - Manual Creation 109
Create a New Design Window 109
Design Parameters 110
Drawing Origin 111
Example: 12-pin Header Package 112
Adding Pins 113
Drawing Component Outlines 114
Adding Labels 115
Defining Package Areas 116
Saving Symbol Files 117
Labs 118
Lab 4-1: Creating an SOIC14 Using the Package Symbol Wizard 119
Lab 4-2: Creating a 12 Pin Header Package Symbol 123
Lesson 5: Board Design Files 133
Learning Objectives 133
Creating a Board Symbol 133
Elements of a Board Outline 134
Add New Subclass 135
Importing DXF to Create the Board Outline 136
Move Outline to Design Outline Layer 137
Tooling/Mounting Holes 138
Dimensioning with the Dimension Environment 139
Defining Constraint Areas – Keepins and Keepouts 140
Saving Board Symbol Files (.bsm and .dra) 141
Lab 142
Lab 5-1: Creating a Board Mechanical Symbol 143
PCB Editors – Flow Overview 158
Creating a Template Design File 159
Defining Layer Stackup 160
Cross Section – Default View 161
Cross Section – Adding/Removing Layers 162
Lab 163
Lab 5-2: Creating a Template Design (.brd) 164
Lesson 6: Importing Logic Information into PCB Editor 171
Learning Objectives 171
Design Layout Process 172
Integrating Logic Design with Physical Layout 172
OrCAD Capture and PCB Editor Interface Process 173
Transfer Files (pst*.dat) – OrCAD Capture to PCB Editor 174
OrCAD Capture to PCB Editor Logic Import 175
Engineering Changes – Placement and Routing 176
Place Changed Component 176
Routing Changed 177
Labs 178
Lab 6-1: OrCAD Capture to PCB Editor 179
Lesson 7: Setting Design Constraints 183

Learning Objectives 183
Design Layout Process 183
Introduction to Design Rules 184
The Constraint Manager 185
Constraint Manager - Left Pane 186
Constraint Manager - Work Area 187
Setting Default Physical Constraint Values 188
Add Via Selection to a Net or Constraint Set 189
Creating a New Physical Constraint Set 191
Identify the Special Physical Nets 192
Assign the Physical Constraint Set to the Net Class 193
Assign Rules Directly to a Net 194
Lab 195
Lab 7-1: Setting Physical Rules 196
Setting Default Spacing Constraint Values 199
Creating a New Spacing Constraint Set 200
Identify Special Spacing Nets 201
Assign the Spacing Constraint Set to the Net Class 202
Net Class to Net Class Spacing 203
Labs 204
Lab 7-2: Setting Spacing Rules 205
Lab 7-3: Setting Class-Class Rules 208
Analysis Modes 210
Design Options and Modes 210
Design Options and Modes (Soldermask) 211
Design Options and Modes (Acute Angle Detection) 212
Design Modes (Package) 213
Electrical Options and Modes 214
Physical Modes 215
Spacing Options and Modes 216
Same Net Spacing Modes 218
SMD Pin Modes 219
Property Assignments and Changes 220
Adding Properties in Constraint Manager 221
Physical Constraint Resolution 222
Spacing Constraint Resolution 223
DRC Marker Display 224
Lab 225
Lab 7-4: Working with Properties 226
Lesson 8: Component Placement 231
Learning Objectives 231
Design Layout Process 231
Placement Prerequisites 232
Placement Edit Application Mode 233
Placement Grid 234
Placement Strategy 235

Floorplanning with Rooms 236
Creating a Room 237
ROOM_TYPE Properties 238
Assign RefDes Command 239
Labs 240
Lab 8-1: Floorplanning 241
Lab 8-2: Assigning Preplaced Packages 243
Placement-Related Properties 244
Placement Commands 244
Manual Placement - Placement List Tab 245
Manual Placement - Advanced Settings Tab 247
Changing the Default Orientation 249
Lab 250
Lab 8-3: Manual Placement 251
Quickplace Command 256
Aligning Components 258
Deleting/Unplacing Components 259
Lab 8-4: Using the Quickplace Command 261
Lesson 9: Additional Placement Features 265
Learning Objectives 265
Ratsnest Display 266
Selecting Alternate Packages 267
Updating Symbols in a Design 268
Updating Padstacks 269
Modifying Padstacks in a Design 270
Create Fanout Command 272
Copy Fanout Command 274
Creating a Library from a Design 275
Cross Selection with OrCAD Capture – Prerequisites 276
Cross Highlight between Board and Schematic 278
Labs 279
Lab 9-1: Displaying Ratsnests 280
Lab 9-2: Creating and Copying Fanouts 281
Lab 9-3: Using the OrCAD Capture Schematic for Manual Placement 284
Lesson 10: Interactive Routing and Glossing 287
Learning Objectives 287
Design Layout Process 287
Accessing Interactive Routing Modes 288
Routing Grids 289
Adding Signal Connections 290
Inserting Vias 291
Selecting Via Types 292
Define Blind/Buried Via 293
Using B/B Vias in the Design 293
Routing - Options Tab 294
Routing - Options Tab - Bubble/Gridless 295

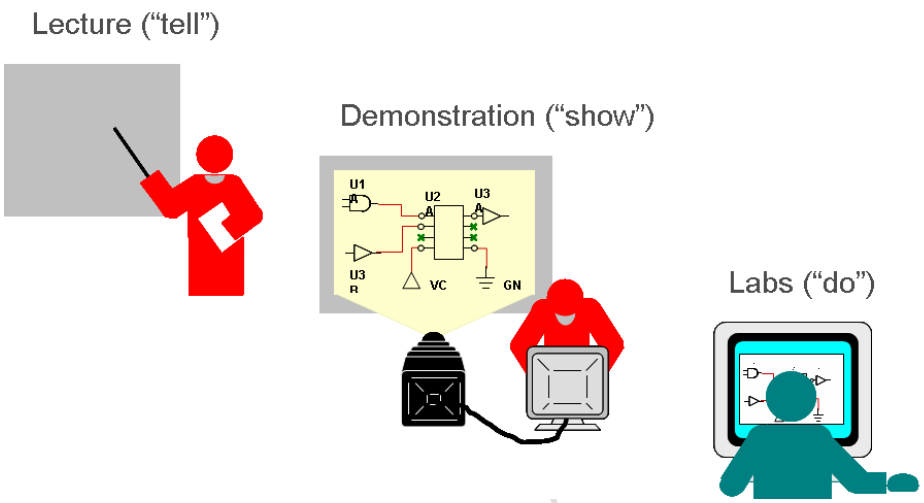
Routing - Options Tab - Smooth 296
Scribble Route Mode 297
Setting Interactive Route Parameters 298
Labs 299
Lab 10-1: Defining Etch Grids 300
Lab 10-2: Adding and Deleting Connect Lines and Vias 301
Editing Existing Etch 307
Moving Etch with the Slide Command 307
Editing Vertices 310
Changing the Layer of a Connection 311
Changing the Line Width of a Connection 312
Deleting Etch 313
Using the Cut Option 314
Interactive Routing Properties 315
Gloss Line Parameters 316
Line Smoothing 316
Labs 318
Lab 10-3: Improving Routed Connections 319
Lab 10-4: Using the Cut Option 321
Lab 10-5: Running Gloss 323
Lesson 11: Copper Areas and Positive Planes 325
Learning Objectives 325
Design Layout Process 325
Copper Area Images 326
Adding a Copper Area 327
Rectangular Shape Options 329
Global Dynamic Parameters 330
Global Dynamic Parameters - Shape Fill 331
Global Dynamic Parameters - Void Controls 332
Global Dynamic Parameters – Clearances 333
Global Dynamic Parameters - Thermal Relief Connects 334
Editing Copper Shapes 335
Split Planes 336
Strategy for Split Planes 337
Shape Edit Application Mode 338
Chamfers 339
Labs 340
Lab 11-1: Creating an Internal GND Plane 341
Lab 11-2: Creating a Split Plane for VCC Layer 344
Lab 11-3: Copper Pour Areas 350
Lab 11-4: Shape Edit Application Mode 353
Lesson 12: Preparing for Post Processing 357
Learning Objectives 357
Design Layout Process 357
Checking for DRCs and Unconnected Pins 358
Waiving DRCs 360

Renaming Reference Designators 361
Rename Reference Designators Main Form 362
Rename Reference Designators Setup Form 363
Rename Reference Designators — Key Points 364
Backannotation 365
Backannotation Examples 365
Integrating Physical Layout with Logic Design 366
PCB Editor to OrCAD Capture Backannotation 367
Labs 368
Lab 12-1: Checking for DRCs and Unconnected Pins 369
Lab 12-2: Renaming Components 374
Lab 12-3: PCB Editor to OrCAD Capture Back Annotation (Optional) 377
Lesson 13: Preparing the Board Design for Manufacturing 379
Learning Objectives 379
Design Layout Process 379
Creating Silkscreens 380
Creating Silkscreens — Menu 381
Incremental Update of Silkscreens 383
Generating Reports 384
Labs 385
Lab 13-1: Creating Silkscreens 386
Lab 13-2: Generating Reports 389
Creating Fabrication Drawings 390
Drill Customization Spreadsheet 391
Drill Symbols and Legend Table 392
The NC Parameters File 394
Generating an NC Drill File 395
Creating the Cross-Section Chart 396
Creating Assembly Drawings 398
Labs 399
Lab 13-3: Creating Fab and Assembly Drawings 400
Lab 13-4: Creating an NCDRILL File 403
Generating Artwork 404
Artwork Control Form - General Parameters Tab 405
Artwork Control Form - Film Control Tab 407
Artwork Control Form - Film Options 408
Artwork Control Form - Generating Gerber Files 409
Labs 411
Lab 13-5: Creating Artwork Files 412
Creating an IPC-2581 Database 417
Labs 419
Lab 13-6: Creating an IPC-2581 File 420
Appendix A: Preselection Mode 421
Creating a Selection Set 421
Context-Sensitive Right-Mouse-Button Pop-Up Menu 421
Etch Edit Default LMB Drag Command Execution 422

General Edit Default LMB Drag Command Execution 423
Routing Pop-Up Menu Options 424
Appendix B: Scripts and Macros 427
Scripts 427
Macros 428
Macro and Script Results 429
Appendix C: Pin and Gate Swapping 431
Swapping of Functions (Gates) and Pins 431
Interactive Swap 432
Lab C-1: Component and Gate Swapping 434

How to Use This Manual

This PCB Editor Training Manual closely complements the PCB Editor training lectures, slides, and software demonstrations. Concepts and skills taught during this course are based on an "explain", "show," and "hands-on" method.



Each lesson begins with an explanation of application features and associated dialog boxes. Lab exercises follow that provide guided hands-on experience.

Course Agenda

Lesson 1: Cadence® PCB Editor User Interface
Lesson 2: Managing the PCB Editor Work Environment
Lesson 3: Padstacks
Lesson 4: Component Symbols
Lesson 5: Board Design Files
Lesson 6: Importing Logic Information into PCB Editor
Lesson 7: Setting Design Constraints
Lesson 8: Component Placement
Lesson 9: Additional Placement Features
Lesson 10: Interactive Routing
Lesson 11: Copper Areas and Positive Planes
Lesson 12 Preparing for Post Processing
Lesson 13: Preparing the Board Design for Manufacturing

Appendices

Appendix A: Pre-Selection Mode and Selection Set
Appendix B: Scripts & Macros
Appendix C: Pin and Gate Swapping

Other Related Courses

- **OrCAD Capture Essentials**: This class teaches you how to use the OrCAD Capture schematic tool to design and process electrical schematics.
- **OrCAD Capture CIS/CIP**: This class teaches what a part database is and how the Cadence OrCAD Component Information System can help manage parts and usage with a parts database.
- **Analog Simulation with PSpice**®: This class teaches you how to use the Cadence PSpice A/D simulator for analog design.
- **PSpice Advanced Analysis**: This course teaches how to use the features in the Cadence PSpice Advance Analysis package - Sensitivity, Monte Carlo, Smoke Analysis, and the Cadence PSpice Optimizer.
- **PCB Editor Professional**: This course teaches how to customize the PCB Editor, set high speed constraints, define differential pairs and their constraints, create rigid flex zones, set inter layer rules, set DFM constraints, use placement replication, use the auto router and testpoint generation.
- **SPECCTRA for OrCAD**: During this course, you will learn how to use the Cadence SPECCTRA for OrCAD and interactive wire editing tools.

Formatting Conventions

The following formatting conventions are used throughout this training manual:

- For the purpose of this manual, OrCAD Capture CIS will be referred to as OrCAD Capture as the actual functions performed are "Done" by OrCAD Capture and not the OrCAD Capture CIS option. Also, some dialog boxes refer to OrCAD Capture tools as Design Entry CIS (Capture) which is aliased by DE CIS.
- When lab procedures instruct you to click a dialog box button, tab, option, or toolbar icon, the item is formatted in ***bold, italic*** text.
- When lab procedures instruct you to select a file name, the name of the file is formatted in `courier` text.
- When lab procedures instruct you to access a directory path, the path is formatted in ***bold italic*** text.
- When you are instructed to select a menu option, the option is formatted in ***bold, italic*** text.
- When you are instructed to select a series of menu options, the primary and secondary menu options are separated by the (***-***) symbol.
- When lab procedures instruct you to press a key on your PC keyboard, the name of the key is enclosed in brackets. For example: <***key***>.
- When lab procedures instruct you to enter information in a field, type in the appropriate information and then hit the Tab or Enter keyboard key.

Lesson 1: PCB Editor User Interface

Learning Objectives

In this lesson, you will:

- Identify the user interface components of the PCB Editor
- Navigate within the PCB Editor window and access UI features to tailor the tool to your individual needs

In this section, you will be introduced to the PCB Editor. You will explore the PCB Editor's graphical user interface as well as the various programs that comprise the PCB Editor system. Information about online documentation and websites will be provided.

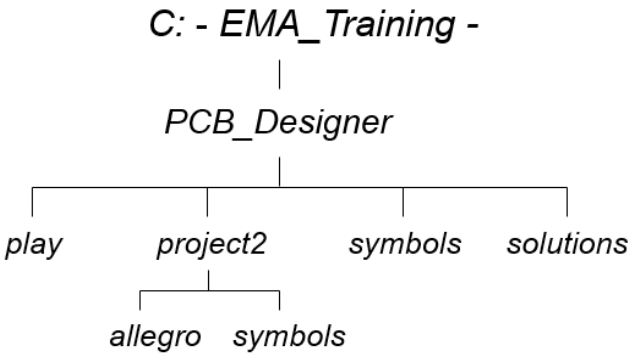
Note The pictures in this manual are taken using a Windows 10 operating system. They may vary slightly if you are using Windows 7 or Windows 8.

Version 17.4 Notations

When you install the PCB Editor Version 17.4 software on your computer you need to be aware of the following:

- Version 17.4 will only run on a 64-bit architecture (Windows 10)
- Once the board design or symbol file is saved in version 17.4, it may be exported or downrev'd to 17.2, but not any older versions, such as 16.6.

Course Directory Structure



C or D drive depending on the training computer you are using

Important

It is very important to understand and remember the directory structure presented, especially when working with the labs. The *project2* directory structure contains a front to back design with an OrCAD Capture schematic. The *project2 directory contains* the `release.dsn` schematic file. The allegro subdirectory contains the 3 `pst*.dat` Packager files used for netlisting, as well as the `*view.dat` files for back annotation.

Other directories that you will see within the course installation are:

- *Symbols* - All the `.psm`. and `.dra` symbol files used for PCB Editor `.brd` designs reside in this subdirectory.
- *Play* - This is the working directory where you build library files and practice using the PCB Editor.
- *Solutions* - This directory contains all of the reference board files for all of the labs as backup files.

Primary PCB Editor Programs

When you install the PCB Editor software on your computer, the installation program automatically includes several tools accessible from ***Windows Start*** product selections.

Depending on the operating system on your computer will depend on the access from the Windows Start.

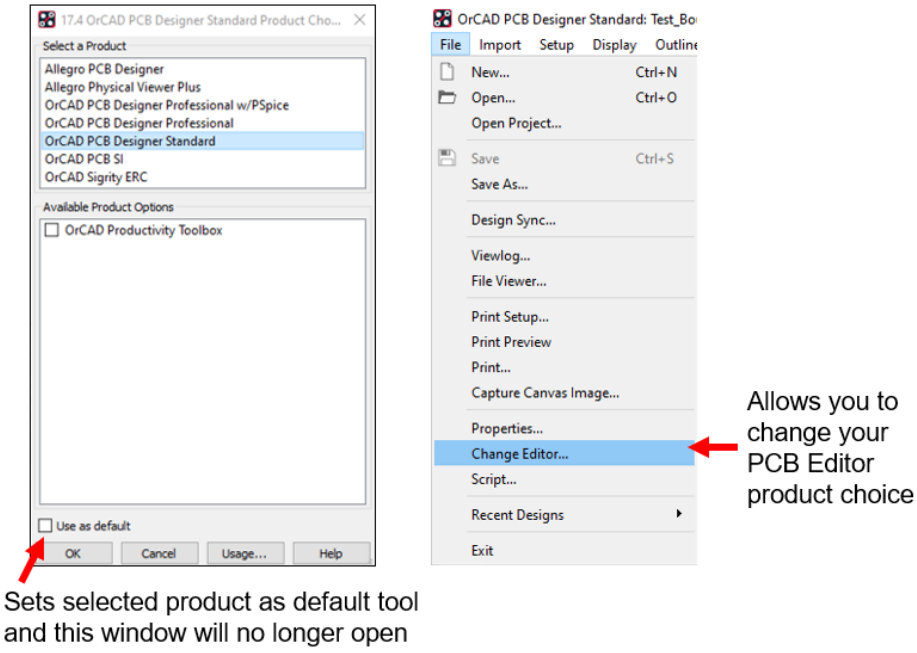
- Windows 10
  - PCB Editor: ***Start – Cadence PCB 17.4-2016 – PCB Editor 17.4***
  - Padstack Editor: ***Start – Cadence PCB Utilities 17.4-2016 – Padstack Editor 17.4***

The PCB Editor lets you create printed circuit board designs and footprint symbols required by those designs.

The Pad Designer lets you create or modify library padstacks, including:

- Defining the parameters of your padstacks
- Creating through-hole, blind and buried, and via padstacks

PCB Editor Tools



If you purchased more than one type of the PCB Editor tool, the Product Choices form will appear when you invoke the PCB Editor. Select from the list the product you wish to use. If you want the same product each time you use the program and do not wish to see the product choices menu each time, you can toggle the *Use as Default* option in the form. With this option checked, the product you have selected when you click the OK button will be used each time you run the PCB Editor. If you want to use a different product after starting the PCB Editor, use ***File - Change Editor*** to reopen the PCB Editor Product Choices form.

The **OrCAD PCB Designer Standard** tool is a baseline product. It includes Differential Pair Constraints but does not include an autorouter. All features taught in this class are available in OrCAD PCB Designer Standard.

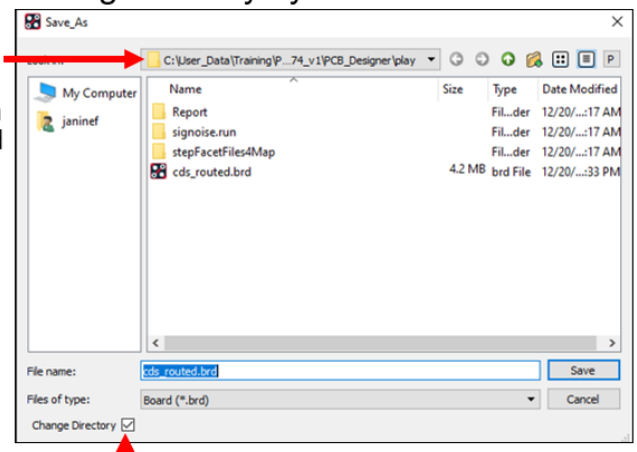
The **OrCAD PCB Designer Professional** tool has support for some Electrical Rules, such as Differential Pairs, Propagation Delay, Matched Delay, Impedance and Total Etch Length. It also supports all physical and spacing rules that may be required, including Region Rules.

The **OrCAD PCB Designer Professional with PSpice** tool has the same rule selection as the OrCAD PCB Designer Professional tool, but also includes PSpice A/D.

Setting and Changing Your Working Directory

All files that are created or saved from within PCB Editor are written to the current working directory by default.

When opening or creating files, you can change the directory to a new location by browsing to the desired directory.



Use this option to change to the new selected directory. If not checked than the file will save to the original working directory

When opening and saving files, you must pay attention to the directory that is set as your Current Directory. This directory is displayed in the title bar of the PCB Editor window. When you open or save files, you can change the Current Directory by using the standard browser. If you browse to a different directory, you can make that directory the Current Directory by selecting the ***Change Directory*** option at the bottom of the window.

The first time you invoke the PCB Editor, the Current Directory is set to a location that is specified during the software installation.

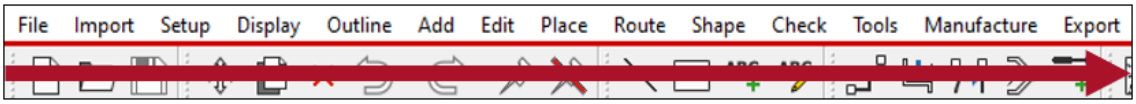
PCB Editor Workspace

There are several different areas that you need to become familiar with when using the PCB Editor.

- **Title bar** - Located at the very top of the window, indicates the PCB Editor product that is currently running, the database that is currently opened, and the working directory.
- **Menu bar** - Located directly underneath the title bar, contains all the commands required to create and modify a design. To execute a command, select the pulldown menu with the LMB, then select the command with the LMB. For example, to execute the **Open** command, select ***File - Open*** from the menu bar with the LMB.
- **Icon toolbar** - Located immediately below the menu bar, the icon tool bar can be displayed or hidden in groups. This area will be discussed in more detail shortly.
- **Design Workflow Pane –** The design workflow is great for new users. It guides new users through the design flow and eliminates searching for icons, or menus. It is also possible to create custom flows.
- **Start Page –** When PCB Editor first opens, the start page will be visible on top of the design window. The start page provides easy access to valuable information. It includes a Recent Design List, Get Started section with Tips and Tricks and Best Practice papers.
- **Design window** – Once a board file, or footprint is opened, the design window will move on top of the start page. This is where you will do most of your work on the printed circuit board design such as placing your parts and routing the design.

PCB Editor Menu Restructuring

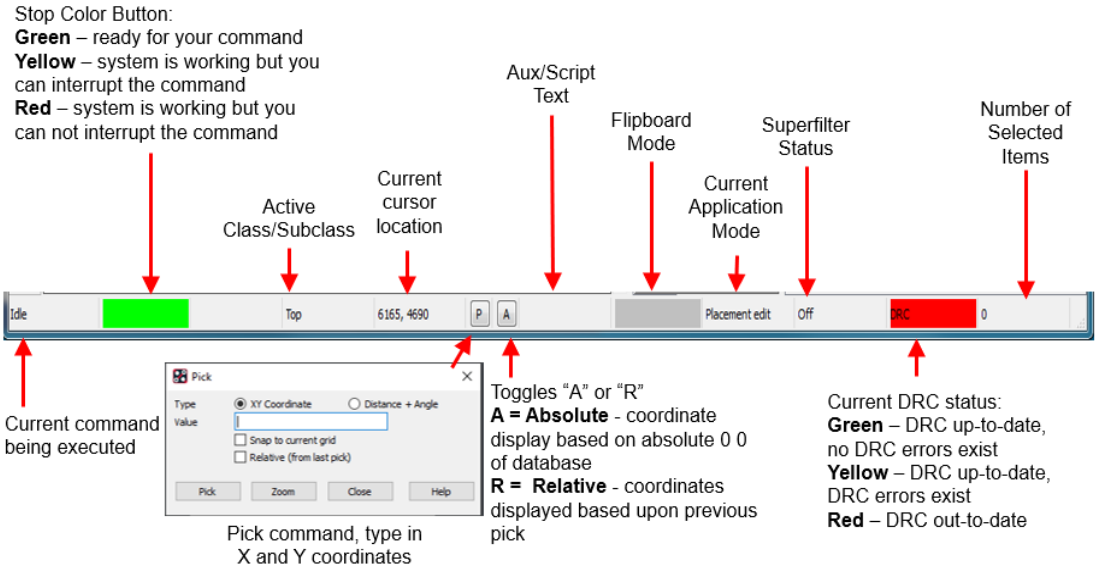
Since the release of 16.6-2015, Cadence introduced a vastly improved menu structure for the PCB Editor based on numerous requests of making your design experience faster and more intuitive.



Replicating a physical design flow, the menu structure has been re-arranged so that it works in both horizontal and vertical axis. The more common menus such as Import and Export have been exposed to the main canvas while infrequently used menus are regulated further down the tree. Mouse clicks have been minimized by adapting a “two-deep” menu philosophy.

The menus in the Symbol Editors remain as they were in the past.

Status Bar



The **Status Bar** is located at the bottom of the window.

First, the Status Bar contains the current command being executed. In this case, the word **idle** is displayed because no command is currently active.

Next is a **Stop Color** box that is used to halt the execution of the currently active process. Green means that the system is ready for a command. Yellow means the system is working but you can interrupt the command. Red means that the system is working but you cannot interrupt the command.

Next is the **Class/Subclass** window which displays the current active class. Clicking on this window produces a pop-up menu that enables the user to change to active class/subclass from a list.

Next, the current X and Y coordinates of the cross hairs is displayed.

Next are two buttons. The **P** button runs the pick command which allows you to type in an X and Y coordinate rather than selecting with your left mouse button. The **A** button is a toggle that will display either "**A**" or "**R**". The "**A**" toggle stands for Absolute, and the coordinate display mentioned earlier will be based upon the absolute 0 0 of the database. The other toggle is "**R**", which represents Relative mode. The coordinates displayed in relative will be based upon the previous pick, and not upon the origin of the database.

Next, the current Application Mode is displayed. The full name of the application mode is spelled out. Clicking on this window will produce a selectable pop-up listing all available application modes.

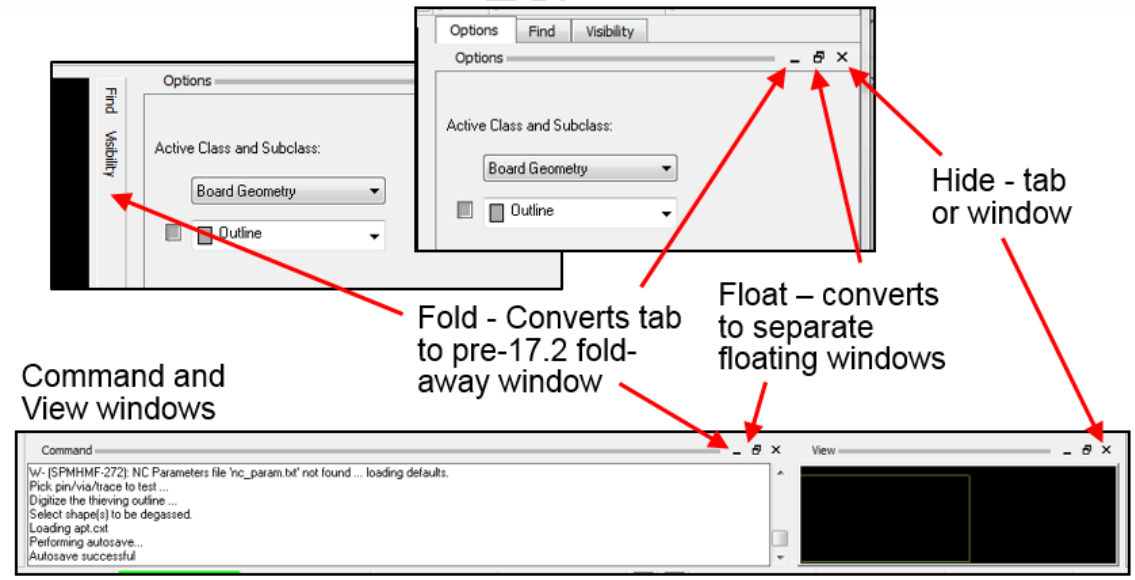
Next, the Aux/Script Text window displays the name of the current script file you are running. It also displays at which angle you are placing an object.

Next is the Super Filter status window. Clicking on this window will produce a selectable pop-up listing possible super filter values for the user to assign.

Next is the Current DRC Status. If the string "**DRC**" appears, this indicates that online design rule checking is enabled. A red color box indicates DRC is out of date and a Batch DRC is required. A yellow box indicates DRC is up to date, but DRC errors exist. A green color box indicates DRC is up to date and no DRC errors exist.

The last field is the Number of Selections, or how many objects are presently selected in the canvas. This is also a selectable field with a pop-up offering the user options previously available only within the Right Mouse Button "Selection Set" pop-up.

Control Panel Selections and Workspace Windows



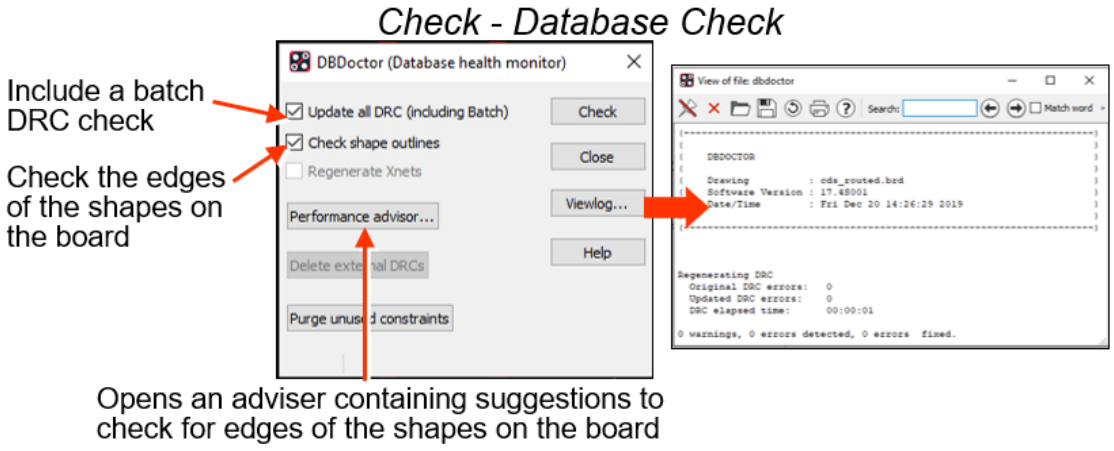
Note: If you accidently closed a window by clicking on the X icon, go to *Display - Windows* to reselect and open it. It goes back to the previous state.

Foldable window tabs allow you to customize the amount of usable area within the PCB Editor. Each of the five foldable windows has three icons to control the operation of the window. The left-most icon is a *Pin/Unpin Window* option.

With the pin/unpin in a vertical orientation, the window is permanently fixed in the open position. With the pin/pin in a horizontal orientation, the window is only expanded when you move the mouse over the window tab. The *Expand Pinned Window* icon will cause the window to expand to the entire size of the area. The *Hide Window* closes the window and removes it completely from the interface. In order to be able to access the window again, you must use the ***Display - Windows*** command and enable the window.

- **Options tab** - Contains parameters that are used to control the current interactive command.
- **Find tab** - Used to control what types of objects are selected. This window has options for use when selecting items with the mouse or when selecting items by their name.
- **Visibility tab** - Quick ways to control the visibility of conductor elements in your design such as etch, pins, vias and so forth.
- **View window** - Another way that you can control panning, zooming, and redrawing of your graphical area.
- **Command window** - Has two major functions. The first function is to display messages and prompts to you. The second function is to allow you to type in commands.

Database Check Tool – DB Doctor



As you work with the PCB Editor, the database can be corrupted by an incorrect command sequence or the use of the wrong sequence of coordinates when defining a shape. This does not happen often but if it does, you have DBDoctor to help you.

The DBDoctor tool is supplied to help you correct such problems and is accessible from within the PCB Editor from the ***Check – Database Check*** menu command. The DBDoctor command checks the consistency of the database and brings the DRC count up to date. Users find it helpful to run the DBDoctor command at the end of each day. It is recommended that you run this command before sending out manufacturing data.

The DBDoctor tool combines several individual tools that were available in previous releases:

- **dbfix (database fix) -** Analyzes the **`.brd`** file and fixes any elements if needed. It improves performance on larger designs, sorts out duplicate vias and checks the integrity of the board design file. If the dbfix tool cannot fix the problem, it will tell you how to fix it, such as by replacing a shape or sending the database to Customer Support.
- **Batch DRC -** In the Constraints Manager you set the DRC modes to Always, Never, or Batch. You may use Batch DRC to run DRC in a batch, or background mode.
- **dbcheck (database check) -** Gives you a report of the number of database errors in your board and whether dbfix was able to fix it, or not. Note that this is different from DRC errors.
- **Uprev -** Updates an existing database that might have been created in a previous release to make it current with the existing release of software.

The following options are available in the DBDoctor tool:

- **Update all DRCs (including Batch) -** Choose this option to reanalyze all DRCs in the entire design. If you don't check this option, DRCs will not be updated.
- **Check shape outlines -** Choose this option to analyze all shape elements in the database for problems and delete rectangles comprised of straight lines, or shape outlines overlapping themselves. Errors found in shapes indicate the segment on which the error was found.
- **Check -** Click to initiate the check command
- **Performance advisor -** Click to analyze designs for performance issues and generate a report that provides solutions and recommendations.

Note Performance Advisor is only available for tools or designs that support nets. Certain functionality, such as constraint region analysis, is unavailable if the tool does not support that functionality.

- Delete external DRC's - Click this option to remove external DRC's that occur as a result of user defined DRC codes.
- Viewlog - Click this option to review the **`dbdoctor.log`** containing the results of the database check

Note Dbstat is a command you can execute at a shell (Command Prompt) command line that gives you the version of the database (.brd) on which you have run this command. It will tell you the type of system (Windows7 or LINUX) that the file was last worked on. It will also report if the database is locked. The syntax is: **`dbstat <filename>.brd`**

Note Database errors and DRC errors are not the same. The DBDoctor tool will fix database errors or let you know what needs to be done to fix the problem. However, if you have a board with DRC errors, you will need to clean them up.

Lab

Lab 1-1: PCB Editor Tour

- Start the PCB Editor and other programs
- Choosing a tool from the PCB Designer program suite
- Traversing the course structure
- Setting your working directory
- Opening a board design
- Touring the PCB Editor user interface

Lab 1-1: PCB Editor Tour

Objective: Learn how to start the PCB Editor, set your working directory and view a design.

You may see icons for starting the PCB Editor executable on the desktop display, but instructions in this book will refer to the Windows Start button.

Important

Lab Directory Instructions: The labs refer to the course installation directory which is in the following location. ***C: - EMA_Training - PCB_Designer*** Whenever you see a file path in the lab instructions, you must replace the <course_inst_dir> with the above path.

Logging on

Logging on requires that you issue a username and a password, press **Ctrl+Alt+DEL** (all keys at the same time). The Login Information dialog box displays.

1. Provide the following information in the Login Information dialog box, then click **OK**: At this point, you should be logged onto your system and ready to start the PCB Editor. Use the following login information:
   - Username: **`ematrain`**
   - Password: **`train`**

At this point you should be logged onto your system and ready to start the PCB Editor.

Choosing Products and Starting PCB Editor

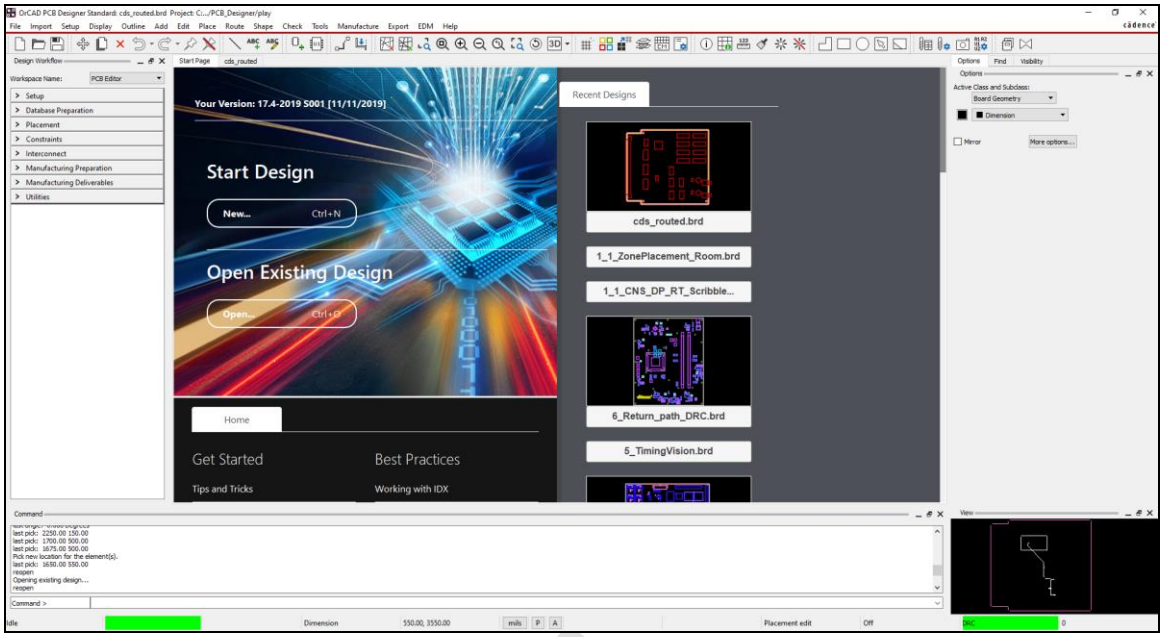
In this lab, you will open a routed PCB design in the PCB Editor window, then explore aspects of the design as well as the PCB Editor's User interface.

1. Start the PCB Editor by clicking the ***Windows Start*** button (bottom left of your screen) and choosing the ***Cadence PCB 17.4-2019 - PCB Editor 17.4*** option.

   If this is the first time you have launched the PCB Editor, the Cadence Product Choices dialog box may appear. If this happens, select ***OrCAD PCB Designer Standard*** from the product choices. Otherwise, the PCB Editor window appears.

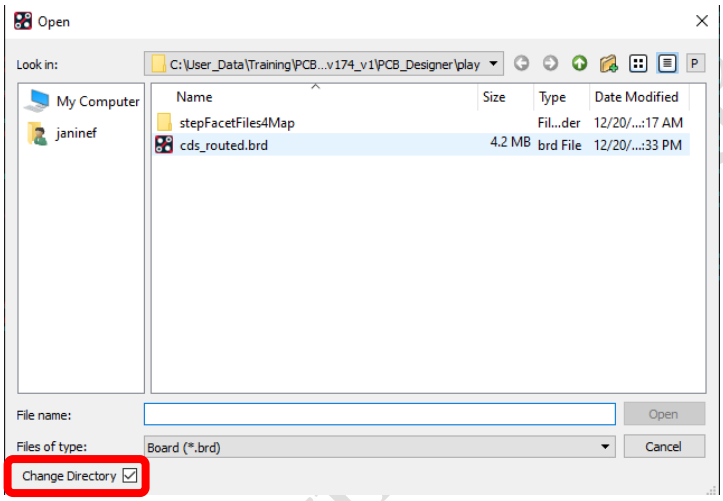
2. If the Cadence Product Choices dialog does not appear, choose ***File - Change Editor*** from the top menu bar in the PCB Editor in order to change the product.
   The Cadence Product Choices dialog box appears.

3. Select ***OrCAD PCB Designer Standard*** and click ***OK***. This is the version we will use throughout this course.
   Your PCB Editor window will look something like the figure below:



Set Your Working Directory, Open a Board Design, and View Tool Sets

1. From the top menu bar choose ***File - Open***.
   An Open file browser window appears.
2. Navigate to the `<course_install_dir> - play` directory and select the `cds_routed.brd` file.
   You will find the ***play*** directory under the ***PCB_Designer*** directory on your system.



3. Verify that the Change Directory box is checked. This option will set your working directory to *play*.
4. Click ***Open***. The `cds_routed.brd` design file is displayed in your PCB Editor's work area.

Note You can also open a file by double-clicking its name in the Open form.

Exploring the PCB Editor User Interface

In this part of the lab, you will explore various menus and buttons in the PCB Editor window to see how the user interface works.

1. Click the ***Maximize*** icon  in the top righthand corner of PCB Editor to fill your screen with the application.
2. Referring to the overview discussed earlier, identify the following parts of the PCB Editor window:
   - Menu bar organization and options
   - Icon ribbon toolbars
   - Design window
   - Design Workflow
   - Control Panel
   - Command window (and command line)
   - World view window
   - Status Bar with its "traffic light" and coordinate readouts

   You will access all these features in more detail in later labs.

3. Using the ***Fold icons***, fold the ***Options, Find*** and ***Visibility*** tabs in the Control Panel. Click on the folded away tab to again dock them in place. Having them all folded away allows you to have the largest Design Window for your work within the PCB Editor.
4. ***Display – UI Settings – Reset UI to Cadence Default*** will reset all windows to their default configuration. This may be used if you accidentally click the ***Close icon*** and close a window instead of folding it away. 
5. Select "***Yes***" to reset the windows.

Note  The configuration of windows and the locations and contents of icon toolbars are stored in the pcbenv/allegro.ini file. Based upon previous classes, your PCB Editor window may not appear in the default configuration.

6. View the menu options. Click the ***File*** menu option and note the available options. Slowly pass your cursor over the menu items (***Import***, ***Setup***, ***Display***, ***Outline*** and so on) from left to right. Note the various menu options available under each menu.
7. Click in the PCB Editor work area where your cursor is not located over a graphical item to close your latest pull-down menu.
8. View the command names on the toolbar icons. Slowly drag your cursor across the toolbar from left to right. When your cursor hovers over an icon, read the tool tips that appear. DO NOT CLICK. When you come to the ***Zoom Fit*** icon, click it. The entire `cds_routed.brd` design is framed in your PCB Editor graphical window. **End of Lab**

Mouse Buttons

Three-button mouse:

- **L**eft **M**ouse **B**utton (LMB) - Select design elements, menu buttons and icons. Window selection available by dragging
- **R**ight **M**ouse **B**utton (RMB) - Open pop-up menus
- **M**iddle **M**ouse **B**utton [wheel] (MMB) - Pan, zoom control

Left Mouse Button

Use this button to select graphic elements in a design (such as lines, pads, and text). The selected feature is highlighted. Must be used in conjunction with an active command.

To select a group of items, you create a selection rectangle. To do so, first you click the Left-Mouse-Button to pick a corner for the rectangle, then you hold the Left-Mouse-Button and drag your mouse, creating a rectangle. All applicable items within the rectangle are selected.

Use this button to select commands from menus or icons.

Some forms contain entry fields with a list of built-in options. To display and select these options, use the Left-Mouse-Button in the data field (for example, the *Options* tab).

Right Mouse Button

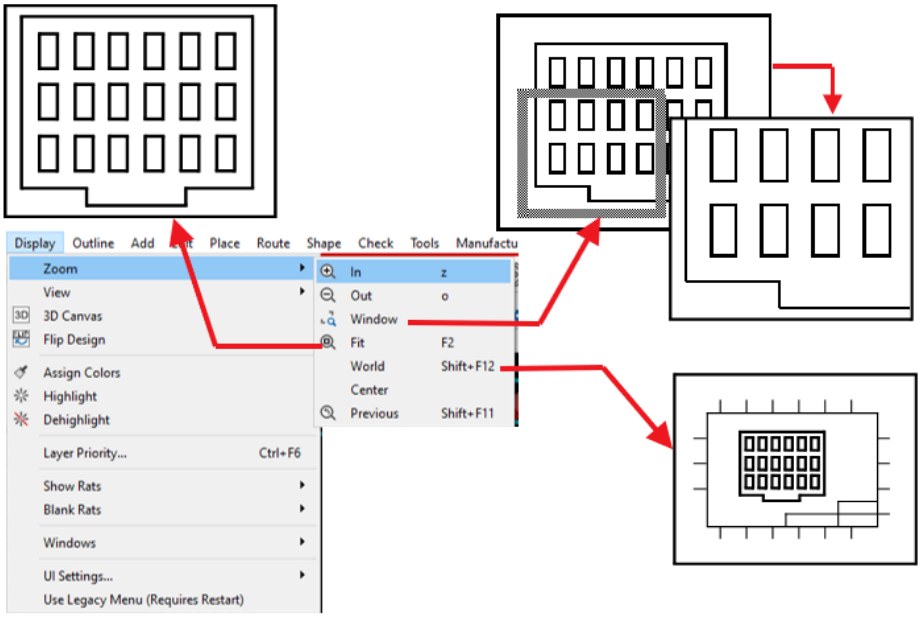
Displays a pop-up menu containing options associated with the current command.

Middle Mouse Button (Mouse Wheel)

Press and hold the Middle-Mouse-Button (mouse wheel) while moving the mouse in the direction you want to pan. If you move the middle mouse wheel forward the system will zoom in and if you move it backward the system will zoom out.

Controlling the Window Display – Zoom Options

Display - Zoom … menu options

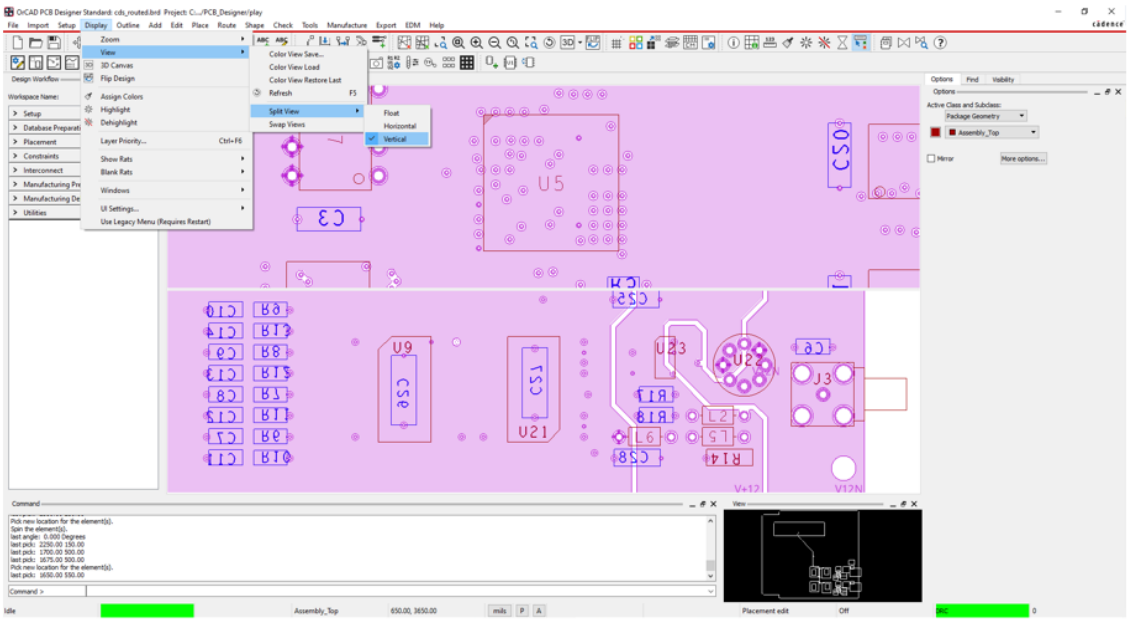


There are several commands available to change what is displayed in your current work area or the Design Window. By choosing the ***Display – Zoom*** pull-down menu in the menu bar, you have the following zoom options:

- **In** - Magnifies or zooms in to a smaller area of the drawing.
- **Out** – Zooms out or increases the displayed area of the drawing.
- **Window** - Specifies a new display area by letting you pick two diagonally opposed points. After you pick the first point, a frame stretches from the first point to the cursor. Picking a second point defines the size of the new work area.
- **Fit** - Creates a view that includes, but is no larger than, the board outline.
- **World** - Displays the entire extents of the drawing in the work area.
- **Center** - Redisplays the drawing area with the center being a point that you select.
- **Previous** - Displays the previous viewing area. Switches back and forth between the last two views only.

Controlling the Window Display – View Options

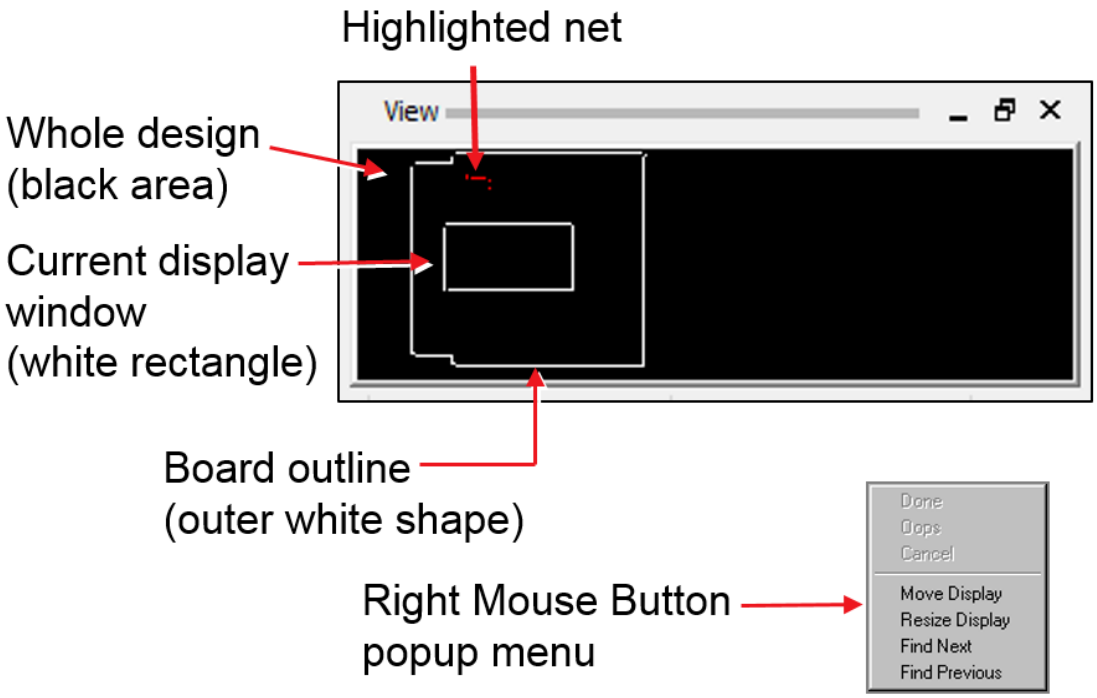
Display - View … menu options



There are several commands available to change what is displayed in your current work area or the Design Window. By choosing the ***Display – View*** pull-down menu in the menu bar, you have the following zoom options:

- **Refresh** - Simply performs a redraw of the current display area.
- **Split View** - Allows you to view another area of the design canvas while still working with the standard main editing canvas.
- **Swap Views** – Swaps the views between the work area and the Split View window

Navigating Using the View Window



The View window is located at the bottom of the PCB Editor window. It gives you quick and convenient access to the panning and zooming commands. The View window has a representation of the board outline and also indicates what portion of the board you are currently zoomed in on.

To display the View window pop-up menu, right-click within the View window. The pop-up menu appears.

- **Move Display** – Moves the display to the location you specify in the View window. You can also accomplish this by clicking and holding the Middle-Mouse-Button and moving the cursor in the World View window.
- **Resize Display** – Changes the work area display size. You can also accomplish this by clicking and holding the Left-Mouse-Button and dragging the cursor in the World View window.
- **Find Next** – Centers the work area view on the next highlighted object. You can also accomplish this by clicking with the Left-Mouse-Button in the World View window.
- **Find Previous** – Centers the display on the previously highlighted object in the list.

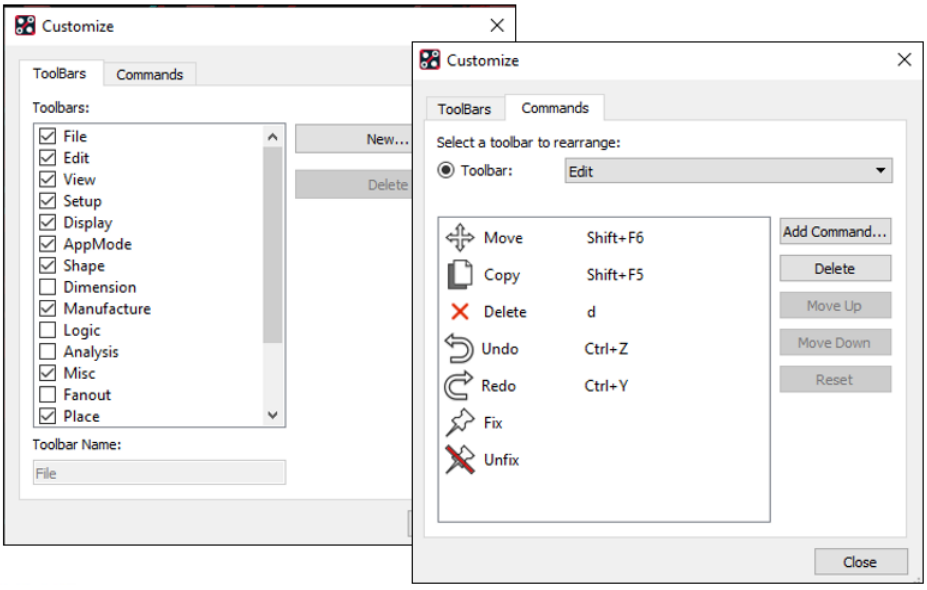
Default Aliases for Function and Control Keys

Key	Command	Key	Command
F2	zoom fit	SF2	property edit
F3	add connect	SF3	slide
F4	show element	SF4	show measure
F5	redraw	SF5	copy
F6	done	SF6	move
F7	next	SF7	dehighlight all
F8	oops	SF8	highlight pick
F9	cancel	SF9	vertex
F10	grid toggle	SF10	save_as temp
F11	zoom in	SF11	zoom previous
F12	zoom out	SF12	zoom world
CF2	next	CF6	layer priority
CF5	color192	CSF5	status

The function keys on your keyboard are aliased to an PCB Editor command. The above table shows the default function key aliases. For example, to invoke the ***Zoom In*** command, you could either select ***Display - Zoom - In*** from the menu bar or simply press the ***F11*** key on your keyboard.

Controlling the Toolbars

Setup - More - Customize Toolbar

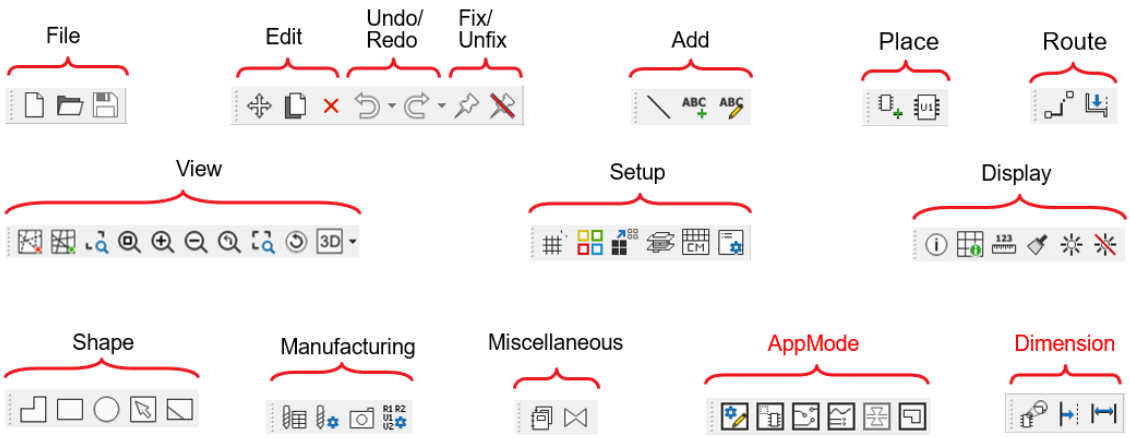


You can customize the toolbar by selecting ***Setup - More - Customize Toolbar*** from the pulldown menu bar. Under the Toolbars tab you can add or remove groups of icons from the toolbar.

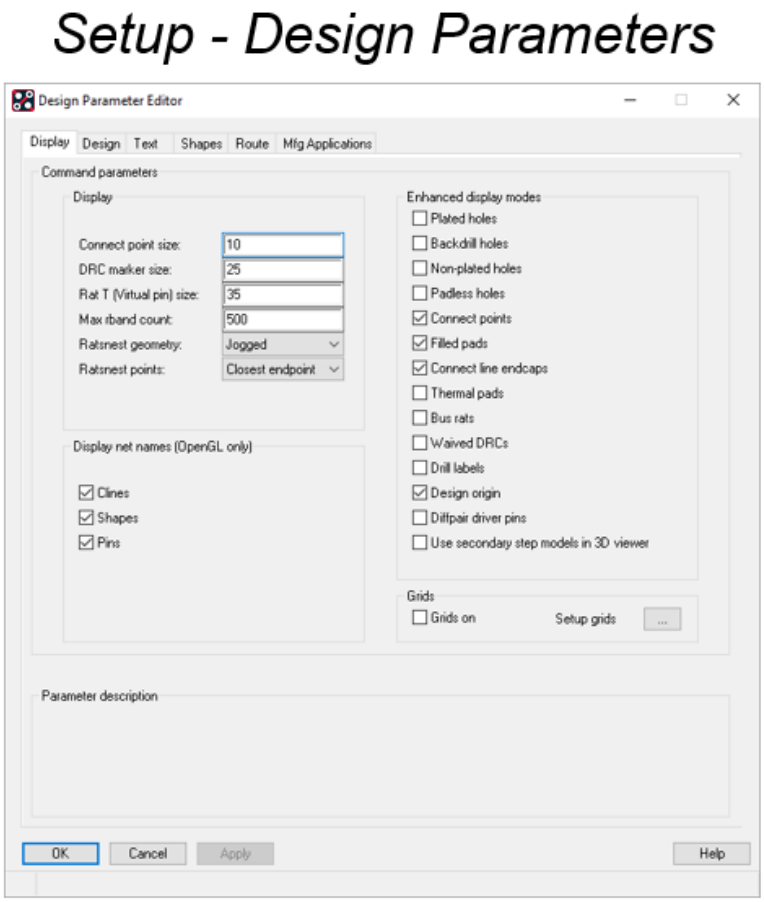
Under the Commands tab you can control the order that the icons are displayed in each of the toolbar groups. The toolbar settings are stored in a file in the registry on your system. This file is not user editable and is read each time you invoke the PCB Editor. These settings are not stored in the PCB Editor database.

Toolbar Icons

Toolbars are used to store common icons in a group. Toolbars may be added, modified, or made invisible by using the ***Setup – More – Customize Toolbar*** command.



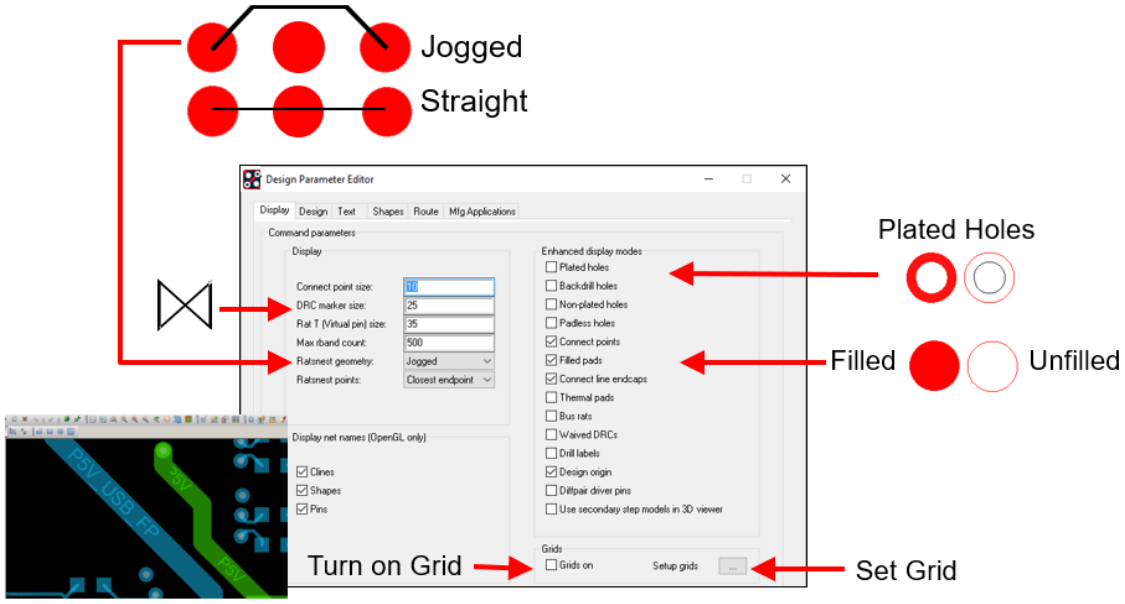
Design Parameters Editor



The Design Parameters Editor form provides a convenient, centralized location for editing parameters that are saved and stored in the database. In the Design Parameter Editor, select tabs for Display, Design, Text, Shapes, Route, and Manufacturing Applications and edit the specific parameters in each of these categories. All of these tabs will be discussed at various times later.

The Parameter description section of the form will be displayed in the Display, Design, Text and Route folder tab. In this section, there will be displayed a brief description of the parameter description when you move your cursor into a field.

Display Tab



The Display Folder tab displays current settings for various design operations. It is divided into the Display, Display Net Name, Enhanced Display Modes and Grids sections.

The Display Section:

- **Connect point Size** - Specifies the size of a connect point in user units. Default is 10.
- **DRC Marker Size** - Determines the size, in user units, of the displayed DRC "bow tie."
- **Rat T (Virtual pin) size** - Allows you to control the graphical size of a Rat T.
- **Max rband count** is the maximum number of rubber bands displayed when placing or moving a component. The default is 500.
- **Ratsnest geometry** - Determines shape of ratsnest lines. Options are: Jogged or Straight. The default is "Jogged".
- **Ratsnest points** - Lets you choose the closest distance on a line or between two pins. Options are: Closest endpoint or Pin to pin. The default is "Closest endpoint".

The Display net name (OpenGL only)

- **Clines** - Displays the net names on cline segments.
- **Shapes** - Displays the net name on dynamic shapes.
- **Pins** - Displays the net name on pins.

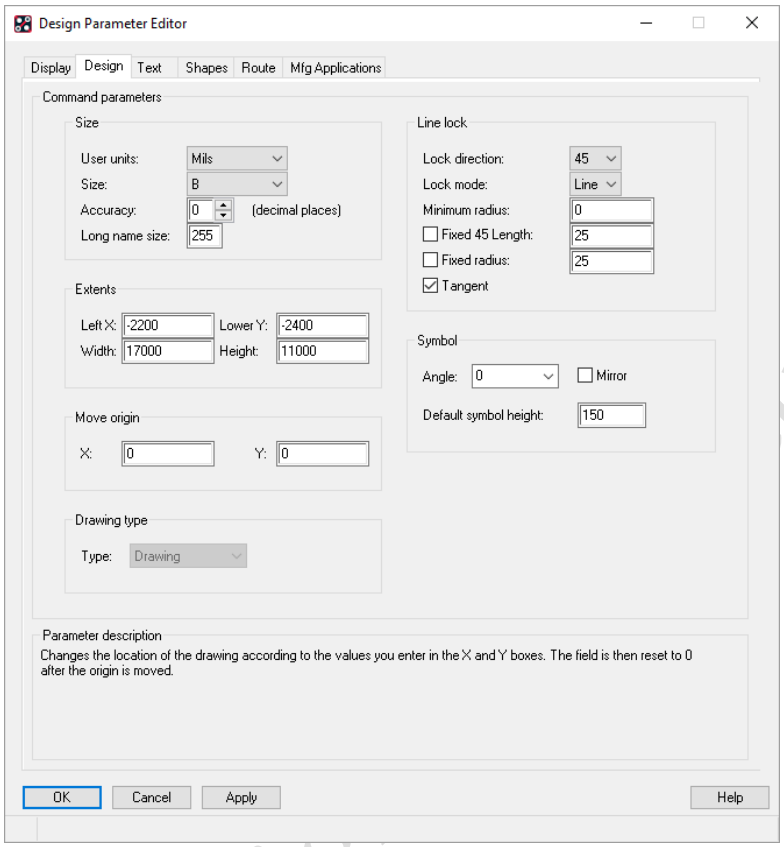
The Enhanced Display Modes section:

- **Display plated holes** - Displays the drill hole along with the pad of plated holes.
- **Backdrill holes** – - Available in Allegro PCB Designer and requires High Speed option to be enabled.
- **Display non-plated holes** - Displays non-plated drill holes, i.e. mounting, tooling holes.
- **Display padless holes** - Displays padless holes due to visible pads all being NULL or suppressed as unused.
- **Filled pads** - Indicates whether pins and vias are displayed filled or unfilled.
- **Connect line endcaps** - Controls onscreen display and rounds line vertices to more closely approximate artwork.
- **Thermal Pads** - Displays thermals and anti-pad rather than the regular pads when there is a negative plane.
  Bus Rats - Displays the middle portion of ratsnest lines with the same BUS_NAME property so that they appear to be merged into a thick line.
- **Waived DRCs** - Displays waived DRCs.
  Via Labels - Displays labels on top of each Blind/Buried via, including the 'from-to' subclasses spanned by the 'via'. Subclass numbers are displayers which are shorter than subclass names. Labels fit within the visible pad shape. A colon character (:) indicates a single via (ex: 3:4). A dash character (-) indicates a stack of connected vias spanning the entire subclass range (ex: 2-6)
- **Display Origin** - Displays an origin figure at absolute 0 0 coordinates on the DRAWING FORMAT class DRAWING_ORIGIN subclass.
  Diffpair Driver Pins - Displays a figure on top of each visible differential pair driver pin. The pin use code OUT is required for the figure to be displayed.
- **Use Secondary Step Models in 3D Viewer** - Displays secondary STEP models in 3D viewer.

The Grids section:

- **Grids on** - If checked, displays the current grid as dots. If unchecked, the dots are not displayed.
- **Setup Grids** - Browser will open the Define Grid dialog box. Setting the grids will be discussed later.

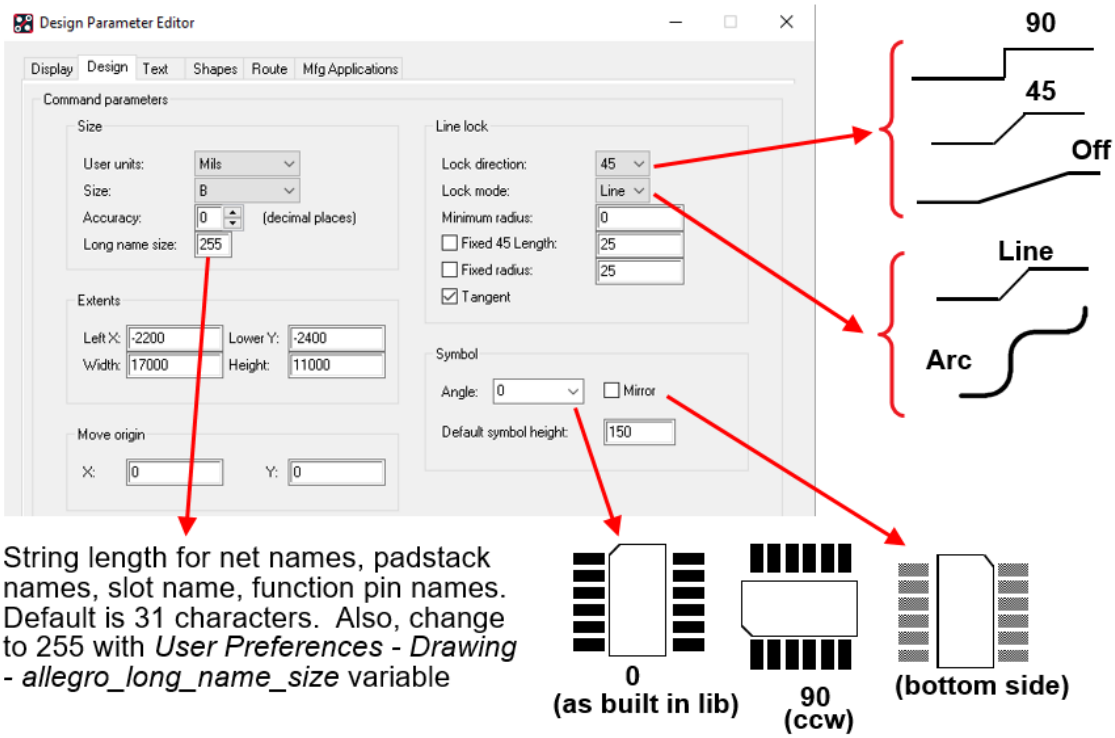
Design Tab – Command Parameters Section



Command Parameters Section:

- **User Units** - Specifies the unit of measure used during the design process. The options are Mils (default), Inches, Microns, Millimeters, or Centimeters.
- **Size** - Specifies the size of the drawing area required. The standard sheet sizes are: **A** (11x8.5), **B** (17x11), **C** (22x17), **D** (34x22), or **Other** (user-specified).
  Accuracy sets the accuracy of the drawing database. This value (ranging from 0 to 2) denotes the number of decimal places that can be used when defining feature sizes (pad sizes, grid sizes, line widths, and so on), or when entering X, Y coordinates at the PCB Editor command line. If the user unit is mils, an accuracy of zero means sub-mil values are either rounded up, or not accepted at all. Accuracy settings should be compatible across all design processes to avoid rounding off problems.
- **Extents** - Shows the height and width of the drawing, and the location of the lower left corner with respect to the drawing origin (located in the lower left corner by default).
- **Move Origin** - Relocates the drawing origin (datum 0/0). The X, Y coordinates for the new origin are transferred into the Drawing Extents section. (Changes are indicated in the Left X field and the Lower Y field in the Drawing Extents form.)

Design Tab – Line Lock and Symbol Section



The Line Lock Section:

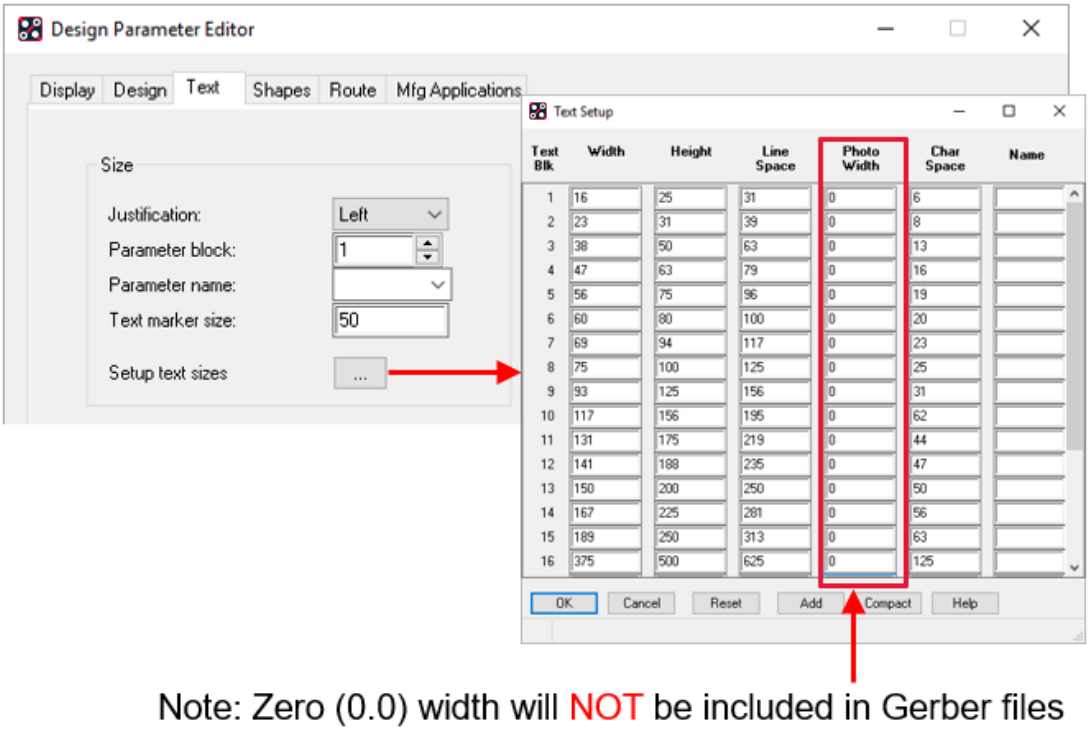
- **Lock Direction** - Lets you specify whether orthogonal, diagonal, or any-angle lines can be added. The available values are 45, 90, and Off.
- **Lock Mode** - Specifies whether new lines will be added as straight segments or arcs.
- **Minimum Radius** - Determines the minimum radius allowed for an arc.
- **Fixed 45 Length** - Specifies the length, in user units, of 45-degree segments.
- **Fixed Radius** - Specifies the radius, in user units, of arcs.
- **Tangent** - Causes an added arc to lock on to the tangent of a line.

The Symbol Section (footprints):

- **Angle** - Specifies the initial rotation of package symbols during manual placement.
- **Mirror** - During manual placement, the PCB Editor tools assume the active side is the top (default). Toggle this button **on** to change that default setting to the bottom (or solder) side.

Note You can change the above fields at any time during the design process.

Text Tab



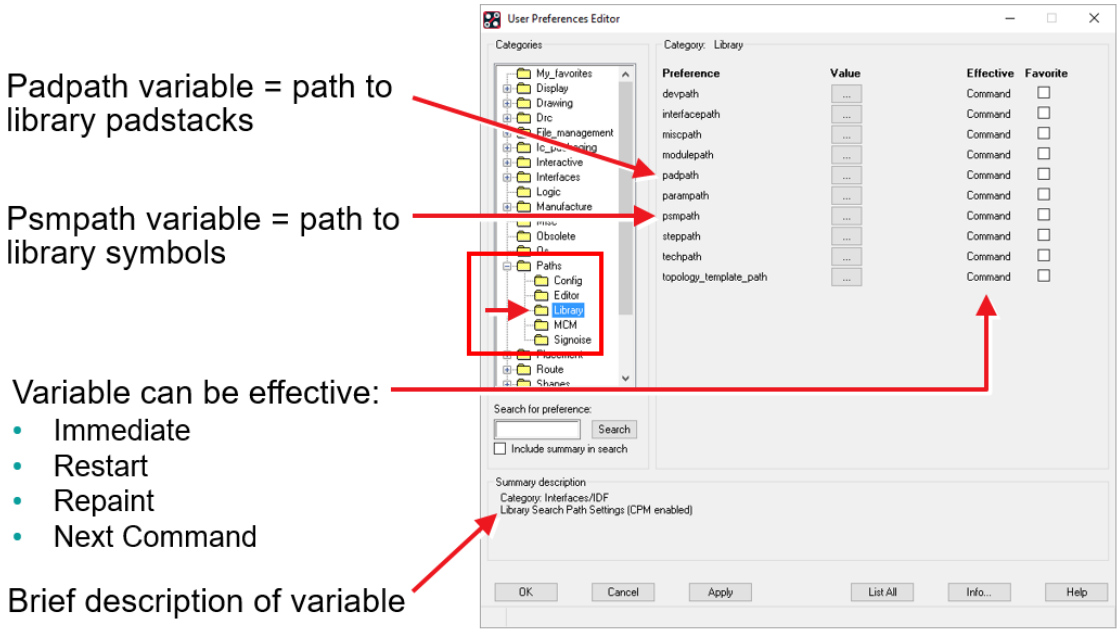
The Text Section:

- **Justification** - Controls when entering text if the text is Left Justified, Right Justified or Center Justified
- **Parameter Block** - Specifies the Text Block size to be used. To see and/or modify the text blocks, select the Setup Text Sizes browser button in the form.
- **Text Marker Size** -Specifies the size of a triangle marker that is displayed when a blank line of text is entered. This marker is displayed so the text can be edited at a later point in time.
- **Setup Text Sizes** -Opens the dialog box where you can specify the text block sizes. All text is drawn within a specific block size. For each block size, you must specify the block width and the block height. The Line Space parameter is used to specify the distance between the bottom row of one line of characters and the top row of the next row of characters when you enter text and press the Enter key.

Note The designer MUST add an actual Photo Width value to each text block size otherwise the text will NOT display in the artwork's Gerber generated file.

User Preferences

Setup - User Preferences



The User Preferences Editor allows you to set or unset the PCB Editor preferences, also known as the PCB Editor environmental variables. All changes are written to the end of your "*env*" file. This section of the *env* file should NEVER be modified manually. If the *env* file does not exist, it will be created upon successful completion of this command.

The major sections of the User Preferences Editor are as follows:

Categories

All preferences that can be set are grouped together based upon like functionality. All available categories are listed on the left side of the form. Select the category name in this section of the form to enable the setting of the preferences.

Category: <category name>

When you select a category from the left side, all the preferences in that category are listed in the Category section, located on the right side of the form. Note that certain variables can only be set or unset, while other variables require values to be entered.

This section contains the Preference name, the current Value, and the Effective period. The Effective period can have several values, including Next Command or Restart. Next Command specifies that the preference will take effect after the OK button has been selected. Restart specifies the preference will not take effect until the PCB Editor has been terminated and restarted again. Repaint specifies the new setting will be viewed the next time the tool repaints the screen.

Summary description:

This section of the form displays a description of the preference selected.

Favorites:

When enabled includes the variable in the *My Favorites* category. The *My Favorites* category centralizes frequently accessed variables.

Key User Preferences for Library Search

Library path variables:

The variables that define the location of the PCB Editor symbol and padstack libraries are available from the Paths category - Library folder.

- Padpath variable - Defines the search path for the library padstacks (`.pad`)
- Psmpath variable - Defines the search path for the library symbols (`.psm, .bsm, .osm, .ssm, .fsm`)

If the symbols and padstacks are not located in one of the folders defined in these variables the PCB Editor will not find them.

Lab

Lab 1-2: Navigating the PCB Editor User Interface

- Manipulating mouse buttons
- Choosing options from a pop-up menu
- Panning your view
- Applying the Zoom command options
- Working in the View window
- Customizing your view and toolset by changing toolbars
- Setting drawing options
- Setting User Preferences

The following lab will teach you how to use the mouse, pan, zoom and use the View window to change your display area, work with menus, and set the drawing parameters.

Lab 1-2: Navigating the PCB Editor User Interface

Objective: Navigate within the PCB Editor window and customize the user interface.

Using a Pop-Up Menu and View Panning

1. Open PCB Designer using the `cds_routed.brd` design in the *play* directory, if you do not already have it running.
2. Select ***Display - Zoom – In,*** or the  icon to zoom into an area of the board.
3. Choose the ***Route - Slide*** option from the top menu by using the ***Left-Mouse-Button*** (**LMB**).
4. Move your cursor into the work area window and right-click.
   A pop-up menu appears. There are different pop-up menus associated with different tools. Pop-up menus are context-specific.
5. Select the ***Cancel*** option in the pop-up menu to exit the ***Route - Slide*** command.
6. Place the cursor in the work area. Press (and hold) the Middle-Mouse-Button (***wheel***) down and slide the mouse to the left, right, up, and down.
   Notice how the design shifts in the direction of your cursor movement. This is *panning*. Also, notice how the view changes in the World View window at the bottom right of the PCB Editor window.

Using the Zoom Command Options

In this part of the lab, you will use the ***Display - Zoom*** command from the top menu.

1. Select ***Display - Zoom - Window*** from the top menu, or the  icon.
   The PCB Editor Command window prompts you to pick the first corner of a new view window.
2. Click to place the first corner of the new window.
   As you move your cursor, a rectangle with inscribed diagonals representing the new window, is formed.
3. Click again to fix the size of the new window.
   Your work area zooms to display only the area you just outlined within the rectangle.

4. Select the ***Display - Zoom - World*** menu item.
   This command fits the entire extents of the drawing to your work area. There is no icon for this zoom option.

5. Select the ***Display - Zoom - Fit*** menu item, or the  icon.
   This command fits the layout to the work area.

6. Select the ***Display - Zoom - In*** menu item, or the  icon.
   The view in the work area zooms in.

7. Select the ***Display - Zoom - Out*** menu item, or the  icon.
   The view in the work area zooms out.

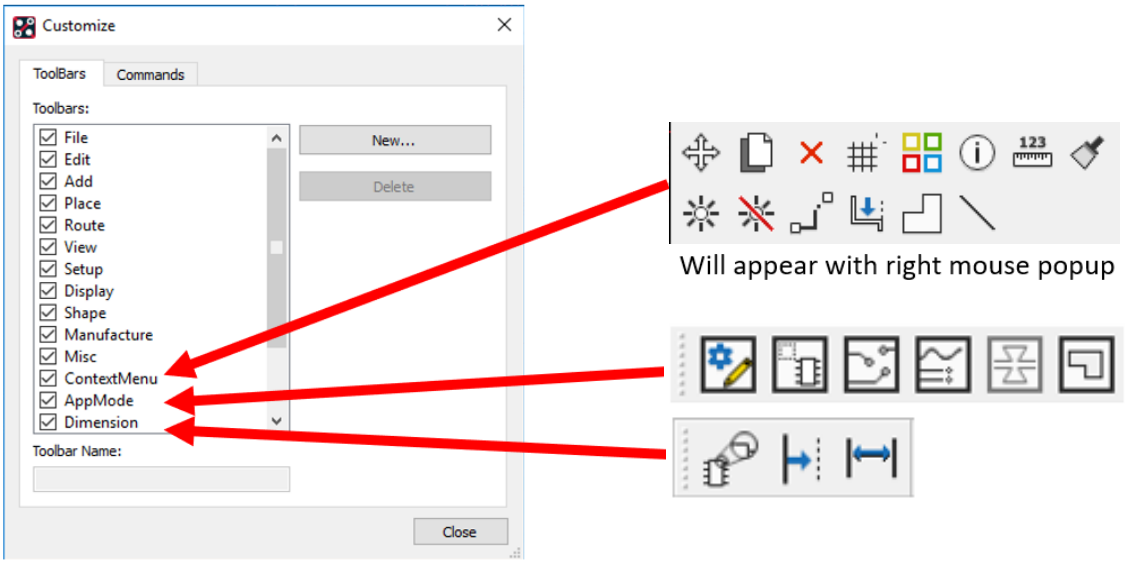
Using the Middle-Mouse-Button (Wheel) to Zoom In and Out

The middle mouse button can also be used to zoom in and out of your display.

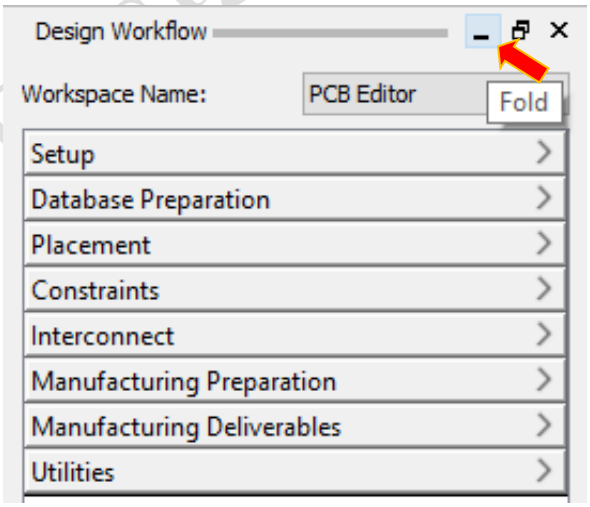
1. Place the cursor somewhere in the work area. Click, but do NOT hold, the Middle-Mouse-Button in the work area.
2. Without moving the mouse, move your mouse wheel forward and notice that the view enlarges or zooms in at the area you clicked on.
3. Now move your mouse wheel backwards and notice that the view decreases or zooms out at the area you clicked on.
4. Now hold the mouse wheel down while moving your cursor. You are now panning across the work area as you move the cursor.

Customizing Your View and Toolset

1. Select the ***Setup - More - Customize Toolbar*** menu item. The Customize dialog box appears.

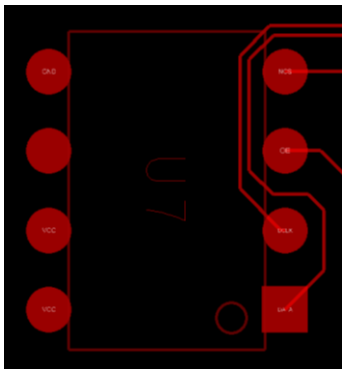


2. Check the boxes next to ***Context Menu, AppMode*** and ***Dimension*** to turn them **ON**.
3. Click **Close** to close the Customize dialog box.
4. Click on the **–** to fold the Design Workflow window, as we will not be using it in this class and it will give us more working area for our designs.

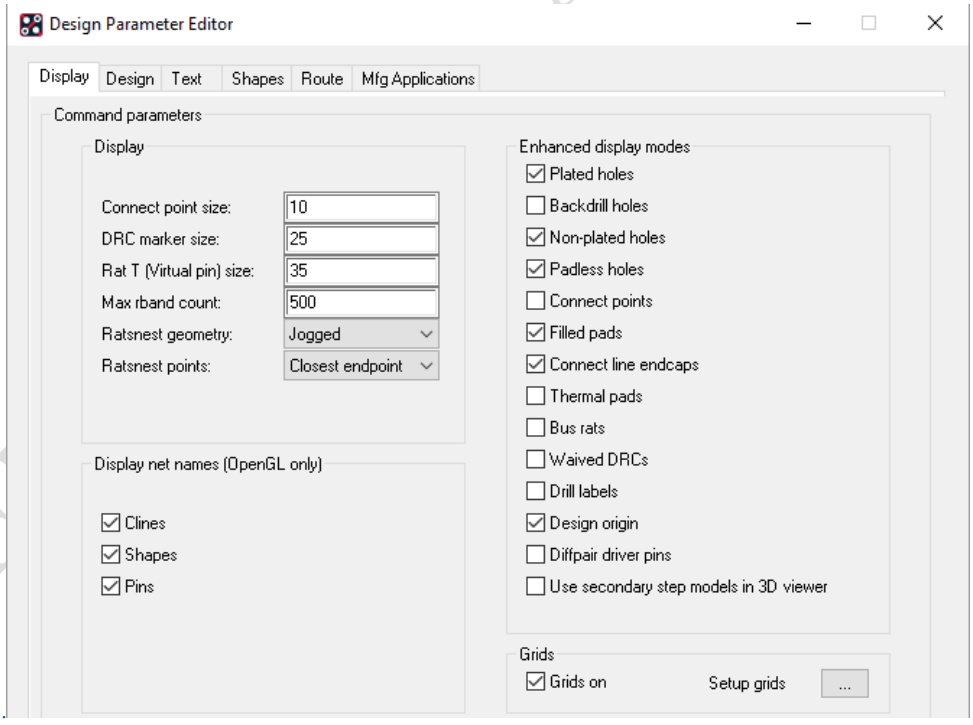


Choosing Drawing Options

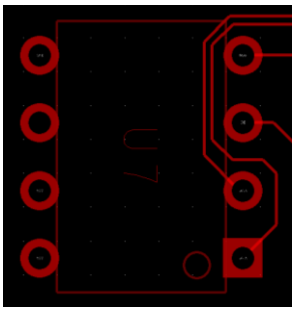
1. Zoom into the area around the ***U7*** component in the upper left part of the board.



2. Select ***Setup - Design Parameters*** to open the Design Parameters Editor dialog form. The ***Design Parameters Editor*** dialog box appears. Notice the six tabs near the top of this dialog box.
3. Click the ***Display*** tab to bring it forward if it is not already in the front.
4. Make sure all of the following display settings are **Enabled** for ***Plated holes***, ***Non-plated holes***, ***Padless holes, Filled pads***, ***Connect line endcaps, Design Origin***, and ***Grids on***, as shown in the figure, then click ***OK.***

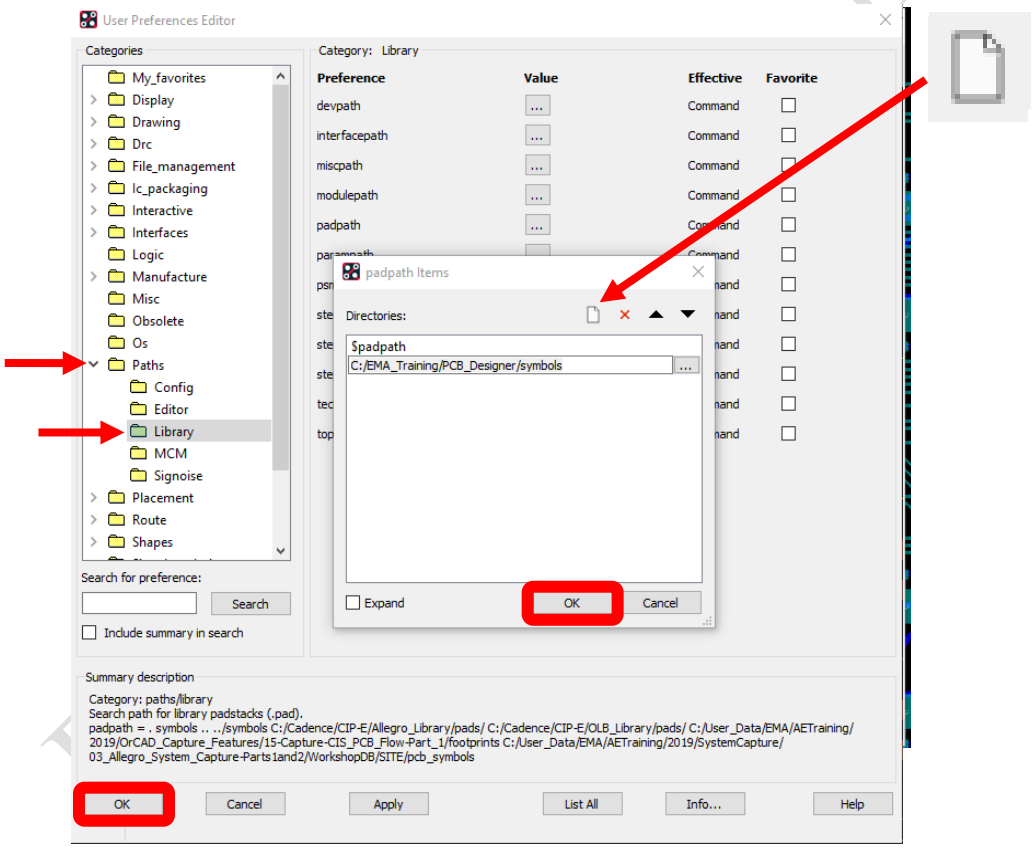


The drawing now shows the holes in the pads and the grid points.



Setting User Preferences

1. Choose the ***Setup - User Preferences*** menu item.
   The User Preferences Editor displays.
2. Go to the ***Paths - Library*** folder in the Categories pane on the left.
3. Click on the **…** button for the ***padpath*** setting in the right pane.
4. The padpath items windows opens
5. Click on the earmarked page icon to add a new path then, using the **…** button, browse to the symbols folder: ***C:/EMA_Training/PCB _Designer/symbols***



6. Click ***OK*** to accept the changes and close the padpath items dialog.
7. Using the same process, set the psmpath to the same location.
8. Click ***OK*** to accept all changes and close the User Preferences Editor.
9. Do ***not*** exit out of the PCB Editor. We will use this board for the next lab.

End of Lab

Lesson 2: Managing the PCB Editor Work Environment

Learning Objectives

In this lesson, you will:

- Control the color and visibility of objects
- Use the Find tab to locate board database objects and report information about them

In this section, you will familiarize yourself with the user interface and understand how you can streamline repetitive tasks. You will also view the PCB Editor classes and subclasses, work with setting colors and visibility of objects, and learn how to use the ***Check - Elements*** command to query design objects.

Categories, Classes and Subclasses

A design file is a composite of drawing layers. The drawing elements on each of these layers may be selectively colored and turned on or off as visible or invisible layers.

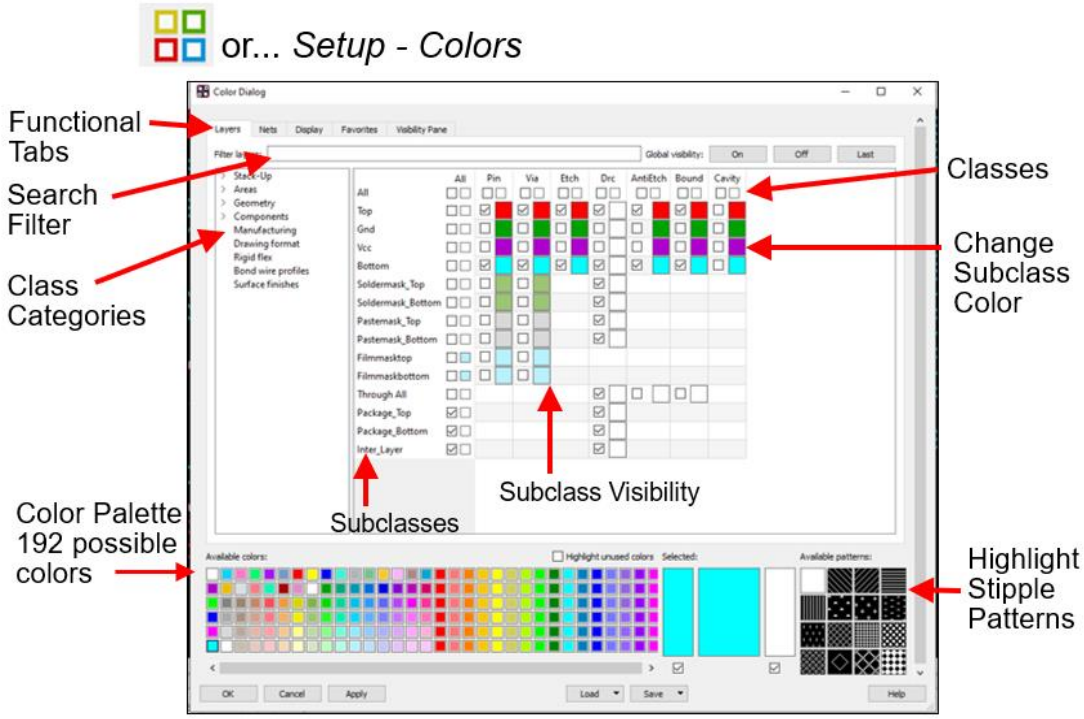
The PCB Editor organizes drawing layers into a hierarchy of classes and subclasses. Each class has a number of subclasses. The names and the classes are pre-defined and cannot be modified or deleted. There are a number of predefined subclasses for each class. These pre-defined subclass names cannot be modified or deleted either. However, you can add as many subclasses as you wish. Your graphical elements will appear on one of these class/subclass pairs. For example, your board outline will appear on the class titled Board Geometry and the subclass titled Design Outline.

At first glance, it appears that there is duplicate data contained in the database. As an example, there is a Silkscreen_Top subclass under the Board Geometry class, and a Silkscreen_Top subclass under the Package geometry class as well. However, since these are different class/subclass pairs, they can and typically will contain different data. The Board Geometry - Silkscreen_Top pair would contain information that is unique to the current board being created, maybe the board number. Whereas, the Package Geometry - Silkscreen_Top pair would contain information that is unique to the footprint or package as it is known in the PCB Editor. So, it could contain the silkscreen outline for the part and maybe a symbol to indicate the positive side of a polarized capacitor.

Each class/subclass has its own color and visibility settings. Folders are classes that have been combined to aid you in controlling the color and visibility and are only used in the color form, which will be discussed shortly.

All of the board routing will appear on subclasses under the class called Etch. These subclasses have special DRC checking properties that most of the other subclasses do not have. You need to create a subclass for each layer of the printed circuit board. So, if you have a six-layer printed circuit board, you need to have six subclasses under the class called Etch. Each board layer will also have a subclass under the classes Pin, Via, DRC, Ant Etch, Boundary, and Cavity.

Controlling Color and Visibility



The Color Dialog form is displayed by selecting the ***Setup - Color*** option from the top menu or by selecting the ***Color192*** icon. You will use this form to turn on or off the visibility for subclasses, as well as to set colors for subclasses. A checkmark "✓" in the box indicates that the subclass is currently visible. A blank box means the class/subclass pair is invisible.

Five functional tabs are available across the top of the form to break up the major features into their own sections. The functional tabs are: Layers, Nets, Display, Favorites, and Visibility Pane.

- **Layers** – Controls the color and visibility for all classes and subclasses
- **Nets** – Provides the ability to color a single net or group of nets (i.e. GND).
- **Display** – Controls the colors for elements such as temporary highlight, grid, ratsnest, drill holes, and background. It also controls the Transparency settings and Shadow Mode brightness.
- **Favorites** – Contains the classes and subclasses that the user chooses to include for quick access without having to browse all of the subclasses in the individual class categories.
- **Visibility Pane** - Configures the options that are available in the Visibility tab of the Control Panel.
- **Filter Layers option** - Has been added directly below the Functional tabs to easily search for specific subclasses or groups of subclasses based on a class category.

The left most pane contains all of the categories of classes for the design. Select on the appropriate category to display the associated classes and subclasses for that category. Some of the categories are expandable to display sub-categories to help simplify what is displayed in the main window.

In the main window section of the form the classes are displayed across the top and all subclasses are displayed in the left-hand side of the window.

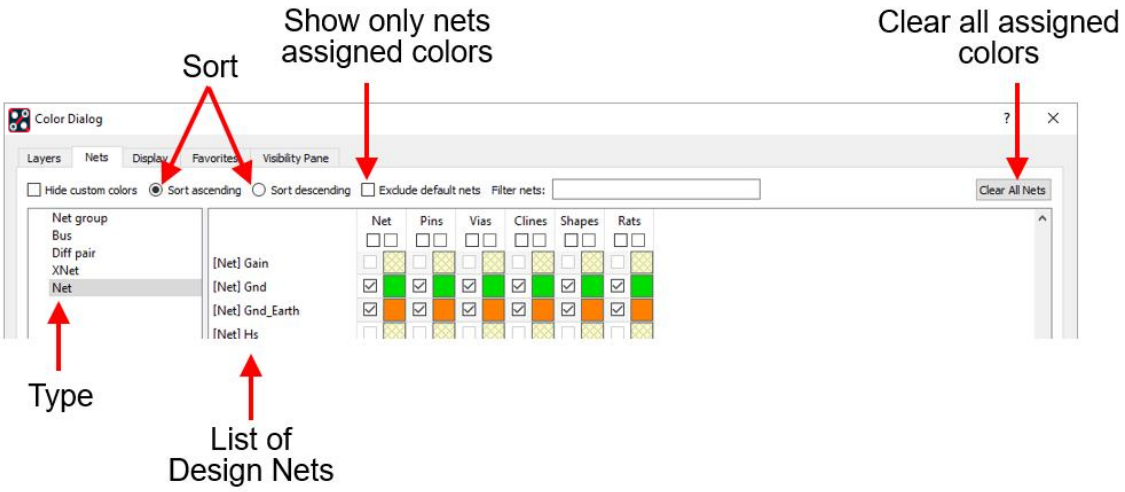
- You can make all subclasses under a class visible or invisible by selecting the box under the desired class name.
- You can make all classes for a given subclass visible or invisible by selecting the box to the right of a desired subclass name.
- You can make a single class/subclass pair visible or invisible by selecting the box for that pair.

At the top right of the form are two buttons for Global visibility. If you select the "On" button, all classes and subclasses for the entire design will be made visible. If you select the "Off" button, all classes and subclasses for the entire design will be made invisible. If you select the "Last" button all of the classes and subclasses that were previously visible prior to selecting the Global visibility "On" or "Off" options will be displayed.

To change the color of a class, subclass, or an individual class/subclass pair, first, select the desired color from the Available colors area. Then select the color chip for the desired class, subclass, or individual class/subclass pair. There are a total of 192 colors that can be utilized.

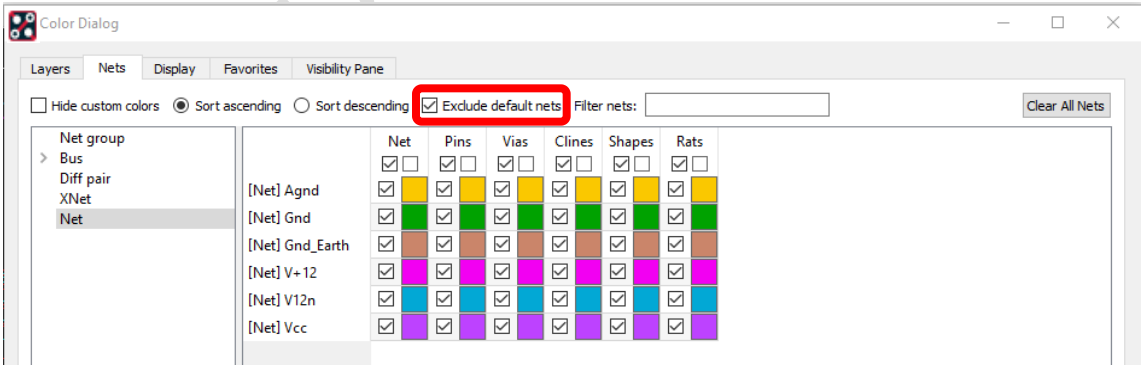
Information about colors assigned to individual layers, and which layers are visible and invisible, is stored in the PCB Editor database.

Coloring Nets in the Color Dialog



The Color Dialog also includes a section to apply a Net level color scheme. When you toggle on the Nets tab, the Color Dialog form will display all nets in the database. You can also apply colors to Net Groups, Buses, Differential Pairs and Nets. You can assign colors to the entire net, or to portions of the net such as pins, vias, connect lines, shapes, and ratsnests. To de-assign all assigned colors, click on the **Clear all nets** button. To de-assign the color from a specific net, right select on the color chip on that net and select Clear Custom Color.

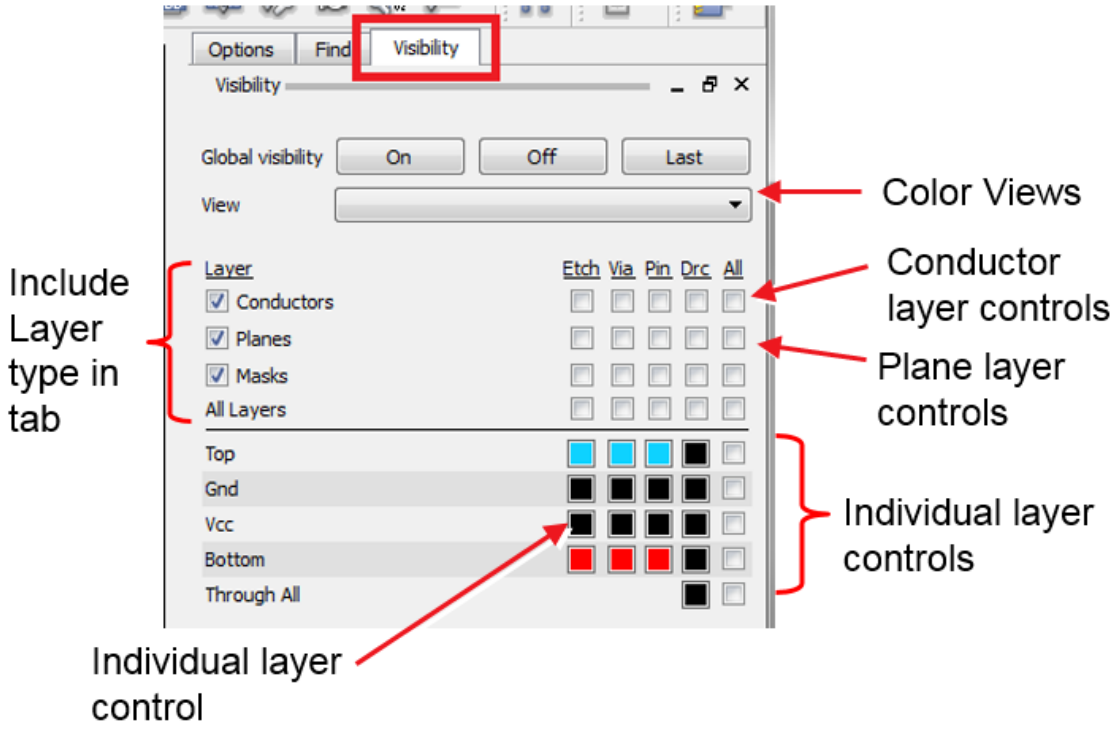
To refine the display of the current type use “Exclude default nets” to only display nets that have assigned colors.



You can also use the Sort fields “Sort ascending” and “Sort descending” to change the alphabetical order of the net names.

A related ***Display - Assign Color*** menu command assigns a color and highlights an element without requiring the use of the Color Dialog form.

Controlling Etch Visibility



Using the Visibility tab is a quick way to turn on or off certain layers or elements. You can separately control etch routing layers from the plane and mask layers, as well as Etch, Pins, Vias and DRCs.

Conductor Controls

The Conductor check boxes let you individually turn on or off all etch, pin, vias or DRCs for all layers defined as conductor. By selecting the **All** check box, you can turn on and off all etch, pins, vias and DRCs for all conductor layers at once.

Plane Controls

The Planes check boxes let you individually turn on or off all etch, pin, vias or DRCs for all layers defined as plane. By selecting the **All** check box, you can turn on or off all etch, pins, vias or DRCs for all plane layers at once.

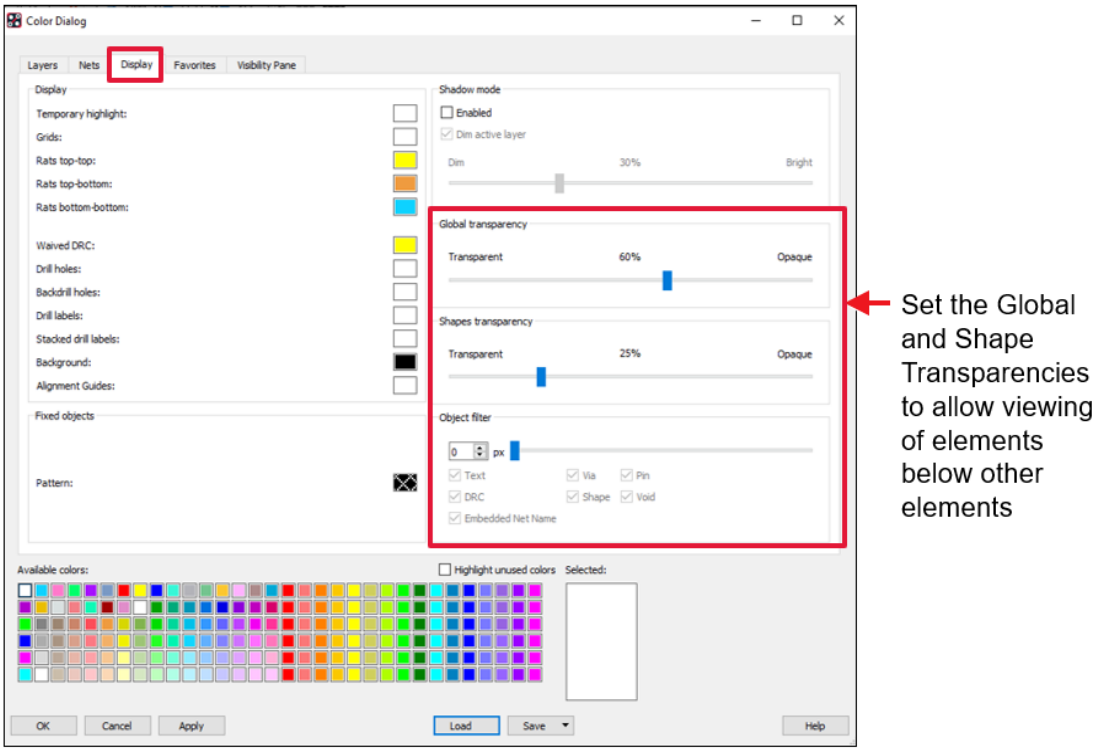
Individual Layer Control

By selecting the check box under the **All** column in the individual layer row, you can turn on or off all etch, pins, vias or DRCs for that layer.

Individual Element Control

You can turn on or off a single element type (etch, via, pin) by selecting the element. If you select on an individual element type chip with the Right Mouse Button, the color palette window will be displayed where you can change the color of the selected element.

Transparency Options



The OpenGL integrated Application Programming Interface displays elements semi transparently, allowing the user to view elements that lie beneath other elements.

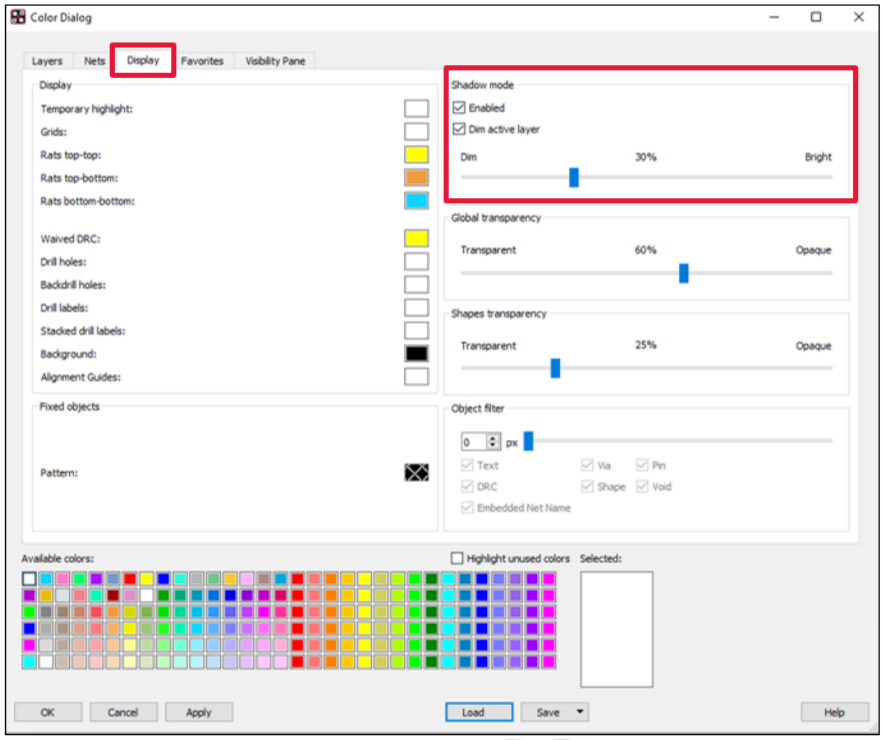
Global Transparency assigns varying degrees of transparency to all elements in the design except shapes.

- Sliding the bar completely to the right causes everything to be displayed opaquely.
- Sliding the bar to the left causes filled geometry, such as connect lines and pads, to display with less intensity.

Shape Transparency assigns varying degrees of transparency to shapes and planes only.

- Sliding the bar completely to the right causes shapes to be displayed opaquely.
- Sliding the bar to the left causes the shapes to display with less intensity.

Graphics Dimming or Shadow Mode



Icon toggles Shadow Mode on and off

The Shadow Mode option gives you the ability to provide distinct levels of visibility that are based on the importance or highlighting of an object. The main control for shadowing is located in the Color Dialog form under the Display tab. With Shadow Mode turned on, the brightness slide bar controls the color intensity of the non-important or nonhighlighted objects. The higher the brightness percentage, the less difference in the color between the important and the non-important objects. After changing the Brightness factor using the slider, select the **Apply** button to see the changes in the graphics window. You may use the **Shadow Toggle** icon to turn on and turn off the shadowing feature.

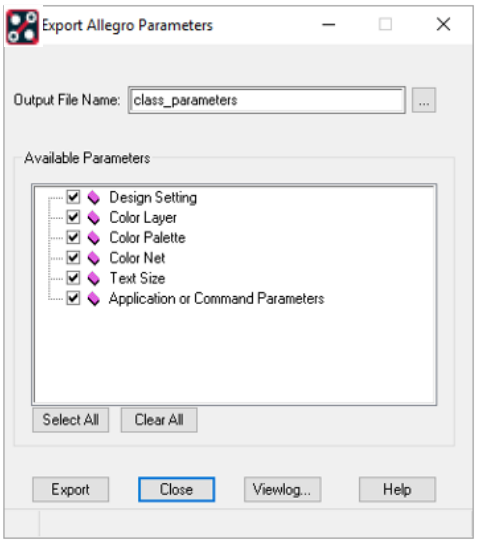
Objects of importance are defined as follows:

- Items that have been highlighted using the **Highlight** command
- Items that are highlighted by the current active command
- The current Active layer as defined in the Options window

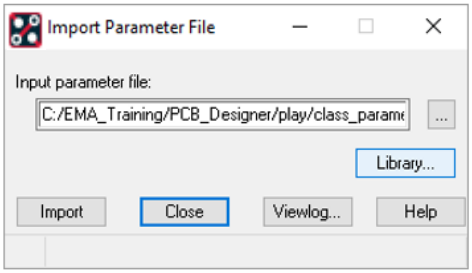
The default is to have Shadow Mode disabled. When Shadow Mode is first enabled, the default brightness is 50 percent.

Export and Import Design Parameters

Export - More - Color/Board Parameters



Import - Color/Board Parameters



Exports/imports a database parameter (`.prm`) file containing design parameter records

A parameters file can be exported from one database and imported into another. This allows you to have the same look and feel from one database to another. The types of parameters that can be written/read are as follows:

- **Design Setting** - Global values and grid settings. This includes the settings in the Design Parameters Editor form and the grid settings.
- **Artwork** - Artwork film definitions. This includes the film record definitions and the parameters for each film record.
- **Color Layer –** Color parameters and color table.
- **Color Palette –** The color palette is written to the parameters file.
- **Color Net** - Net custom color and states. When a file containing net color data is imported into any design, only the nets that exist in that design are read; the rest are ignored. Net color assignments are not overwritten, but rather incremented. To completely replace net color assignments, click Clear All Nets in the Nets section of the Color dialog box before importing a file containing net color data.
- **Text Size** - Text size settings. This includes the total number of text blocks and their text size parameters, such as text block width, text block height, and so on.
- **Application or Command Parameters** - All other supported parameters, including those for auto rename, auto assignment, auto silkscreen, global dynamic fill, autovoid, export logic, drafting, gloss line fattening, gloss dielectric generation, Options window tab settings, test prep, automatic placement, auto swap, thieving, backdrill, interactive flow planner (PCB Editor only), and Signoise analysis.

Lab

Lab 2-1: Controlling Visibility and Color

- Controlling visibility
- Controlling colors
- Setting colors using the Import/Export parameters command
- Using the shadow mode option

Lab 2-1: Controlling Visibility and Color

Objective: Set up colors and visibility of graphical elements in a design.

In this lab, you will change the default visibility and color assignments on each new layer to suit your personal preferences. Changing layer visibility and assigning colors is a procedure you will need to do over and over again. You can save a parameters file to capture your preferred color setup.

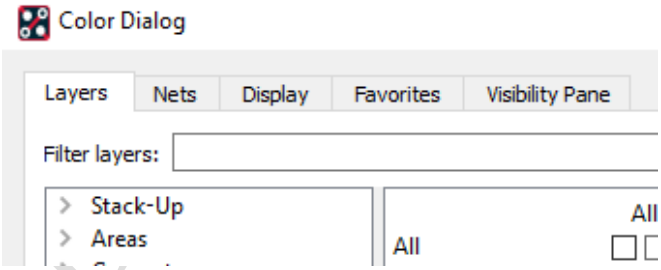
Controlling Visibility

First, let's set the visibility and color assignments for the design.

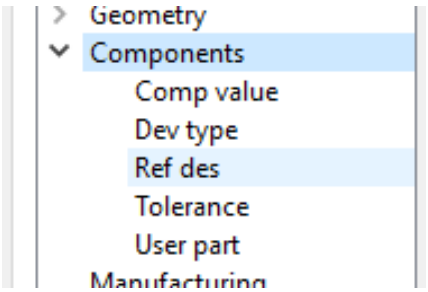
1. Start PCB Editor and open the `cds_routed.brd` file in the *play* directory, if you do not already have it running.
2. Click the ***Color192*** icon.

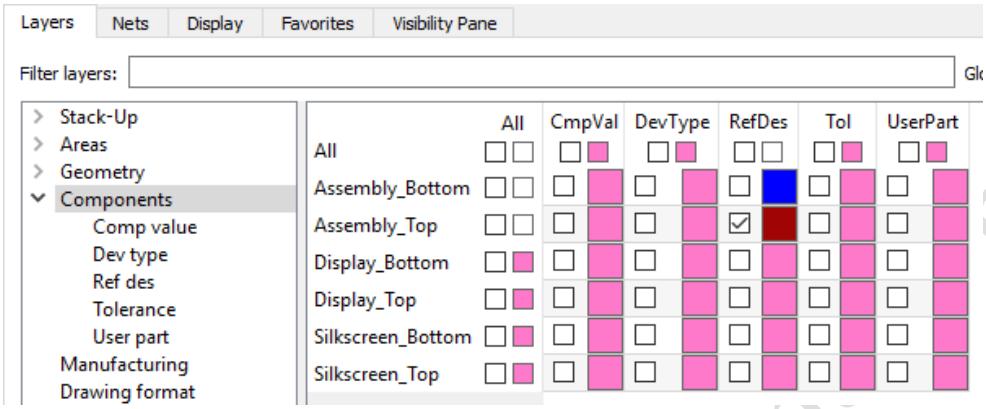
   The ***Color Dialog*** form appears.
3. At the top of the Color Dialog form, make sure that the ***Layers*** tab is selected.

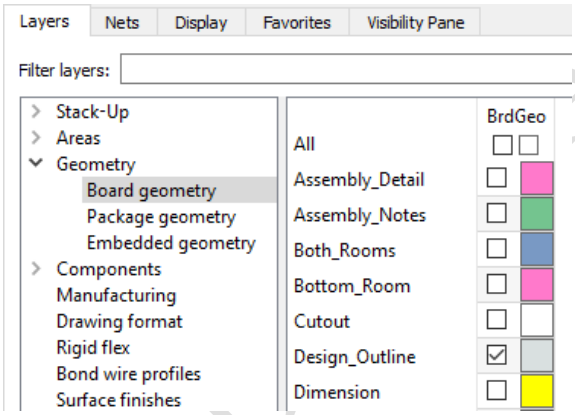
4. Near the top right of the form, select the ***Global Visibility*** '***Off***' box.
   This action turns off the visibility of all layers in the design, so you can begin turning on only the layers that you wish see.
5. Expand the ***Components*** category and select the ***Ref Des*** class as shown.

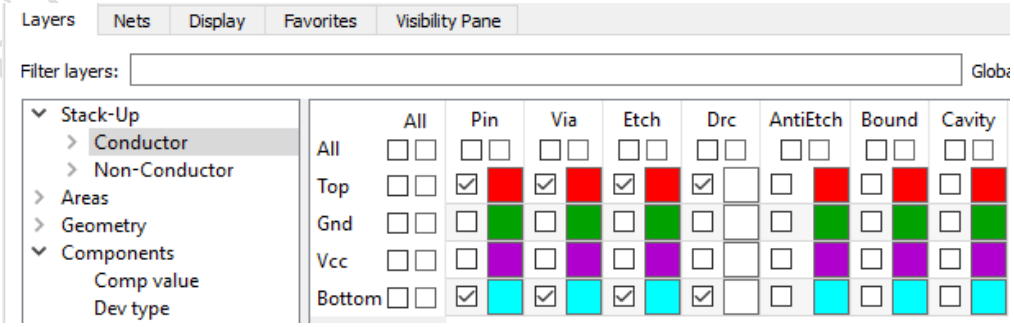
6. Under the Subclasses column, enable the visibility box for the subclass ***Assembly_Top***. A checkmark (✓) in the box indicates the subclass is turned ON.



7. Select the ***Geometry*** category and in the ***Board Geometry*** class enable the visibility for the ***Design_Outline*** subclass.



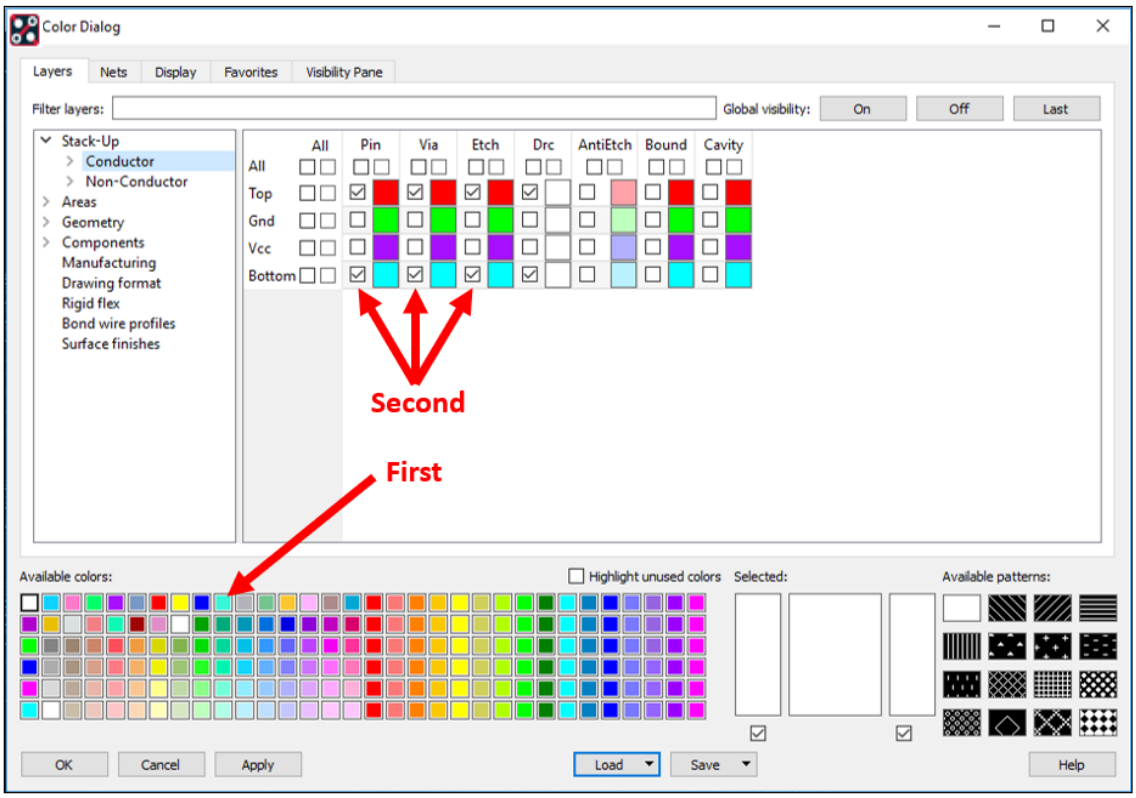
8. While still in the geometry category, select the ***Package Geometry*** class and enable the visibility for ***Assembly_Top***.
9. Expand the ***Stack-Up*** category and select the ***Conductor*** group.
10. Enable visibility for subclasses in this group, as shown in the figure, then click ***Apply***.



Controlling Colors

Change the colors of some of the subclasses in the ***Stack-Up - Conductor*** category.

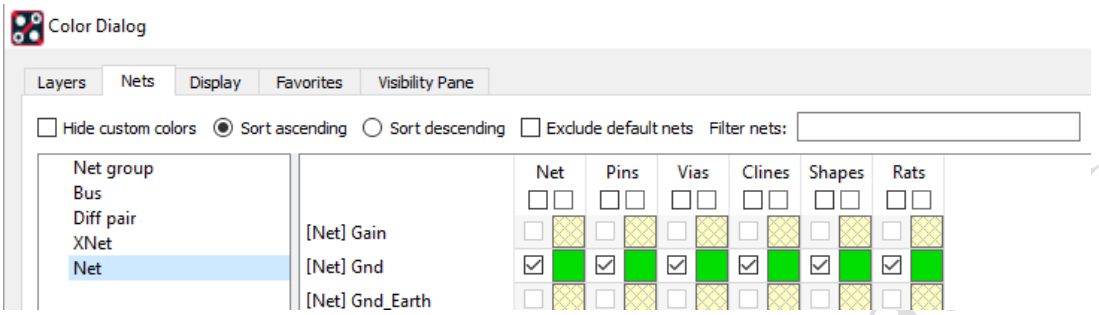
1. Click any color button in the ***Available colors*** area of the ***Color Dialog***, then select the subclass color button next to ***Bottom*** for ***Etch***, ***Pin*** and ***Via***. (It is generally recommended that the subclass elements be set to the same color.)



2. If you like, change the color of any other conductor subclass to any color you want. If you have time, feel free to change the color of any other class/subclass.

Coloring Nets

1. At the top left of the form, select the ***Nets*** tab.
2. Click any color button in the ***Available colors*** area, then select the ***Net*** class color button for the net ***GND*** as shown below.

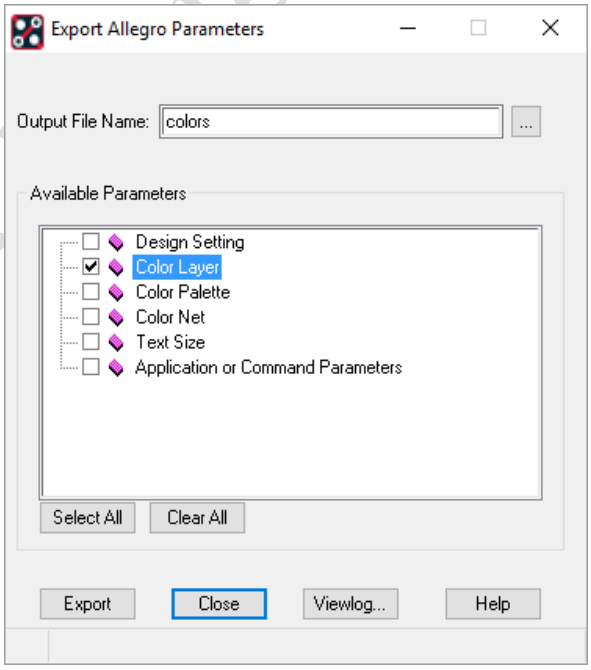


It is recommended that the classes (Net, Pin, Vias, Clines, Shapes, rats) for this net all be set to the same color. Remember that the classes appear in the top row of the selected category.

3. Click ***OK*** to apply and close the ***Color Dialog*** form.

Setting Colors Using the Import/Export – Parameters Command

1. Now that we have assigned our preferred color settings, select ***Export – More – Color/Board Parameters*** from the top menu.
2. In the resultant ***Export Allegro Parameters*** form, check the box next to ***Color Layer*** and enter the name of ***colors*** in the ***Output File Name*** field (See the figure below).



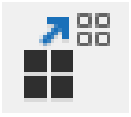
3. Click the ***Export*** button.

The file `colors.prm` will be written to the current working directory.

4. Click the ***Close*** button to close the ***Export Allegro Parameters*** form.
5. On the PCB Editor Command line, type **`reopen`** to again open the board design at its last saved view.
   This is the same as ***File - Open*** or clicking on the open icon.
6. In the ***Visibility*** Tab of the ***Control Panel***, check the ***Global Visibility - Off*** box.
   This action resets all visibilities to off.
7. Select ***Import – Color/Board Parameters*** to open the ***Import Parameter File*** form.
8. Enter ***colors*** in the ***Input parameter file*** field.
9. Select ***Import*** to start the ***Import Parameters*** command.
   Notice how the colors have been set to the changes you previously made, and that the visibilities have also been changed.
10. Select ***Close*** to close the ***Import Parameters File*** form.

Using the Shadow Mode Option

1. Make sure you are zoomed out around the entire board outline.
   Hint: Use ***Zoom fit***.
2. Click the ***Color192*** icon.
   The Color Dialog form appears.
3. Select the ***Display*** tab.
4. Select ***Enable*** for the ***Shadow Mode*** option.
5. Check the box to ***Dim active layer***
6. Select and drag the ***Brightness*** slide bar to ***25*** or ***30%***.
7. Click ***OK*** to close the Color Dialog form.
   Notice how the color of all layers is drawn in the dimmed color and the highlighted net shows up much better.
8. Select the ***Shadow Mode*** toggle icon to turn off the shadow mode.



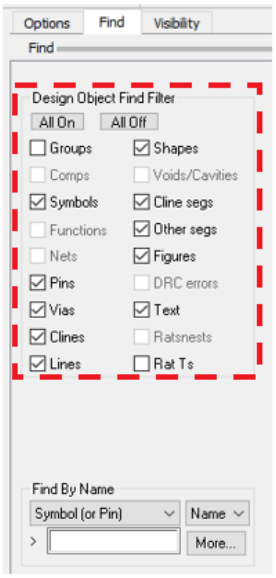
End of Lab

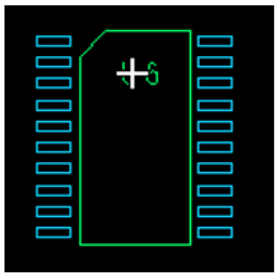
Find Tab - Selectable Objects List

You use the *Design Object Find Filter* section of the *Find* tab when selecting data base elements with the mouse

- The "list" is searched for items that are checked
- The selection order goes from the top left (Groups) to bottom right (Rat Ts)
- If there are multiple items found at the selection point, the first checked box found in the element selection list will be used

Challenge: Given the settings to the right, when the *Move* command is executed, what will be moved in the example picture (note the cursor location)?





The ***Find*** tab is more commonly referred to as the *Find Filter*. This is one of the more important forms used in the PCB Editor. It is critical that you pay attention to and understand the settings.

The top section of this form contains the ***Design Object Find Filter*** box. This section determines what types of objects in the design are to be acted upon when you select elements with the mouse.

If the pick occurs at a point where there are multiple items displayed or the items could be classified in different categories, the system prioritizes the selection by going from the top object in the left column (Groups) to the bottom object in the right column (Rat Ts) and finding the first checked item. For example, in the example shown, the entire part would be moved. This is because the Symbols item would be the first check box found in the Find Filter even though a piece of text was selected in the picture.

Using the ***All On*** and ***All Off*** buttons is a quick way to turn on or off all the items in the ***Design Object Find Filter*** box. Some of the boxes will be greyed out, depending on the active command.

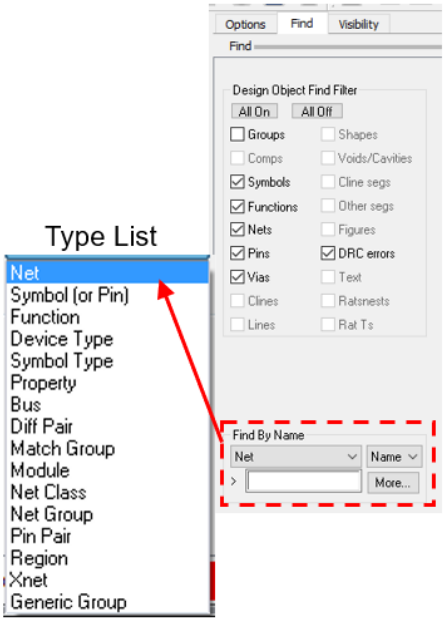
If you drag with the Left-Mouse-Button and create a selection rectangle, all elements that match any item checked in the Find Filter will be selected.

Using the Find by Name Section

Use the *Find by Name* section of the *Find* Tab to:

- Highlight a net name
- Locate a part placed in the design by its refdes
- Use the pull-down field to set which type of a name you will enter
- Enter the name in the blank (>) field or use the *More* button to display a scrollable list of all elements matching the desired "type"

NOTE: The check boxes selected in the *Design Object Find Filter* section have no affect when using the *Find by Name* section, with the exception of the *Property* pull-down field.

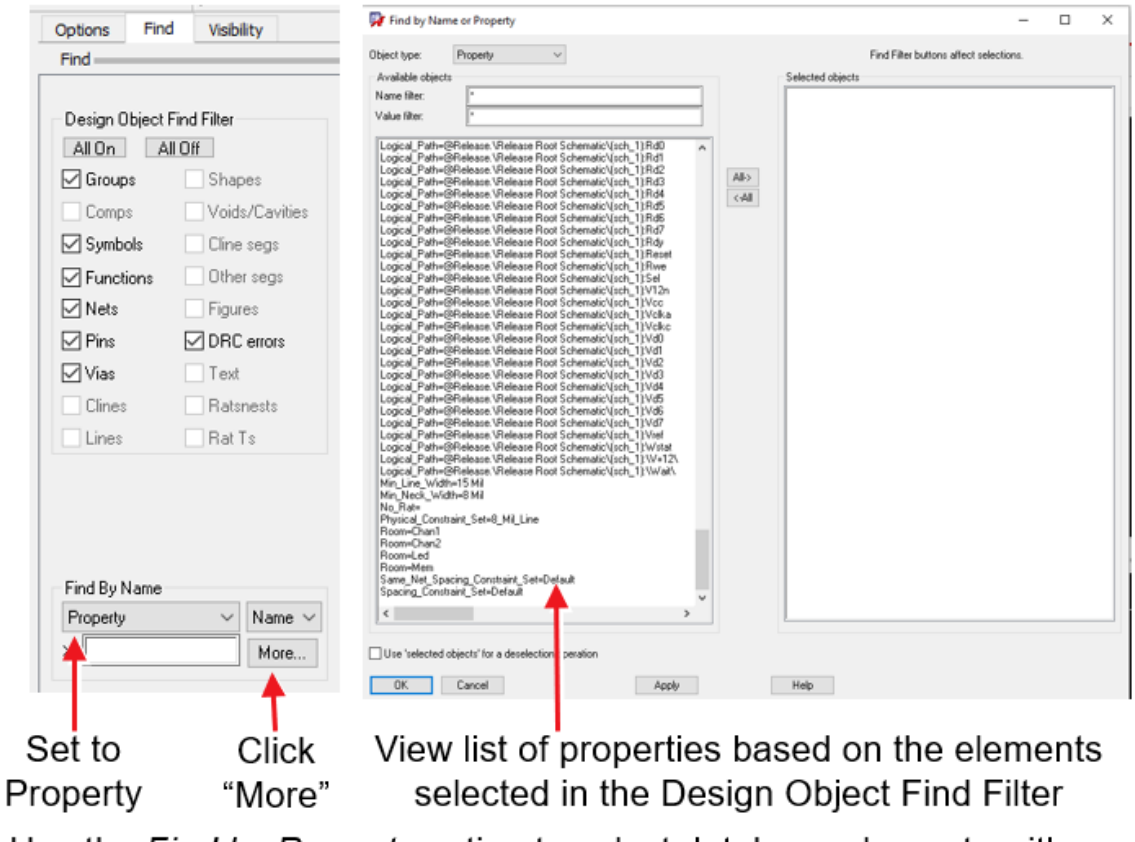


The bottom section of the ***Find Filter*** contains the ***Find by Name*** box. You use the ***Find by Name*** section to select elements by a name rather than graphically.

For example, if you wanted to highlight the net called GND, you would execute the ***Display - Highlight*** command, go down to the ***Find by Name*** section of the ***Find*** tab click the down arrow and select *Net*. Then in the blank field immediately below the ***Net*** pull-down field, enter **GND**, and press ***TAB***. The net named GND would then be highlighted.

The ***More...*** button in the lower right corner of the ***Find by Name*** section opens a scrolling window that lets you choose from a list of all available net names, component names, properties, etc. It should be noted that when you use the *Find by Name* section, the check boxes in the ***Design Object Find Filter*** section are ignored, unless the Property pull-down option is used.

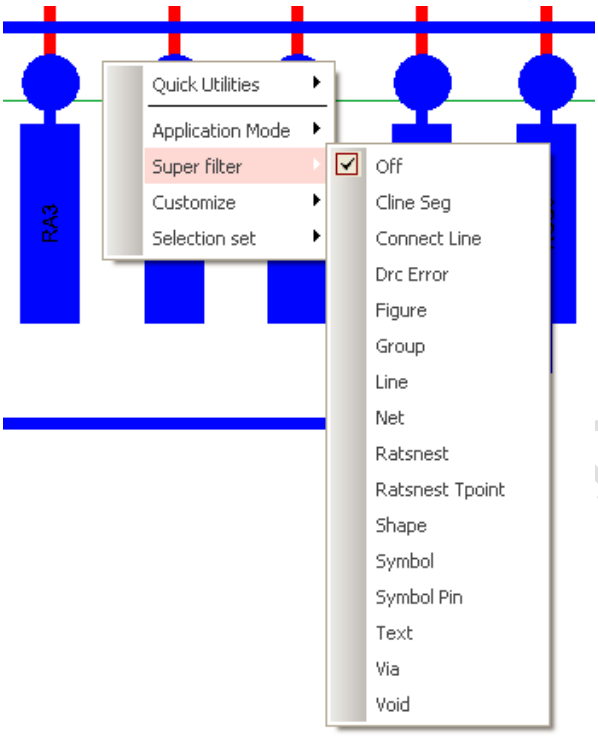
Using Find by Name – Property Selection



Use the *Find by Property* option to select database elements with a common property such as "*FIXED*", "*MIN_LINE_WIDTH*", etc.

As previously noted, the ***Property*** option under the ***Find by Name*** box uses the ***Design Object Find Filter*** section. When you select the ***Property*** option and click the '***More***' button, all properties are gathered that are attached to the checked items. A scroll list is generated specifying all the unique properties that were found.

The Super Filter



The Super filter lets you choose a particular element type to refine your selection set and temporarily disable all other elements from the Right-Mouse-Button pop-up menu rather than the Find Filter. You can only choose one database element type using the Super filter.

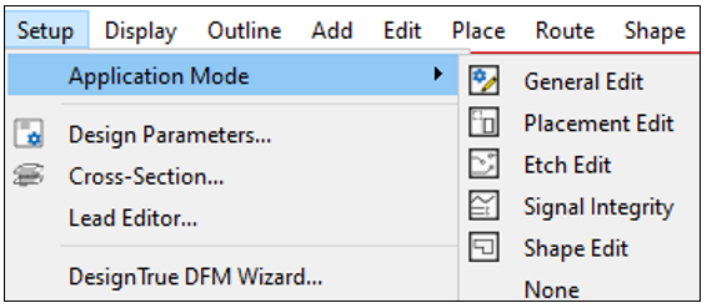
For example, let's suppose you want to move many parts in your design. Without using the Super Filter, you would need to hover your mouse over a part, use the tab key to select the symbol, then move the part. By using the Super Filter and turning on only symbols, as soon as you hover your mouse over a part, the symbol is immediately selected and ready to move.

Note The Super filter only applies when you are working in the pre-selection mode.

Application Modes

Application Modes available:

- General Edit
- Placement Edit
- Etch Edit
- Signal Integrity
- Shape Edit
- None



Application Modes may be accessed through several methods:

- *Setup – Application Modes*
- *OrCAD PCB Editor selects command based on object clicked on*
- Application Mode may be set using the Status bar

Application modes provide an intuitive environment in which commands used frequently during a particular phase of the design, such as component placement, or routing are automatically selected based on the element the user clicks on.

As an example, if you are in Etch Edit application mode and you click on a component pad, PCB Editor will automatically select the Add Connect command for you.

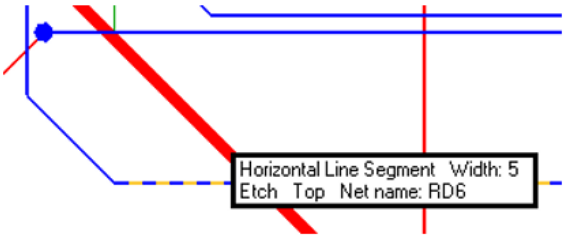
The application modes available are:

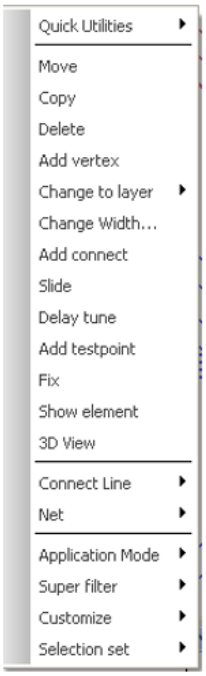
- **General Edit** - This is the default mode. It allows you to perform editing tasks, including place and route, as well as moving, copying and mirroring items.
- **Placement Edit** – This application mode customizes your environment for component placement and alignment. If you click on a component while in this mode, PCB Editor will select the Move command for you automatically.
- **Etch Edit** - This application mode customizes your environment to perform interactive routing. If you click on an existing trace segment while in this mode, PCB Editor will select the Slide command for you automatically.
- **Signal Integrity** - This application provides quick and easy access to frequently use SI commands. We will not cover any Signal Integrity tools in this class
- **Shape Edit** - This application is a tuned environment primarily designed to increase efficiency with shape boundary editing. If you click on a shape edge while in this mode, you will either be able to slide or cut a notch out of that edge, depending on what is set in the Options tab. You can also easily chamfer or round a corner of a shape, depending on the Options tab setting.
- **None** - This mode completely disables the pre-select mode and restores the pre-16.0 version behavior.

Pre-selection Mode

To use Pre-selection Mode

- Set Find Filter
- Hover mouse over element
- Tab through hierarchical elements if necessary
- Right Mouse Button to select a command
- Don't need to use the commands from the main menu or toolbar





The PCB Editor defaults to a pre-selection use model, which lets you choose a design **element (noun)**, and then a **command (verb)** from the Right-Mouse-Button pop-up menu. This pre-select mode is based on what elements were enabled in the Find filter.

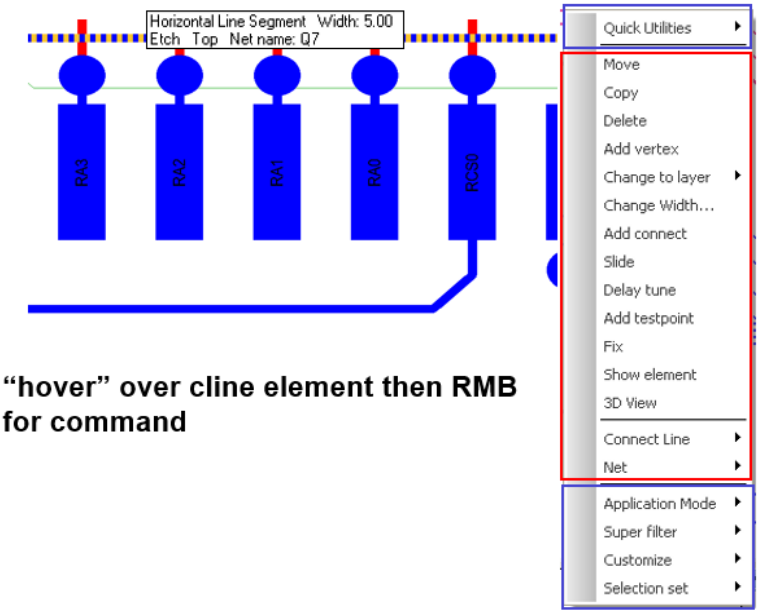
The pre-selection use model lets you easily access commands based on the design elements you've chosen, which the tool highlights and uses as a selection set, thereby reducing mouse clicks and allowing you to remain focused on the design canvas.

While base elements such as cline segs, pins, and vias cannot be parents of other elements, they are the building blocks of which hierarchical elements such as nets, clines, and components are made. A pin is a child of a net, as well as a child of a symbol. Similarly, a cline is a child of a net.

If you enable more than one base or hierarchical element in the Find Filter, the base element determines the hierarchical elements you may choose. You may navigate through the hierarchy by using the Tab or Shift-Tab key. Note that the Tab key is unavailable when you select by window, which chooses only top-level hierarchical elements.

Right-Mouse-Button Command Use

Right-Mouse-Button selections while “hovering” over specific element



“hover” over cline element then RMB for command

The commands that are shown in the Right-Mouse-Button pop-up menu depend upon where your cursor is when you select with the mouse. In the left picture, the mouse was hovered over a Horizontal line segment. The Right-Mouse-Button contains four sections. The top and bottom sections will be discussed shortly.

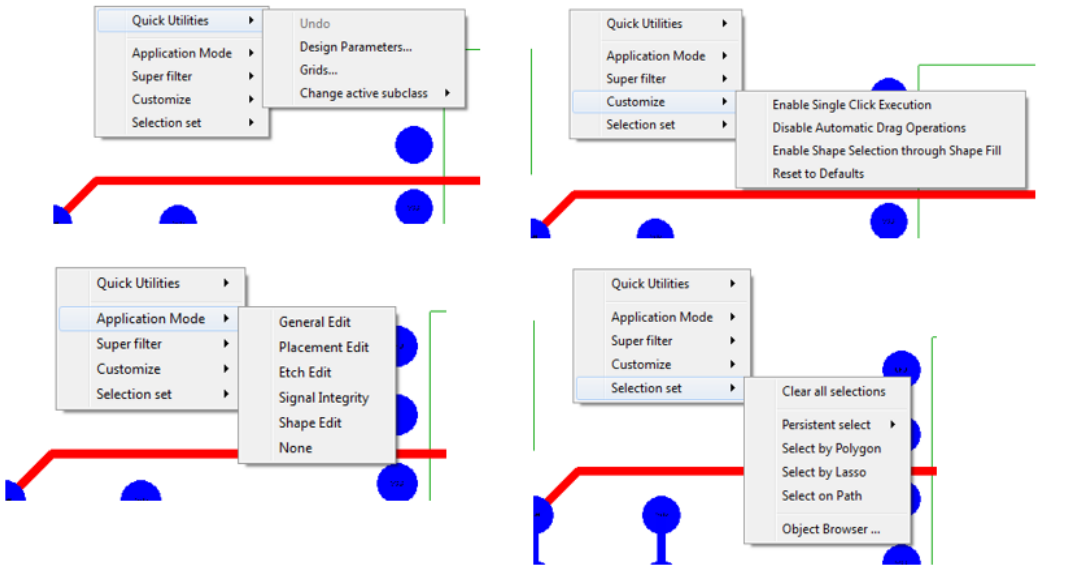
The second section contains commands that can be executed on the element or elements that were selected when the Right-Mouse-Button was pushed. These commands are preconfigured in the software and cannot be customized. In the case shown, because a Horizontal line segment was selected, some of the commands that can be executed are Delete, Change width, and so on.

The third section of the pop-up menu contains sub-menus that contain commands that can be executed on the hierarchical members of the selected item or items. In this case, because a Horizontal line segment was selected, the hierarchical parents could be either the connect line or the net.

In the right-hand picture, the Right-Mouse-Button was hovered over a non-etch line object. The pop-up menu now allows you to move the lines and text from outside their present class/subclass to another class/subclass. Hover over the line or text or rectangular element then use the Right-Mouse-Button to access the Change class/subclass command. Select a new class then target subclass form the pop-up menu selections.

Right-Mouse-Button Common Area Commands

Right-Mouse-Button selections while not “hovering” over any element



Quick Utilities - contains the following options/sub-menus:

- **Undo** - Performs the standard undo command.
- **Design Parameters** - Displays the Design Parameters form as described earlier.
- **Grids** - Displays the Define Grids form. This form will be discussed later.
- **Change Active Subclass** - Lets you change the current active subclass.

Application Mode - Allows you to change the application mode.
Super Filter - Allows you to set filtering that supersedes the standard Find Filter.

Customize - Contains the following options:

- **Enable Single Click Execution** - Sets command execution to single click.
- **Disable Automatic Drag Operations** - Initiates select by window.
- **Enable Shape Selection through Shape Fill** - Allows the selection of a shape in the Pre-Select mode when cursor is hovering over any part of the shape.
- **Reset to Defaults** - Resets the above three options to their default state.

Selection Set - Contains the following options:

- **Clear All Selections** - Empties the selection set.
- **Select by Polygon** – Allows the user to create a selection set by drawing a polygon around elements.
- **Select by Lasso –** Allows the user to create a selection set by drawing a free-form polygon around elements.
- **Select by Path –** Allows the user to create a selection set by drawing a line through the elements.
- **Object Browser** - Allows you to search for elements by name or by property. Using the Find by Name/Property dialog.

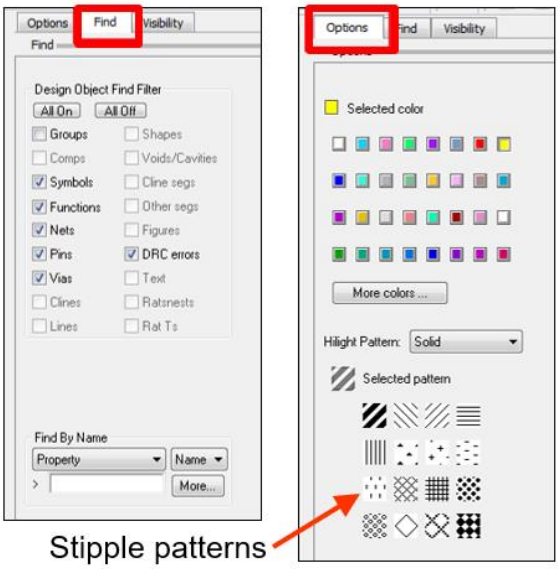
Coloring Elements

Display – Assign Color

...Or 

Common sequence for coloring elements with the mouse is:

1. Select the command
2. Activate the *Find Filter* tab
3. Turn on desired elements
4. Select desired color in Options tab
5. Select stipple pattern (optional)
6. Select the elements in the design window to color



The ***Display - Assign Color*** command is used to display a database element in a certain color with the option of overlaying a stipple pattern on it. The type of database element highlighted is based upon the Find Filter. Once colored, the elements remain colored until they are de-highlighted using the ***Display - Dehighlight*** command.

You initially have a choice of 32 different colors and 15 stipple patterns to choose from in the ***Options*** tab. Clicking on the "***More colors***" button opens a palette that contains the complete 192 colors defined in the ***Setup - Colors*** command.

When invoking the "***Assign color***" command, select a color and/or a stipple pattern from the ***Options*** tab. The pull-down menu located in the center of the form sets the selected highlight state:

- Solid
- Selected Pattern - the selected color and pattern are assigned to database elements. The 'selected pattern' is displayed in the 'Selected pattern' button.

The "blank" pattern button is used to deselect the stipple pattern. When the stipple pattern is cleared, 'Highlight Pattern' pulldown is set to 'System Defaults' state.

The ***Color Dialog*** form has been enhanced to allow a stipple patterns to be assigned to layers. Assigning a pattern to a color cell applies the pattern to all objects on that layer.

Stipples applied to Constraint Regions and Keepouts (layer basis) in the above example.

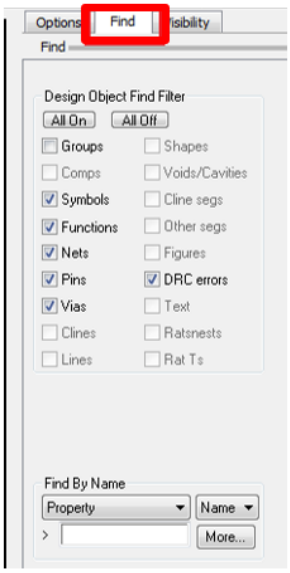
Highlight Elements

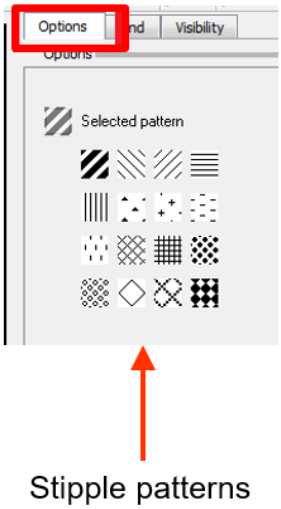
Display – Highlight

...Or

Common sequence for coloring elements with the mouse is:

1. Start the command
2. Activate the *Find Folder* tab
3. Click the *All Off* button
4. Toggle on desired elements
5. Select stipple pattern
6. Select the elements in the design window to highlight



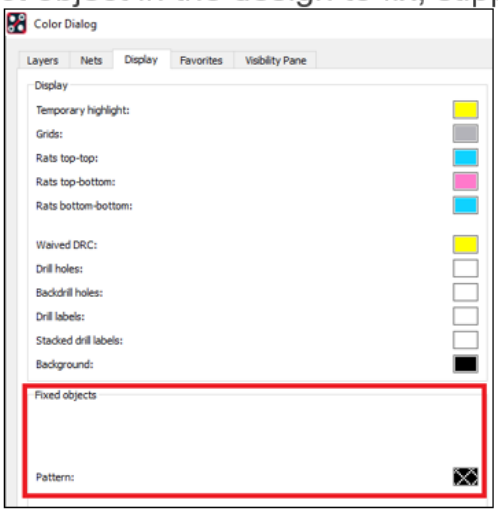


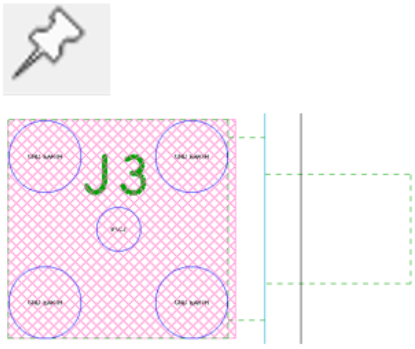
The ***Display - Highlight*** command assigns stipple patterns to elements without affecting the base color. This is handy for highlighting nets where changing color might confuse the user as to what layer the net is routed on. The type of database element highlighted is based upon the Find Filter. The Options form supports 15 patterns. Once highlighted, the elements remain highlighted until they are de-highlighted using the ***Display - Dehighlight*** command.

Highlighting Fixed Objects

Common sequence for highlighting fixed objects:

1. Set the stipple pattern in the *Color Dialog - Display* tab
2. Activate the *Fixed* command
3. Select object in the design to fix, stipple highlight appears





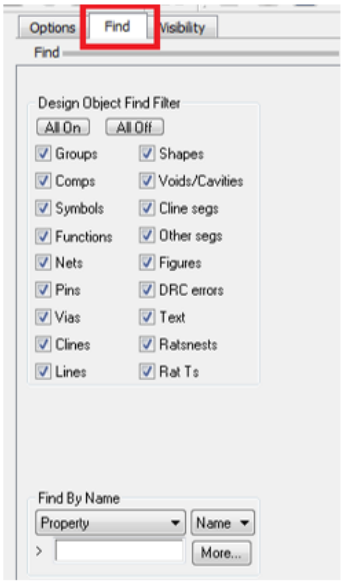
Spotting fixed objects in a database can often be a trial and error exercise for the designer. One might attempt to slide a cline only to find out that it has been fixed. The ability to overlay a stipple pattern on any fixed element helps to identify them. Assigning one of the available 15 stipple patterns to the ***Fixed Object*** entry located in the ***Display*** tab of the ***Color Dialog*** form allows the user to easily spot fixed objects.

Using the Show Element Command

Check – Elements …Or 

Common sequence for using *Show Element* with the mouse is:

1. Start the command
2. Activate the *Find* tab
3. Click the *All Off* button
4. Toggle on desired elements
5. Select the elements in the design window

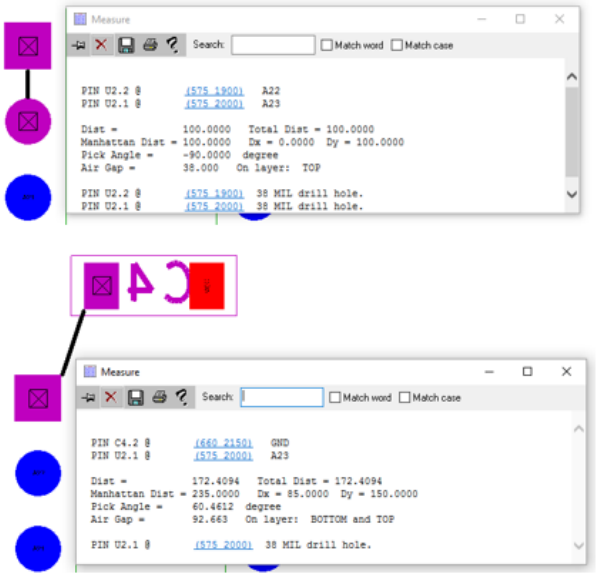


You can use the ***Show Element*** command to view information about any item in the design. The Find Filter is used to determine what type of element you will be quarrying. Based upon the Find Filter settings, you can determine a net name, a component's reference designator, which padstack a pin uses, etc.

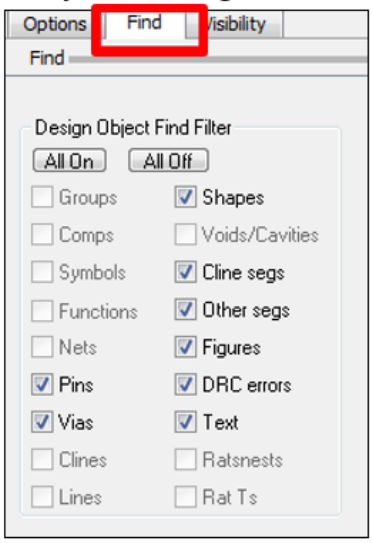
Remember that the Find Filter is hierarchical. If you set the Find Filter to Nets and click on a trace, you see the net name, pin and via counts, total etch length, pins on the net and any properties attached to the net. However, if you set the Find Filter to Clines and click on the same trace, you will see the layer the cline is on, the net the cline is part of, the length of that cline, the pins and/or vias it goes between and the width of that cline.

Using the Measure Command

Check - Measure …Or



Verify the settings in the *Find* tab



May display primary and alternate units by enabling the *showmeasure_altunits* variable in the *Display – Elements* folder of the User Preferences

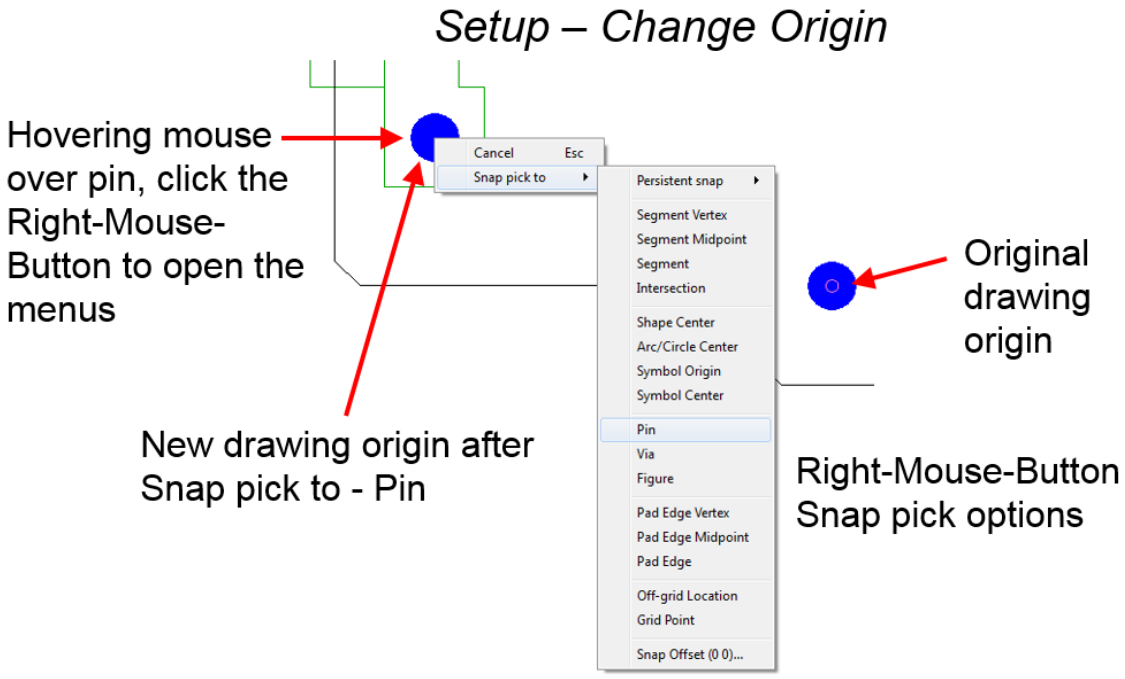
You may use the ***Check - Measure*** command to determine the distance between two points. After the two points have been selected, a window is displayed detailing information about the distance between the two elements. Information displayed includes total distance, Manhattan distance, pick angle, and the air gap.

The air gap is displayed even if the two selected elements do not reside on the same class and subclass. Again, it is important to remember that the Find Filter settings determine which database elements will be selected by this command. If the selection point contains no items that match the Find Filter settings, then the closest grid point will be used for determining the distance.

You can also use the ***Snap pick to*** option to make sure you are selecting the element (pin, via, segment vertex, etc.) you intended to.

The Measure command has the ability to display the measurement values in dual units (i.e. Mils and MM). You can do this by setting the ***showmeasure_altunits*** variable in the ***Display – Element*** category of the ***User Preferences***.

Change Origin Command

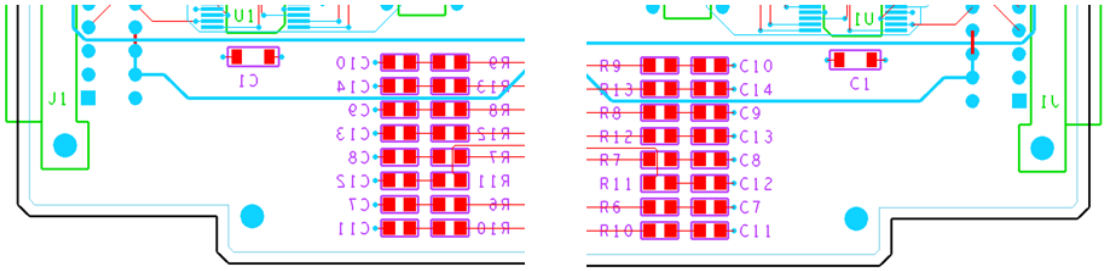


The ***Setup - Change Drawing Origin*** command allows you to change the design's origin based on selection options in the ***Right-Mouse-Button - Snap pick to*** menu. Example: activating the command and then selecting the ***Right-Mouse-Button - Snap Pick to - Pin*** option allows you to position the drawing origin on the center of the pin of your choice.

You can set the drawing origin to be visible or invisible and to a selected color in the ***Drawing Format*** category – ***Drawing_Origin*** subclass of the ***Color Dialog*** form.

Using the Flip Design Command

Display – Flip Design

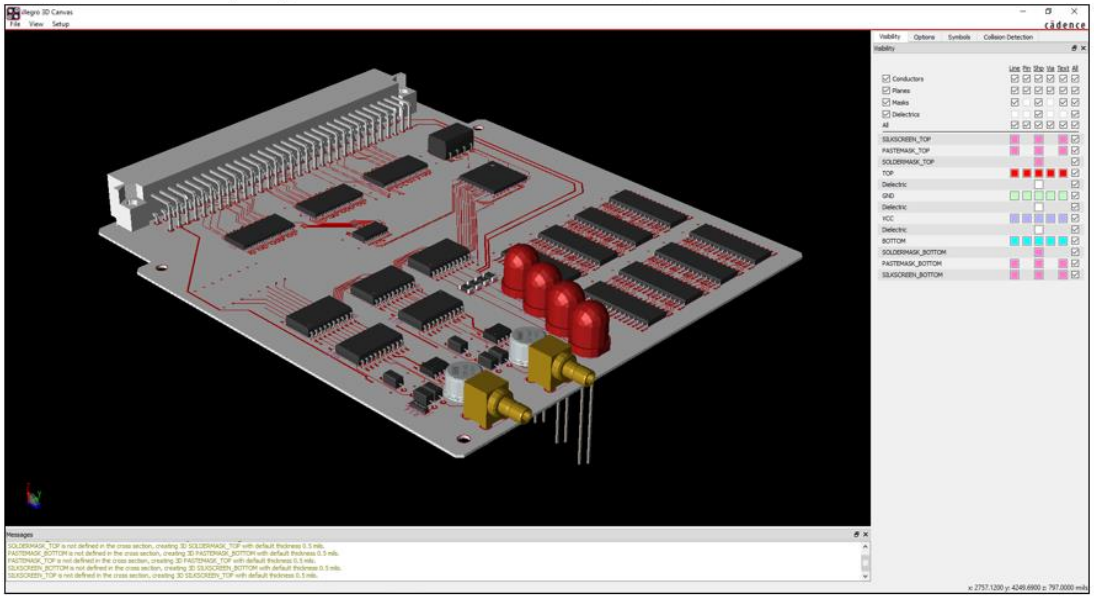


Top View Bottom View

The ***Display – Flip Design*** command allows you to flip the design and view it from the top or the bottom side. The benefit is that, when flipped, everything on the bottom is right-reading. Since all the editing capabilities are still intact, designers can continue to work on the board even in the flipped state.

Using the 3D View Command

Display – 3D View …Or 3D



Use the ***Display - 3D View*** command to display the design in a 3-dimensional view based on STEP models, or the Place_Bound_Top and Place_Bound_Bottom shapes. This view may be rotated to provide the 3-D view from various positions. Using the Control Panel to the right, you may control the visibility of different layers, control the visibility of various components and run collision detection information.

Labs

Lab 2-2: Using the Find Filter and Pre-Selection Mode

- Using the Find by Name selection
- Using Preselection Mode

Lab 2-3: Using the Find Filter with Show Element Command

- Using the Find Filter with the ***Check - Elements*** command
- Using the Find Filter with the ***Check - Measure*** command

Lab 2-4: Changing the Drawing Origin

- Change the position of the drawing origin

Lab 2-5: Using the Flip Design and 3-D View Command

- Using ***Display - Flip Design*** to flip between the top and bottom views
- Using ***Display - 3D View*** to display the design in a 3-Dimensional view

Lab 2-2: Using the Find Filter and Pre-Selection Mode

Objective: Use the Find Filter as a selection aid.

Locating a Component Using the Find by Name Section

In this lab you will learn how to use the Find Filter and its Find by Name data entry field and the two field description boxes.

1. Start PCB Editor and open the `cds_routed.brd` file in the *play* directory, if you do not already have it running.
2. Perform the ***Display - Zoom - Fit*** command to show the entire board.
3. Click with the ***Right-Mouse-Button*** and choose ***Selection set - Clear all selections***.
4. Choose ***Edit - Move*** from the top menu.
5. Click on the ***Find*** tab, if it is not already the active tab.
6. If needed, change the setting in the ***Find by Name*** field to ***Symbol (or Pin)*** as shown, and enter **`U3`** in the field.
7. Press the ***Tab*** key.
   Part U3 snaps to your cursor and the display is redrawn to be zoomed to this part. Whatever you enter in the Find by Name field is selected for manipulation by the active command - in this case, ***Move***.
8. Right-click and choose ***Cancel*** from the pop-up menu.
   Part U3 snaps back to its original location as you exit the active command.

Using the Pre-Selection Mode

Now, we will use pre-selection mode to ***Move*** U3.

1. Select the ***General Edit Application Mode***.
2. In the ***Find*** tab's ***Design Object Find Filter*** section, select the ***All Off*** button and then toggle on ***Symbols***.
3. Hover your mouse over a pin on ***U3***.
   A datatip window should appear identifying **U3** as an **SOIC48**.
4. Click the ***Right-Mouse-Button*** and select ***Move*** from the popup menu.
   Part U3 snaps to your cursor.
5. Right-click and choose ***Cancel*** from the pop-up menu.
   U3 snaps back to its original location.
6. Right-click and choose ***Selection Set - Clear all selections***.
   Even though you cancelled the Move command for U3, it is still selected. You should always make sure that you have nothing selected (unless wanted) in the pre-selection mode as certain commands will automatically act upon pre-selected items.

End of Lab

Lab 2-3: Using the Find Filter with the Show Element Command

Objective: Query information about objects in a design.

The ***Show Element*** command displays helpful information about selected objects. You can use this command to evaluate net names, reference designators and pin numbers, line widths, wire lengths, package types, padstack names, measured distances, assigned properties, DRC errors, and more.

Remember, the Find Filter controls what is selected, and therefore the data that is reported to you.

Using the Show Element Command

1. Zoom in to a view area around the ***U2*** component, which is a small SOIC24 footprint located just left of the board center, and to the right of the three SOIC48s at the left side of the design.
2. Click the ***Show Element*** icon.

Note The ***Show Element*** command can also be accessed from the ***Check – Element*** menu or by pressing the ***F4*** key.

3. In the ***Find*** tab, select ***All On***.
   This ensures that the check boxes for all objects are toggled ON. Select one of the pins on the ***U2*** component that has etch connected to it.
   The *Show Element* report appears.
4. If your ***Show Element*** report window is covering the *Find Filter*, move it so you can also see the *Find Filter* and the *U2 component*.
   At the top of the ***Show Element*** form is a description of the type of object that is selected, <COMPONENT INSTANCE>. The data in this report corresponds to a description of the component instance of the Comps items in the Find Filter because the Comps category is higher in the selection hierarchy than pins or etch.
5. In the ***Find Filter***, disable the check box next to ***Comps***.
6. Select the same pin on the same component again.
   This time the ***Show Element*** form refreshes to display ***SYMBOL*** information for this component package.
   This report focuses on the characteristics of the physical package symbol and corresponds to the Symbols entry in the Find Filter. Symbols is now the priority item in the Find Filter. If more than one item in the Find Filter is turned ON, then the priority goes to the highest active item in the list.

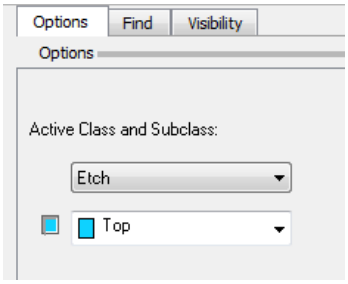
7. In the ***Find Filter***, disable ***Symbols*** and select the same pin again.
   The ***Show Element*** form refreshes to display ***FUNCTION*** information for this package. This information corresponds to the Functions entry in the Find Filter. (The pin you selected is seen as part of a function or gate within this package.)
8. In the ***Find Filter***, disable ***Functions*** and select the same pin again.
   The ***Show Element*** form refreshes to display ***NET*** information for this pin. This information corresponds to the Nets entry in the Find Filter. Notice the information about etch length and any attached properties.
9. In the ***Find Filter***, disable ***Nets*** and select the same pin again.
   The ***Show Element*** form refreshes to display ***PIN*** information. This information corresponds to the Pins entry in the Find Filter. Notice the padstack information.
10. In the ***Find Filter***, disable ***Pins*** and select the same pin again.
    The ***Show Element*** form refreshes to display ***CONNECT LINE*** information for the connection to the pin. This information corresponds to the Clines (etch) entry in the Find Filter.
11. In the ***Show Element*** form, click on an ***(X Y)*** coordinate (the blue numbers in parentheses) by clicking on the coordinates.
    The PCB Editor window will center the zoomed area on this coordinate. These forms are contact-sensitive. Try this a couple more times.
12. Right-click in the work area window and choose ***Cancel*** from the pop-up menu.

Selecting the same object generates different information, depending upon the settings in the Find Filter. It is not just which item you select, but also the selection priority in the Find Filter that matters.

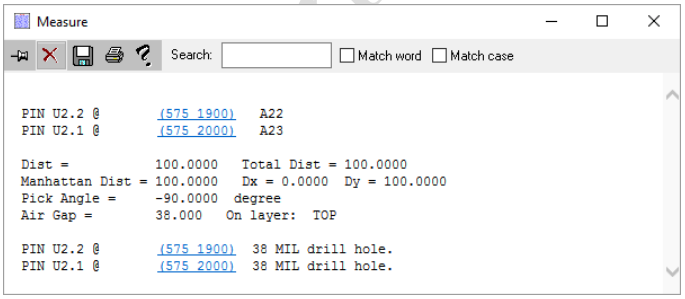
When choosing the ***Check - Element*** menu item, disable all the objects in the ***Find Filter***. Then enable only the object(s) that will generate the information you want to see.

Using the Check - Measure Command

1. In the ***Options*** tab, set the ***Active Class*** to ***ETCH*** and the ***Subclass*** to ***TOP***, as shown.



2. Choose ***Check*** - ***Measure*** from the top menu bar.
   The PCB Editor message area prompts you to:
   `Make two picks for the distance calculator.`
3. Select two objects that you wish to measure the distance between. Remember to check the settings in the Find Filter.
   The ***Measure*** report appears, showing information about the objects (if any) selected, the Manhattan Distance, and air gap information. An example of the measure output is shown below. Yours will probably not match this display exactly.



4. To exit from the ***Check- Measure*** command, right-click and choose "***Done***" from the pop-up menu or click the ***red X icon*** in the toolbar menu.
5. Practice some more with this command if you have the time.

End of Lab

Lab 2-4: Changing the Drawing Origin

Objective: Use the Change Origin command to experiment with relocating the position of the drawing origin.

In this lab, you will use the Change Origin command to reposition the location of the drawing origin.

Note  You will ***NOT*** save the changes made in this lab.

1. Zoom into the lower left corner of the board so that you can see both the mounting hole that is currently the drawing's origin and the lower mounting hole of the preplaced DIN64 connector.
2. Choose ***Setup - Change Origin*** from the top menu.
3. While hovering your mouse over the ***mounting hole*** for the ***DIN64*** connector, use the ***Right-Mouse-Button*** pop-up menu to select ***Snap pick to*** and then '***Pin***' from the selection list.
   This DIN64 mounting hole should now be the new drawing origin.

End of Lab

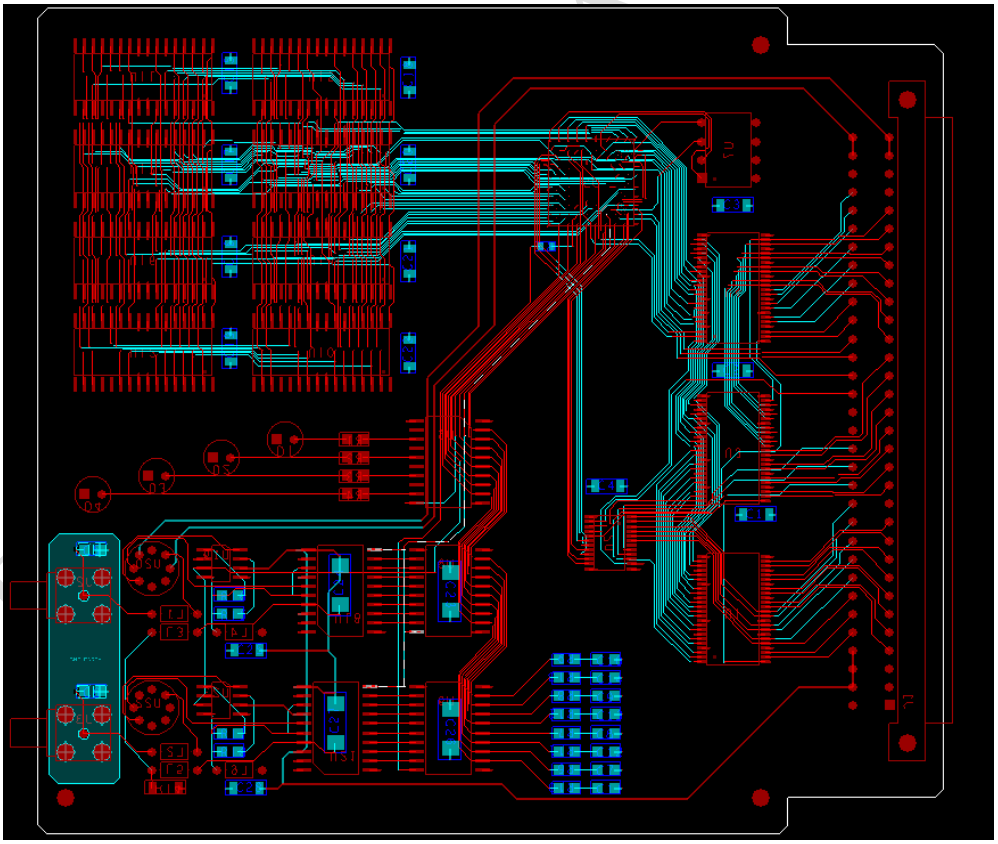
Lab 2-5: Using the Flip Design and 3D View Commands

Objective: Display your design in a flipped view and 3D view.

In this lab, you will use the Flip Design command to swap between the top and bottom views and look at the board 3 dimensionally to display the heights of the components.

Using the Display – Flip Design Command

1. On the command line type `reopen`.
   This will reopen the design at its last saved state.
2. Select ***Display - Zoom - Fit*** to display everything within the board outline.
3. Select the ***Display – Flip Design*** menu command or click on the ***Flipdesign*** icon.
4. Flip the design back to the top side view.

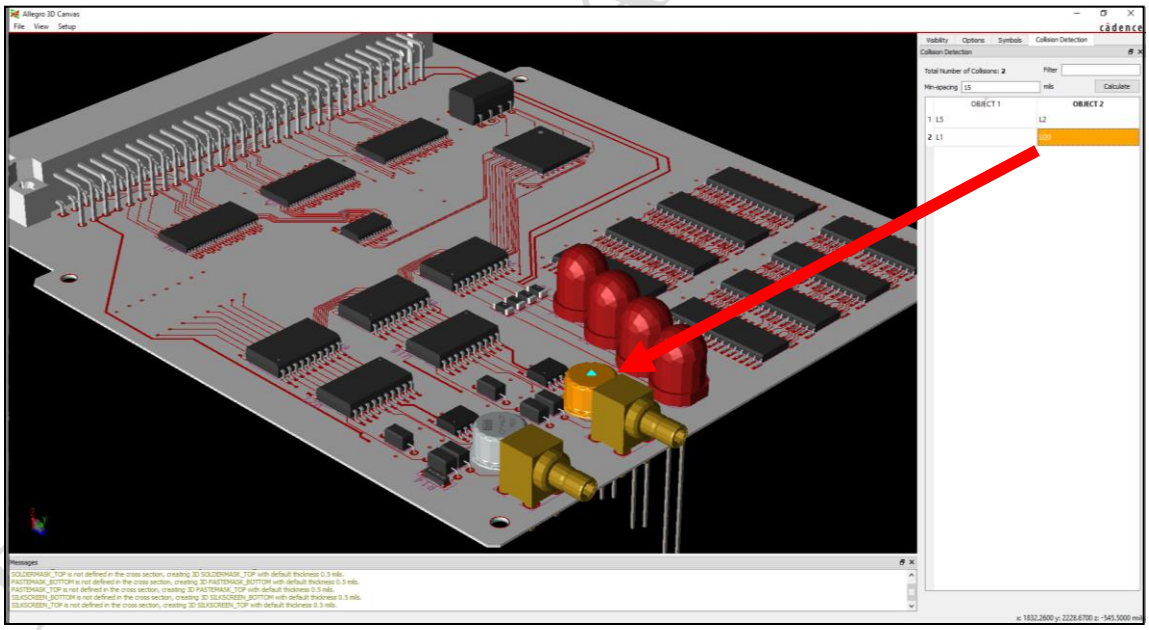


Using the Display - 3D View Command

1. Select ***Display - Zoom - Fit*** to display everything within the board outline.
2. Select the ***Display - 3D View*** menu command or click on the ***3D Viewer*** icon.

   The ***Allegro 3D Viewer*** window opens a 3-dimensional display of your design with STEP models. This view may be rotated to allow you to view your design in 3-D at multiple angles.

3. Hold down the ***SHIFT*** key and use the ***Middle Mouse Key*** to rotate the view.
4. Select the **Visibility** tab in the **Control Panel** to the right and try turning off and on the various layers.
5. Now, select the ***Collision Detection*** tab
6. Type ***15*** into the ***Min-spacing*** field
7. Click ***Calculate***
   You should see two collisions. The first one between L3 and L1 and the second one between L2 and L5.
8. Click on one of the components showing a collision in the Control Panel.
   You will see it is now highlighted (see figure below).



9. Select ***File - Exit*** from the top menu.
10. When prompted to save the board, click ***NO***.

End of Lab

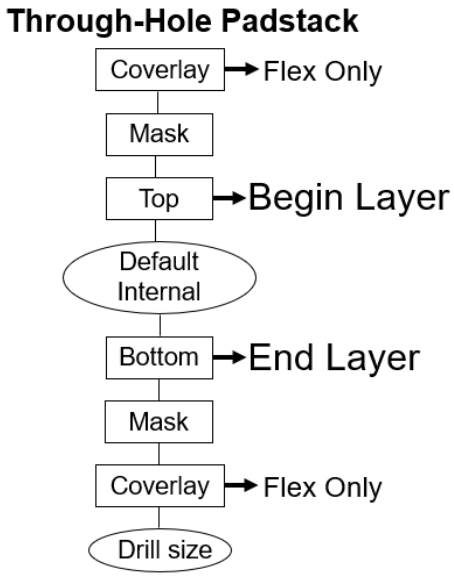
Lesson 3: Padstacks

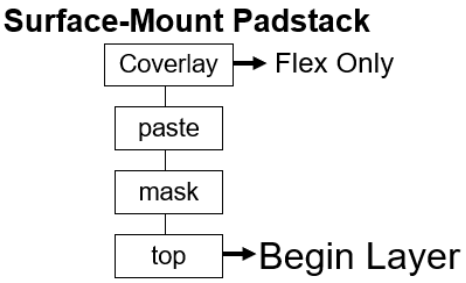
Learning Objectives

In this lesson, you will:

- Use the Pad Editor to create padstacks for typical pins, such as through-hole and surface-mount pads.
- The Pad Editor's user interface is based on the padstack's usage.
- In this section, you will create padstacks that will be used to model pins in the PCB Editor 'footprint' symbols and vias on the printed circuit board.

Anatomy of a Padstack





You define the pad size and shape for all etch and non-etch layers in the Padstack Editor. Default routing layers are BEGIN layer, DEFAULT INTERNAL, and END layer. The DEFAULT INTERNAL padstack definition is used on all internal layers in your design. When the padstack is placed in the footprint, the BEGIN layer is mapped to the TOP layer, and the END layer is mapped to the BOTTOM layer.

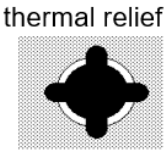
Non-etch layers include SOLDERMASK_TOP, SOLDERMASK_BOTTOM, PASTEMASK_TOP and PASTEMASK_BOTTOM.

Note If you require sub-mil values to describe padstacks, set the accuracy of your package symbol drawings to a minimum of the same sub-mil value as the padstack, to avoid rounding of padstack features.

Padstack Geometry Details

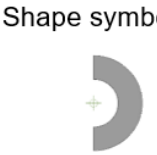
Regular Pad: A pad with a regular shape (circle, square, rectangle, rounded rectangle, chamfered rectangle, oblong, octagon, donut).

Thermal Relief, Positive: *Optional;* used to connect pins to a copper area. Is a combination of the regular pad, thermal relief geometry, and tie bars. Size is specified as the opening size in the copper shape. May be defined based solely on constraint values.



Anti-Pad: *Optional;* used to disconnect pins from a surrounding copper area. Size is specified as the opening size in the copper shape. May be defined based solely on constraint values.

Shape: Irregularly shaped (custom) pad created manually with the Symbol Editor and referenced in the padstack.



When you are defining the regular pad, you must remember that you are defining a "generic" pad. I may be used on a routing layer, or it may be used on a plane layer.

Therefore, it is usually best to define all of the regular, Begin Layer, Default Internal and End Layer definitions when creating the initial padstack. For each of these definitions, you must define the shape of the pad as a circle, a square, an oblong, a rectangle, a rounded rectangle, a chamfered rectangle, an octagon, a donut, or a shape.

Shape is used for any definition that is not a circle, a square, an oblong, a rectangle, a rounded rectangle, a chamfered rectangle, an octagon, or a donut. A Shape symbol must be created manually using the PCB Editor's Symbol Editor. It is then browsed to and referenced in the padstack.

What Does the Padstack Editor Do?

The Padstack Editor gives you the ability to create or edit library padstacks:

- Select the type/usage of padstack
- Define the padstack parameters
- Define the padstack layer geometry
- Copy padstack layer geometry

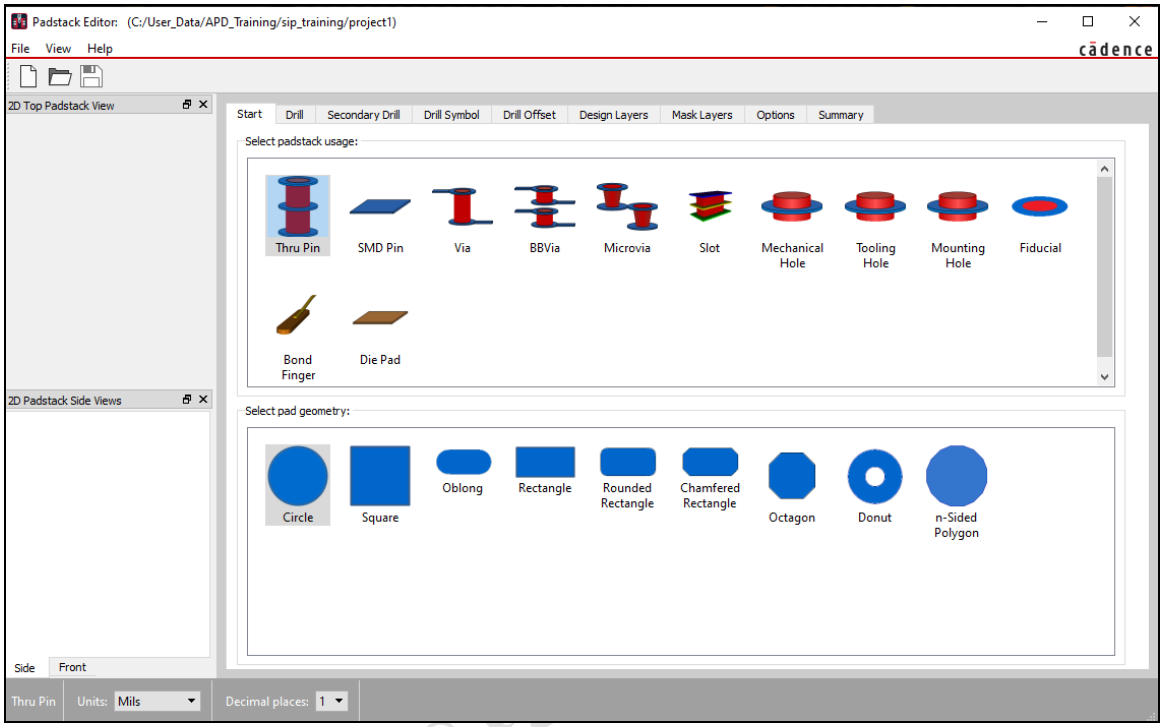
You MUST create padstacks before they can be used. Therefore, you need to proceed with this step before you can create your package symbols, which are the physical footprints.

You define the pad size and shape for all etch and non-etch layers in the Pad editor. As previously discussed, you define the default routing layers (BEGIN LAYER, DEFAULT INTERNAL, and END LAYER). When a padstack is added to the board it expands to match the number of electrical layers defined for the board.

A "via" must also be defined as a padstack before it is added to a board design. We will cover how to add a "via" to a board design later in the course.

Padstack Editor

The Padstack Editor is accessible from ***Windows Start – Cadence PCB Utilities 17.4-2019 – Padstack Editor 17.4***.



The Padstack Editor is a tabular formatted tool based on the selected padstack usage. The usages are: Thru Pin, SMD Pin, Via, BBVia, Microvia, Slot, Mechanical Hole, Tooling Hole, Mounting Hole, Fiducial, Bond finger, and Die Pin. As this tool is used to create padstacks for multiple design tools some of the usage types will not apply to board/symbols associated with the PCB Editor.

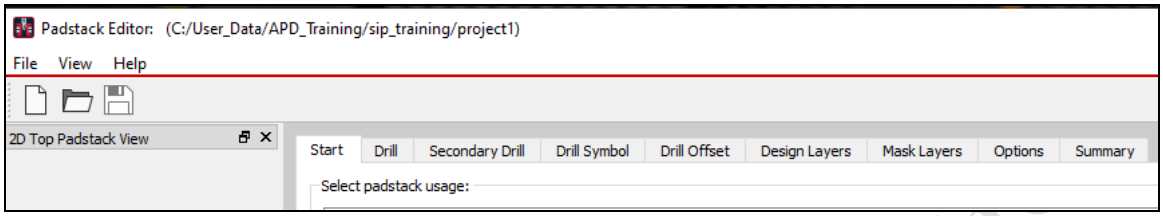
The default pad geometry styles are Circle, Square, Oblong, Rectangle, Octagon, Rounded Rectangle, Chamfered Rectangle, Donut, and N-Sided Polygon.

On the left side of the Pad Editor you will find two view windows; 2D Top padstack View and 2D Padstack Side Views. As you build your padstack walking through the various tabs, the images of the padstack will appear in these windows.

Selecting ***File – New*** from the Pad Editor menu will open a New Padstack window that allows you to browse to the appropriate directory you wish to save it in and assign a

name to it. You will then select the Padstack usage type in the new padstack window. This will set the tabs appropriately.

Pad Editor - Title Bar and Tabs



When you first open the Pad Editor the Title bar will display the name of the tool and the directory that it opened to. However, once you start a new padstack or open an existing padstack the title bar will include the padstack name and the directory it is either create or opened in.

The tabs are Start, Drill, Secondary Drill, Drill Symbol, Drill Offset, Design Layers, Mask Layers, Options, and Summary.

Padstack Editor – Start Tab

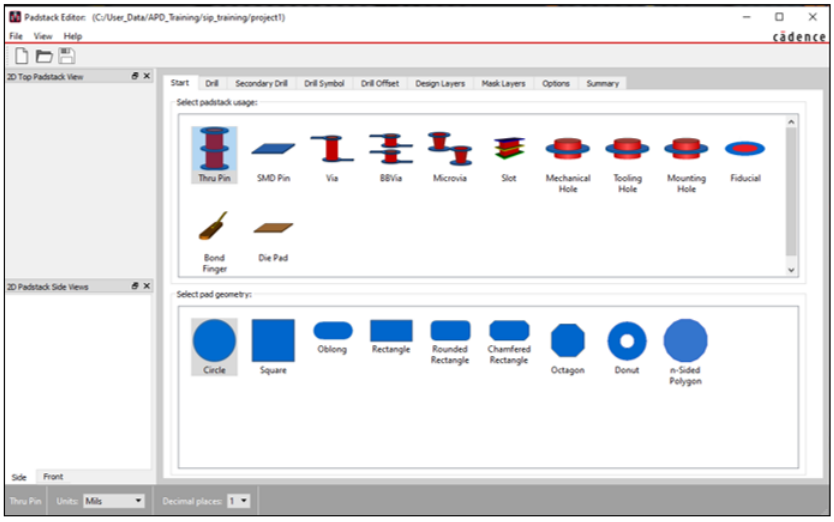
Start tab displays the various padstack usage types and geometries.

Padstack Usages: (Aligned with IPC-2581)

- Thru Pin
- SMD Pin
- Via
- BBVia
- Microvia
- Slot
- Tooling Hole *
- Mounting Hole *
- Fiducial *
- Bond Finger
- Die Pad

Padstack Geometries:

- Circle
- Square
- Oblong
- Rectangle
- Rounded Rectangle
- Chamfered Rectangle
- Octagon
- Donut Pad
- Multisided Polygon
  (8 to 64 sides - even numbers only)



The Start tab displays the various padstack usage types and default pad geometries.

Padstack usages that align with the IPC2581 schema:

- Tooling Hole
- Mounting Hole
- Fiducial

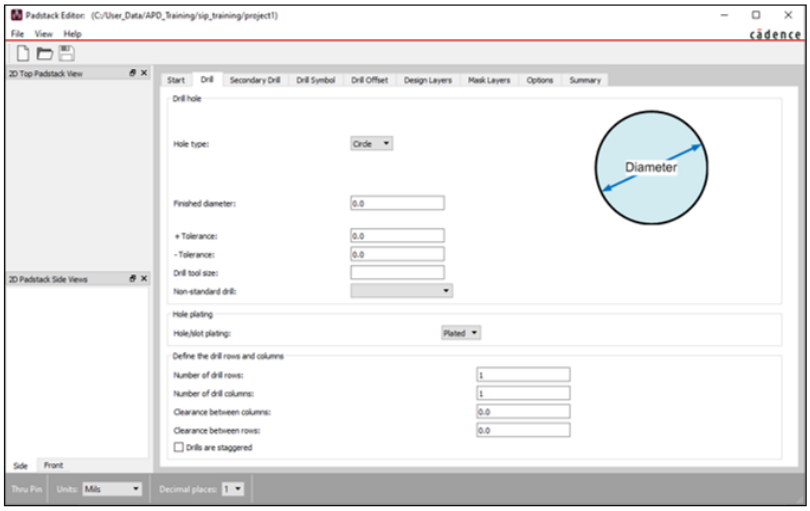
Specialized padstack geometries:

- Rounded Rectangle (all corners or specific corners)
- Chamfered Rectangle (all corners or specific corners)
- Multisided Polygon (8 to 64 sides but limited to even count only)
- Donut pad

Pad Editor – Drill Tab

Drill tab controls the parameters for the drilled hole type

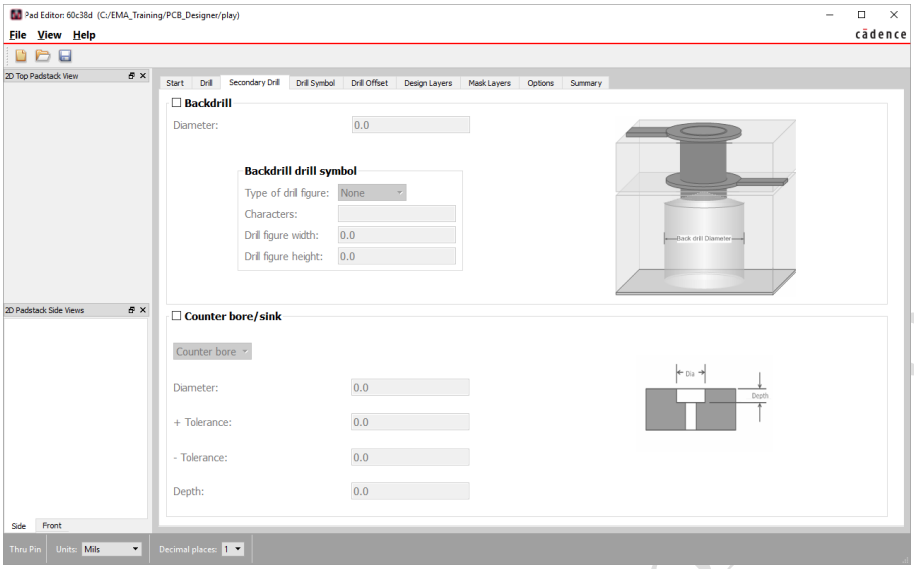
- Finished drill hole - diameter after plating
- Hole Type
  - Circle
  - Square
- Drill tool size - drill size before plating (Output to NC Legend and exports to IPC-2581)
- Non-standard drills:
  - Laser
  - Plasma
  - Punch
  - Wet/Dry Etching
  - Photo Imaging
  - Conductive Ink Formation
  - Dual
  - Other



The Drill tab controls the parameters for the ‘Hole type’, finished diameter, tolerance, drill tool size, non-standard drilling operation, plating, and number of drills based on rows and columns.

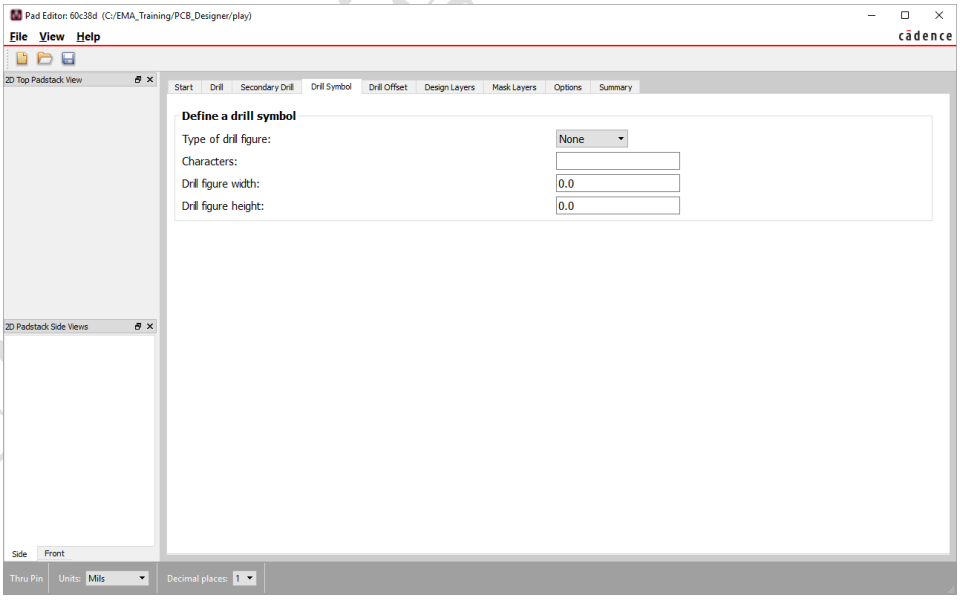
The ‘Hole type’ options are Circle and Square, Square is a new hole type option. Use this tab to set the finished drill size, the tolerance, and whether you want to have multiple holes inside the padstack. The ‘Hole plating’ is determined automatically based on the padstack usage you selected. You can also specify the plating thickness by defining both the Dill tool size and the Finished diameter.

Pad Editor – Secondary Drill Tab



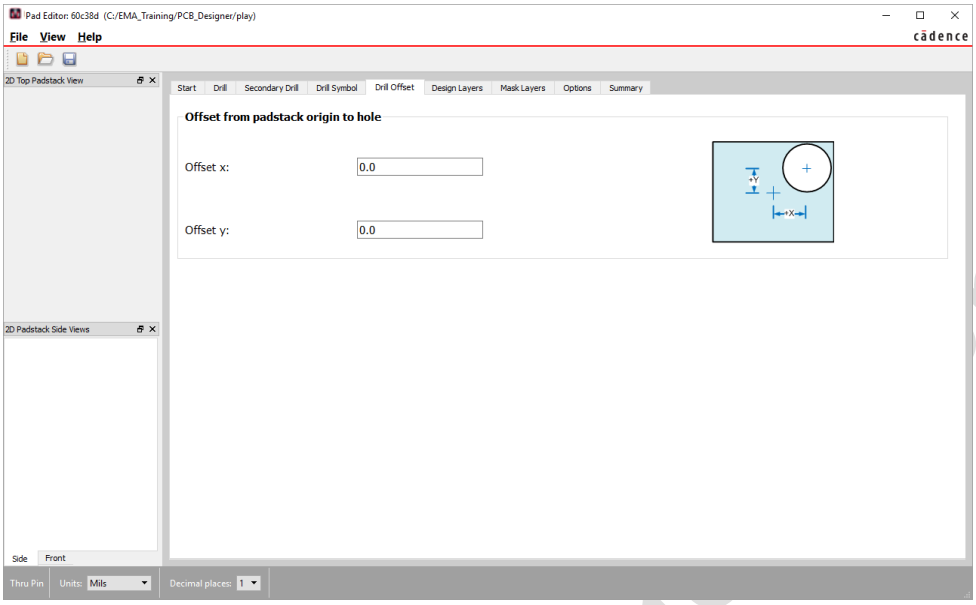
The Secondary Drill tab controls the parameters for operations such as Backdrilling (supported in the higher tier tools) and Counter Bore/Sink. If the counterbore or countersink operation is required, the creation of the NC legend will generate a separate legend specific with this information based on the layer the operation is performed on.

Pad Editor – Drill Symbol Tab



The Drill Symbol tab defines the drill or slot figure representation for the purpose of the NC Drill Legend. If you want the padstack to control the drill figure representation used by the NC Drill Legend you would define the shape and size of the figure here. You can also add a character to the representation here.

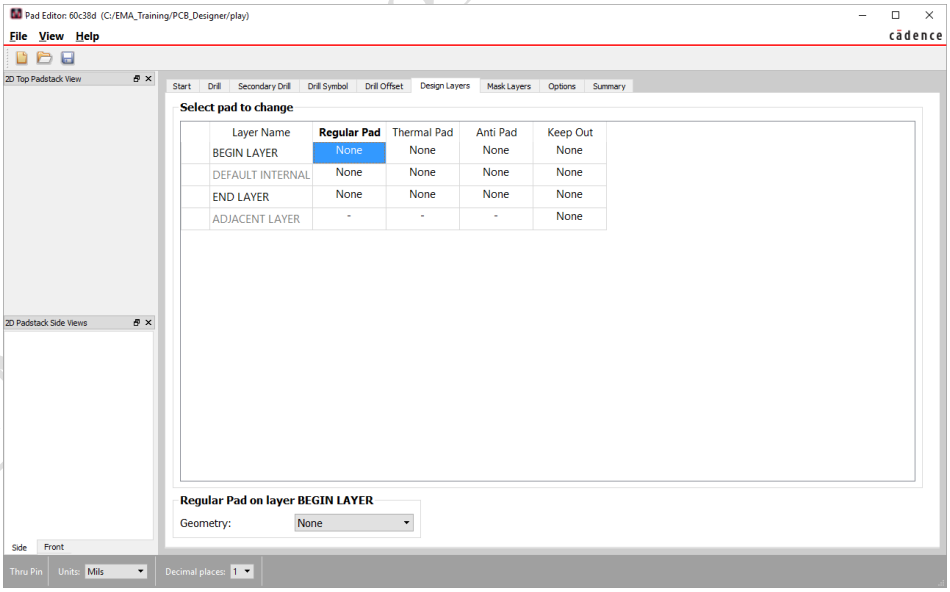
Pad – Drill Offset Tab



The Drill Offset tab defines the offset of the padstack origin to the hole.

You only need to use this tab if you intend to offset the drilled hole in the X or Y direction or both directions in relation to the origin of the padstack.

Pad Editor – Design Layers Tab

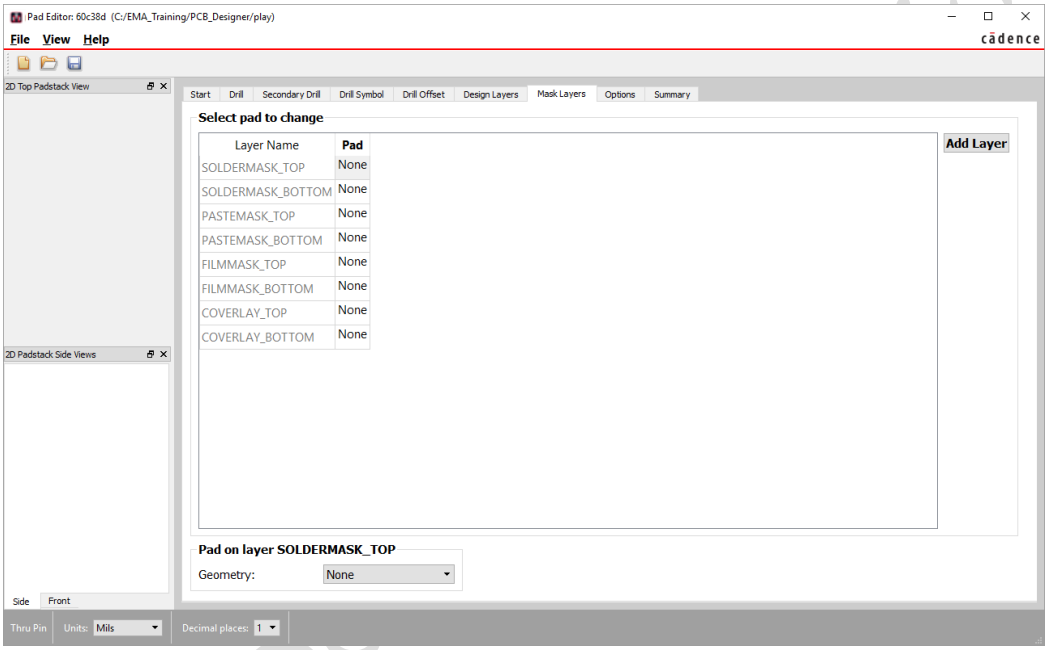


The Design Layers tab defines the geometry size for the Regular pad, Thermal Pad opening, Anti Pad opening and Keepout for the BEGIN LAYER, DEFAULT INTERNAL and END LAYER pads.

When you click on a cell, such as Regular for the BEGIN LAYER, you then select the Geometry option at the bottom of the form. This will open the window where you define the geometry and size for the padstack cell.

If you want to copy the same geometry and size to another cell, simply click the populated cell, Right-Mouse-Button and select **Copy**. Now select the cell to copy to Right-Mouse-Button and select **Paste**.

Pad Editor – Mask Layers Tab

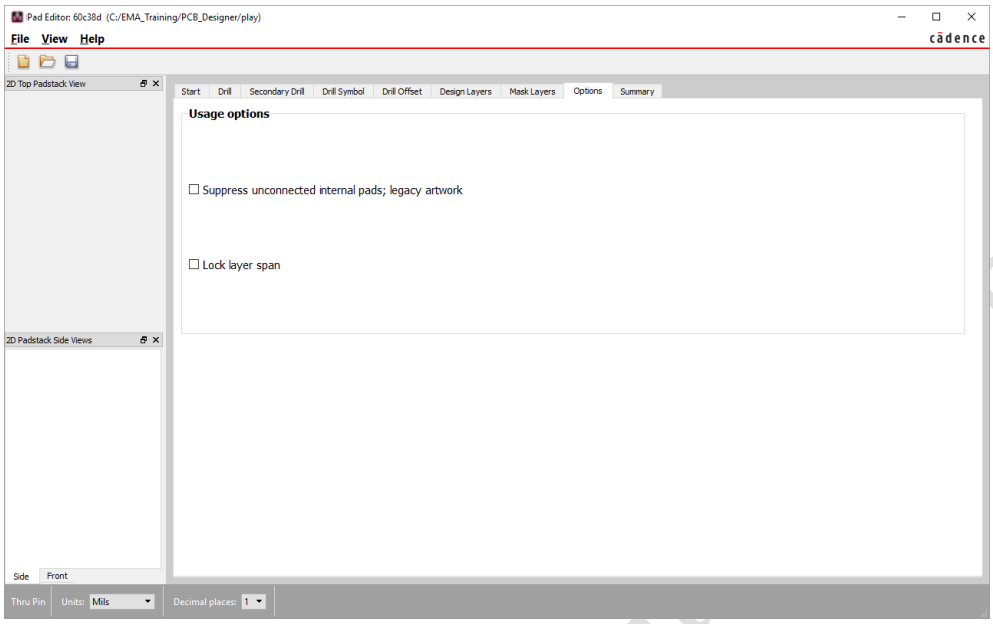


The Mask Layers tab defines the geometry size for the Soldermask opening, Pastemask, Filmmask and Coverlay layers.

When you click on a cell, such as SOLDERMASK_TOP, you then select the Geometry option at the bottom of the form. This will open a window where you define the geometry and size for the padstack cell.

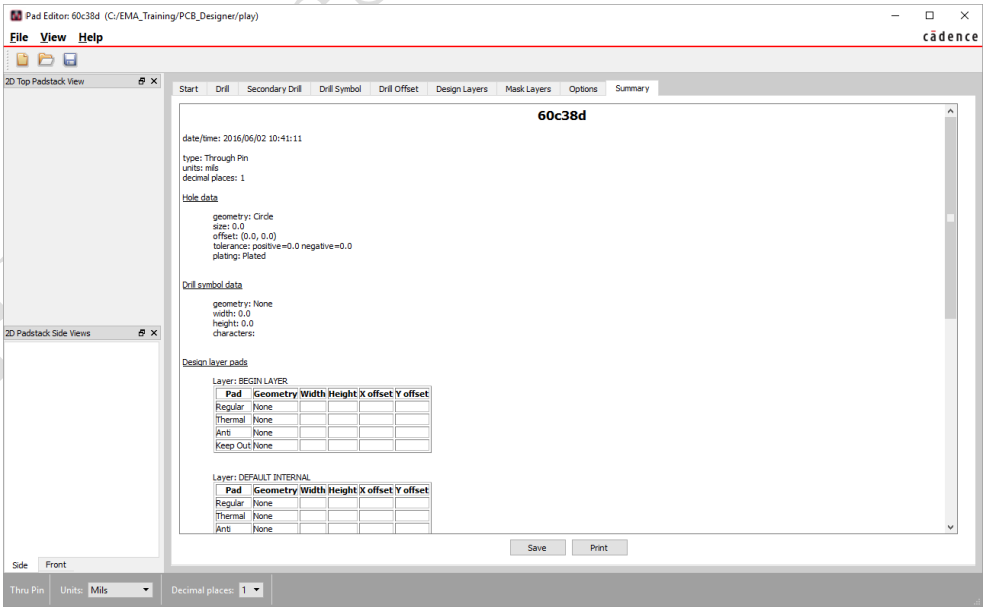
If you want to copy the same geometry and size to another cell, just click the populated cell, Right-Mouse-Button and select **Copy**. Now, select the cell to copy to, Right-Mouse-Button select and **Paste**.

Pad Editor – Options Tab



The Options tab controls the suppress unconnected internal pads option. The PCB Editor has a utility that gives you the ability to suppress unconnected pads on internal layers. This utility will not work if the "Suppress unconnected internal pads; legacy artwork" option is not enabled here in the padstack.

Pad Editor – Summary Tab



The Summary tab provides a detailed summary of all of the tab settings for the padstack.

Labs

Lab 3-1: Creating Padstack for a Through-Hole Device

- Create a round padstack for a through-hole pin

Lab 3-2: Creating a Padstack for a Surface-Mount Device

- Create surface-mount padstack

Lab 3-1: Creating a Padstack for a Through-Hole Pin

Objective: Use the Pad Designer to create a padstack for a through-hole pin.

You will continue working in the *play* directory during this lab to create a round padstack named 60c38d. This is a 60-mil-diameter circular pad with a 38-mil plated hole.

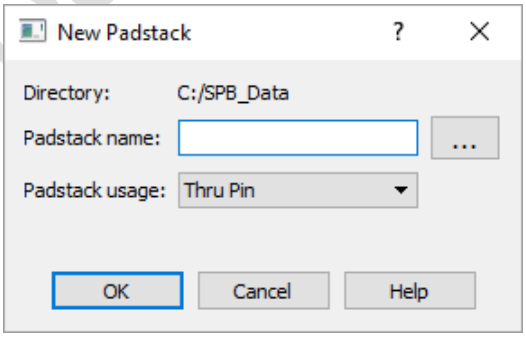
Starting the Padstack Editor

1. Select ***Start - Cadence PCB Utilities 17.4-2019 - Padstack Editor 17.4***.
The Pad Editor form is displayed.

Creating the Circular Padstack in the Correct Directory

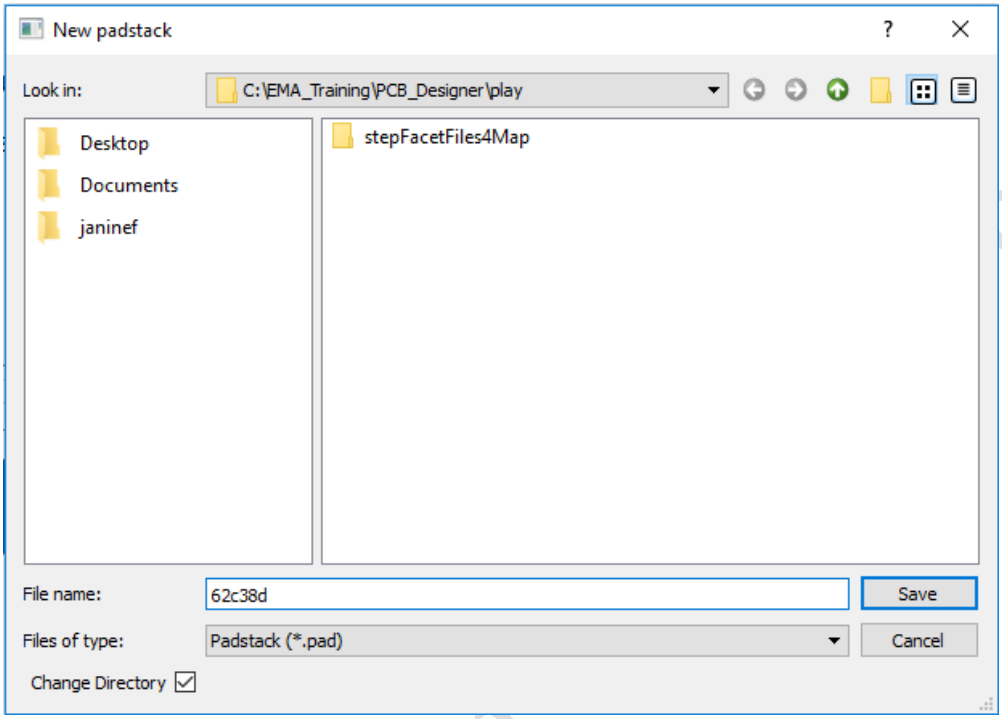
The **first** time Pad Designer is run by a user, the current working directory will be set to a location defined by the software installation. The following steps will be used to create the padstacks in the correct working directory.

1. Click ***Thru Pin*** in the ***select padstack usage*** section of **Pad Editor**.
2. Select ***File - New*** from the Pad Editor main menu.
   A *New Padstack* form opens.



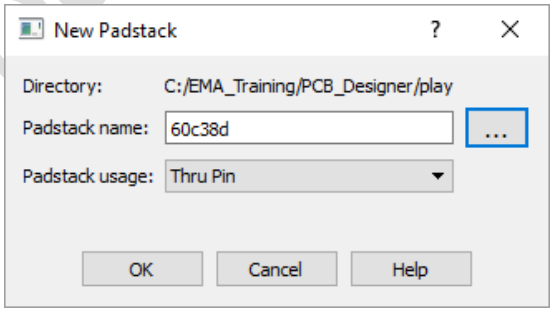
3. Browse to the ***<course inst dir> - PCB_Designer - play*** directory.

4. In the ***File Name*** field of the *New padstack* form, type the name for this padstack: **`60c38d`** and then click the ***Save*** button.



The ***New Padstack*** form will display with the directory you browsed to and the name of the padstack you assigned.

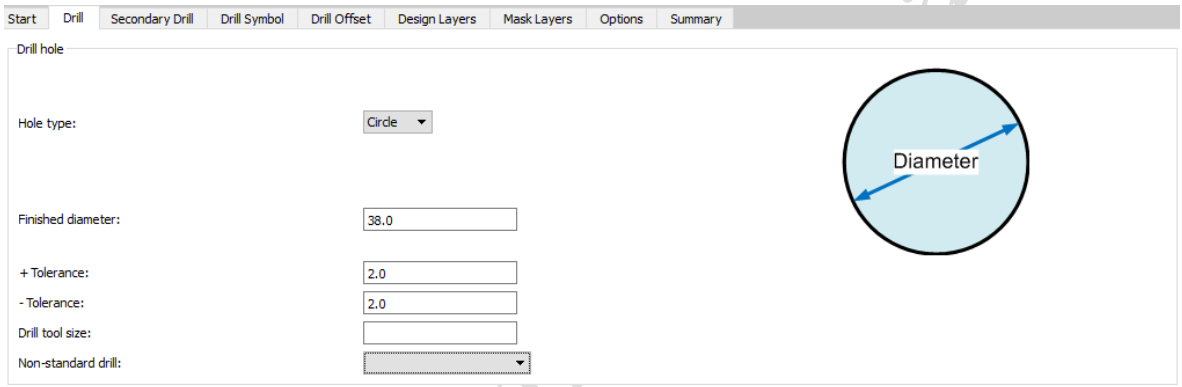
5. Click ***OK*** in the ***New Padstack*** form.



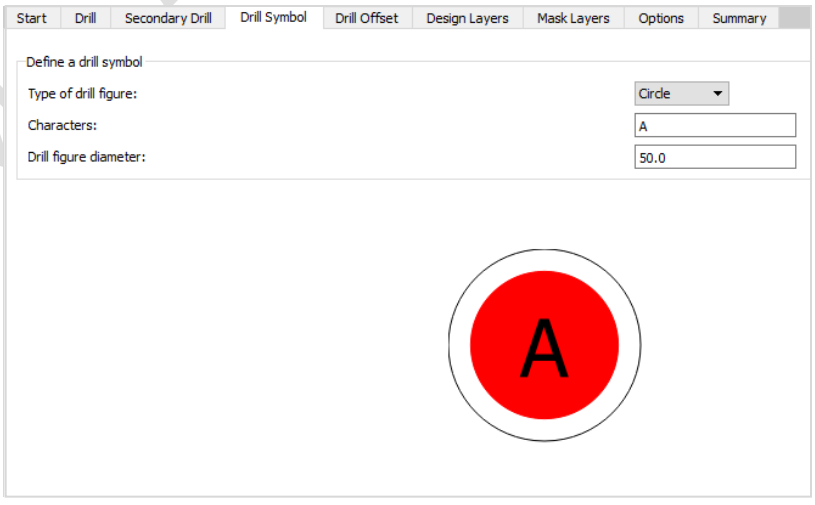
Describing the NCDRILL Requirements

We will use the ***Drill*** tab of the Pad Editor to define the "Hole Type", "Finished diameter", "Tolerance" and "Plating" for this padstack. We will also use the ***Drill Symbol*** tab to define the symbol representation for the NC Drill Legend.

1. Fill out the ***Drill*** tab of the form as follows:
    - Hole type: Circle
    - Finished Diameter: 38
    - Tolerance: +2, -2
    - Hole Plating: Plated

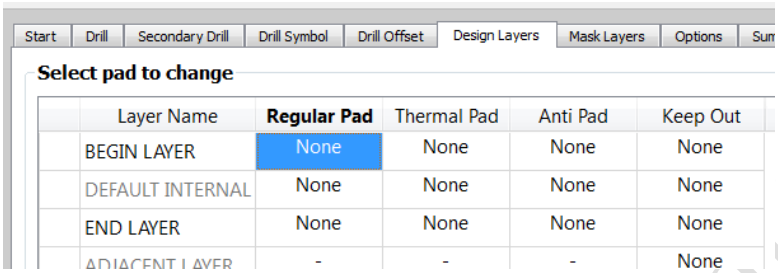


2. Fill out the ***Drill Symbol*** tab of the form as follows:
    - Type of drill figure: Circle
    - Characters: A
    - Drill figure diameter: 50

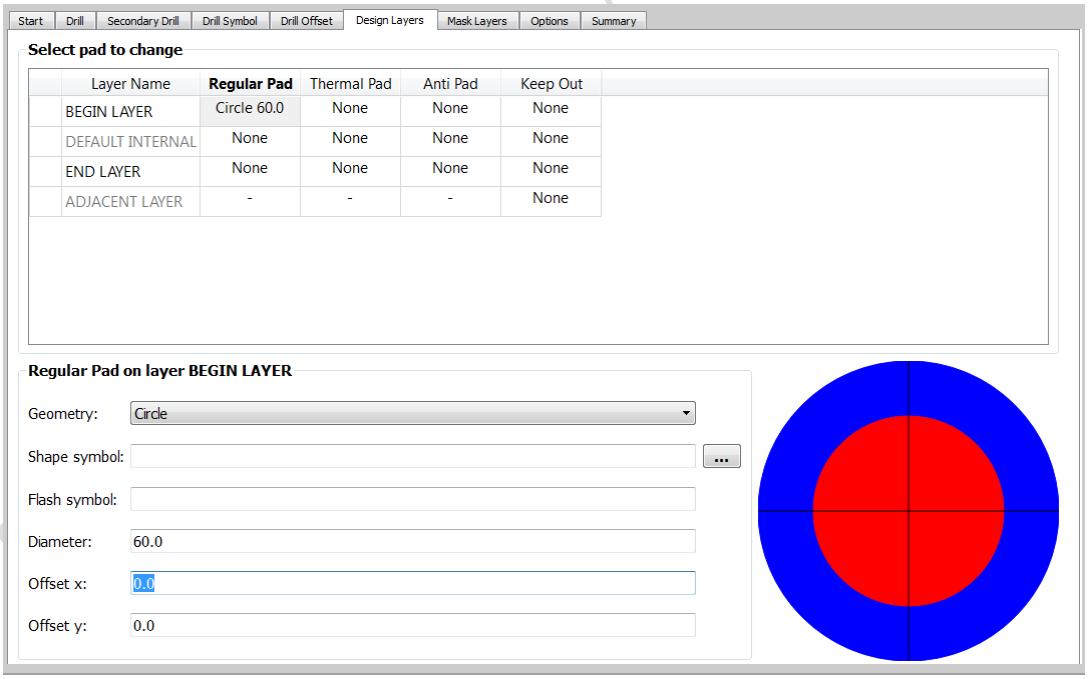


Describing the BEGIN LAYER Pad

1. Select the ***Design Layers*** tab
2. Click in the ***BEGIN LAYER*** cell under ***Regular Pad***



3. At the bottom of the form click on the ***Geometry*** option to define the "***Regular Pad on layer BEGIN LAYER***" and select ***Circle***.
   This will expand the "***Regular Pad on layer BEGIN LAYER***" window.
4. Set the ***Diameter*** to ***60***.
   It will populate the Regular Pad cell setting for the BEGIN LAYER.

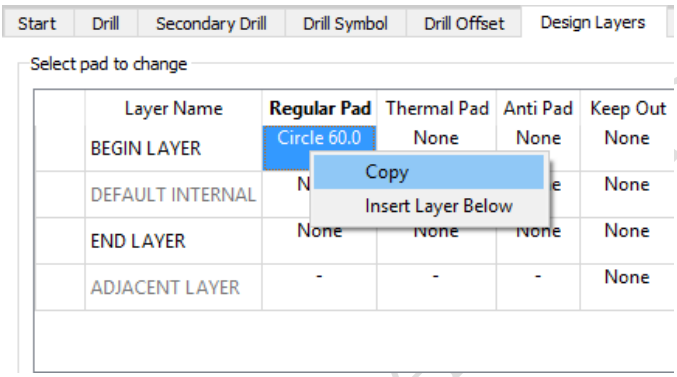


Note Thermal and anti pad definitions are only truly required when generating negative planes. Since we will only be dealing with positive planes, we will not be filling in the ***Thermal Pad*** and ***Anti Pad*** fields.

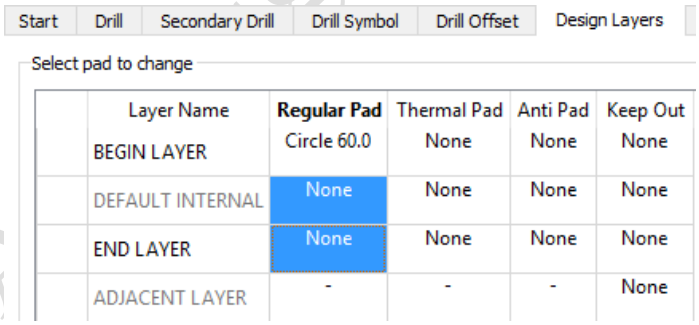
Describing the DEFAULT INTERNAL and END LAYER Pads

Because the DEFAULT INTERNAL and END LAYER pads are generally the same size and shape as the BEGIN LAYER, you will use the **Copy** command to save time.

1. To copy the ***BEGIN LAYER*** pad definition, click on the ***Regular*** cell of the ***BEGIN LAYER***
2. While selected, select ***Copy*** from the ***Right-Mouse-Button*** pop-up menu as you see in the figure below.



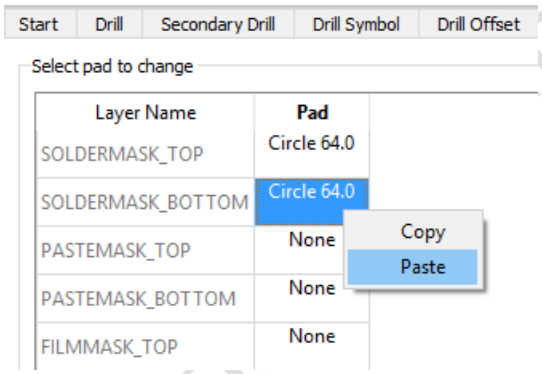
3. Now, click in the ***Regular Pad*** cell for ***DEFAULT INTERNAL*** and scroll to ***END LAYER*** to select both fields as shown below.



4. While selected, select ***Paste*** from the ***Right-Mouse-Button*** pop-up menu.
   The DEFAULT INTERNAL and END LAYER will now have the same settings as those for the BEGIN LAYER.

Describing the SOLDERMASK Pads

1. Select the ***Mask Layers*** tab
2. Click in the ***SOLDERMASK_TOP*** cell under ***Pad.***
3. At the bottom of the form click on the ***Geometry*** option to define the "***Pad on layer SOLDERMASK_TOP***" and select ***Circle***.
   This will expand the "***Pad on layer SOLDERMASK_TOP***" window.
4. Set the ***Diameter*** to ***64***.
   It will populate the Pad cell setting for the SOLDERMASK_TOP.
5. You may copy and paste from the ***SOLDERMASK_TOP*** to the ***SOLDERMASK_BOTTOM*** as we did earlier.



Saving the 60C38D Circular Padstack

1. Select ***File – Save*** from the top menu of the Pad Editor.
   The padstack, `60c38d`, is saved to disk.

Note It is important that you save ALL padstacks you create in this module in the play directory.

There is no need to close the Padstack Editor until you have completed all your pad editing work.

End of Lab

Lab 3-2: Creating a Padstack for a Surface Mounted Device

***Objective:* Define a padstack for a surface-mounted device.**

In this lab, you will create a padstack named 76x24smd. This is a 76-mil by 24-mil rectangular pad with no drilled hole (for surface-mount devices). It is assumed that the Padstack Editor menu is still open. To reopen it, use the steps you learned in Lab 3-1.

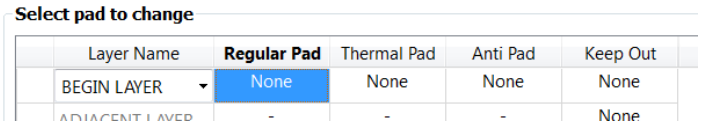
Naming the Padstack

Since the padstack you are now about to create has no similar features to the previous padstack, use the following technique to remove all the information currently in the Padstack Designer form, and create a new padstack.

1. Set the ***Package usage*** field to ***SMD Pin***.
2. Select ***File - New*** from the top menu of the Pad Editor to open the *New Padstack* form. If you are asked if you would like to save the current padstack, click **No**.
3. Using the browse button, browse to the ***<course inst dir>/PCB_Designer/play*** directory if you are not still there.
4. In the ***File Name*** field of the *New padstack* form, type the name for this padstack: **`76x24smd`** and then click the ***Save*** button.
   The ***New Padstack*** form will display the directory you browsed to and the name of the padstack you assigned.
5. Click ***OK*** in the ***New Padstack*** form.
6. Make sure the padstack usage is still set to ***SMD Pin***.

Describing the BEGIN LAYER Pad

1. Select the ***Design Layers*** tab.
2. Click in the ***BEGIN LAYER*** cell under ***Regular Pad***



3. At the bottom of the form click on the ***Geometry*** option to define the "***Regular Pad on layer BEGIN LAYER***" and select ***Rectangle.***
   This will expand the "***Regular Pad on Layer BEGIN LAYER***" window.
4. Set the ***Width*** to ***76*** and the ***Height*** to ***24***.
   It will populate the Regular Pad cell setting for the BEGIN LAYER.

Describing the SOLDERMASK Pad

1. Select the ***Mask Layers*** tab.
2. Click in the ***SOLDERMASK_TOP*** cell under ***Pad***
3. At the bottom of the form click on the ***Geometry*** option to define the "***Pad on layer SOLDERMASK_TOP***" and select ***Rectangle.***
   This will expand the "***Pad on layer SOLDERMASK_TOP***" window.
4. Set the ***Width*** to ***80*** and the ***Height*** to ***28***.
   It will populate the Pad cell setting for the SOLDERMASK_TOP.

Describing the PASTEMASK Pad

We will make the PASTEMASK_TOP the same size as the Regular Pad of the BEGIN LAYER

1. While still in the ***Mask Layers*** tab, click in the ***PASTEMASK_TOP*** cell under ***Pad***
2. At the bottom of the form click on the ***Geometry*** option to define the "***Pad on layer PASTEMASK_TOP***" and select ***Rectangle.***
   This will expand the "***Pad on layer PASTEMASK_TOP***" window.
3. Set the ***Width*** to ***76*** and the ***Height*** to ***24***.
   It will populate the Pad cell setting for the PASTEMASK_TOP.

Note No SOLDERMASK_BOTTOM or PASTEMASK_BOTTOM pad definitions are required. If a part is placed on the bottom side of the board, the system automatically "moves" all TOP definitions to the BOTTOM.

For surface-mount padstacks, you only require the ***BEGIN LAYER***, ***SOLDERMASK_TOP*** and ***PASTEMASK_TOP*** pad layers. All others should read "None" or "-".

Saving the Padstack to Disk

1. Select ***File - Save*** from the top menu
   The padstack file (`76x24smd.pad`) is saved to disk.
2. Select ***File - Exit*** from the top menu of the Pad Designer form. The Padstack Designer closes.

End of Lab

Lesson 4: Component Symbols

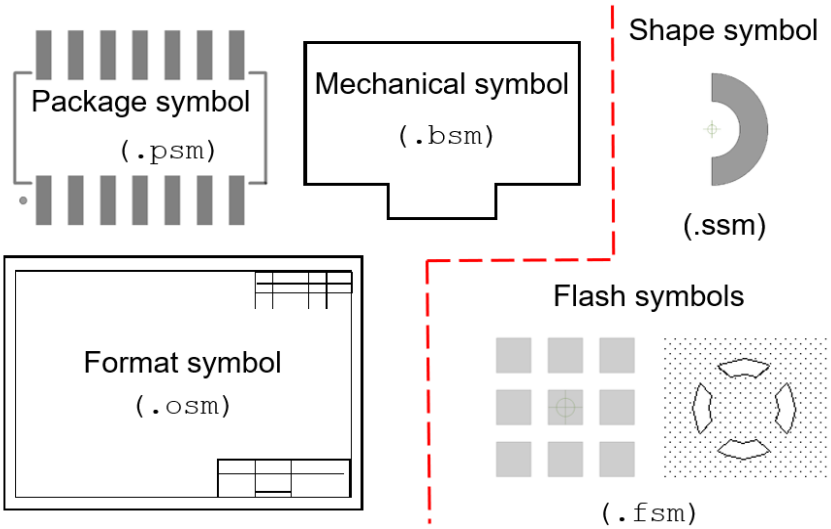
Learning Objectives

In this lesson, you will:

- Use the *Package Symbol Wizard* to create a package symbol
- Use the *Package* Symbol Editor to create a package symbol

In this section, you will create PCB Editor symbols that model the components that are placed on the printed circuit board. You will learn how to use the Package Symbol Wizard to create footprints and, how to manually create footprints.

PCB Editor Symbol Types



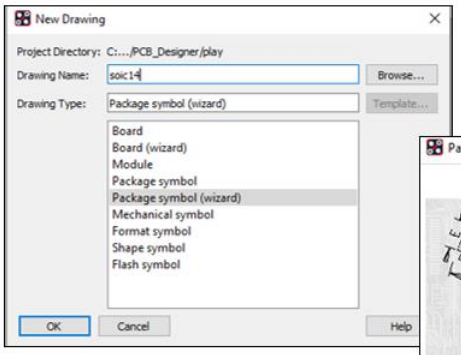
Each symbol type has its own unique .dra file

The PCB Symbol Edit mode lets you create the following symbols:

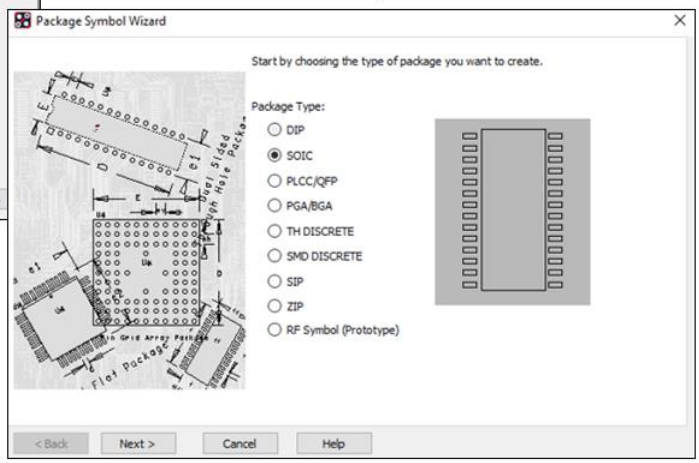
- **Package Symbol** (`.psm`) - Used for footprints such as SOIC, BGA, QFP, etc. Minimum requirements; reference designator and at least one pin with pin number.
- **Mechanical Symbol** (`.bsm`) – Used for mechanical symbols, such as card outline, mounting hole, tooling hole, board stiffener, etc. Minimum requirement; at least one mechanical pad.
- **Format Symbol** (`.osm`) – Used for A through D size page format symbols, title block symbols, company logos, assembly/fab notes, etc.
- **Shape Symbol** (`.ssm`) - Creates a filled polygon (*shape*) used for custom pads.
- **Flash Symbol** (`.fsm`) – Contains filled polygons that represent a thermal relief connection on a negative plane layer, or windowpane paste mask.

Package Symbol Wizard

File – New



Note: If you add the symbol name and then browse to a directory the Drawing Name field may have a `.dra` extension after the symbol name



Use the package Symbol Wizard to create a package symbol footprint:

- Select the type of footprint to be created
- Select and load a template to be used
- Define units and reference designator prefix
- Define the number of pins, pin spacing, and package size
- Select the padstacks to be used
- Define origin of footprint

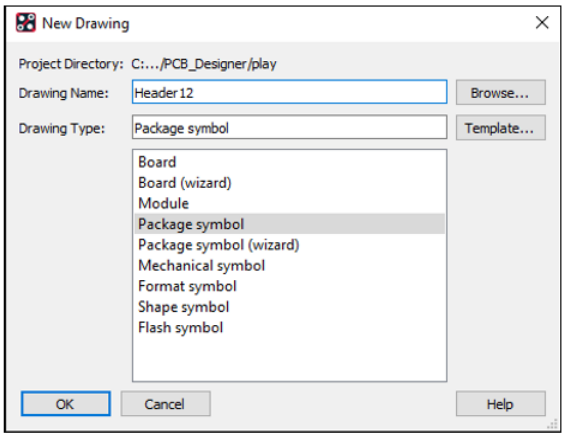
The Package Symbol Wizard can create many different styles of footprints, including DIPs, SOICs, PLCCs, BGAs, and QFPs. You can define information such as design units, number of pins, pin spacing, padstacks to use.

A template is a `.dra` file that contains basic information for the package symbol. Cadence supplies a default template, or you can create your own template that contains basic information on colors, text sizes, or documentation for your symbol.

After running the Package Symbol Wizard, you can edit and modify any of the items created by using the standard Package Symbol Editor User Interface.

Package Symbol - Manual Creation

File – New

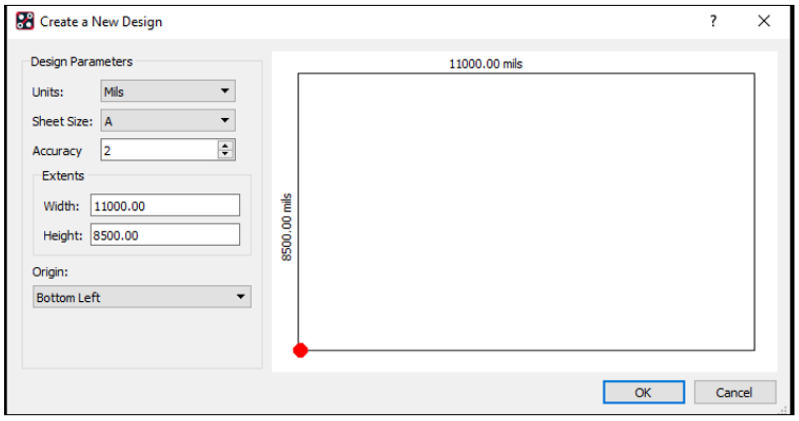


Note: If you add the symbol name and then browse to a directory the Drawing Name field may have a `.dra` extension after the symbol name

Using the drawing type of ***Package symbol*** opens the PCB Editor in Package Symbol editor mode. In this mode you manually set the various selections to be used to build your package symbol.

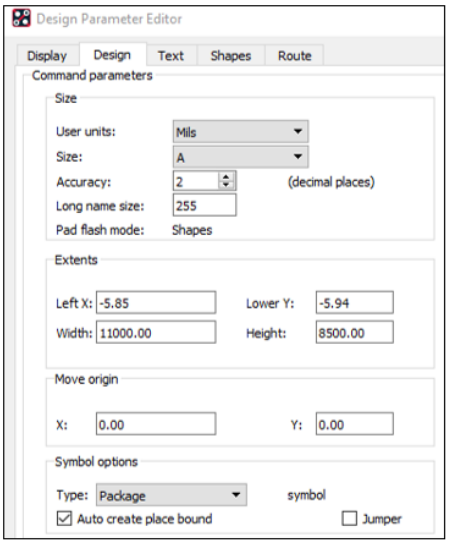
Create a New Design Window

Contains some parameters found in ***Design*** tab of ***Design Parameters*** dialog



The ***Create a New Design*** windows comes up automatically and allows you to set several of the parameters found in the **Design** tab of the ***Design Parameters*** dialog. Parameters set here may be modified in the Design tab of the Design Parameters editor window.

Design Parameters



User Units: Specifies the unit of measure used during the design process

Size: Specifies the size of the drawing area required

Accuracy: Sets the decimal place accuracy of the drawing database

Drawing Extents: Shows the height and width of the drawing, and the location of the lower left corner with respect to the drawing origin (located in the lower left corner by default)

Move Origin: Relocates the drawing origin (datum 0,0). The X, Y coordinates for the new origin are entered into this section (Replaced with the Change Drawing Origin command)

You use the **Setup > Design Parameters** command to open the Design Parameter Editor window. Select the Design tab to modify the parameters for the footprint to be created. Pay close attention to the following fields in the window.

User Units: This field is used to specify the units to be used to create the footprint. The available units are mils, inches, microns, millimeters, or centimeters.

Size: This field is used to specify the overall size of the drawing area. For English units, the options are **A, B, C,** and **D.** For metric units, the options are **A1, A2, A3,** and **A4.** You may also set a custom size; in which case the size field will show **Other**.

Accuracy: This field specifies the number of decimal places to be carried with each database unit. For example, if the units were set to mils, and the accuracy was set to 2, you would be able to specify a number with a resolution of one one-hundredth of a mil.

Extents: These fields are used to specify the overall drawing size and their relationship to the 0,0 origin. When one of the pre-defined sizes is specified, these fields will be filled in automatically. When a size of "Other" is specified, you must enter the values you wish in these fields. The **Width** and **Height** fields show the size of the overall drawing area. The **Left X:** and **Lower Y:** fields display the location of the 0,0-origin relative to the lower left-hand corner of the drawing area.

Move origin: These fields relocate the 0,0-origin to a new position. The value you enter in one of the fields is subtracted from the current origin to determine the new location. In this example, if the value 1000 was entered in the X field, when the tab key was pressed, the Left X Extents field would be changed to -3200. While this is still used it has primarily been replaced by using the ***Setup – Change Drawing Origin*** command.

Drawing Origin

When you start a new symbol drawing, the origin (0/0) is located in the lower left corner by default. This origin must be relocated to a point somewhere on the symbol (for example, pin 1 or the body center), and will be used as the package symbol origin during placement on the board.

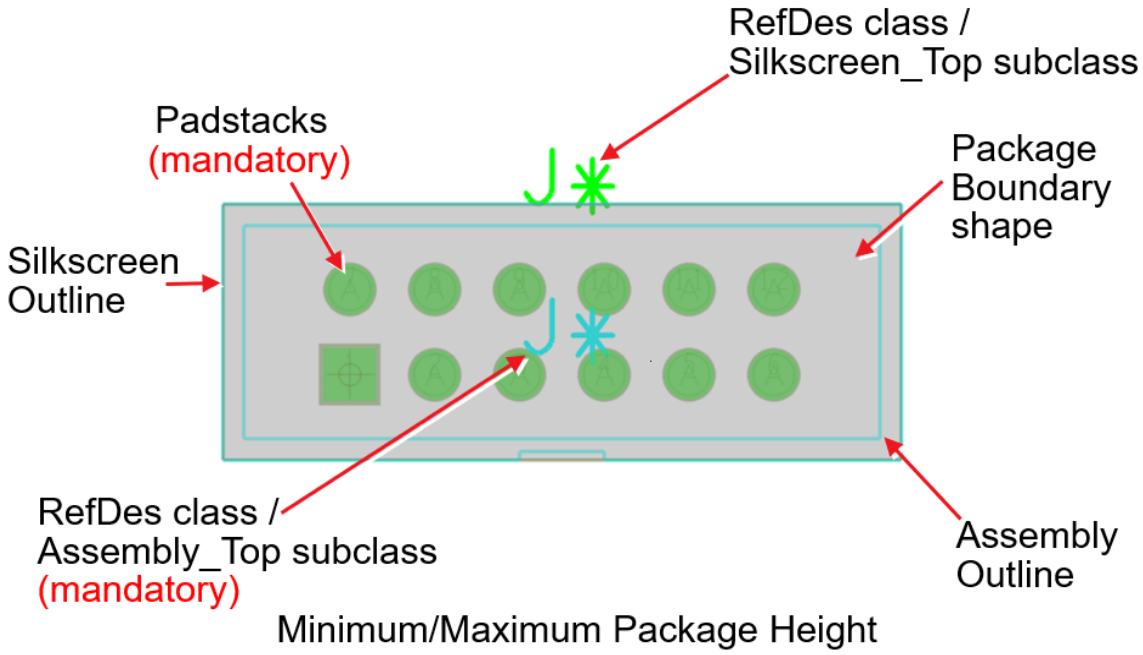
You may find it convenient to move the drawing origin before placing the pins of the device. If not, you can move the origin any time during the creation process by selecting ***Setup - Change Drawing Origin*** from the main menu. You can also move the origin by selecting ***Setup - Design Parameters*** and then using the Design tab.

There are two methods within the ***Design Parameters – Design tab*** that you can use to move the origin of the footprint.

- Using the ***Move origin*** section, you enter the amount you want to move the origin based upon its current location, entering positive X and positive Y values.
- You can also use the Drawing Extents section to move the origin of the footprint. When using this section, you enter in the new negative value for the Left X and Lower Y fields. Use the **Tab** key to proceed to the next field.

Note When you enter a value in the Move Origin section, use the **Tab** key to have the value take effect. When you press the **Tab** key, the Move Origin field will reset to 0 and the Left X or Lower Y field of the Drawing Extents section will be updated.

Example: 12-pin Header Package



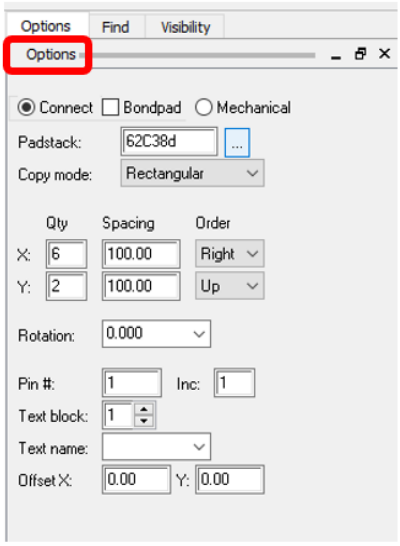
A typical package symbol contains pins (padstacks), assembly and silkscreen outlines, assembly and silkscreen reference designator placeholders and a package boundary with package height information attached.

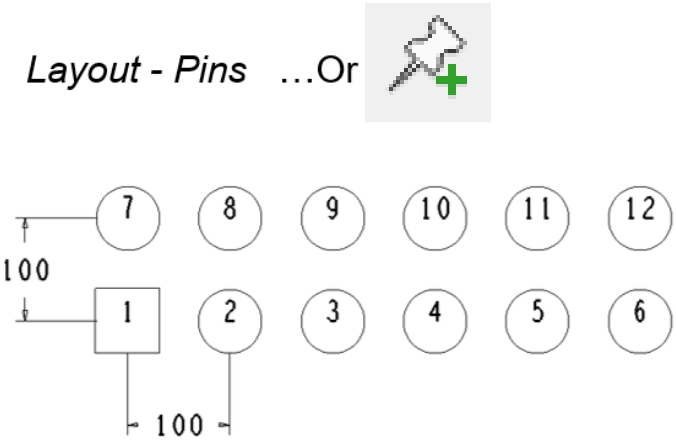
To create an PCB Editor package symbol:

- Add pin(s) (padstacks) – Must have at least 1 pin with a pin number
- Draw component outlines for assembly and silkscreen layers
- Add the placeholders for assembly and silkscreen reference designators (Assembly_Top is default mandatory)
- Define package boundary
- Assign Minimum Package Height and/or Maximum Package Height, using the ***Setup - Areas - Package Height*** command
- Save the drawing file (`.dra`). This is a drawing graphics file; it can be used for editing purposes only. Use ***File - Save*** to save this file
- Create a symbol file (`.psm`). This is a compiled binary file, used during placement only. It cannot be read by the Package Symbol Editor. It is by default created automatically when you save the drawing (`.dra`) file. If you do not have your preferences set to create this automatically on the save command, you can use ***File - Create Symbol*** command to generate this file.

Note It is important to keep the symbol (`.psm`) and drawing (`.dra`) files synchronized by saving the drawing file each time you create the symbol file.

Adding Pins

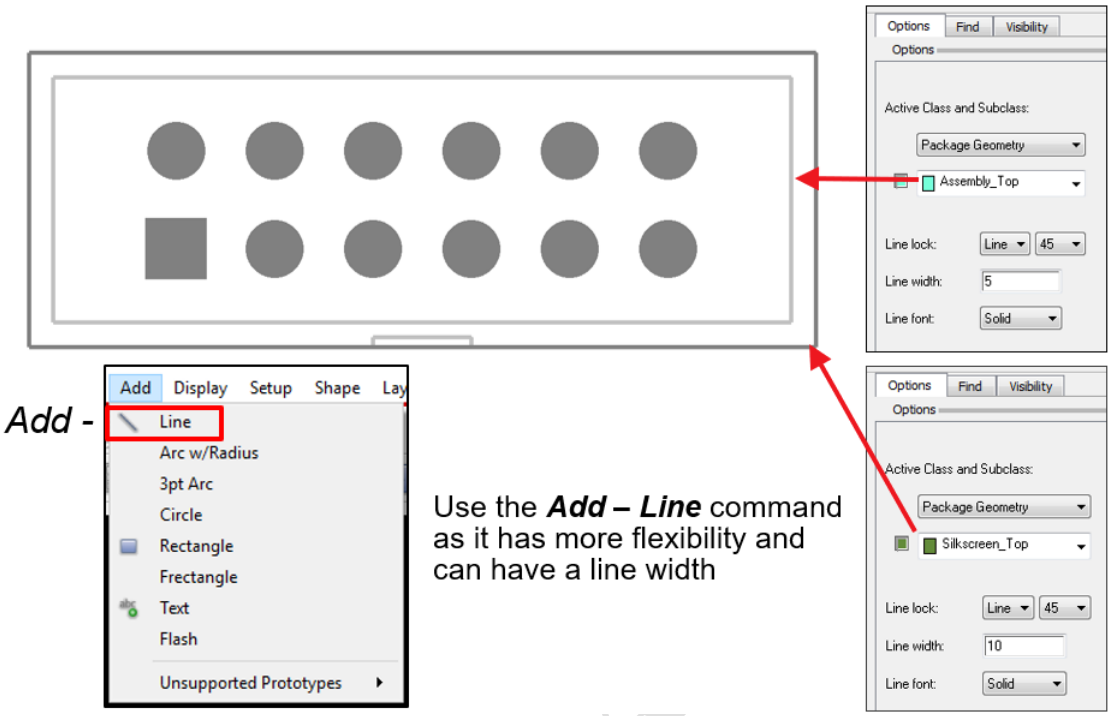




The PCB Editor will search the padstack directories defined by your PADPATH variable for the padstack you specify. This variable is defined in the *env* file.

- **Padstack** - Enter the padstack name (not case sensitive, looks for lowercase file on disk) or use the browse button
- **Copy Mode** - Can be either Rectangular (default) or Polar. Polar is used for creating a set of pins in a circular pattern.
- **X (Qty)** - The number of pins to be added in the X direction (columns)
- **Y (Qty)** - The number of pins to be added in the Y direction (rows)
- **Spacing** - Used to specify pin-to-pin spacing within the column(s) and row(s).
- **Order - Left/Right** - A toggle field used to specify direction of column expansion
- **Order - Up/Down** - A toggle field used to specify direction of row expansion
- **Rotation** - Can be 0, 45, 90, 135, 180, 225, 270, 315, or user-defined angle. The default is 0.
- **Pin #** - Shows the next pin to be added. Alphanumeric pin names are okay. Last character of pin number is incremented first (A1->A2, 1A->1B, 1AZ- >1BA).
- **Inc:** - Specifies pin numbering increment. The default is 1.
- **Text Block** - Each pin you add includes a visible pin number. This parameter determines the size of the pin number. Enter text block number 1-16.
- **Offset X/Y** - Offsets the pin number text with respect to the pin center. The default is - 50, 0 (left of pin center).

Drawing Component Outlines



You will create the Assembly Outline of your symbol using the ***Add - Line*** command. Set the class and subclass in the Options form to PACKAGE_GEOMETRY and ASSEMBLY_TOP and define the outline of the component using lines. You should also be defining a line width at which to draw the line.

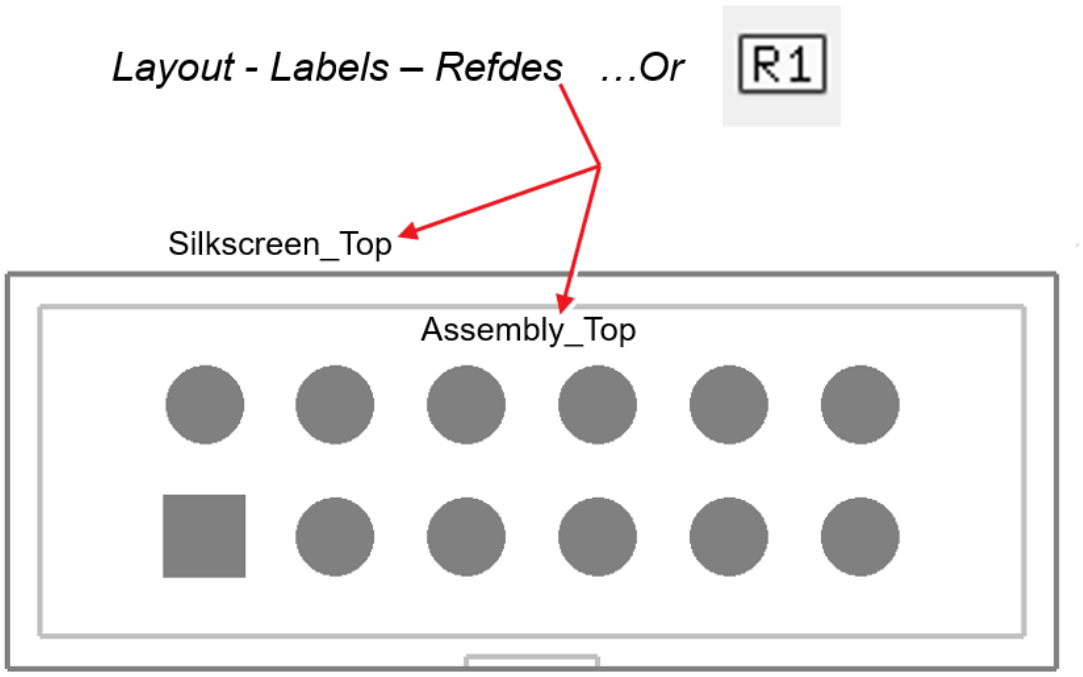
You will create the silkscreen for the component in the same fashion. By adding lines, the silkscreen outlines will be added on the SILKSCREEN_TOP subclass. Be sure to set the ***Line Width*** field to an appropriate value when adding lines on the silkscreen. The line width will define the line width of the silkscreen line on the actual printed circuit board.

You do not need to create the Assembly and Silkscreen on both the Top and Bottom subclasses. When placing parts, if you move the part to the bottom side of the design, the outlines will be moved automatically to the appropriate Bottom subclass. In other words, all graphics on the Assembly_Top will be moved to the Assembly_Bottom subclass, and all graphics on the Silkscreen_Top will be moved to the Silkscreen_Bottom subclass.

Note The outlines depicted are not meant to be a standard that you should follow. Your company will probably have its own guidelines or rules for outlines.

Rectangles should NOT be used for outlines as rectangles are shapes that a line width cannot be applied to.

Adding Labels

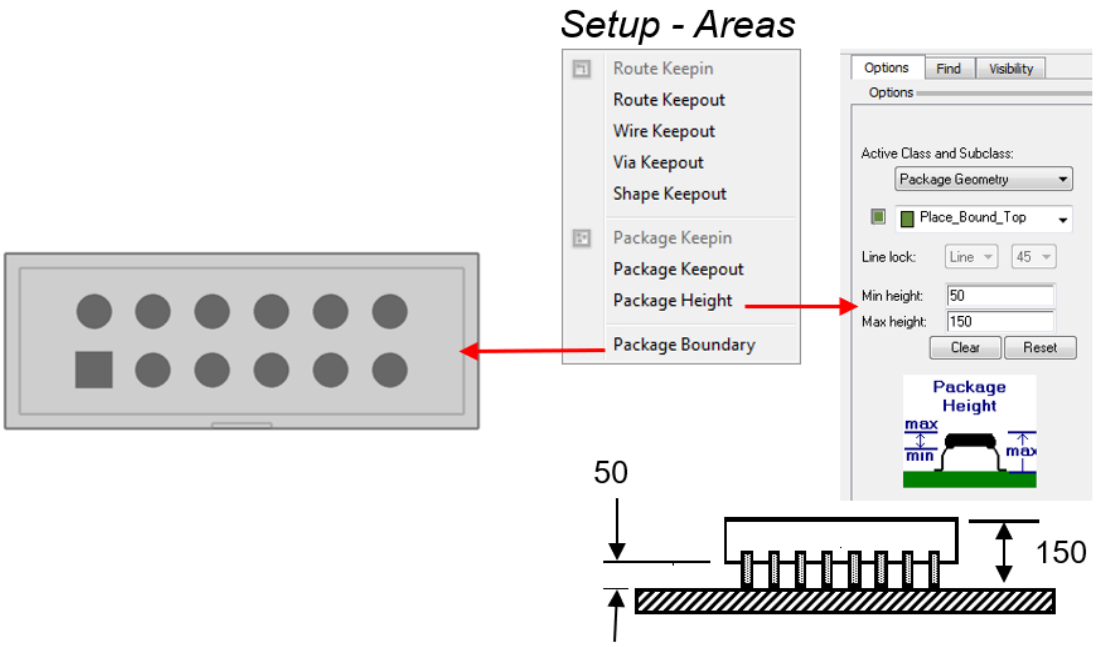


Labels are placeholders for component data such as assembly and silkscreen reference designators. It is also possible to add Component Value, Tolerance, User Part Number and Device Type placeholders. The location of the label determines where the data is displayed. You must define at least one reference designator label in order to successfully create a footprint.

When adding a label, use the Options tab to specify the text block size. This controls the size of the displayed data.

Use the Options tab to specify the class and subclass for your text label. Depending on which command you select, the Options form will default to an appropriate class/subclass setting. If you are creating silkscreen text labels, you will need to toggle the Subclass field to Silkscreen_Top.

Defining Package Areas



To define areas, use the pull-down menu from the ***Setup - Areas*** command.

- **Route Keepout** - A user-defined polygon that prohibits all etch
- **Wire Keepout** - A user-defined polygon that prohibits routing but allows vias
- **Via Keepout** - A user-defined polygon that prohibits vias but allows routing
- **Shape Keepout** - A user-defined polygon that prohibits shapes but allows routing and vias
- **Package Height** - Defines the package height (z dimension) that is attached to the package boundary. The height is a range from the bottom of package (Min Height), top of package (Max Height). If only one value is specified, it assumes the package starts from the board surface and extends to the given Max Height.
- **Package Boundary** - Defines a two-dimensional filled-polygon that is used to check for package overlap. If one is not user-defined, one is automatically created for you with the ***Create Symbol*** command.

To add a package height restriction to a component, first you must define the Package Boundary using ***Setup - Areas - Package Boundary***. Then use ***Setup - Areas – Package Height*** and select the package boundary area just created. Fill in the ***Options*** tab with the desired height restrictions, move your cursor back into the work area, and select ***"Done"*** from the ***Right-Mouse-Button*** to exit the command.

Saving Symbol Files

Two files are necessary to create a package symbol:

- A **`.dra` file** - Is the graphical file used to view or edit the symbol in the event you need to make a revision
- A **`.psm` file** - Is the compiled binary equivalent of your drawing file, and is the file used during placement to represent a component's physical layout

While performing the ***SAVE*** command to the .dra file:

- The system executes the *Create Symbo*l command automatically producing a package symbol compiled file (`.psm`) and a drawing file (`.dra`) with the same name. *Create Symbol* checks the drawing for common errors before "compiling" the symbol. The drawing file must also be kept in the library in the event a revision is needed.

The PCB Editor in the package creation mode can only read a drawing (*.dra)* file. It does not read the package symbol (*.psm)* file. Therefore, it is important to save the .dra file along with the .psm file. While executing the **Save** command the system will automatically compile the symbol and create a *.psm* file along with the *.dra* file.

The save command automatically checks the drawing for common errors and then creates a *.psm* file if no errors are found. For example, it checks to make sure you have at least one connect pad (padstack) and one reference designator label. It also checks for package boundaries. If your package symbol has no package boundary defined, it will be automatically created using either the Package Geometry - Assembly_Top outline, or the device pins with, whichever area is largest.

The *.psm* file is the compiled binary equivalent of your drawing file, and is the file used during placement to represent a component during physical layout. The .dra file is not used for placement. This is why you need to have both files available at all times.

Labs

Lab 4-1: Creating an SOIC14 Package Using the Package Symbol Wizard

- Use the Package Symbol Wizard to create an SOIC14 package symbol

Lab 4-2: Creating a header12 Package Symbol

- Add pins
- Add the Assembly/Silkscreen outlines
- Add the Reference Designator labels
- Add the Package Boundary and Package Height
- Save the footprint and create the symbol

Lab 4-1: Creating an SOIC14 Using the Package Symbol Wizard

Objective: Use the Package Symbol Wizard to create a through-hole package symbol.

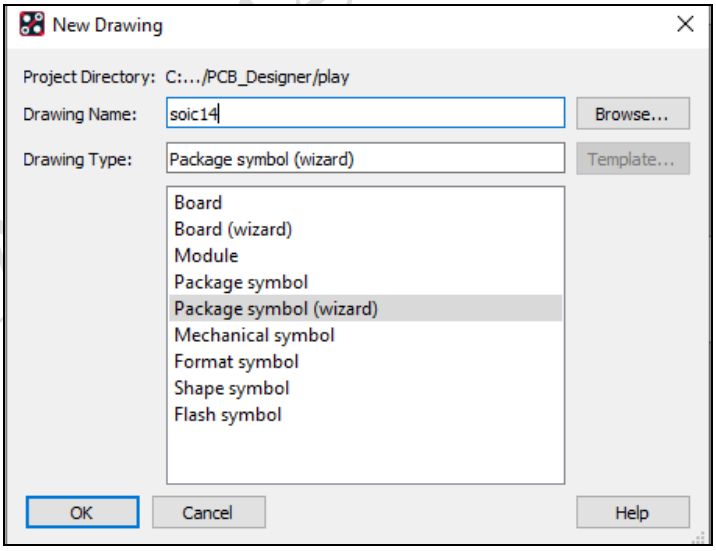
This lab shows you how to create a package symbol for an SOIC14 using the Package Symbol Wizard. You will use the surface mount padstack that you created earlier.

Naming the Symbol

1. Start the PCB Editor.
2. Make sure you are still working in the ***play*** directory.

Note You learned how to start the PCB Editor in the previous labs.

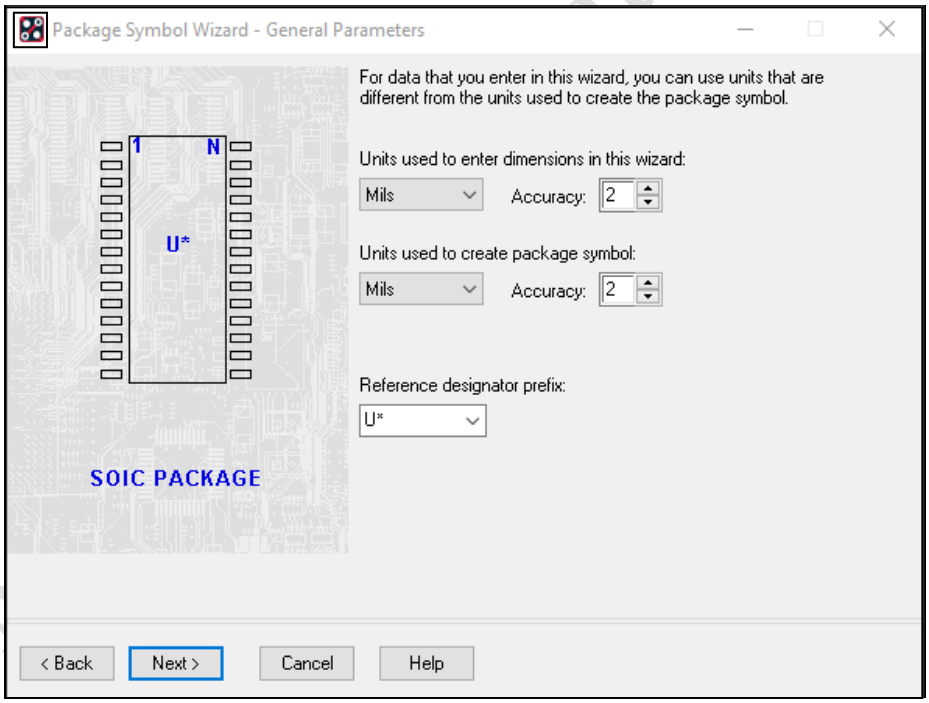
3. Select ***File - New*** from the top menu
   The ***New Drawing*** dialog box appears
4. Type `soic14` in the ***Drawing Name*** field
5. Select ***Package symbol (wizard)*** from the scrolling list of drawing types, as shown below:



6. Click ***OK*** to close the ***New Drawing*** dialog box.
   The ***Package Symbol Wizard*** form is displayed in the foreground and the Package Symbol editor is displayed in the background. This ***Package Symbol Wizard*** form is used to specify the type of package symbol to be created.

Using the Package Symbol Wizard

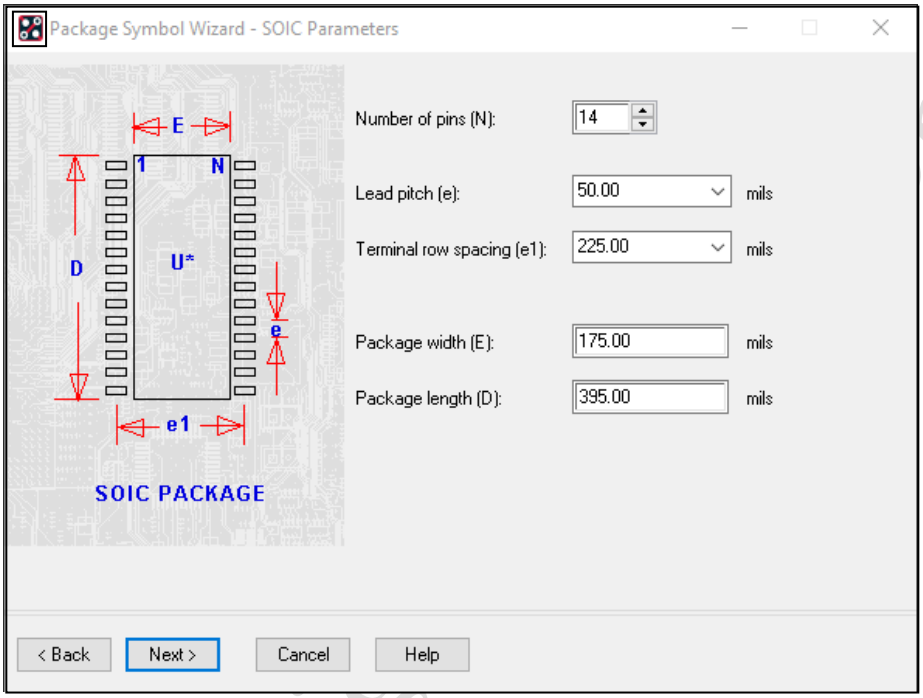
1. Select ***SOIC*** as the Package Type
2. Select ***Next>*** to use the SOIC wizard and continue to the next form
   The ***Template*** form is displayed. This form is used to specify the drawing template to be used when creating the symbol. The drawing template "seeds" such items as color of classes and subclasses, units of the drawing, accuracy of the drawing, and so forth.
3. Select ***Default Cadence supplied template*** if this option is not currently selected.
4. Select ***Load Template*** to load the default template.
5. Select ***Next>*** to continue to the next form.
   The ***General Parameters*** form is displayed. This form is used to specify some of the drawing parameters, as well as the reference designator labels. The values for Units and Accuracy are obtained from the drawing template specified in the previous form.
6. Set the values of ***Units*** to ***Mils*** and ***Accuracy*** to ***2*** for the fields "***Units used to enter dimensions in this wizard***" and "***Units used to create package symbol***", if these values are not currently set.
7. Set the ***Reference Designator Prefix*** to *U** if this value is not currently set.



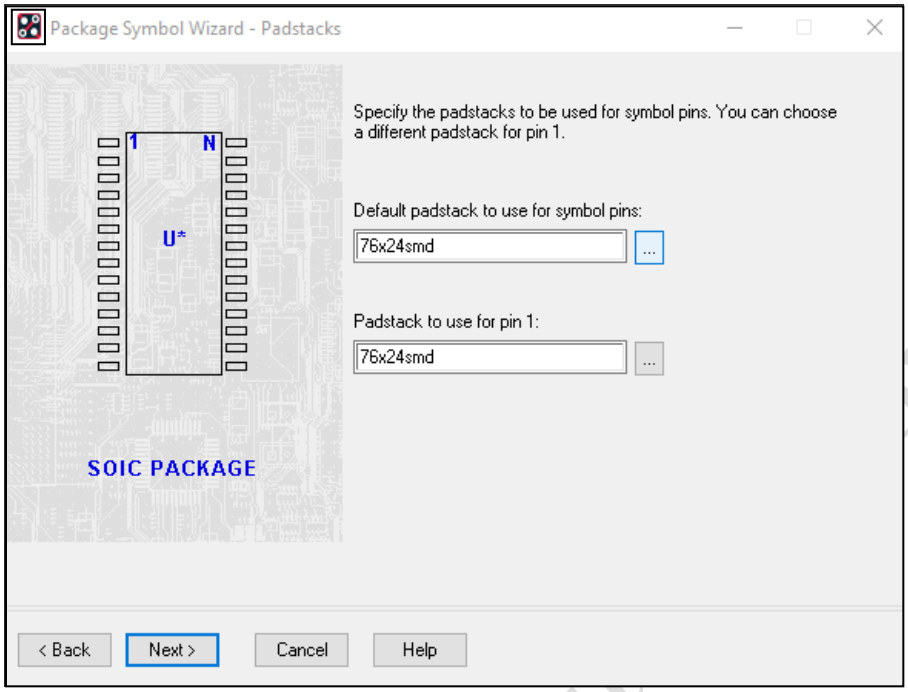
8. Select ***Next>*** to continue to the next form.

The ***SOIC Parameters*** form is displayed. This form is used to specify SOIC-specific parameters. This includes items such as pin-to-pin spacing, spacing between columns, and the overall package dimensions used to create the assembly and silkscreen outlines.

9. You will use the default ***SOIC Parameters*** shown in the figure below:



10. Select ***Next>*** to continue to the next form.
    The ***Padstacks*** form is displayed. This form is used to specify the padstacks to be used for the pins. You can specify a different padstack for pin 1 if needed.
11. Select the **"..."** button next to the empty field for "***Default Padstack to Use for Symbol Pins***".
    A Package Symbol Wizard padstack browser appears.
12. Select the padstack **76x24smd** (case is unimportant).
13. Select ***OK*** to close the Padstack browser form.
14. Notice that the "***Padstack to Use for Pin 1***" field is populated with the same padstack name. For this footprint you can use that same padstack.



15. Select ***Next>*** to continue to the next form.
    The ***Symbol Compilation*** form is displayed. This form is used to specify the location of (0/0) origin of the part, as well as whether or not to compile the symbol.
16. Select ***Center of symbol body*** as the location of the symbol origin (if this option is not currently selected).
17. Select '***Create a compiled symbol***' to enable the Package Symbol Wizard to generate the compiled portion of the symbol (if this option is not currently selected).
18. Select ***Next>*** to continue to the next form.
    The ***Summary*** form is displayed. This form is used to verify that the correct files are to be created. This is also your last chance to go "backwards" through any previous forms to change any data or specifications.
19. After verifying that the files `soic14.dra` and `soic14.psm` will be created, select ***Finish*** to complete the Package Symbol Wizard and create the soic14 symbol. The soic14 drawing (`soic14.dra`) and symbol (`soic14.psm`) are created and the footprint is opened in the Package Symbol Editor. At this point you can make any changes that you require. If you do make changes, be sure to save the drawing and create the symbol.

End of Lab

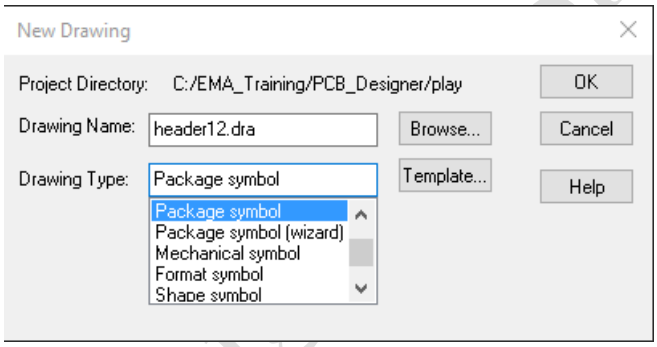
Lab 4-2: Creating a 12 Pin Header Package Symbol

Objective: Use the Package Symbol Editor to create through hole component.

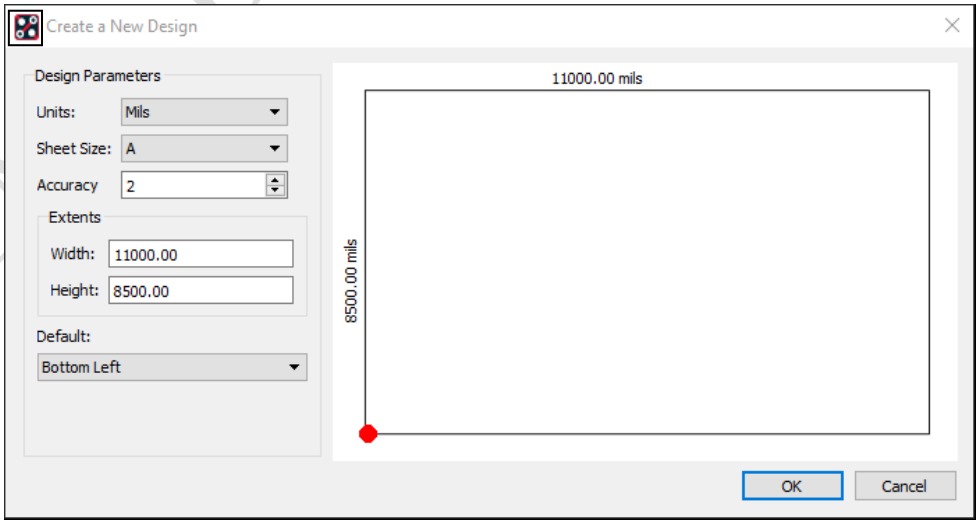
In this lab, you will use padstacks you created earlier to create a 12-pin header.

Starting in Symbol Edit Mode

1. Select ***File – New*** from the top menu.
   The ***New Drawing*** dialog box appears.
2. Type **`header12`** in the ***Drawing Name*** field and make sure you are still working in the ***Play*** directory.
3. Select ***Package Symbol*** from the scrolling list of drawing types, as shown below:



4. Click ***OK*** to close the ***New Drawing*** dialog box.
   The ***Create a New Design*** form appears.
5. Fill in the ***Create a New Design*** form as you see in the figure below.



6. Click ***OK*** to accept the values and dismiss the form.
   The ***Package Symbol*** editor is displayed.

Setting the Design Parameters

Use the Drawing Parameters form to modify the parameters in the Design tab, if needed. Also use this form to move the drawing origin from the lower left corner to a point inside the drawing area.

Note The origin of this package symbol drawing will become the package origin when you are in the component placement phase of your design.

1. Select ***Setup - Design Parameters***.
   Many of the parameters should match the previous package symbol as long as you did NOT close the PCB Editor.
2. Select the ***Design*** tab and modify the parameters as required to match the following values:
   - Type: ***Package***
   - User Units: ***Mils***
   - Size: ***A***
   - Accuracy: ***2***
   - Left X: ***-500***
   - Lower Y: ***-1500***
3. Click ***OK***.
   The ***Drawing Parameters*** form closes. The drawing origin is now nearer the center of the work area.

Adding Pins

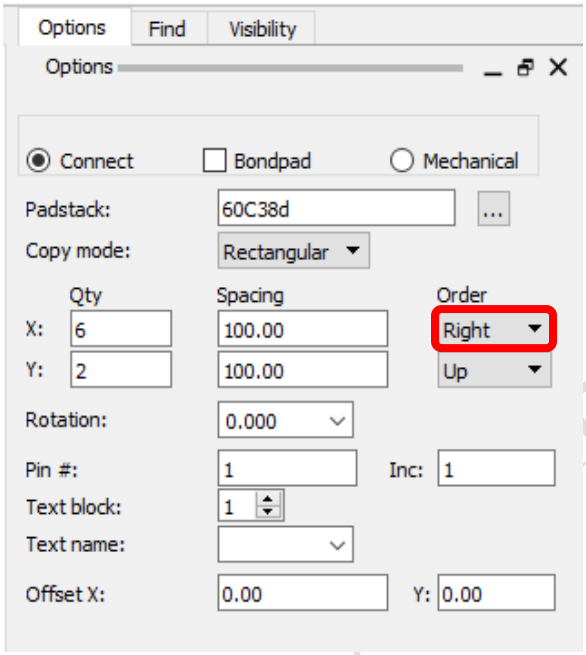
In this package, pin 1 is a square pin and the rest are round. The easiest way to add the pins is to initially add all pins using a round padstack and then replace the round padstack for pin 1 with a square padstack.

1. Select ***Layout - Pins*** from the top menu.
2. In the ***Options*** tab of the ***Control Panel***, click the **"..."** button next to the ***Padstack*** field.
   A padstack browser appears.
3. Select the padstack ***60c38d***.
   You will use this padstack for all pins in this device, for now.
4. Press ***OK*** to enter the padstack name.
   The Symbol Editor's Command window states:

```
Using '60C38D.pad'
```

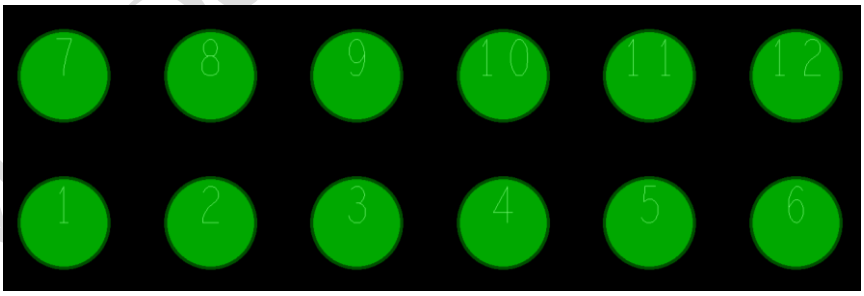
This means that the PCB Editor program was able to locate the padstack you specified. The padstack is now attached to your cursor.

5. Set the rest of the parameters in the Options tab as you see in the figure below:



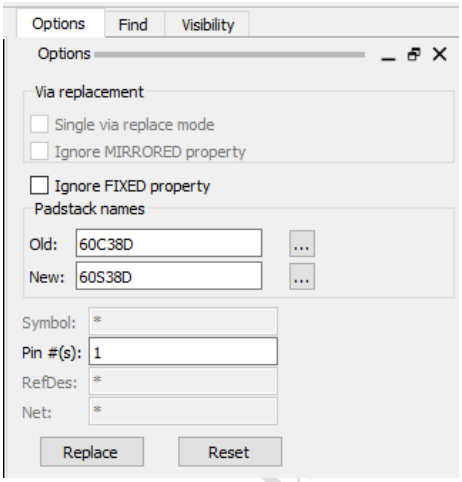
6. To place the pins, click in the PCB Editor command line to activate it, then type the following command: `x 0 0`
The matrix of padstacks is placed with pin 1 at the drawing origin (0,0)

7. Zoom in around pins
You should have 12 round pins placed as you see in the figure below:

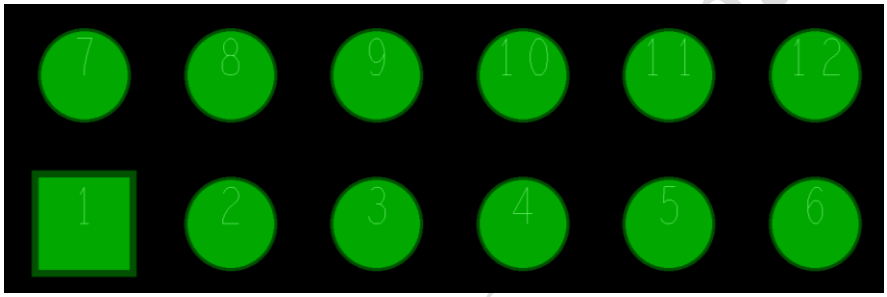


8. Next, select ***Tools – Padstack – Replace*** from the top menu

9. Click on one of the pins in the graphics window
   This will fill in the ***Old*** field in the ***Options Tab***
10. In the ***Options*** tab, click the **"..."** button next to the ***New*** field.
11. Select the padstack ***60s38d*** and click ***OK***
12. Type `1` in the ***Pin #(s)*** field
    The Options tab should look like the figure to the right.
13. Press ***Replace***
    Pin 1 is now replaced with the square pad.



Your footprint, at this point, should now look like the figure below.



14. Click the ***Right-Mouse-Button*** and select ***"Done"*** from the pop-up menu.

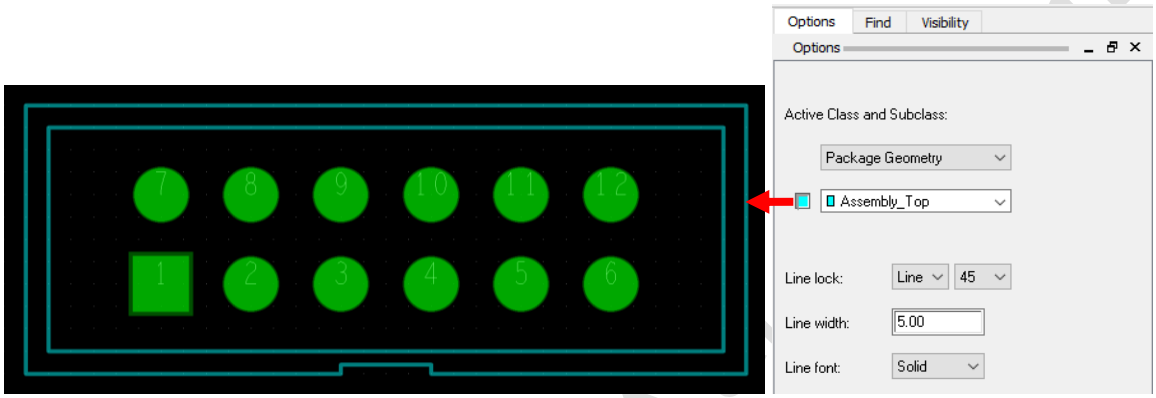
Setting the Non-Etch Grid

Except for the outermost assembly outline, the assembly and silkscreen outlines will be rectangles, created using the ***Add – Line*** command.

1. Select ***Setup - Grids*** from the top menu.
   The ***Define Grid*** form appears.
2. Locate the ***Non-Etch*** section at the top of the form.
3. Double-click in the ***Spacing x*** field and enter: ***25***
4. Double-click in the ***Spacing y*** field and enter: ***25***
5. Click ***OK*** at the bottom of the ***Define Grid*** form.
   If the work area does not display a 25-mil grid, click on the Grid icon.

Adding an Assembly Outline

1. Click ***Add - Line*** from the top menu.
   Make sure that the ***Options*** tab active class and subclass are set to ***PACKAGE GEOMETRY*** and ***ASSEMBLY_TOP***. You will add the assembly graphics to this layer of the symbol drawing, as shown below.
2. Set the line width to 5 mil



We will now draw the outermost outline by typing in the coordinates.

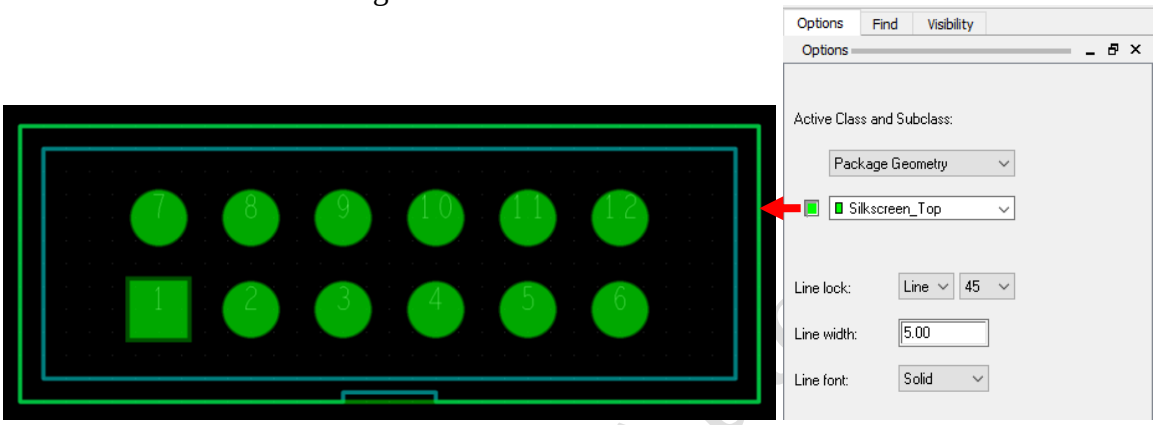
3. At the ***Symbol Editor's Command line***, type each of the following sets of values and press ***Enter*** after each entry.

```
x -150 -100
ix 350
iy 10
ix 100
iy -10
ix 350
iy 300
ix -800
iy -300
```

4. Select ***Right-Mouse-Button*** and select ***Next*** from the popup.
   This will end the current line while leaving you in the ***Add – Line*** command.
5. Draw a second rectangle just ***25 mil*** (the next grid point) inside the first.
6. When you have finished, click the ***Right-Mouse-Button*** and select ***Next*** again from the popup menu.
   This will allow you to add the silkscreen outline without selecting the ***Add – Line*** command again.

Adding a Silkscreen Outline

1. At this point, you should still be in the ***Add – Line*** command. Make sure that the ***Options*** tab active class and subclass are set to ***PACKAGE GEOMETRY*** and ***SILKSCREEN_TOP*** and the line width is still set to 5 mil.
2. Now, click to draw the silkscreen outline rectangle on top of the outermost assembly outline as shown in the figure below.



   Because pin 1 is a square pad, we don't need to add a any other pin1 indicator.

3. To exit the ***Add - Line*** command, click right and select ***"Done"*** from the ***Right-Mouse-Button*** popup menu.

Setting Colors

By default, all objects in a new drawing are set to a similar color. To help differentiate between the assembly and silkscreen outlines, assign each of them a different color.

1. Click the ***Color192*** icon.
   The ***Color Dialog*** form appears.
2. Select the ***Layers*** tab.
3. Select the ***Geometry*** category.
4. Scroll down the ***Package Geometry*** column to the ***ASSEMBLY_TOP*** subclass.
   Next you will change the ASSEMBLY_TOP subclass to blue.
5. Click a color ***blue*** in the Palette area and assign it to the ***ASSEMBLY_TOP*** subclass.
6. Click the color ***green*** and assign it to the ***SILKSCREEN_TOP*** subclass.
7. Click on ***OK*** in the ***Color Dialog*** form.
   The ***Color Dialog*** form closes, and the symbol drawing displays the new color assignments.

Adding Labels

We will now use labels to display the reference designator. The label is simply a placeholder and will be replaced by the actual reference designator on the PCB.

1. Select ***Layout - Labels - RefDes*** from the top menu.
   Make sure the ***Options*** tab active class and subclass are set to ***REF DES*** and ***ASSEMBLY_TOP***. We will add text to this layer first.
2. In the Options tab of the Control Panel, set the following text parameters:
   - **Rotate** ***0***
   - **Text block** ***4***
   - **Text just** ***Left***

   The Symbol Editor Command window area prompts you to:

   ```
   Pick text location.
   ```

3. Click someplace inside the assembly outline.
   The Symbol Editor message area prompts you to:

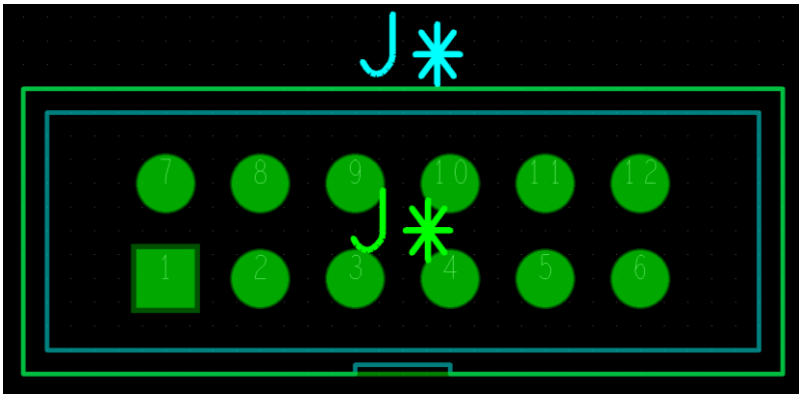
   ```
   Enter text string.
   ```

4. Enter: `J*`
5. Click right and select **"Done"** from the pop-up menu.
6. Select ***Layout - Labels - RefDes*** from the top menu again.
   Make sure the ***Options*** tab active class and subclass are set to ***REFDES*** and ***SILKSCREEN_TOP*** and that the other parameters are still set.

   Notice the prompt on the Symbol Editor command line that says:

   ```
   Pick text location.
   ```

7. Click above the component outline so that the silkscreen text will be in a visible location *after* the component is installed in a board
8. Enter: `J*`
9. Click right and select **"*Done*"** from the popup menu.
   At this point, your footprint should look like the figure below.



Creating a Package Boundary

The DRC program uses the package boundary to make sure a package does not overlap another package or any other objects that can cause a problem (Package Keepout areas, and so forth).

If you do not create the package boundary, it will be created for you automatically when the ***Create Symbol*** command is run.

1. Select ***Setup - Areas - Package Boundary*** from the top menu.
2. In the ***Options*** tab set the Class to ***PACKAGE GEOMETRY*** and Subclass to ***PLACE_BOUND_TOP***.
3. Click to draw a polygon representing the area required for placement. For this footprint, the boundary will be the same size and shape as the Silkscreen outline.
4. Close the polygon, by selecting **"*Done*"**
   The boundary will be automatically filled solid.

Defining the Package Height

The DRC program uses package height to make sure a package does not violate a height restriction area of the board. It is not necessary to define the package height for every device. The PCB Editor tool uses the Design Parameter - Design tab - Default Symbol Height field to define a default package height for all symbols that do not have a Package height assigned to them. To override this default package height, you need to attach a height value to the boundary.

1. Select ***Setup - Areas - Package Height*** from the top menu.
2. In the ***Options*** tab make sure the Class is set to ***PACKAGE GEOMETRY*** and the Subclass is set to ***PLACE_BOUND_TOP***.
   Notice the prompt in the Symbol Editor Command window says:

   ```
   Select or add package shape.
   ```

3. Click on the package boundary (filled polygon) you just created.
   The package boundary is highlighted. The Symbol Editor message area prompts:

   ```
   Enter package PACKAGE GEOMETRY/PLACE_BOUND_TOP height.
   ```

4. In the ***Max height*** field of the ***Options*** tab enter: ***150***
   The package height is 150 mils.
5. To exit the ***Package Height*** command, click right in the PCB Editor's work area and select **"Done"** from the pop-up menu.

The package boundary is a 2-D polygon. When height data is attached to this polygon, the DRC program evaluates the package boundary as if it were three dimensional.
This package now contains explicit height information that will override the default height specification contained in the Design Parameter, Design tab.

6. If you have time, click on the **3-D** icon to view the height of your new footprint.

Saving the Symbol to Disk

1. Select ***File - Save*** from the top menu.

The system saves a `header12.dra` file. This file is used if you ever need to edit the graphics for this symbol.

It also creates a symbol `header12.psm`. This file is used in the design process during component placement.

End of Lab

Lesson 5: Board Design Files

Learning Objectives

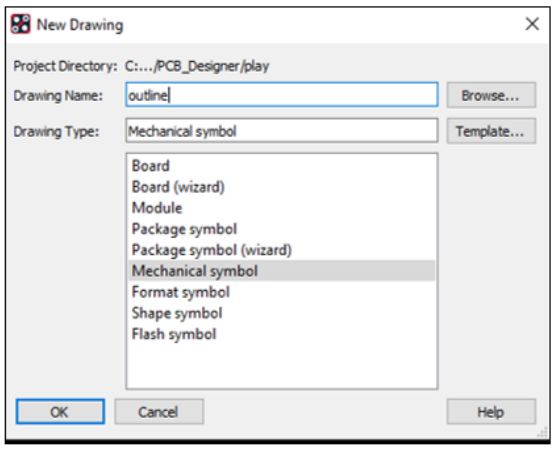
In this lesson, you will:

- Use the **Mechanical Symbol Editor** to create a mechanical board symbol
- Import **DXF** to create the board outline
- Use the **PCB Design Editor** to create a Template board design

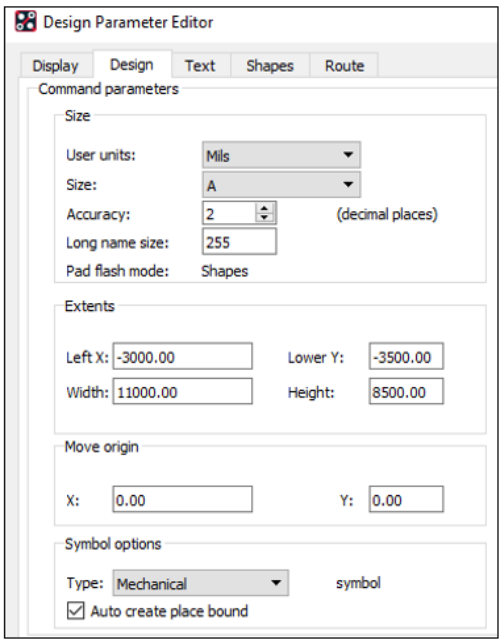
In this section, you will learn how to create board outlines or board mechanical symbols. Creating board outline mechanical symbols can save you time when your designs use the same outline. Board outline mechanical symbols will also improve the quality of the design, since the outline only needs to be checked once. After the outline has been verified, all designs using that outline will be correct.

Creating a Board Symbol

File - New



Setup – Design Parameters



To create a board symbol, select **Mechanical Symbol** as the drawing type. Next, use the Design Parameters form to define the following:

User Units - Mils, Inches, Millimeters, Centimeters, or Microns. Default is Mils.

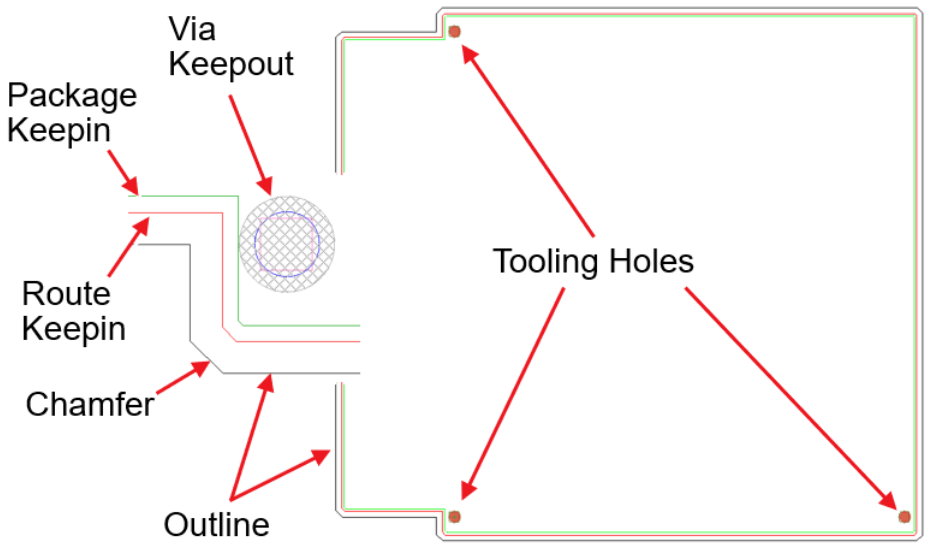
Size - A, B, C, D or Other. (A1, A2, A3, A4 for metric units). Default is A.

Accuracy - The number of decimal places. Range is 0 - 2. Default is 0.

Move Origin - Can be used to place the drawing origin inside the drawing area (to establish a mechanical datum point).

Drawing Type - Mechanical (`.bsm`).

Elements of a Board Outline



This is an example of a card outline with keepin and keepout areas and tooling holes. To create an PCB Editor mechanical outline symbol:

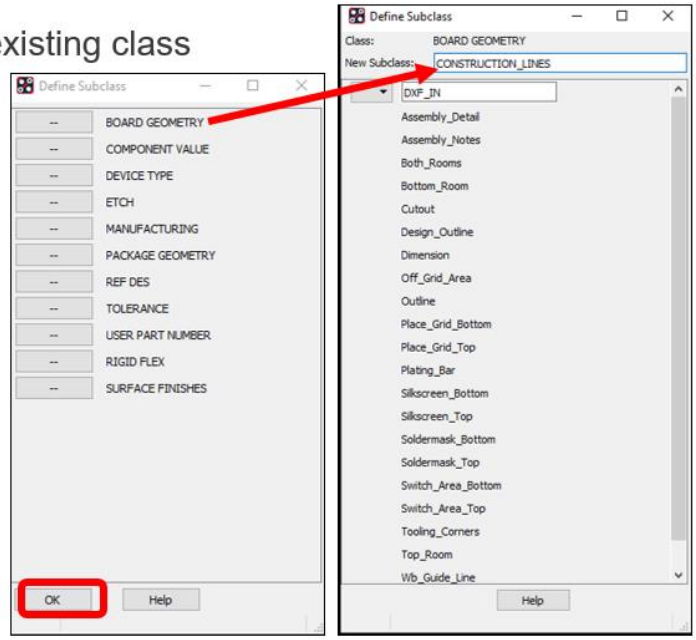
1. Define the card outline.
2. Define mounting holes (added as pins).
3. Define package and routing keepin/keepout areas.
4. Save the symbol's drawing file to create the symbol's compiled file (`.bsm`).

Add New Subclass

Setup – Subclasses

Add a new subclass to an existing class

- Select class
- Add new subclass name
- Hit **Tab** key
- Click OK



Setup – Subclasses in the symbol editor, or ***Setup – More – Subclasses*** in the board layout editor allows the user to add subclasses to those classes which allow user-defined subclasses.

The Define Subclass dialog box displays the list of Classes in alphabetical order. This opens a Define Subclass window which displays all of the subclasses for the selected class in alphabetical order. Add the name of the new subclass in the "New Subclass" field and click the **Tab** key. The new subclass will be added to the top of the subclass list and will display in a white box.

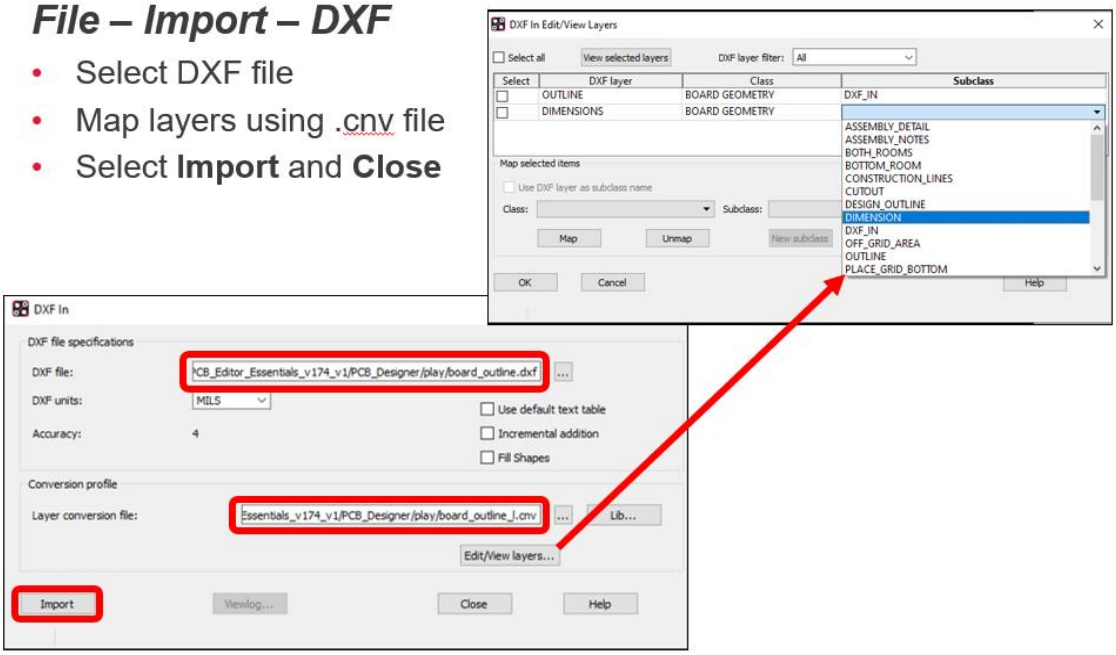
Only those user-defined layers that you created can be deleted as long as there is nothing on them at the time you try to delete them. You cannot delete the software defined layers.

Because the board outline will often come in as lines and lines are not allowed on the Design_Outline layer, you will want to import the DXF of the board outline on a special layer (i.e. DXF_In). Then, the lines may be "composed" into a shape and copied or moved to the Design_Outline layer.

Importing DXF to Create the Board Outline

File – Import – DXF

- Select DXF file
- Map layers using .cnv file
- Select **Import** and **Close**



Typically, the size and shape of the board outline is set by the mechanical engineer. The mechanical engineer can send you the board outline information in the form of a DXF, IDX, or IDF file. You can then easily import that into PCB Editor. For the purposes of this class, we will show you how to import a DXF file.

When importing a DXF file, you will need a layer conversion (.cnv) file. This file maps the DXF layers to the corresponding PCB Editor layers. If this is the first time you have imported a board outline from a DXF file, you will probably have to create the layer conversion file.

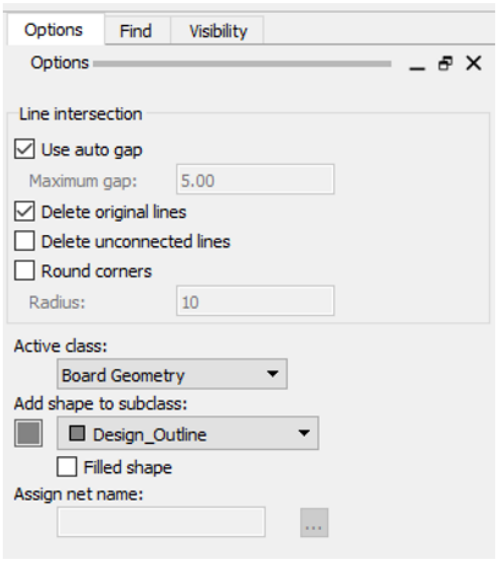
The ***Edit/View layers…*** button will take you to a form that allows you to map the DXF layers to the corresponding PCB Editor layers and then save that information to disk in the form of a layer conversion (.cnv) file.

The layer conversion file may be saved and used to import future board outlines, if the DXF layer names are the same as in the original DXF file.

Move Outline to Design Outline Layer

Shape – Compose Shape

- Changes lines into a shape
- Places shape on preferred layer
- Select Class and Subclass
- Window select outline



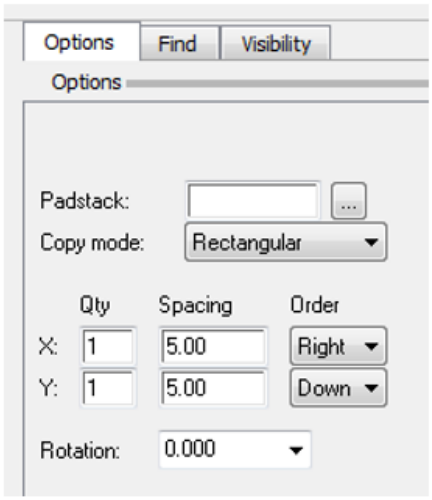
Once you have brought your board outline in on your new special layer, you will need to move it to the **Board Geometry – Design_Outline** layer. If the outline was created using lines, you will also need to "Compose" the lines into a shape. These two functions may be accomplished in one step using the ***Shape – Compose Shape*** command.

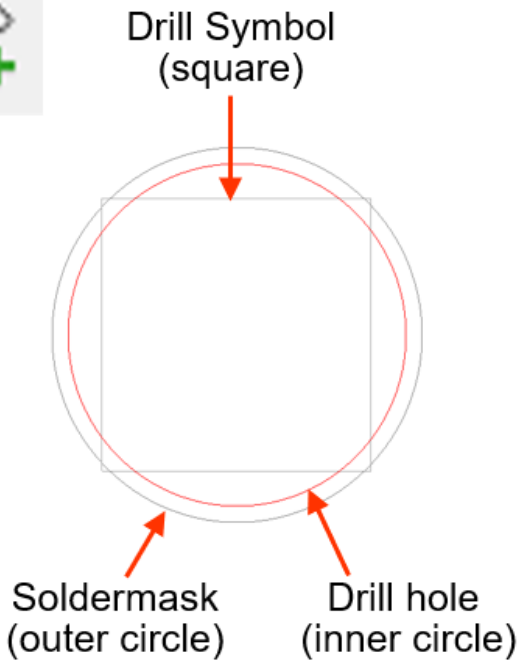
Here are the steps required:

1. Select ***Shape – Compose Shape*** from the top menu
2. In the Options tab of the Control Panel, set the **Active class** field to ***Board Geometry*** and the **Add shape to subclass** field to ***Design_Outline***
3. Window select around the entire board outline
4. Click **RMB** and select ***Done*** from the popup menu

Tooling/Mounting Holes

Layout - Pins …Or 



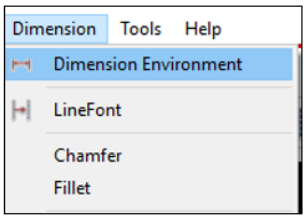


You add tooling holes and mounting holes to your board outline using the same command as adding pins into your package footprint symbols. However, when adding mounting holes and tooling holes, you will notice that in the Options tab there is no field for the pin number. You cannot assign pin numbers to these types of holes. Since you cannot add pin numbers, you cannot assign a net name to these holes either.

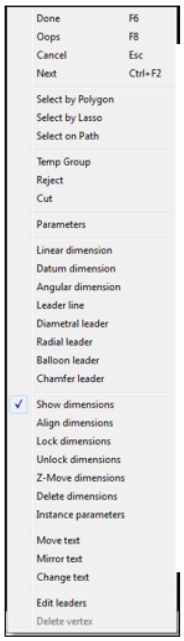
If you wish to assign a net name to a tooling hole or mounting hole - possibly for grounding reasons - you will have to create the mounting hole as a one-pin package symbol and have it added to the board through a schematic or netlist.

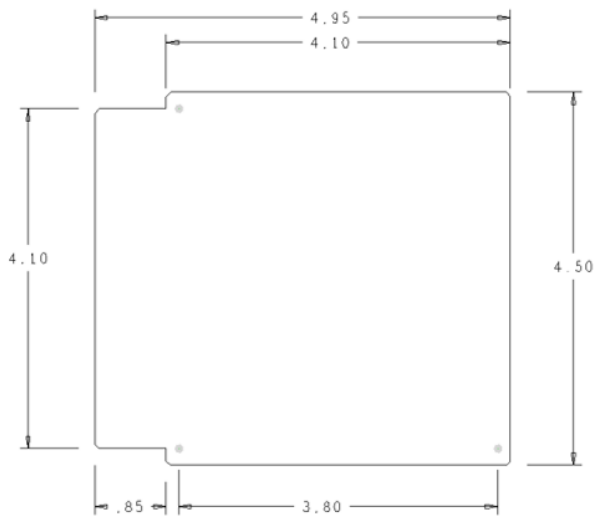
You can use the “x”, “ix” or “iy” commands when adding the tooling/mounting holes. These commands may also be used at any time within any other command, such as move, when placing parts, and so on.

Dimensioning with the Dimension Environment



Select ***Dimension – Dimension Environment***, then **Right-Mouse-Button** pop-up menu to access dimensioning options



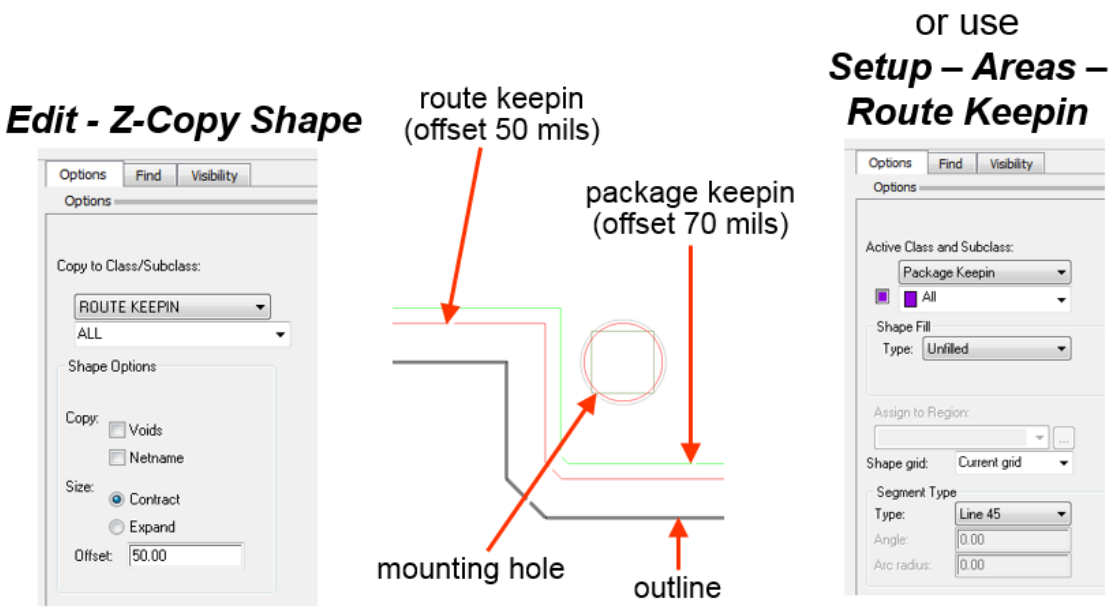


There are MANY different options available for dimensioning your design. The main menu option ***Dimension*** contains the Dimension Environment, LineFont, Chamfer, Fillet, and Create Detail commands.

- Dimension Environment - Contains all of the dimension commands accessible through a Right-Mouse-Button popup menu. The Parameters option allows you to set what type of dimensioning you will be doing, how the dimensions will look, and so on. By default, all dimensions are created on the BOARD GEOMETRY class, DIMENSION subclass.
- LineFont - Sets the appearance of the line being drawn. Choices are solid, hidden, phantom, dotted, and center.
- Chamfer - Places an angle at a vertex point based on the trim segments and angle set in the Options tab. Default is 45 degrees with just the first segment value set.
- Fillet - Places a radius at a vertex point based on the radius set in the Options tab.
- Create Detail - Creates a view that can be scaled and applied to the design for a designer's specific needs (example: enlarged assembly view).

Note In the Symbol editor, the main menu for dimensioning is Dimension. However, when working on a board design in the PCB Designer editor the main menu for dimensioning is Manufacture - Dimension.

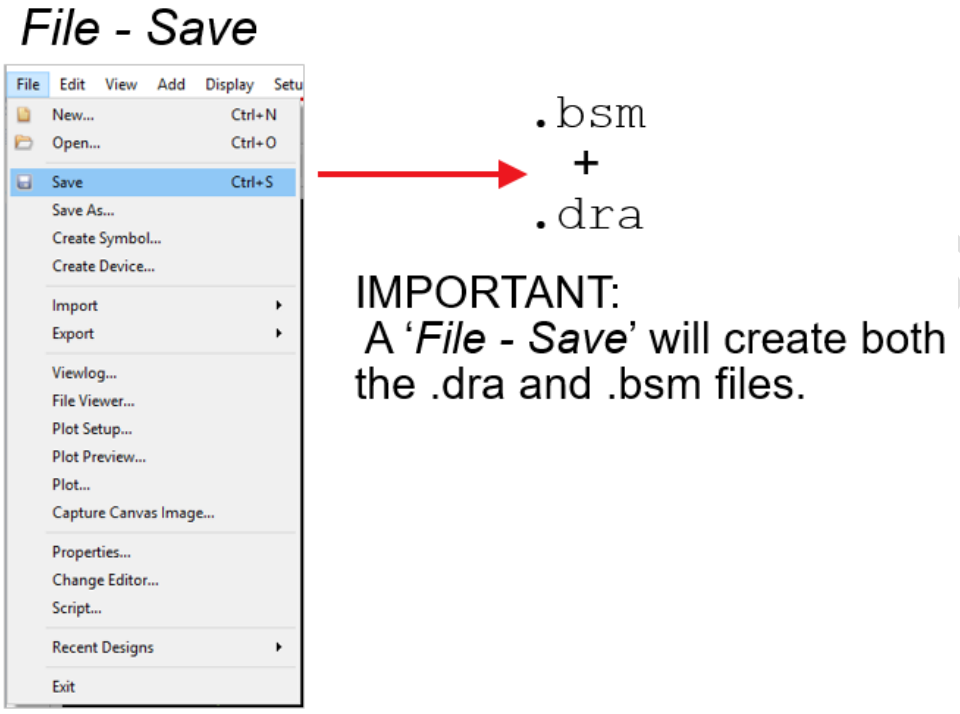
Defining Constraint Areas – Keepins and Keepouts



You define the keepin and keepout areas using the selections in the ***Setup - Areas*** pulldown menu or by using the ***Edit - Z-Copy Shape*** command. There are many different keepin and keepout areas that can be defined. Some of these are:

- **Route Keepin** - User-defined route keepin, drawn as an unfilled polygon. Defines the allowable area for routing. Defined for all etch layers at once. There can only be one Route Keepin in a design. The Route Keepin is used by the Shape program.
- **Package Keepin** - User-defined package keepin, drawn as an unfilled polygon. Defines allowable area for placement. Defined for all placement layers at once. There can only be one Package Keepin in a design.
- **Route Keepout** - User-defined filled polygon that prohibits all etch, vias, and shapes (copper pours).
- **Wire Keepout** - User-defined filled polygon, that prohibits traces but does allow vias and shapes.
- **Via Keepout** - User-defined filled polygon, that prohibits vias but does allow etch and shapes
- **Shape Keepout** - User-defined filled polygon that prohibits shapes but does allow etch and vias.
- **Package Keepout** - User-defined filled polygon that prohibits the placement of components. Defined for top, bottom, or both layers at once.
- **Package Height** - Attached to a Package Keepout area. Converts the 2D area into a 3D keepout. Checks to make sure that components placed in this area are not taller than the height specified. Defined for Top, Bottom, or All.

Saving Board Symbol Files (.bsm and .dra)



Much like package symbols, when you save your mechanical symbol, you get two files created on disk. One is the .dra version, which is the file read in by the mechanical symbol editor, and the other is the compiled symbol which has an extension of `.bsm`. This is the board mechanical symbol that gets placed in the .brd file.

Note Save both the .bsm and the `.dra` files. You can extract these files from an archived design, but you should keep both files available during the current project.

Lab

Lab 5-1: Creating a Board Mechanical Symbol

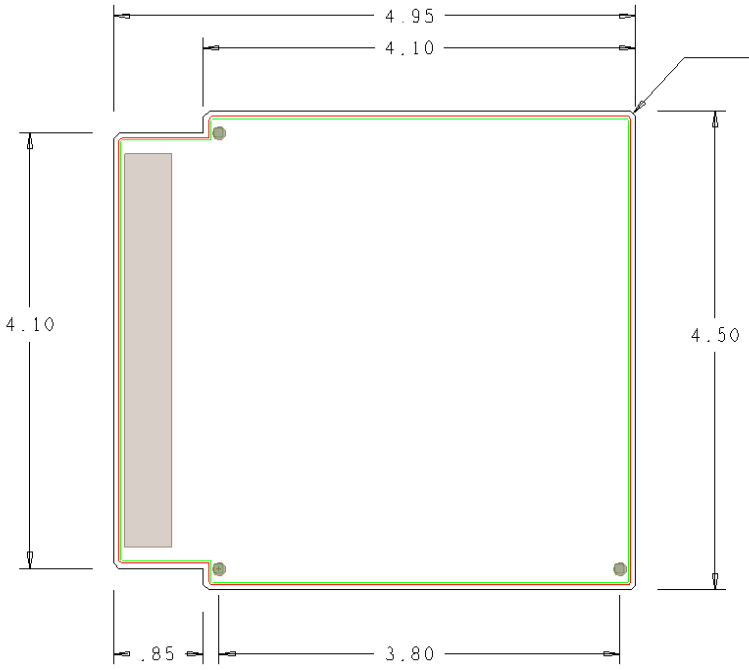
- Name the symbol
- Add new subclass
- Import DXF to create the board outline
- Move outline to Design_Outline layer
- Add tooling holes
- Add linear dimensions
- Dimension a chamfer
- Add Placement and Routing Keepin areas
- Add via keepout area
- Create and save the mechanical symbol (`.bsm`) and drawing (`.dra`) files

The following lab will let you familiarize yourself with the process required to create a board mechanical symbol. Items covered include creating the board outline, adding tooling and mounting holes, and adding keepins and keepouts.

Lab 5-1: Creating a Board Mechanical Symbol

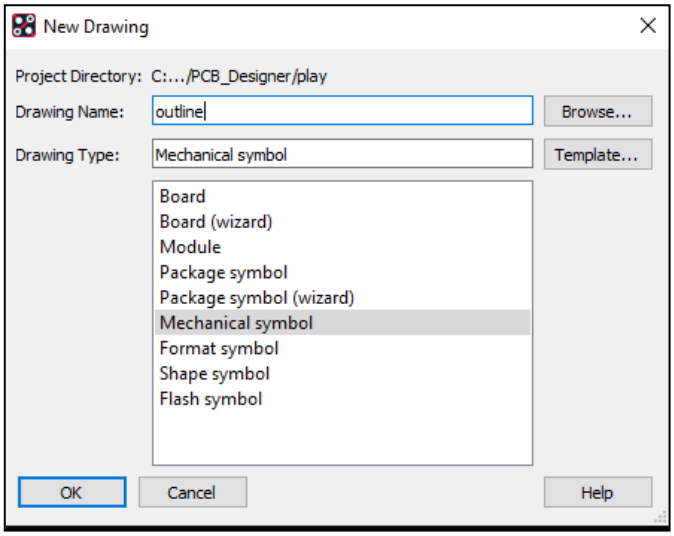
Objective: Use the Mechanical Symbol Editor to create a board outline symbol.

In this lab, you will create a mechanical symbol to match the following design and dimensions.

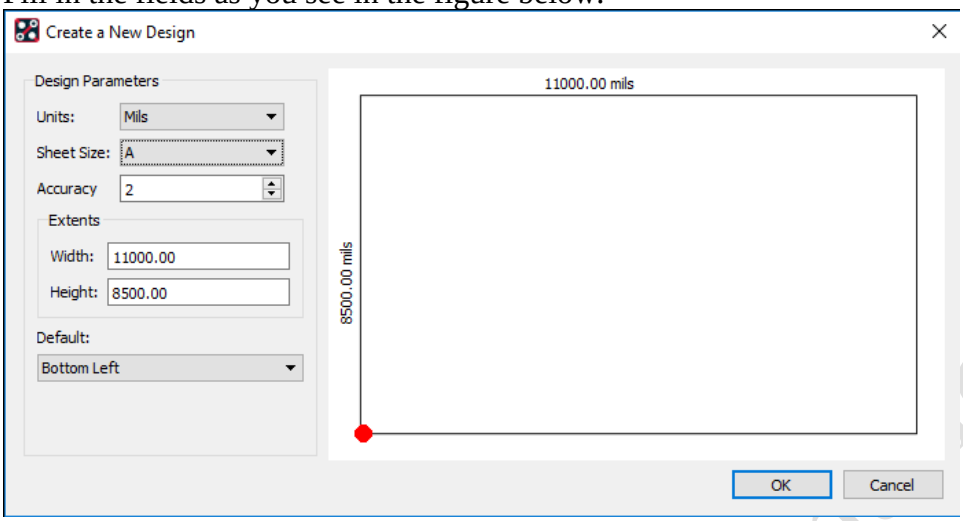


Naming the Symbol

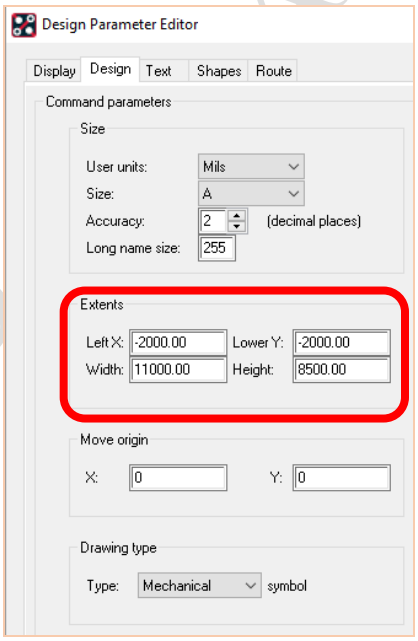
1. Start the PCB Editor if you don't already have the software running.
2. Choose ***File - New*** from the top menu.
   The ***New Drawing*** dialog box appears.
3. In the ***Drawing Name*** field, type the following name:
   `Outline`
4. Choose ***Mechanical Symbol*** from the scrolling list of drawing types, as shown below.
5. Click ***OK*** to close the New Drawing dialog box.
   The ***Create a New Design*** form appears.



6. Fill in the fields as you see in the figure below.



7. Select Setup – Design Parameters from the top menu and click on the ***Design*** tab. Notice that all your previous settings are retained.
8. Change the ***Drawing Extents*** fields to match the values in the following figure and click OK to save the settings and dismiss the form.

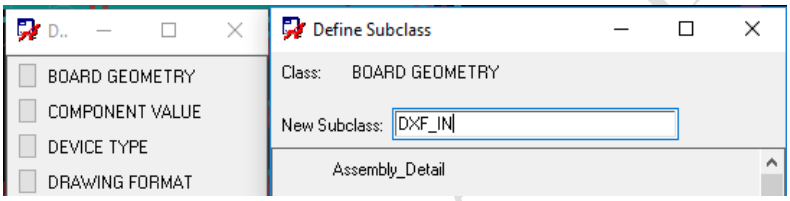


These settings cause the drawing origin to be placed 2 inches (2000 mils) up and to the right of the lower left corner of the drawing.

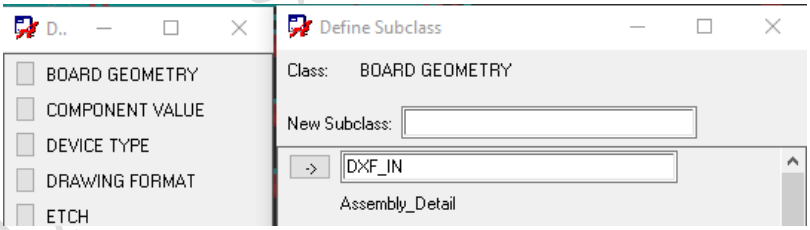
Adding New Subclass

When importing DXF for your board outline, you may want to import it on a special layer first, before copying, or moving it to the Design_Outline layer. So, for this section, we will add a new subclass named **DXF_In** to the Board Geometry class. We can use this subclass for importing our board outline in DXF format.

1. Select the ***Setup – Subclasses*** from the top menu.
2. In the ***Define Subclass*** dialog box, click the button for the ***Board Geometry*** class. This will open a ***Define Subclass*** dialog box that contains subclasses associated with the Board Geometry class. The original Define Subclass dialog box with the list of all of the classes will stay open.
3. In the ***New Subclass*** field type: **`DXF_IN`**



4. Hit the ***Tab*** keyboard key.
   The new subclass will appear in a white box above the software defined subclasses.

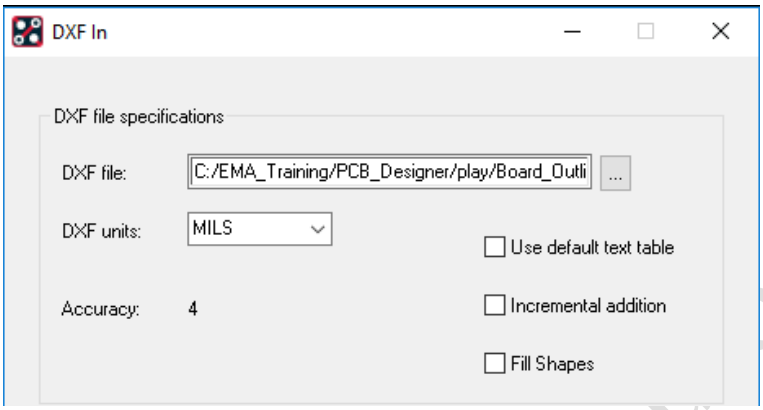


5. Click on the ***OK*** button at the bottom of the first **Define Subclass** dialog box to close out both define Subclass dialog boxes.

Importing DXF to Create the Board Outline

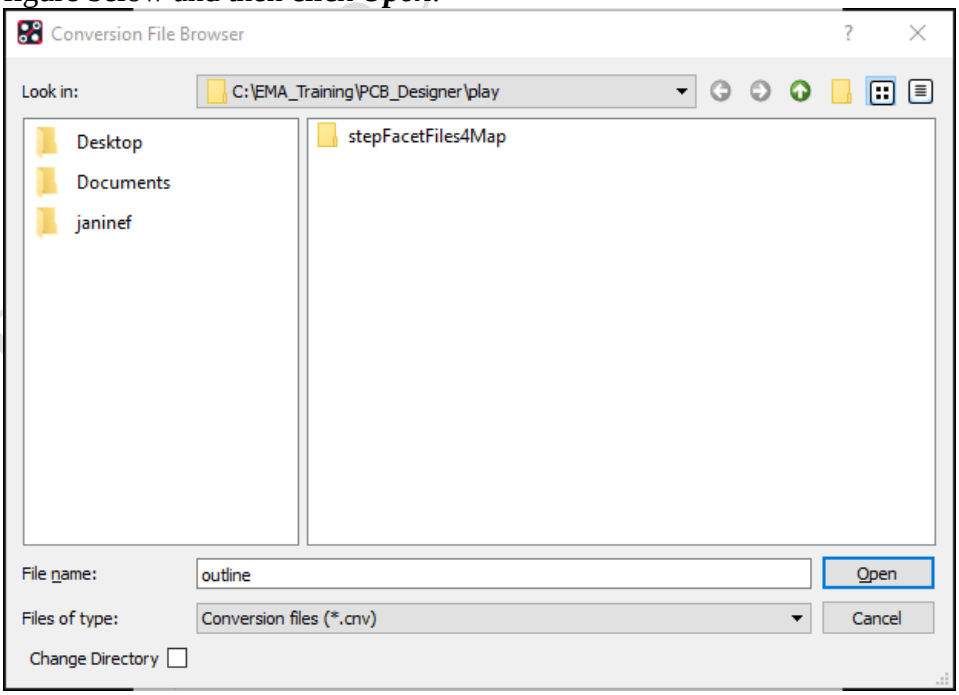
Now, we will import a DXF file to create the board outline.

1. Select ***File - Import – DXF*** from the top menu to open the DXF In form.
2. Click on the **…** button in the top half of the form to browse to the ***board_outline.dxf*** file and set your DXF units to ***MILS*** as you see in the figure below.

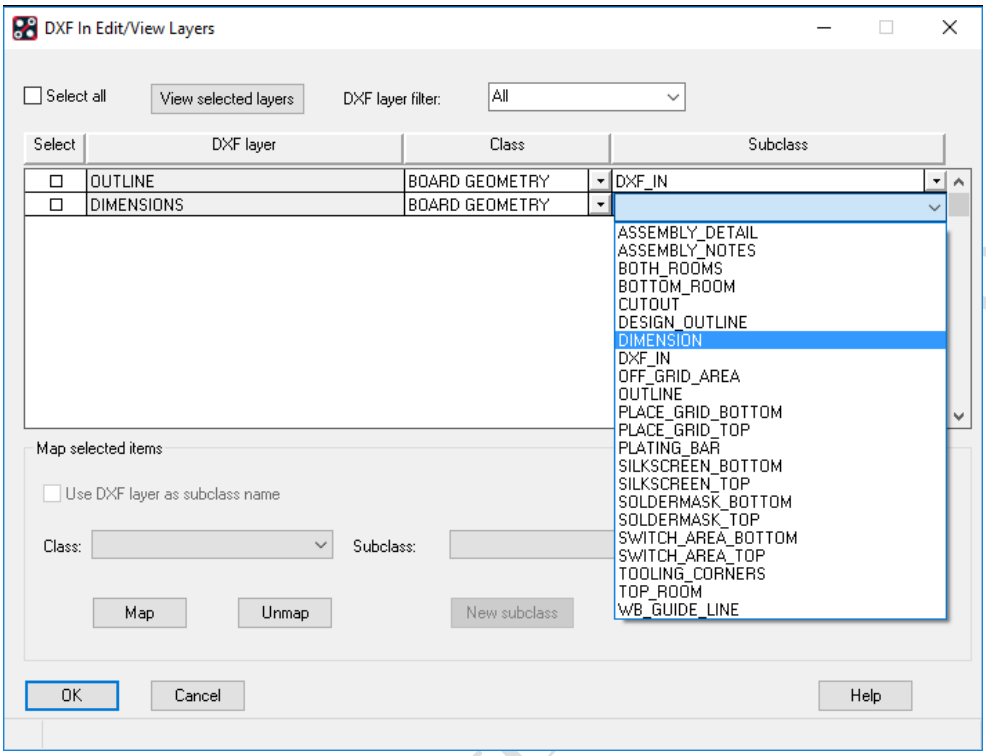


Next, we will map the DXF layers to PCB Editor layers.

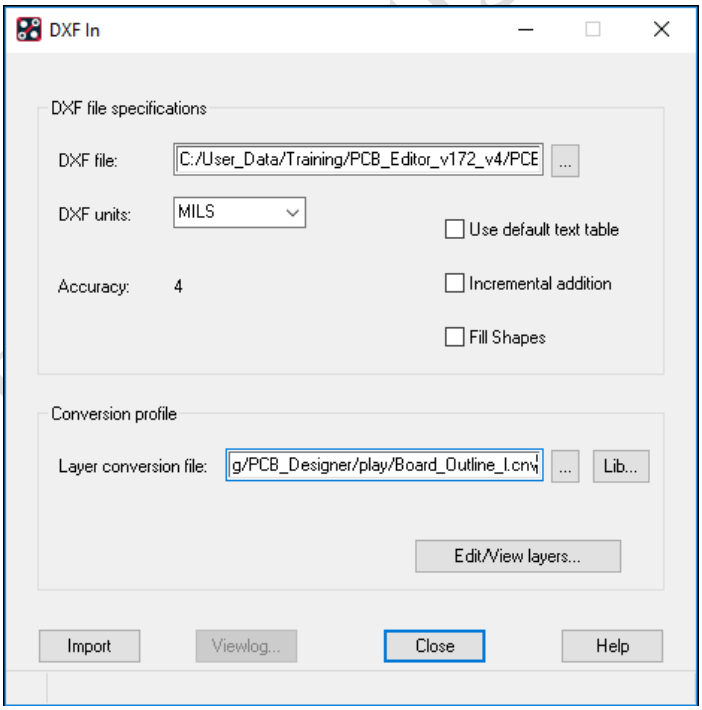
3. First, click on the **…** button in the bottom half of the form to select a Layer Conversion file (.cnv).
   The Conversion File Browser opens, but as you can see, we do not yet have a layer conversion file, so we will have to create one.
4. Type the file name `outline` into the Conversion File Browser as you see in the figure below and then click ***Open***.



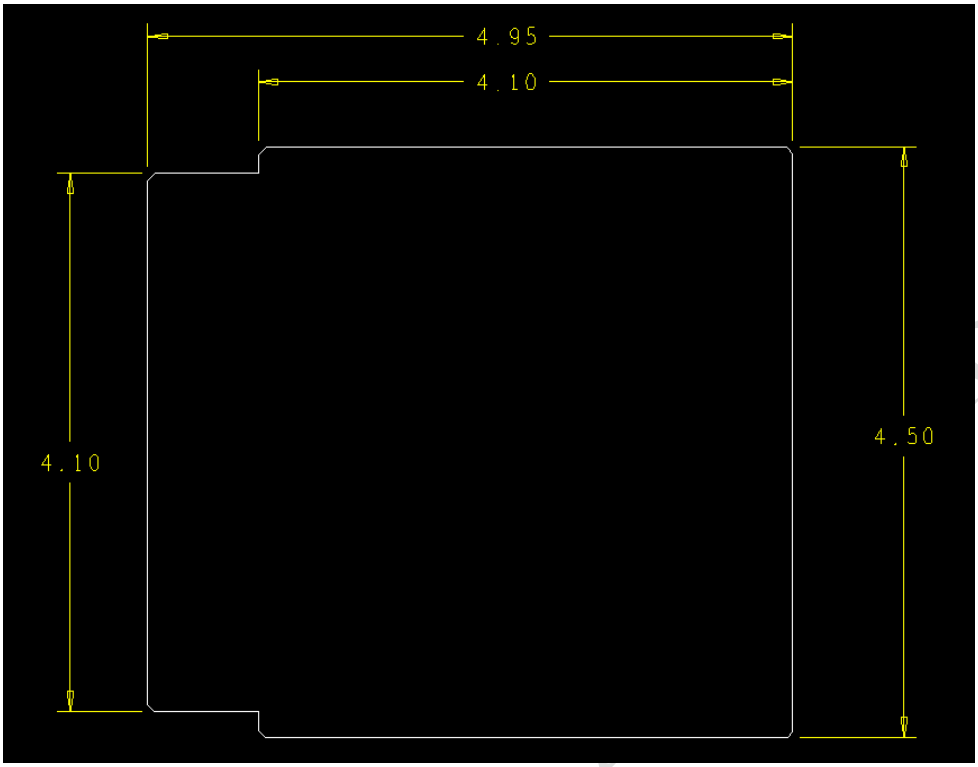
5. Next, click on ***Edit/View layers…*** button and in the resultant window use the pulldowns to map the Classes and Subclasses as you see in the figure below and then click ***OK*** to save your **outline.cnv** file to disk.



6. Lastly, click ***Import*** in the DXF In form.

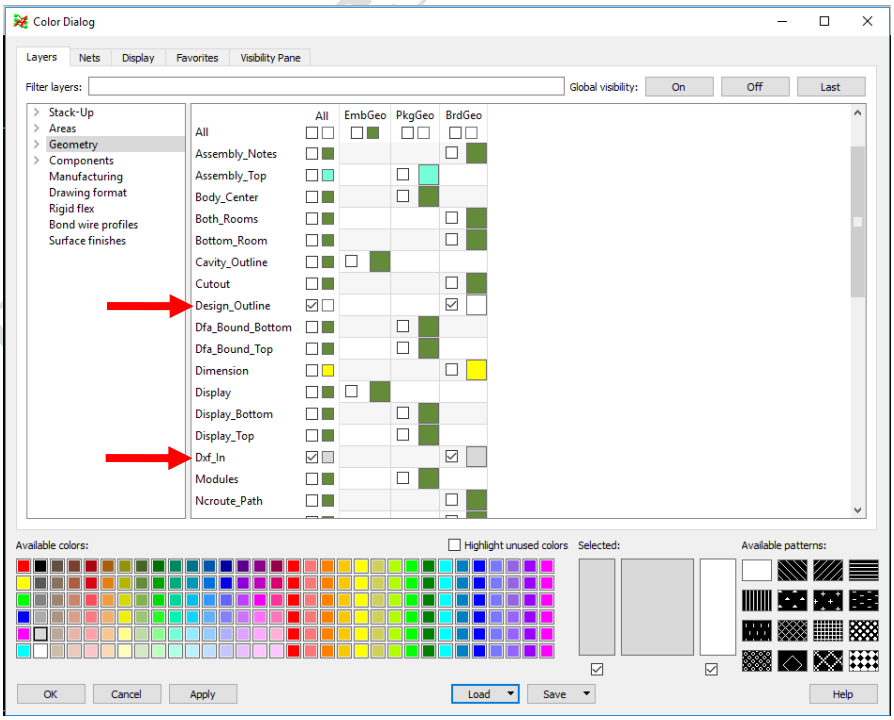


You should now see your board outline along with the dimensions.



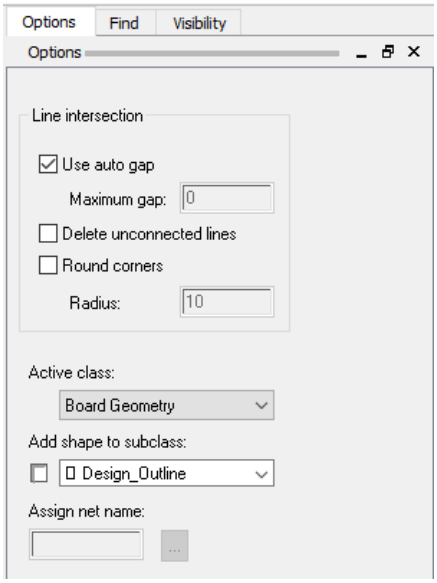
Move Outline to Design_Outline layer

5. Before the next steps, you should turn off all layers except **Board_Geometry – Design_Outline** and **Board_Geometry – DXF_In** and set different colors for them.

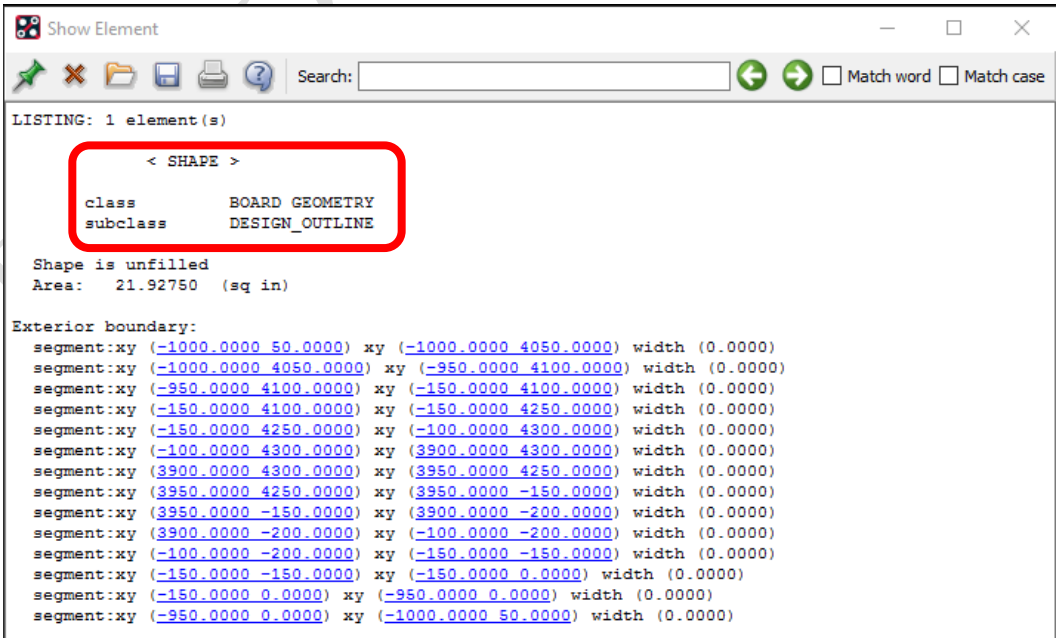


Since the board outline came in as lines and lines are not allowed on the Design_Outline layer, we will need to change it to a closed shape as well as move it from the DXF_In layer to the Design_Oultine layer.

6. Select ***Shape – Compose Shape*** from the top menu.
7. In the Options tab of the Control Panel, set the **Active class** field to ***Board Geometry*** and the **Add shape to subclass** field to ***Design_Outline*** as you see below.



8. Window select around the entire board outline.
9. Click **RMB** and select ***Done*** from the popup menu.
10. Now, select ***Display – Element*** from the top menu and click on the board outline. You should see that the outline is now a shape and is on the **Board_Geometry – Design_Outline** layer.



Adding Tooling Holes

In this part of the lab, you will add three holes. To define these tooling/mounting holes within a mechanical symbol drawing, you must add them as pins (padstacks).

1. In the ***Visibility*** tab of the ***Control Panel*** turn Global Visibility ***On***.
2. Select ***Layout - Pins*** from the top menu or select the ***Add Pin icon***.

The ***Options*** tab of the ***Control Panel*** displays fields for adding pins.

3. In the ***Options*** tab, click the ***Browse*** button in the Padstack field, and from that form select: ***Hole110***
   This is the padstack that will represent the mounting holes on this board.
4. Select ***OK*** from the padstack form.
   The Symbol Editor's command area states:

   ```
   Using 'HOLE110 pad'
   ```

   The hole110 padstack is now attached to your cursor.

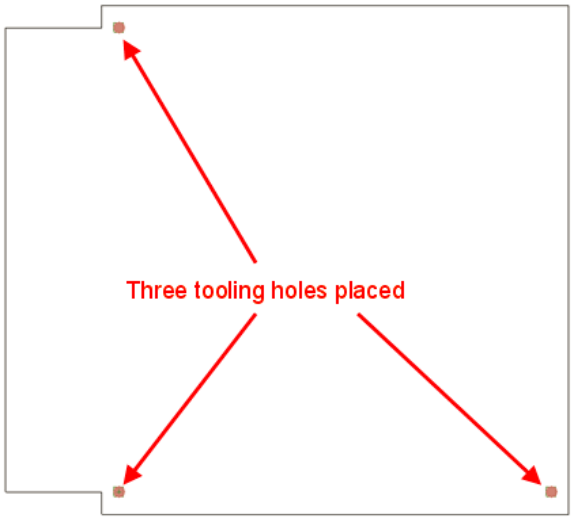
As indicated in the mechanical drawing at the beginning of this lab, the datum (0,0) point for this outline is the center of the lower left mounting hole. We will type absolute coordinates below into the command line to add the mounting holes.

5. At the ***Symbol Editor's command line*** enter:

   ```
   x 0 0
   x 3800 0
   x 0 4100
   ```

6. Right-click and choose ***"Done"*** from the RMB pop-up menu.

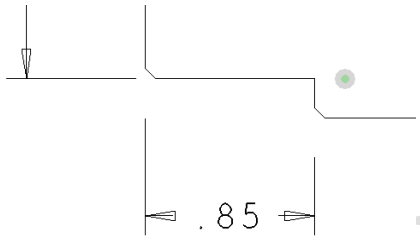
   Three tooling holes are now placed within the board outline. Your outline should look like the figure shown.



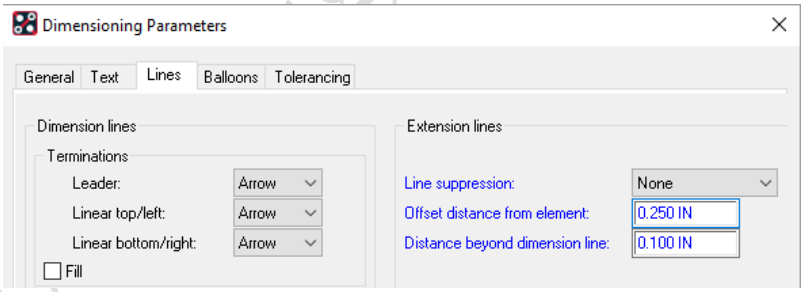
Adding Linear Dimensions

We will now add the dimensions for the mounting holes.

To ensure extension lines don't run into each other (extension lines are the ones that contain the dimension value in the example shown), you first need to set dimension parameters, then add the linear dimensions.



1. From the top menu choose ***Dimension - Dimension Environment***.
2. Move your cursor into the workspace and from a ***Right-Mouse-Button*** pop-up menu select ***Parameters***.
   The ***Dimensioning Parameters*** dialog box appears.
3. Click on the ***Lines*** tab and complete the ***Extension lines*** option as shown in the figure.



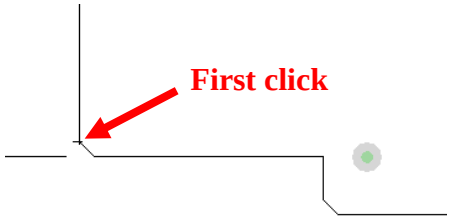
4. Select ***OK*** to apply parameters and close the ***Dimensioning Parameters*** form.
5. Pan to view the bottom half of the board, then from the ***Right-Mouse-Button*** pop-up menu select the ***Linear dimension*** option.
   The message window prompts you to "`Pick a point or element to dimension`". Notice that in the ***Options*** tab the Active Class changed to ***BOARD GEOMETRY*** and the Active Subclass changed ***DIMENSION***.

Note You may want to set the color of the DIMENSION subclass to yellow or some other bright color in the Color Dialog form.

6. Click at the vertex point where the long left vertical edge of the outline meets the chamfer, as shown below.

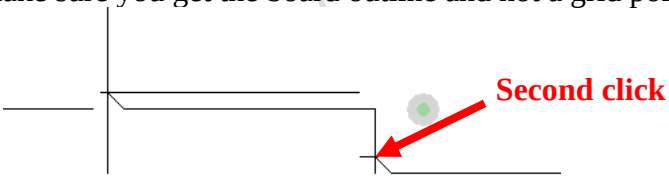
Note As long as you click *within* a grid point spacing of a vertex, dimensioning will snap to the vertex. If you click more than a grid point spacing away from a vertex, PCB Editor assumes you want to dimension the *entire* segment between vertices.

A marker is placed at the vertex on the left edge, as shown.



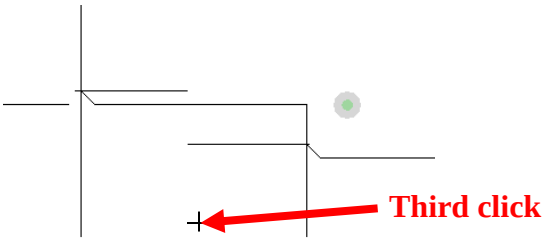
The message window prompts you to pick a second point for the dimension value.

7. Next, click on the vertex at the end of the short line before the chamfer. You may want to zoom in to make sure you get the board outline and not a grid point.



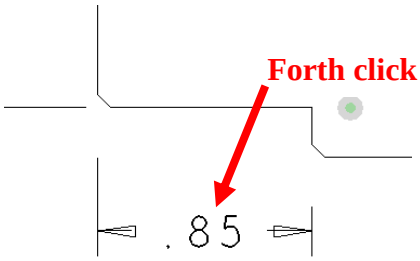
The message prompts you to indicate the X or Y direction next. This is the direction in which you want to have the dimension extension lines.

8. To direct the dimension X or Y, move your cursor down and to the left, to a location outside the board outline and centered between the two vertical lines of the outline, as indicated in the figure below, and click.

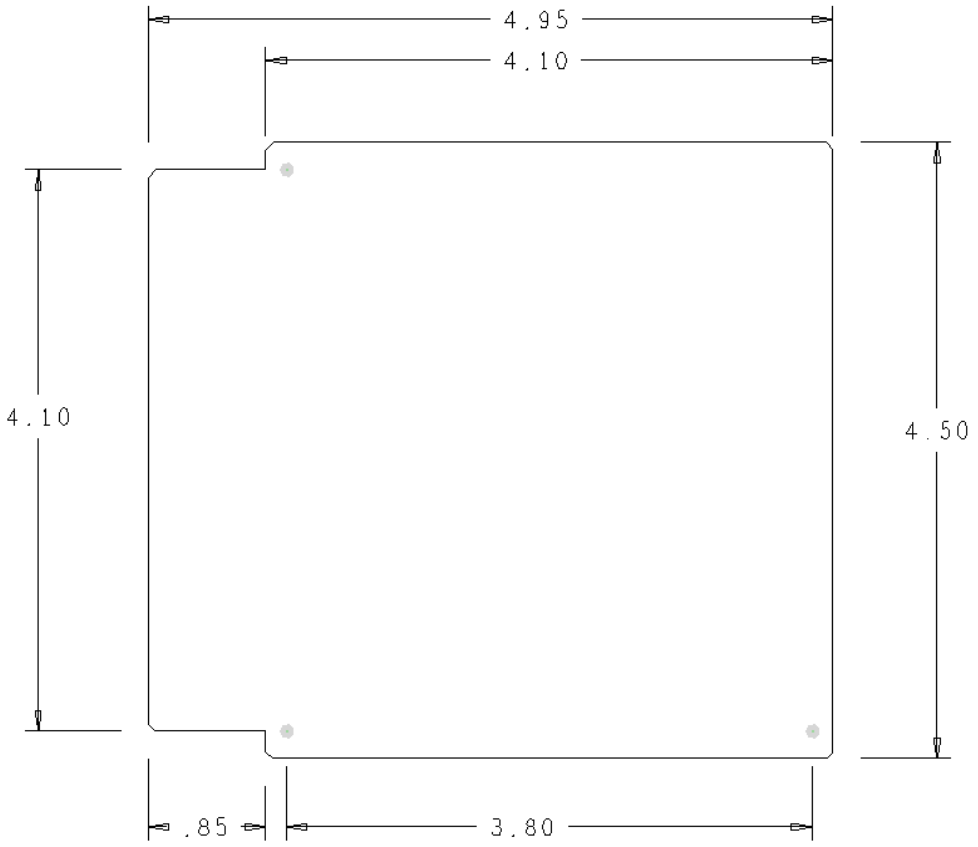


As you do so, notice the extension lines and dimension highlighted. When you click, the value .85 is automatically calculated and appears.

9. Click to place the dimension.
   The dimension .85 inches, with arrows to the left and right, is placed at the point where you have clicked.



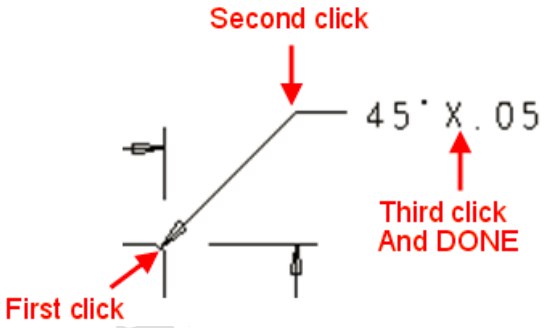
10. Now use Linear Dimension to dimension between the 2 lower mounting holes.



11. When you are finished, right-click and choose **"Done"** from the pop-up menu.

Dimensioning a Chamfer

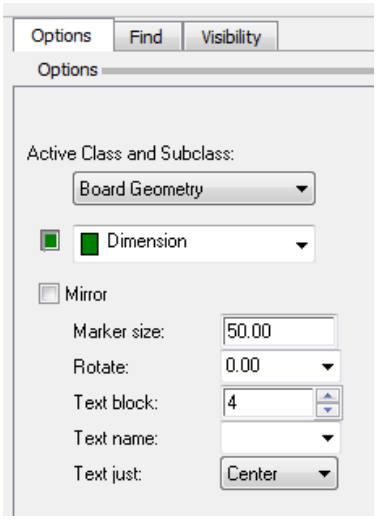
1. Zoom in to the chamfer at the upper right corner.
2. Choose the ***Dimension - Dimension Environment.***
3. Move your cursor into the workspace and from a ***Right-Mouse-Button*** pop-up menu select ***Chamfer leader***.
4. Click on the 45-degree chamfer line.
   The dimension text is attached to your cursor. (See example below.)
5. Pull the cursor up and to the right, then click to create a leader line.
   The leader line is the line between the dimension text and the 45-degree chamfer. Be sure to pull the text away from corners on the leader line. The line is automatically shortened by half the width of the text.
6. Right-click and choose **"*Done*"**.
   Your chamfer dimension should look like the figure below.



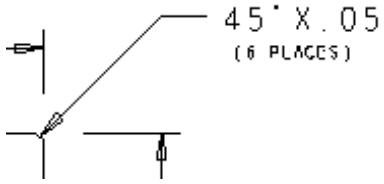
Note Your last click will determine the position of the text in relationship to the chamfer leader.

7. To place the final note text specifying the number of chamfers on the board, choose the ***Add - Text*** menu item.
8. In the ***Options*** tab of the Control Panel, fill in the text parameters to match those in the figure:

   Pay close attention to the command line for prompts as to which action to perform.



9. Place the text as shown in the figure, then right-click and choose **"*Done*"** from the popup menu.

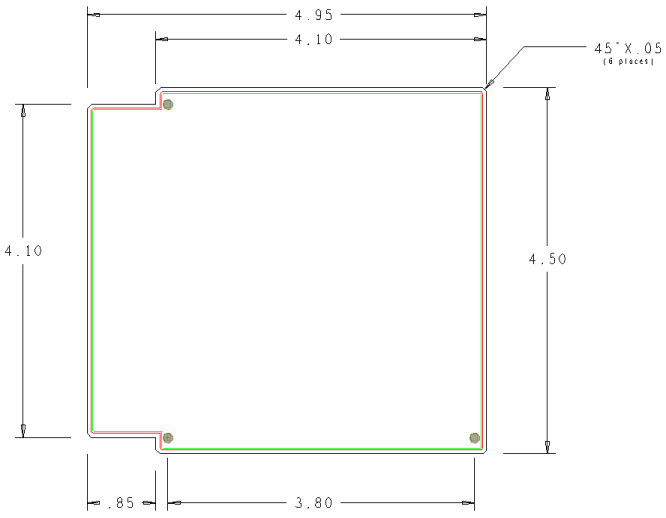


Note You can view the "Drafting and Dimensioning" section of the online help files for more information about this and related topics.

Adding Placement and Routing Keepin Areas

In this part of the lab, you will create package and route keepin areas to define the available board areas that you can use for part placement and signal routing.

1. Use ***Display - Zoom - Fit*** to view the entire board.
2. Choose ***Edit - Z-Copy Shape*** from the top menu.
3. In the ***Options*** tab, set your Active Class to ***PACKAGE KEEPIN*** and Subclass to ***ALL***.
   The message window now prompts you to enter a selection point.
4. Under ***Shape Options***, set the ***Offset*** to ***70*** and enable the **Contract** option.
5. Select on the board outline.
   A package keepin is drawn 70 mils inside the boundary of the board outline.
6. In the ***Options*** tab, set the Active Class to **ROUTE KEEPIN** and Subclass to ***ALL***.
7. Under ***Shape Options***, set the ***Offse***t to ***50*** and make sure the ***Contract*** option is enabled.
8. Select a point on the board outline.
   A route keepin is drawn 50 mils inside the boundary of the board outline. Your board outline should resemble the figure to the right.
9. Right-click and choose **"*Done*"**.



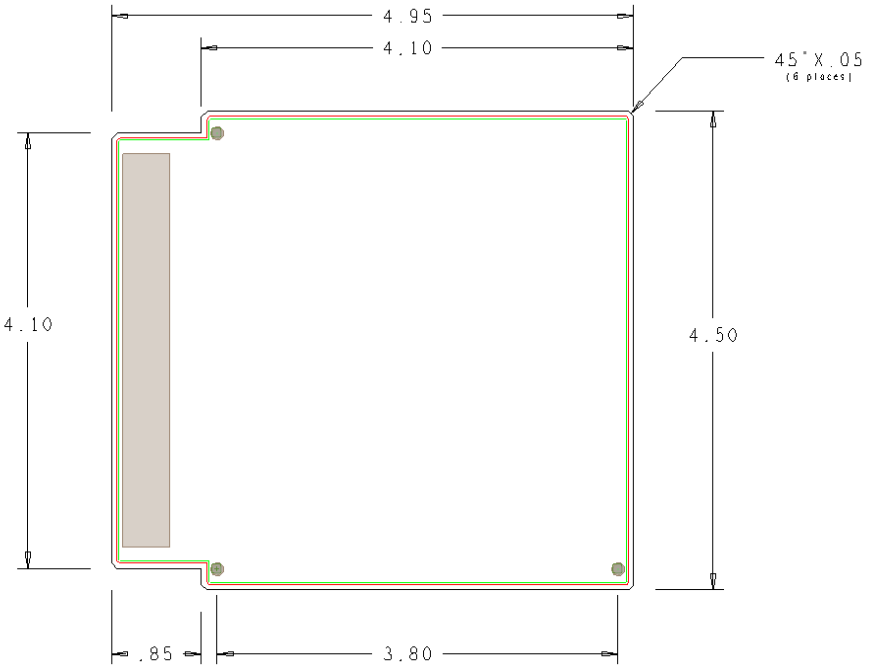
Adding a Via Keepout Area

In this design, you will create a via keepout area to prevent vias from being routed in the region of the plug-in connector. We will type absolute (x) and relative (ix & iy) coordinates into the command line to create the via keepout.

1. Choose ***Setup - Areas - Via Keepout*** from the top menu.
   The Symbol Editor's command area prompts you to enter a shape outline.
2. In the ***Options*** tab, set the ***Segment Type*** option to ***Line Orthogonal***.
   This will add only horizontal and vertical line segments.
3. At the Symbol Editor's command line, enter each of the following sets of values:

```
x -900 200
iy 3700
ix 450
iy -3700
```

4. Right-click and choose **"*Done*"** from the pop-up menu.
   The polygon fills and closes automatically. The complete board outline is shown in the figure.



Note The PCB Editor tool considers keepout areas as filled shapes. When you choose "*Done*", the tool creates a shape boundary line from your last specified point back to the start point (in order to automatically close the polygon).

Creating the Mechanical Symbol and Drawing Files

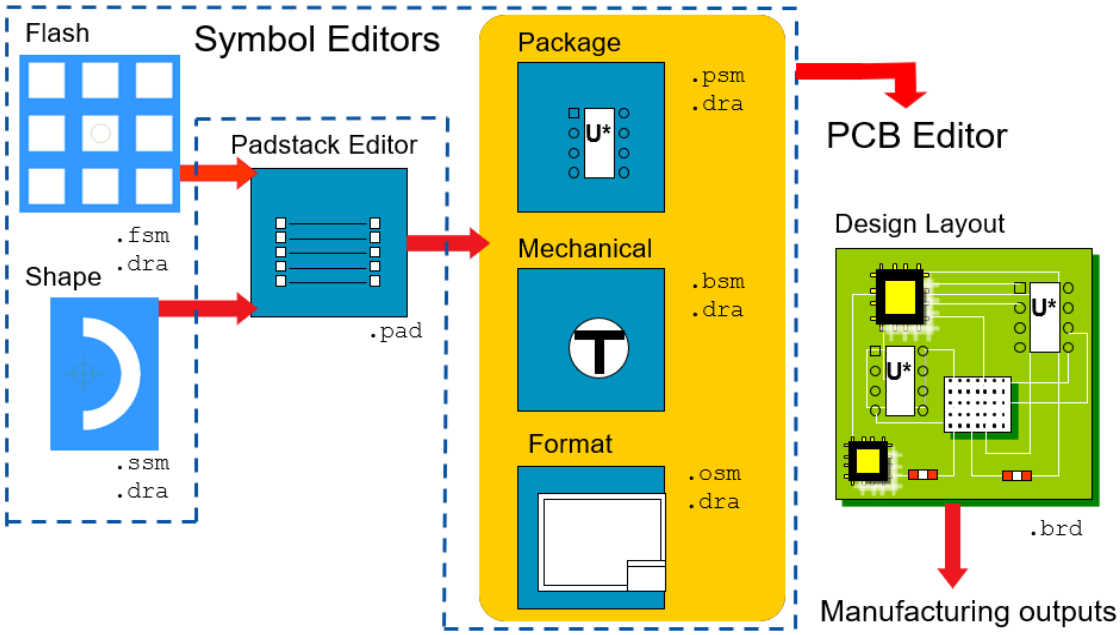
1. Choose ***File - Save*** from the top menu.

The system saves an `outline.dra` file. This file is used if you ever need to edit the graphics for this symbol. You can choose to store this drawing file in a library.

It also executes the **Create Symbol** command, creating a mechanical symbol `outline.bsm`. This file is used in the design process during the building of the board design file.

End of Lab

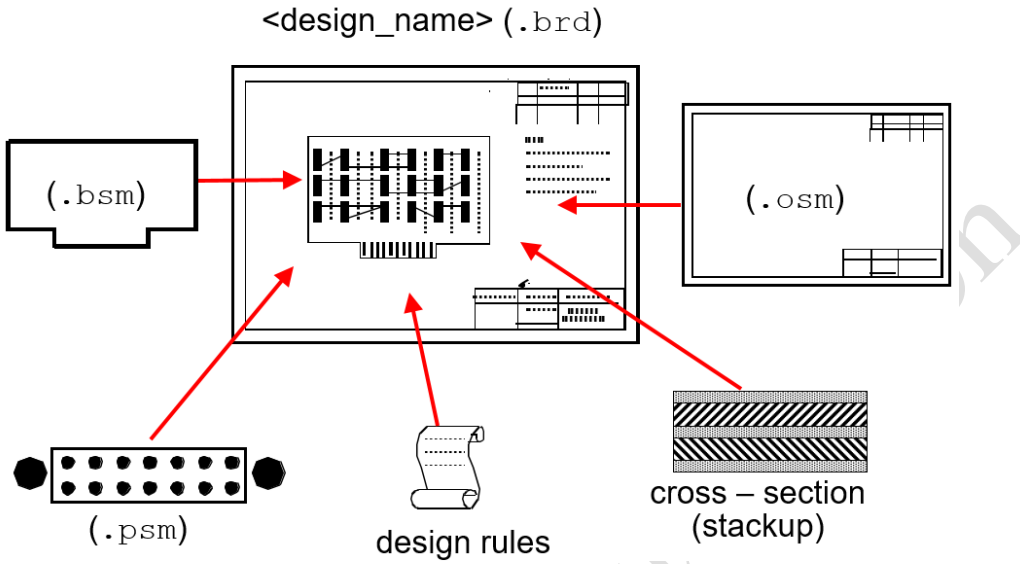
PCB Editors – Flow Overview



Now that we have completed creating library files, let us take a look at this flow overview of the PCB Editors. As you can see, the flow of the work is pretty straightforward. First, you create the flashes or shapes that will be added to the padstacks. Second, you define the padstack in the Padstack Editor adding the flash or shape symbols, as needed.

The Package, Mechanical and Format symbols are then created in their respective editors. Those symbols are added to the resulting board design, either through a netlist or by placing the symbols from the library. All data finally gets processed when it is time to produce the manufacturing outputs.

Creating a Template Design File



When you have the same basic board used many times, it is common to build a Template design file as a starting point. The Template design file may have the board outline placed, the cross section defined, the design rules set, and optionally may have common components such as connectors already placed. The Template design file is simply a board file that is saved in a library so that it may be used as a starting point for multiple designs. Using this method saves time and ensures the accuracy of the design.

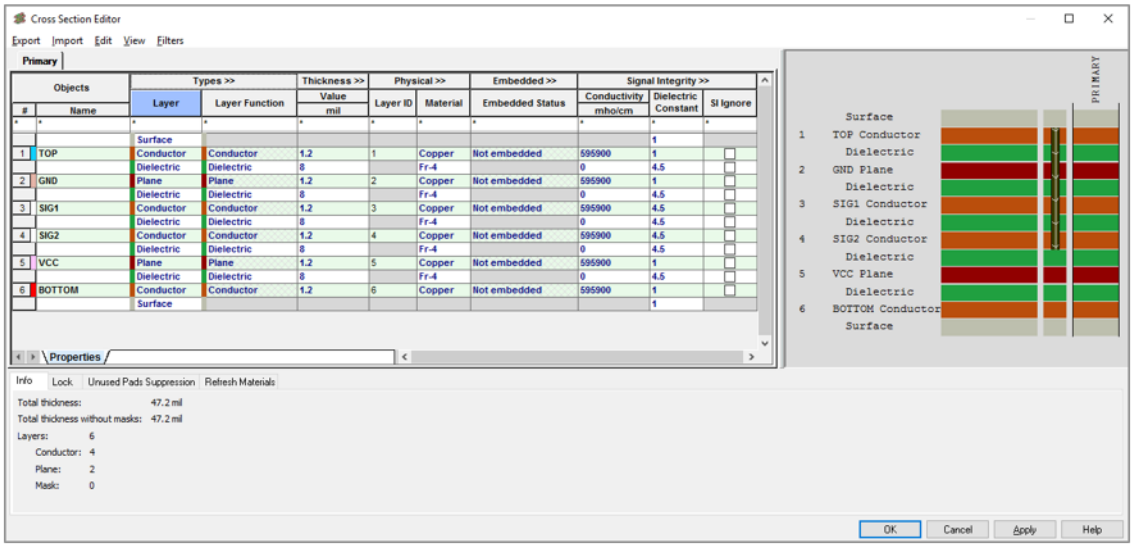
The PCB Editor's design database is created and saved in a design file format known as a board, or `.brd` file. It can be created initially as a mechanically correct (but logically non-intelligent) starting point for all designs using the same physical board configuration. Schematic connectivity information is imported later.

There are advantages to creating a template design file. First, it ensures that all physical layouts with a common geometry start from information that has been thoroughly checked and approved. Second, it provides a way to control the consistency of the end product (for example, drawing formats, fab and assembly notes, drawing size and accuracy settings, and datum points). Third, you can read a "technology file" into this template design to establish the board cross section information and design rules (spacing and physical rule sets).

Use the ***Place – Components Manually*** command to insert package, mechanical, and format symbols into the design database.

Defining Layer Stackup

Setup – Cross-Section … or



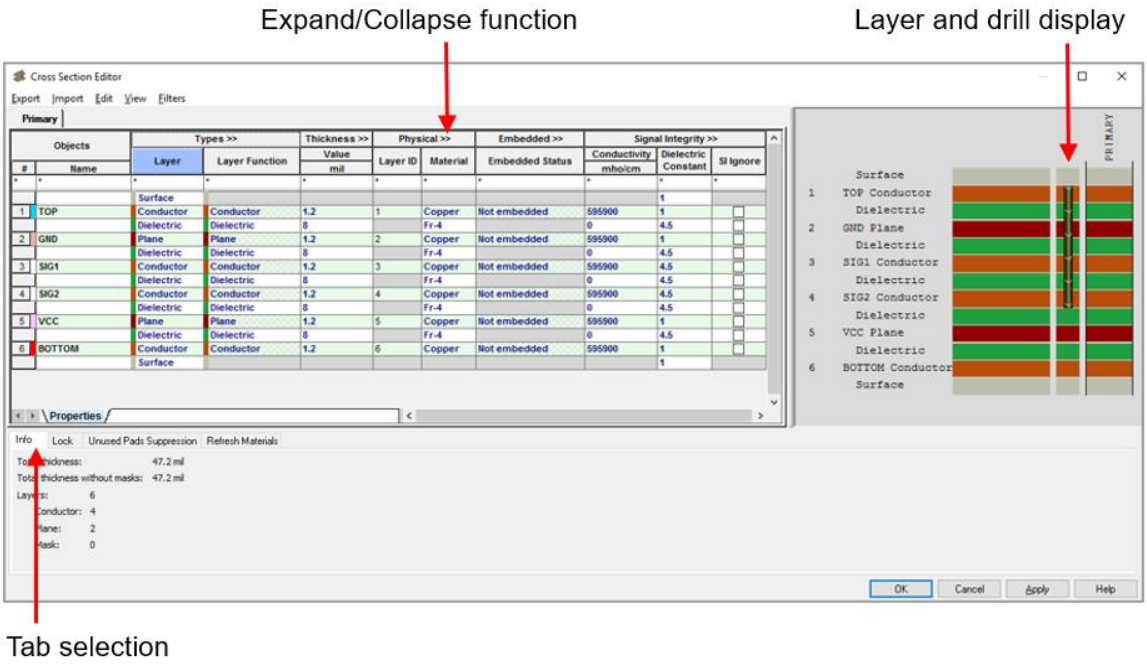
The ***Setup - Cross-section*** command opens the ***Cross Section Editor***. The Cross-Section Editor has been designed leveraging the underlying spreadsheet technology found in the Constraint Manager. It supports features that require the cross section for its setup.

A graphical image of the stackup construct is available in a dock-able window. Basic editing environments include functionality to add layer pairs or a user defined number of layers.

Additional features include;

- Positive/negative tolerance support for each layer
- Controls to prevent editing of layers or values
- Locking of via spans
- Layer type hierarchy
- IPC-2581 defined layer functions

Cross Section – Default View



The default view combines the spreadsheet grid with the stackup viewer. The drill display within the viewer is based on actual padstack usage in the design's database. Vias in Physical Constraint Sets that are unused do not contribute to the display.

Columns by default are collapsed; click the ">>" to expand each column.
Click "<<" to collapse or compress the amount of information shown in the display.

The Layer Types section defines the Layer Function, Manufacture, and Constraints.

- Manufacture - Assigns hierarchical names to signal and plane layers; example INNER_SIGNAL, PLANE. This information is supported in the IPC-2581 schema
- Constraint – Assigns hierarchical names to signal and plane layers similar to the "Manufacture" column, however, their names are integrated into Spacing Constraint set structures and provide the opportunity to manage CSet hierarchy.

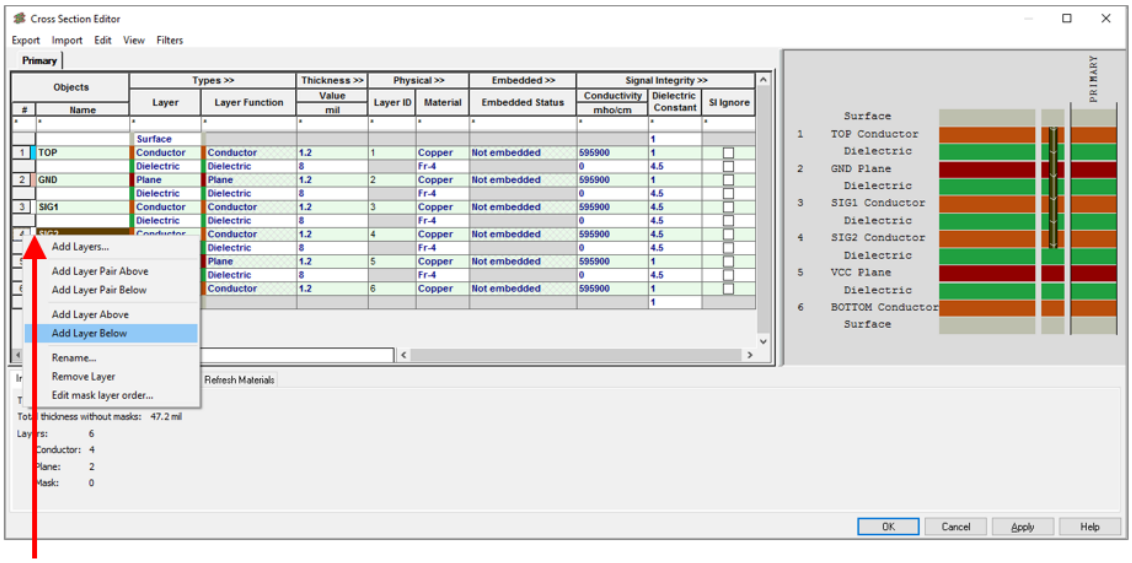
The Thickness section allows the ability to include the 'Plus' and 'Minus' tolerance ranges to the thickness values.

The Physical section defines the layer ID and material specified for the layer. It also includes the ability to set the layers to negative artwork and whether to designate "Unused Pad suppression" for internal layers.

There are five functional tabs located near the bottom of the spreadsheet:

- Info – Displays total thickness and number of layers (Etch + Plane)
- Lock – Prevents editing within the spreadsheet in terms of adding layers or changing values
- Embedded layers Setup – Setup form for Embedded Component Design (requires Miniaturization product option)
- Unused Pads Suppression – Setup form for Unused Pad Suppression
- Refresh Materials – Used to refresh parameters from the materials.dat file

Cross Section – Adding/Removing Layers



Right-Mouse-Button in row provides add/remove and rename layer capability

Selecting a row in the number (#) column with your Right-Mouse-Button allows you to add new layers, remove layers, and rename a layer.

- Add layers - Allows you to add Dielectric layers or Mask layers above the surface layers.
- Add Layer Pair Above and Add Layer Pair Below – Allows you to add two layers at a time either above or below an Etch or Dielectric layer. Has to be between the Top and Bottom layers
- Add Layer Above and Add Layer Below – Allows you to add a single Etch or Dielectric layer
- Rename – Allows you to rename a layer
- Remove Layer – Allows you to remove an Etch or Dielectric layer. The etch layer cannot have anything placed or drawn on the layer being removed

Lab

Lab 5-2: Creating a Template Design (.brd)

- Set drawing parameters
- Place the mechanical symbol
- Add format symbols
- Add package symbols
- Set color and visibility
- Define the cross section (layer stackup)
- Save your board template

The following lab will allow you to familiarize yourself with the process required to create a templet design file. Items covered include placing the board mechanical symbol, adding common footprints, defining the cross section, and so on.

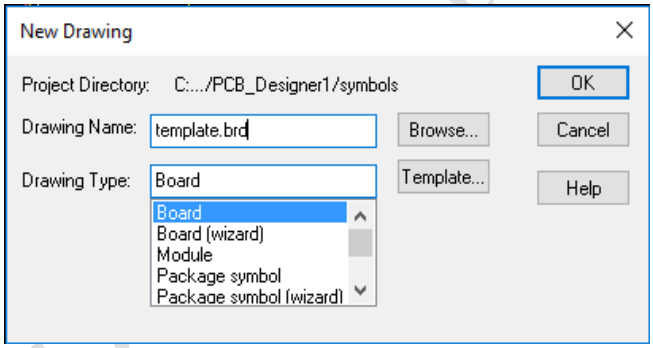
Lab 5-2: Creating a Template Design (.brd)

Objective: Use the PCB Editor to create a design template.

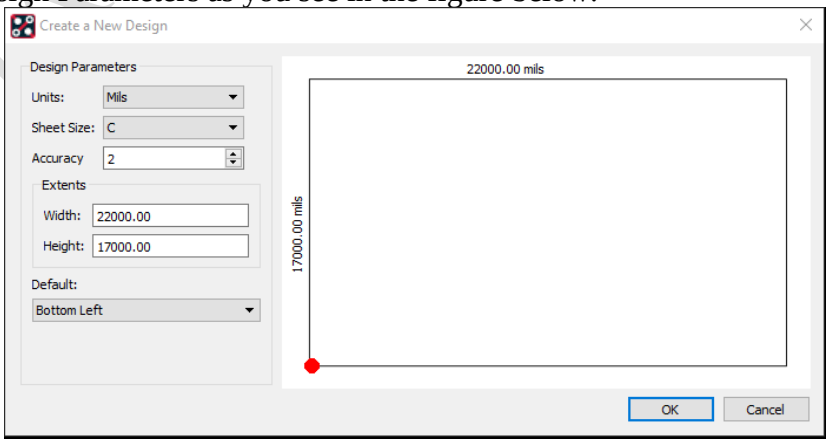
In this lab, you will create an PCB Editor design (`.brd`) file. This design file will contain only mechanical data; no logical (schematic) data will be imported.

This design file serves as a template, or starting point, for all layouts that require the same mechanical specifications. This ensures that all physical layouts with a common geometry start from a mechanical template that has been thoroughly checked and approved for use.

1. Choose ***File - New*** from the top menu.
2. Select ***No*** to not save the changes just made.
   The ***New Drawing*** dialog box appears.
3. Select ***Board*** for the ***Drawing Type*** and type `template.brd` in the **Drawing Name** field.



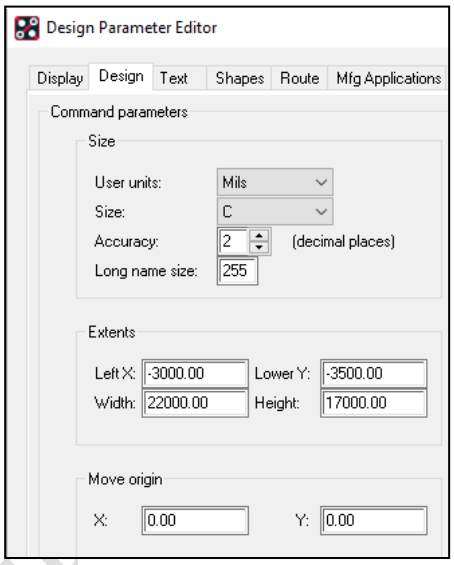
4. Click ***OK*** to close the ***New Drawing*** dialog box.
   The Create a New Design window appears
5. Set the Design Parameters as you see in the figure below.



6. Click OK to accept the settings and dismiss the form.

Setting Drawing Parameters

All designs created from this mechanical template will have the same drawing size, accuracy, and datum point.

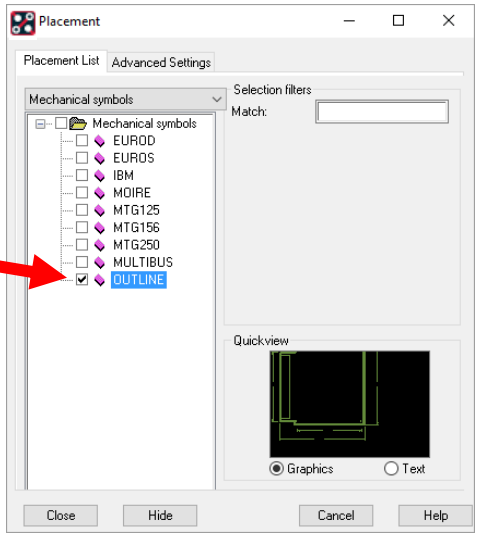


1. Choose ***Setup - Design Parameters***.
2. In the ***Design Parameters Editor*** select the ***Design*** tab.
3. Change the settings to match those in the figure shown below to the right.
   These settings cause the drawing origin to be placed 3.50 inches up and 3.00 inches to the right of the lower left corner of the drawing.
4. Click ***OK*** to close the ***Design Parameters Editor*** form.

Adding the Mechanical Symbol

1. Choose ***Place – Components Manually*** from the top menu.
   The ***Placement*** dialog box appears.
2. In the ***Advanced Settings*** tab and enable both the ***Database*** and ***Library*** options under the "***Display definitions from:***" option.
3. In the ***Placement List*** tab, select the ***Mechanical symbols*** option with the scroll down arrow.

Note: Make sure you check the box to select the outline symbol.



Notice the graphics representation displayed in the Quickview window. This is the `outline.bsm` symbol you completed in previous labs.

4. Click the ***Hide*** button at the bottom of the ***Placement*** form.
   The mechanical symbol is attached to your cursor and the Placement form disappears.
5. At the ***PCB Editor's command line***, enter: ***`x 0 0`***

The outline is placed at the drawing origin.

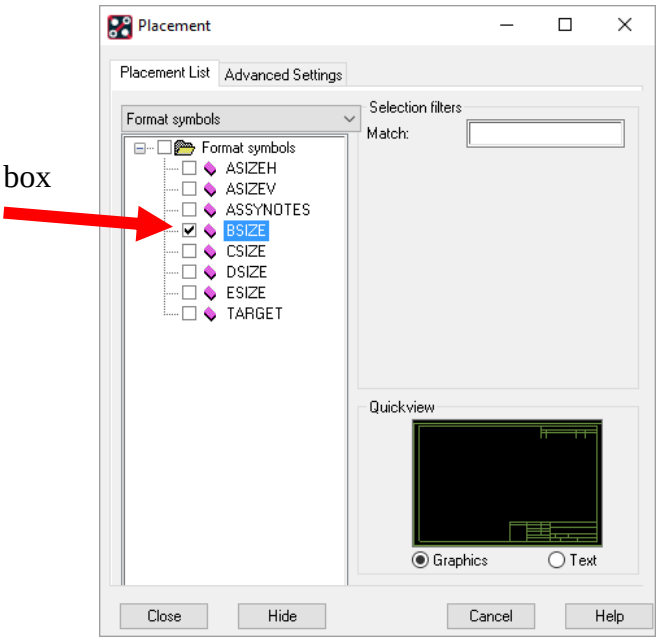
6. Right-click and choose **"*Done*"** from the pop-up menu.
   You will now verify that you have actually placed the same *outline.bsm* symbol that you created.
7. Zoom out to view the entire design, including the dimensions and text.
8. Click the ***Color192*** icon, and under the ***Geometry*** category, toggle the ***Board Geometry*** class ***Dimension*** subclass off.
9. Select ***OK*** to close the ***Color Dialog*** form.
   The dimension text disappears, but the board outline remains visible.

Adding Format Symbols

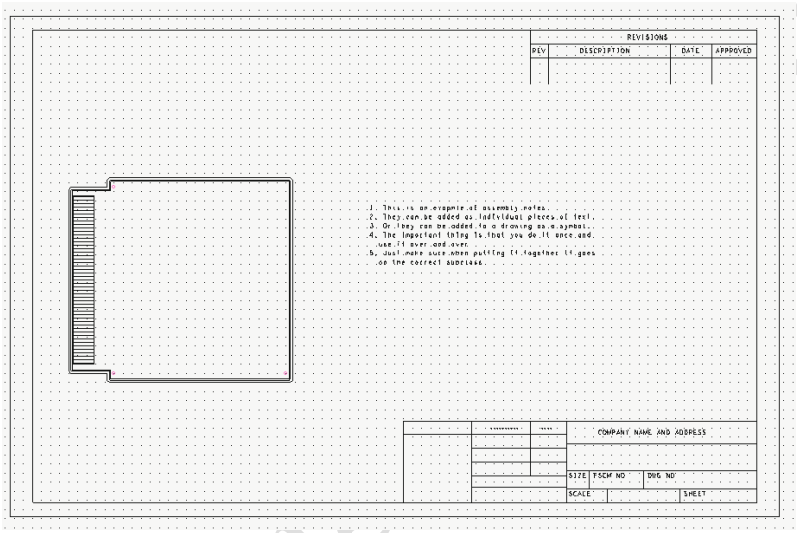
In this part of the lab, you will add a drawing format and fabrication notes.

1. Choose ***Display – Zoom – World*** from the top menu.
   The display area will change to the size of your C Size work area.
2. Choose ***Place – Components Manuall***y from the top menu.
   The ***Placement*** dialog box appears.
3. Click the ***Advanced Setting***s tab and enable the ***Autohide*** option.
   This will automatically hide the Placement form while you are placing a symbol.
4. Click the ***Placement Lis***t tab and select ***Format symbols*** with the scroll down arrow.
   A list of format symbols appears in the dialog box.
5. Click the symbol name ***BSIZE*** in the list, as shown in the figure.
   The format symbol, which is a B size, horizontal drawing format, is now attached to your cursor.

Note: Make sure you check the box to select the BSIZE symbol.



6. Click to place the drawing format in the lower left corner of the design area.
   The board should be surrounded by the drawing format outline but leave some space to the right of the board outline, as shown in the figure below.
7. To add notes, in the ***Placement List*** tab, enable the check box next to the name for the ***ASSYNOTES*** symbol.
8. Click to place the notes where you want them (on the right side of the board outline, within the format borders), as shown in the figure.



Adding Package Symbols

You can add any mechanically constrained devices that are common to all designs. By placing these into a template file, you ensure a consistent level of accuracy, which helps reduce error checking and corrections. Types of devices that should be preplaced in a template design `.brd` file include connectors, LEDs, switches, and any standard part that has a fixed placement.

1. Select ***Package symbols*** with the scroll down arrow in the ***Placement List***.
2. Scroll through the list of library symbols and enable the check box next to the symbol ***DIN64***.
   This is a 64-pin connector symbol. When you move your cursor into the PCB Editor workspace, a connector symbol is attached to your cursor.
3. At the ***PCB Editor's command line*** enter: ***`x -700 500`***
4. Right-click and choose **"*Done*"** from the pop-up menu
   The connector is placed.
5. Zoom in to the lower left corner of the connector area.

Since a template design file is simply a mechanical template with no logical (schematic) database, the edge connector you placed has a generic reference designator (**J***).

6. Choose ***Display - Zoom - Fit*** from the top menu to see the entire board.
7. Select the ***Place – Components Manually command*** to get back into the placement mode.
8. Click the ***Advanced Settings*** tab and ***Disable*** the ***Autonext*** option.
9. Click the ***Placement List*** tab.
10. If it is not the current selection, select the ***Package symbols*** option with the scroll down arrow.
11. Scroll through the list of available package symbols and enable the check box next to the symbol ***BNC***.
12. At the ***PCB Editor command line***, enter the following coordinates:

    ```
    x 3700 350
    x 3700 1150
    ```

    Both BNC connectors are placed on the right edge of the board.
13. Right-click and choose **"*Done*"** from the pop-up menu.

Setting Color and Visibility

In Lesson 2, you exported a color layer parameter (color.prm) file that sets color and visibility for various layers of a drawing. You will use that parameters file now.

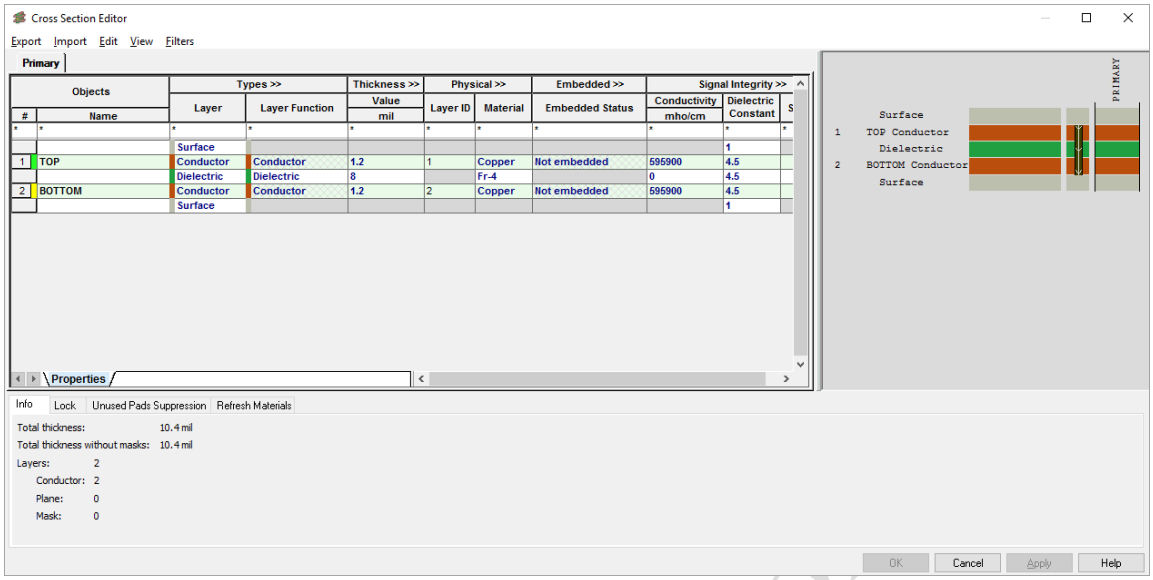
1. Select ***Import – Color/Board Parameters*** from the top menu
   The **Input Parameters File** form appears
2. Click the **…** button and browse to the ***color.prm*** file we created earlier
   Notice that the drawing format, assembly notes, and board dimensions have been turned off, leaving just the board elements on.
3. Choose ***Display - Zoom - Fit*** from the top menu to zoom in around the board outline.

Defining the Cross Section (Layer Stackup)

By default, all new design files are created with just two layers, top and bottom. In this part of the lab, you will learn how to add more layers to the stackup.

1. Choose ***Setup - Cross-Section*** from the top menu.
   The ***Cross-section Editor*** form appears.

Notice that a TOP and BOTTOM layers are already defined as conductor layers.



2. Click on the number 2 (the BOTTOM layer) with the ***Right-Mouse-Button*** and select **Add Layer Above**.
3. Repeat step two 3 more times so that there are ***5 DIELECTRIC*** layers in between TOP and BOTTOM.
4. Set up your stackup layer names and layer type to match the layer specifications shown in the figure below.
   Note that the number associated with the bottom layer will change each time you apply a layer name between the TOP and BOTTOM layers.

Objects		Types >>		Thickness >>
#	Name	Layer	Layer Function	Value mil
*	*	*	*	*
		Surface		
1	TOP	Conductor	Conductor	1.2
		Dielectric	Dielectric	8
2	GND	Plane	Plane	1.2
		Dielectric	Dielectric	8
3	VCC	Plane	Plane	1.2
		Dielectric	Dielectric	8
4	BOTTOM	Conductor	Conductor	1.2
		Surface		

In this template design file, you have added a power and a ground plane. All designs created from this mechanical template would start as 4-layer boards.

5. Click the ***OK*** button to accept the changes and close the ***Cross Section Editor***.

Saving Your Board Template

You have learned how to add internal plane and wiring layers. You can now save the board template, so it can be used again and again.

Important

It is necessary, at this time, to save your `template.brd` file in the directory where you will be working while designing the board. Be aware of which schematic capture tool you're typically working with. This will determine where you will be performing your work in the upcoming labs.

1. Choose ***File - Save As*** from the top menu.
   A ***Save As*** browser window opens.
2. Navigate to your ***new*** working directory ***project2\allegro***.
3. Enable the ***Change Directory*** box if it is not currently enabled.
4. Click ***Save*** to save the `template.brd` file in the correct directory.
   The `template.brd` file is saved to disk. It is important to save the `.brd` to this directory and to use the Change Directory check box.
5. Choose ***File - Exit*** from the top menu to exit the PCB Editor software.
   You have completed the library development section of this course.

Note  Template files may be saved in your company's library directory.

End of Lab

Lesson 6: Importing Logic Information into PCB Editor

Note The labs in this lesson demonstrate how to bring logical data from the schematic capture environment into PCB Editor. In the logic import/export process from within the PCB Editor the Import Logic and Export Logic dialog forms denote the logic type as Design Entry CIS (Capture). The Design Entry CIS (alias DE CIS) encompasses the OrCAD Capture, OrCAD Capture CIS, and Allegro Design Entry CIS products.

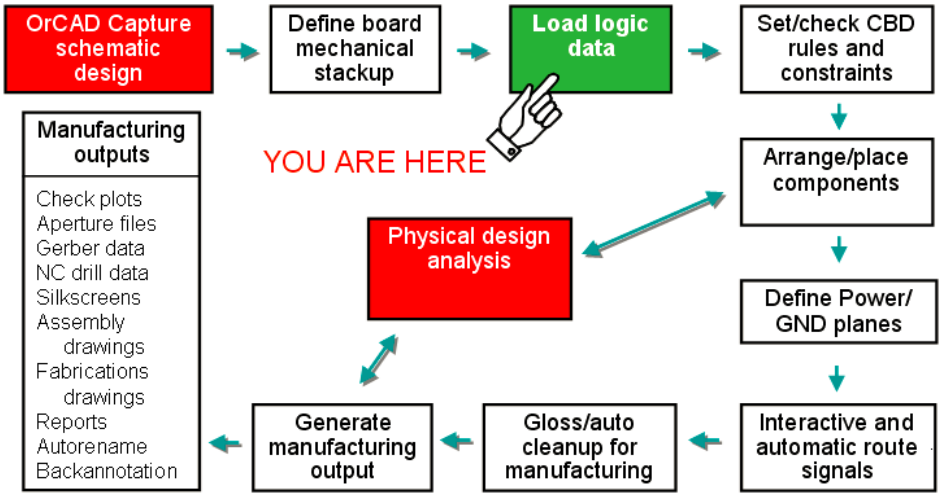
Learning Objectives

In this lesson, you will do the following:

- Working with logic information from a schematic tool, you will understand the key setup choices to be made when importing logic information into the PCB Editor layout environment
- The logic information can come from any one of these Design Entry schematic products
    - OrCAD Capture
    - OrCAD Capture CIS
    - Allegro Design Entry CIS (alias DE CIS)

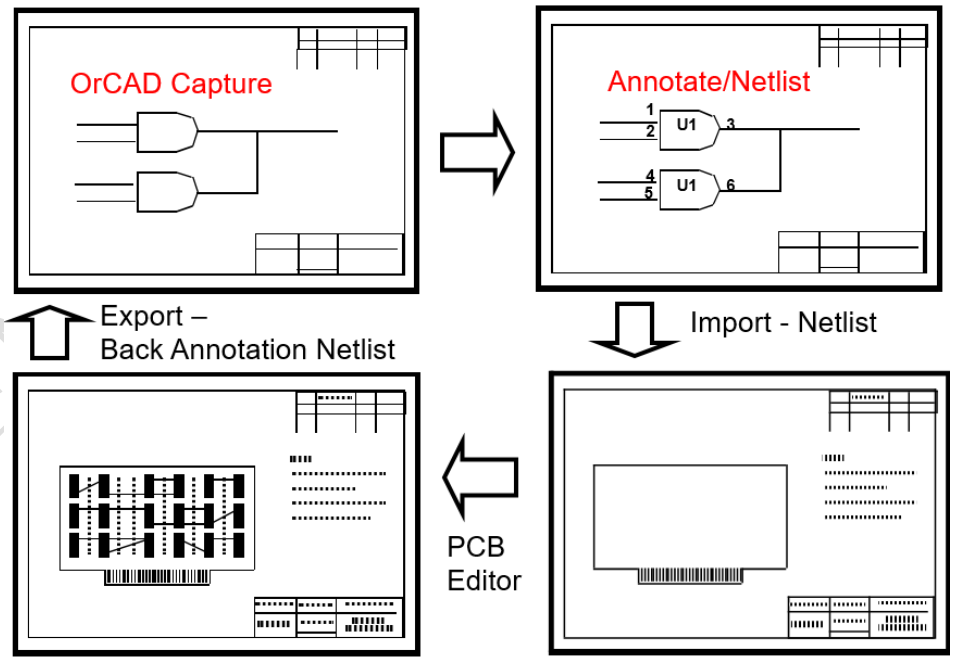
In this section, you will learn about Logic Import, which is the process of importing logic from your schematic capture tool into the PCB Editor database. You will learn how to import from the design entry schematic environment into the PCB Editor environment.

Design Layout Process



This design flow is used throughout the rest of this course. Each box in this flow represents a common step in the design of a printed circuit board. As indicated in the flow, the Load Logic Data box will now be discussed.

Integrating Logic Design with Physical Layout



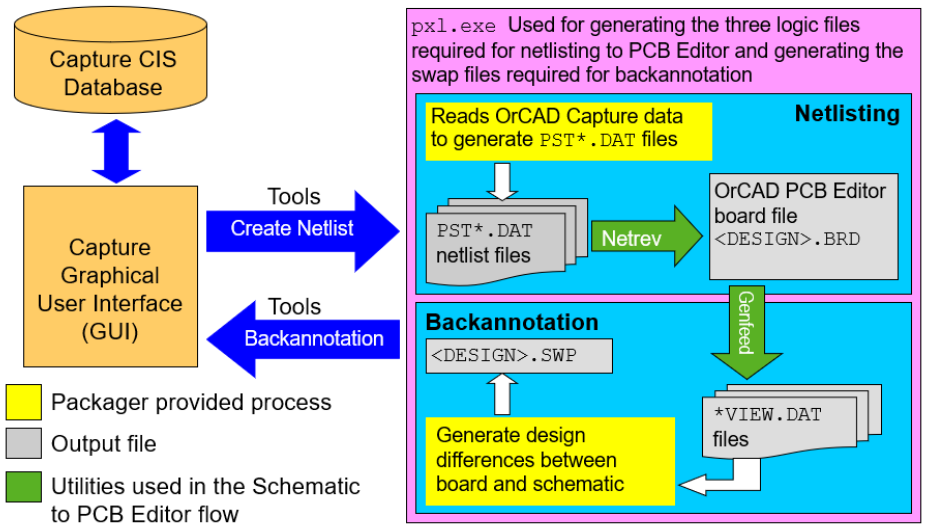
OrCAD Capture Front End

- **OrCAD Capture** - It is not recommended that the schematic design (.DSN) file and the PCB Editor board (.brd) file reside in the same directory. By default, the packager files are placed in a subdirectory named ***allegro***. It is assumed that the board (.brd) file will also reside there. The minimum values required for schematic part transfer are **Value**, **Class**, and **PCB Footprint** (package symbol).
- **Annotate** - The Annotate program maps the logic devices to physical packages, assigning a reference designator and physical pin numbers.
- **PCB Editor Packager** - The PCB Editor Packager creates the transfer files used by PCB Editor. As mentioned previously, these files are placed in the subdirectory named ***allegro*.**

PCB Editor

- **PCB Editor** - Used for component placement and routing; allows for pin and gate swapping for optimum routing results; generates manufacturing output.
- **Import Logic**: After this step has been completed, the design will contain all of the part and connection information.
- **Export Logic** - This program generates back-annotation files that the OrCAD Capture tools use to update the schematic.

OrCAD Capture and PCB Editor Interface Process

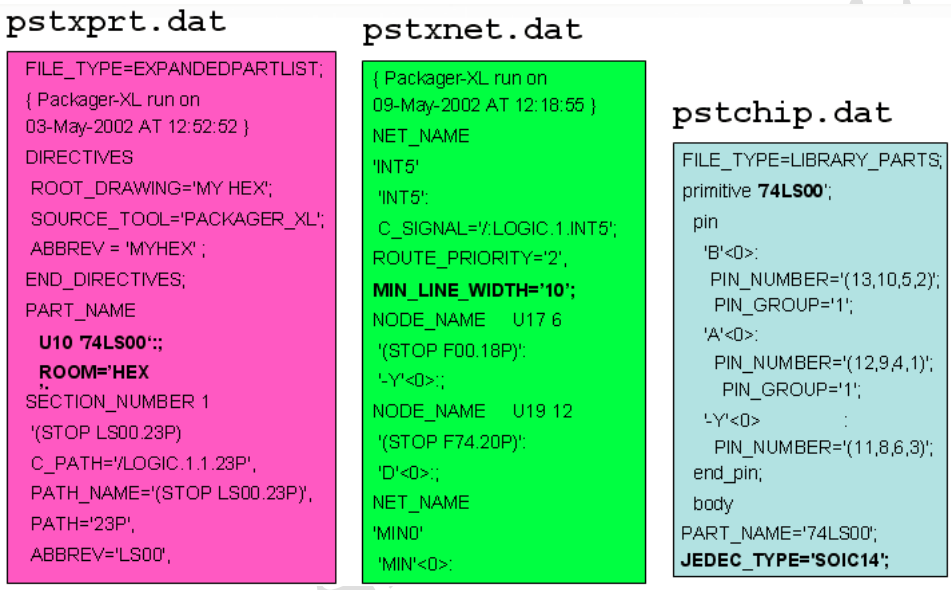


The PCB Editor Packager (pxl.exe) reads the OrCAD Capture database and creates three pst*.dat files. Then, the netrev program is used by PCB Editor to read in those pst*.dat file to create or update the .brd file.

For Backannotation, the PCB Editor program, genfeed is used to create the *view.dat files. These files are then read by packager, which in turn generates the swap file that is used to update the schematic to reflect any changes made to the design by PCB Editor, such as pin and gate swapping, reference designator renaming and property changes.

When you develop the OrCAD Capture schematic libraries, all parts must have a minimum of the following PCB Editor properties: **Class**, **Value**, and **Footprint**.

Transfer Files (pst.dat) – OrCAD Capture to PCB Editor*



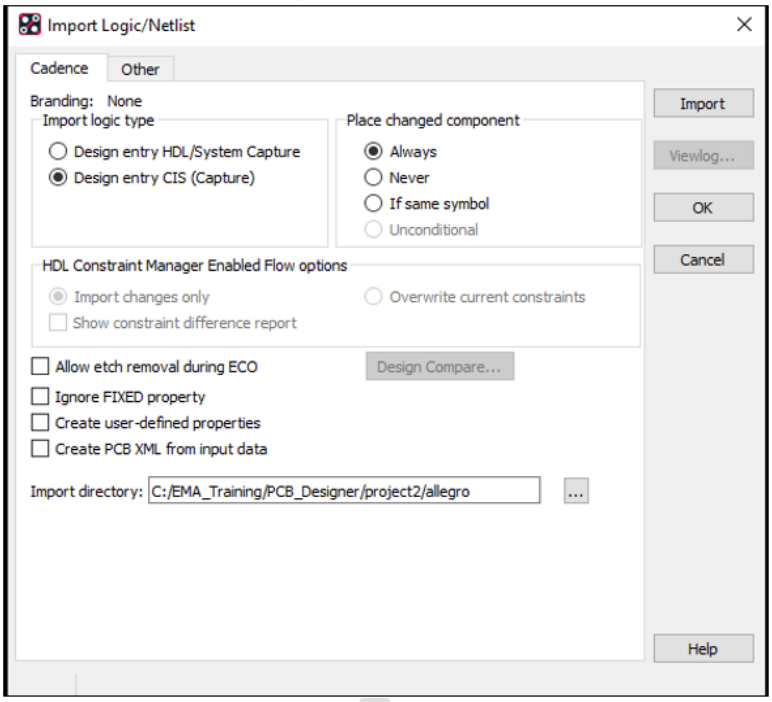
You use the OrCAD Capture Create Netlist command to generate the (pst*.dat) files from the schematic that will be imported into the PCB Editor design.

These files are:

- **pstxprt.dat** file: Parts list file that lists each physical package created by the packager along with its reference designator and device type. For packages composed of multiple sections, this file identifies each section along with their pin numbers. This file also contains any part properties, such as ROOM or VALUE.
- **pstxnet.dat** file: Netlist file that lists reference designators and pin numbers associated with each net in the schematic. This file also contains any net properties, such as ROUTE_PRIORITY or MIN_LINE_WIDTH.
- **pstchip.dat** file: Device definition file that contains electrical characteristics (i.e. pin direction and loading), logical-to-physical pin mapping and voltage requirements. It defines the number of sections in a part and any swapping information. It also contains the footprint (JEDEC_TYPE) and alternate footprint (ALT_SYMBOLS) information.

OrCAD Capture to PCB Editor Logic Import

Import - Netlist



After you have annotated your schematics, you must use the PCB Editor Packager to create the netlist input (*pst*.dat*) files for PCB Editor. In OrCAD Capture select the `<project>.dsn` file in the Project Manager. Using the ***Tools - Create Netlist*** command select the PCB Editor tab in the create netlist form to create the three *pst*.dat* files.

Use the ***Import - Netlist*** command from the top menu in PCB Editor and choose the Design entry CIS (Capture) option. Use the ***Import Directory*** field to point to the directory containing the three packager (pst*.dat) files created by the OrCAD Capture – Create Netlist program. By default, this would be the project's *allegro* directory.

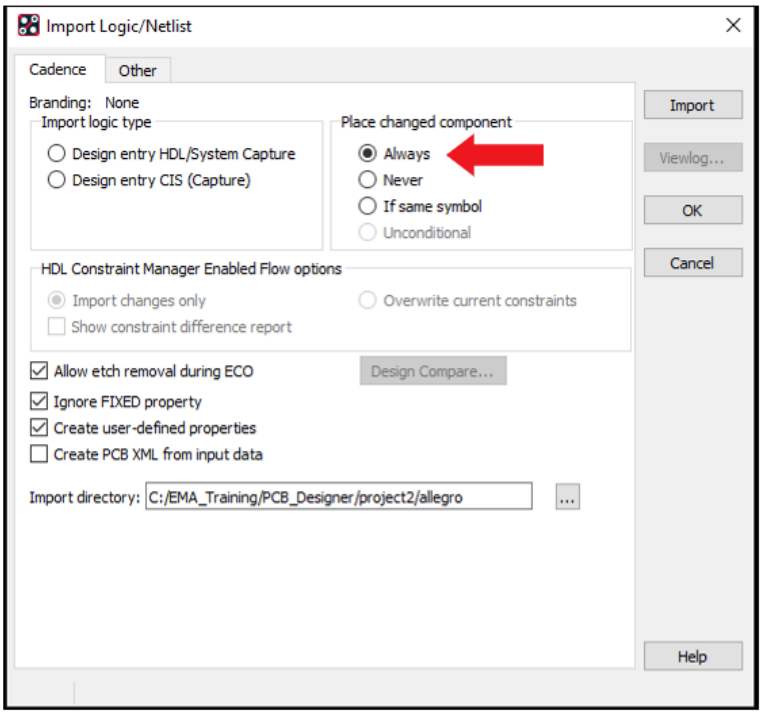
Properties are passed back and forth between these two tools as well. You define which property names are allowed to pass by listing in the `allegro.cfg` file located at *<cdsroot> - tools - capture*.

Engineering Changes – Placement and Routing

With an ongoing design, schematic changes (ECOs) are incorporated with the ***netrev*** process, which brings in the transfer files from the edited schematics. If the PCB Editor design has not been placed or routed, the new transfer files simply replace the original PCB Editor database. If placement and or routing has already occurred, you have several options on how the netrev process should proceed.

Place Changed Component

This section of the Import Logic determines how placed parts are treated in the ECO process. When a part in an edited schematic has a reference designator that matches a placed part in the board layout, parts are compared to determine if there are any changes. If the part has not changed, it maintains its location in the board layout. If the part has changed, you can select one of the following options:

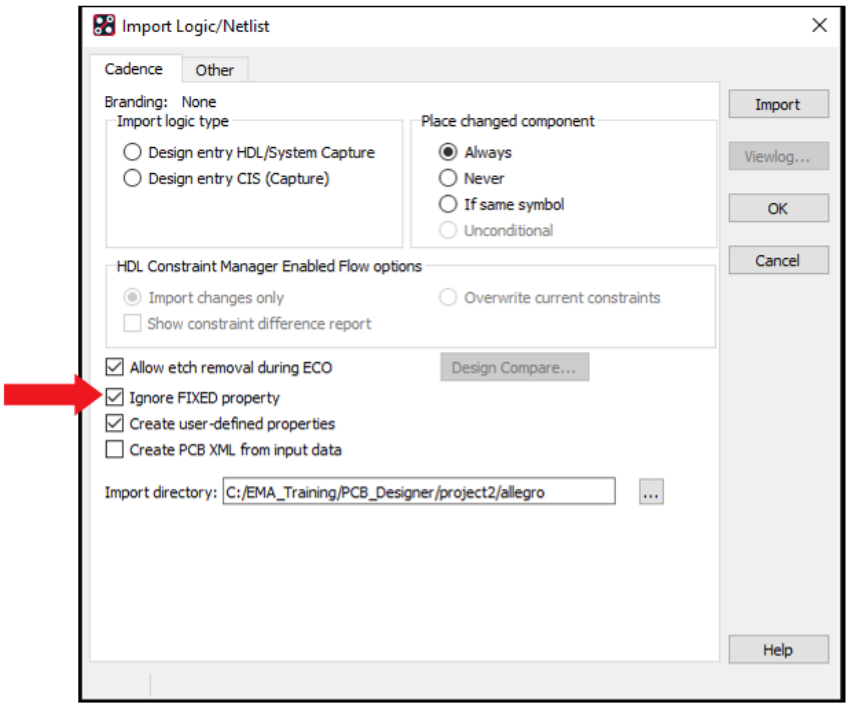


"Always" is preferred

- **Always** - Replaces the old part in the board layout with the changed part from the edited schematic, regardless of the type, value, or package symbol change (at the same x/y location and rotation as the old part).
- **Never** - Removes the old part from the layout and adds the changed part to the board layout database as an unplaced part (placed back in the Placement dialog box).
- **If Same Symbol** - If the package symbol has changed, the old part is removed from the layout, and the changed part is added to the board layout database as unplaced.

Routing Changed

If routing has already occurred, you may choose to select the following option:



"***Ignore FIXED property***" is preferred

Allow Etch Removal During ECO - This function automatically resolves any conflicts between the edited schematic and any existing connections on the board.

- When an existing board connection conflicts with the new schematic data and this option is not checked, the existing etch is flagged with a DRC marker. You can then manually edit the connections in question as needed.
- With this option checked, the PCB Editor tool will remove any wiring that does not match the edited schematic.

When completed, the PCB Editor layout will be free of all conflicting wiring. You are left with unrouted connections, which represent the schematic changes.

All part and connectivity changes made to the PCB Editor layout during the ECO process are documented in a report (`eco.txt`).

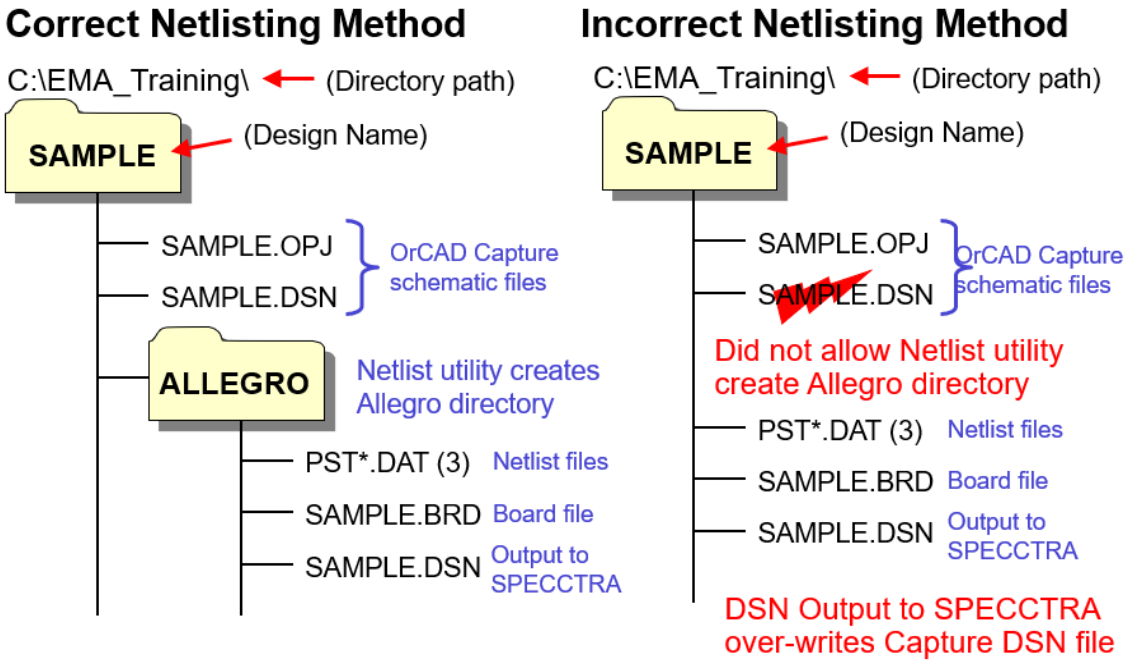
Other options available are:

- **Ignore FIXED property** – If elements in a design have a FIXED property, netlist changes will still rip up etch or replace components, ignoring that property.
- **Create user-defined properties** - Allows new properties added in the schematic to be created while logic is being read in.
- **Create PCB XML from input data** - Outputs an XML file that can be read into the PCB Compare tool.

Labs

Lab 6-1: OrCAD Capture to PCB Editor

- Setup the logic import from OrCAD Capture in the *project2/allegro* directory
- Import logic and save the new `.brd` design containing both the physical and netlist information.



Lab 6-1: OrCAD Capture to PCB Editor

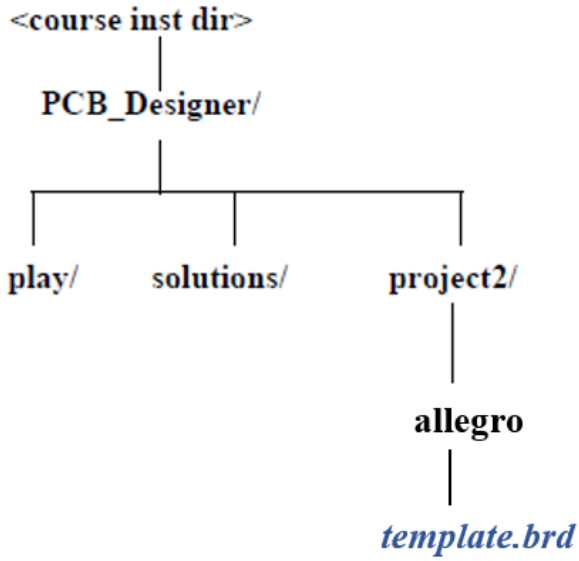
Objective: Read the component and netlist information from an OrCAD Capture schematic packager files into a PCB Editor design file and create a netlist report from the board file.

Important

Lab Directory Instructions: The lab installation directory ***C:\EMA_Training\PCB_Designer*** is referred to as the <course_inst_dir> directory. Whenever you see a file path in the lab instructions, you must replace the <course_inst_dir> directory with ***C:\EMA_Training\PCB_Designer***

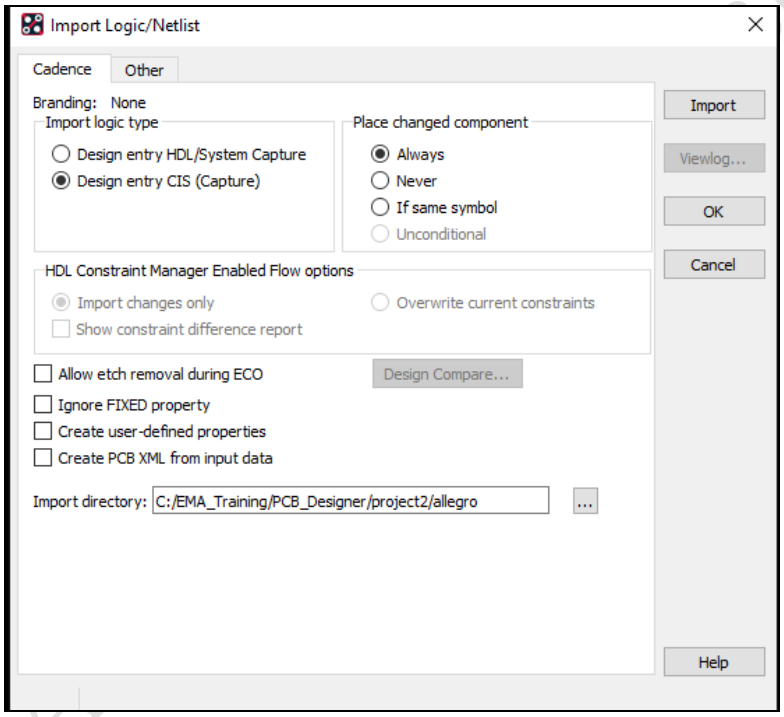
Importing the OrCAD Capture Netlist Files

1. If the PCB Editor is not currently running, start the PCB Editor tool by choose ***Start - Cadence PCB 17.4-2019 - PCB Editor 17.4***.
   The ***17.4 PCB Editor Product Choices*** window will appear.
2. When the ***17.4 PCB Editor Product Choices*** window appears, select ***OrCAD PCB Designer Standard***, and click ***OK***.
3. Open the ***`template.brd`*** design (if is not already open) from within the *project2* directory, as shown:



Note If you did not complete the lab titled "*Creating a Template Design File*", which saved the board file *template.brd* into this ***Project2/allegro*** directory, then use the ***`cds_template.brd`*** file that is provided.

4. Choose ***Import – Netlis***t from the top menu.
   The ***Import Logic*** dialog box appears.
5. In the ***Import logic type*** section, enable ***Design entry CIS (Capture)***.
6. In the ***Import directory*** field, navigate to the ***project2 - allegro*** directory (previously generated netlist is located in this directory).
   Your ***Import Logic*** dialog box should look similar to this:



7. Click the ***Import*** button.
   The OrCAD Capture schematic is checked and imported. If there are errors or warnings, the `netrev.lst` file automatically displays in a report window when the importing is completed. If `netrev.lst` does not appear, select ***File - Viewlog*** from the PCB Editor main menu to open this file.
8. Close the log file window.

Note If you receive a message that the PACKAGER files could not be found, this is because the *Import directory* field is not pointing directly to the directory containing the netlist files.

9. Select ***Export - Quick Reports*** from the top menu and select the ***Bill of Materials Report.***
   The report shows which components are currently in the database. This will verify your success with loading the netlist into PCB Editor.
10. Click the ***X icon*** to close the report.
11. Choose ***File - Save As*** from the top menu.
    A ***Save As*** file browser window opens.
12. In the ***Save in*** field, browse to the ***project2/allegro*** directory.
    Remember, the Change Directory option has to be enabled to change the working directory.
13. In the ***File name*** field, enter ***`unplaced`***
14. Click ***Save*** to save the `unplaced.brd` file in the *project2 - allegro* directory.
    The OrCAD Capture schematic data has been combined with the template design file (mechanical template) to create a new design file called `unplaced.brd`. Use this design file to proceed to the next layout phase.
15. At this point you can either exit from the PCB Editor program by selecting ***File - Exit***, or you can leave this design open, ready to begin lab exercises for the next lesson.

Note When you exit from the PCB Editor program, files are saved that record your current working directory settings as well as configuration settings and the last file you were working on. If you exit from PCB Editor at this point in the lab, when you restart PCB Editor it will automatically open the `unplaced.brd` file in the *<course inst dir> - PCB_Designer - project2 - allegro* directory. This is what you want for the next lab.

End of Lab

Lesson 7: Setting Design Constraints

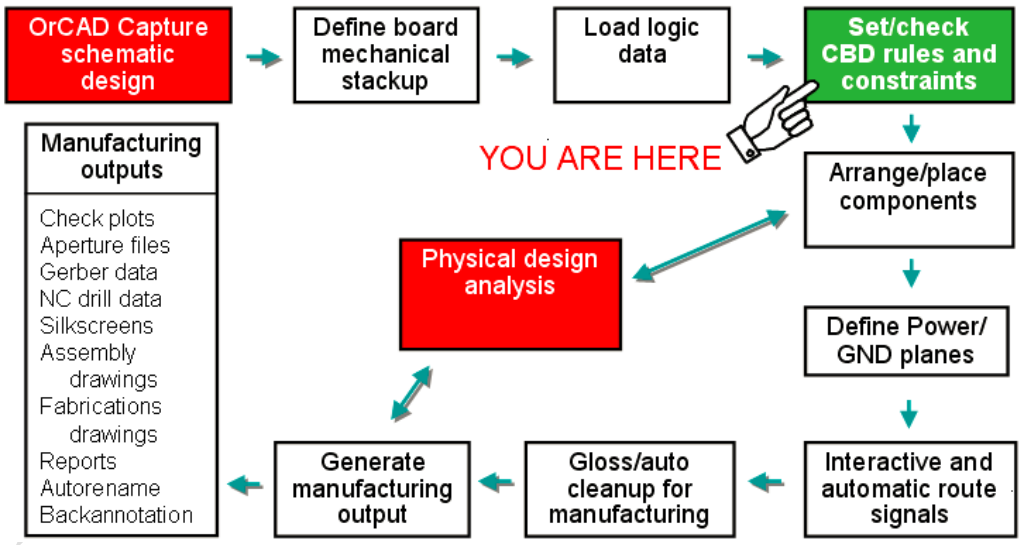
Learning Objectives

In this lesson, you will:

- Explore the design rule system and apply physical and spacing design rules
- Add, change and delete properties of components and nets

In this section, you will set up your design rules. Design rules are known as Constraints in PCB Editor and are the rules that must be followed while routing your design. Typical constraints include the line width to be used during routing, line-to-line spacing, line-to-pad spacing, etc.

Design Layout Process



This design flow is used throughout the course. Each box in this flow represents a common step in the design of a printed circuit board. As indicated in the design flow, the Set/check CBD (Correct by Design) rules and constraints step will now be discussed.

Introduction to Design Rules

There are five types of design rules:

- **Electrical Constraints -** Performance characteristics
- **Physical Constraints -** Line width, via selection, and some layer restrictions
- **Spacing Constraints -** Clearances between lines, pads, vias, and copper areas (shapes) on different nets
- **Same Net Spacing Constraints -** Clearances between lines, pads, vias, and copper areas (shapes) on the same net
- **Design Constraints -** Package checks, soldermask checks and negative plane island checks

For Physical & Spacing, there are two categories of DRCs:

- **Default Rules** - Used to specify the rules to be applied to nets having no special routing requirements
- **Special Rules** - Used for any net requiring specialized rules applied to them

The PCB Editor tool has a set of predefined rules, such as Line-to-Pin Spacing, or Minimum Line Width. You can define values for each rule within the context of a constraint set. A constraint set is a group of rules that have been bundled together to make value assignments easier for the user.

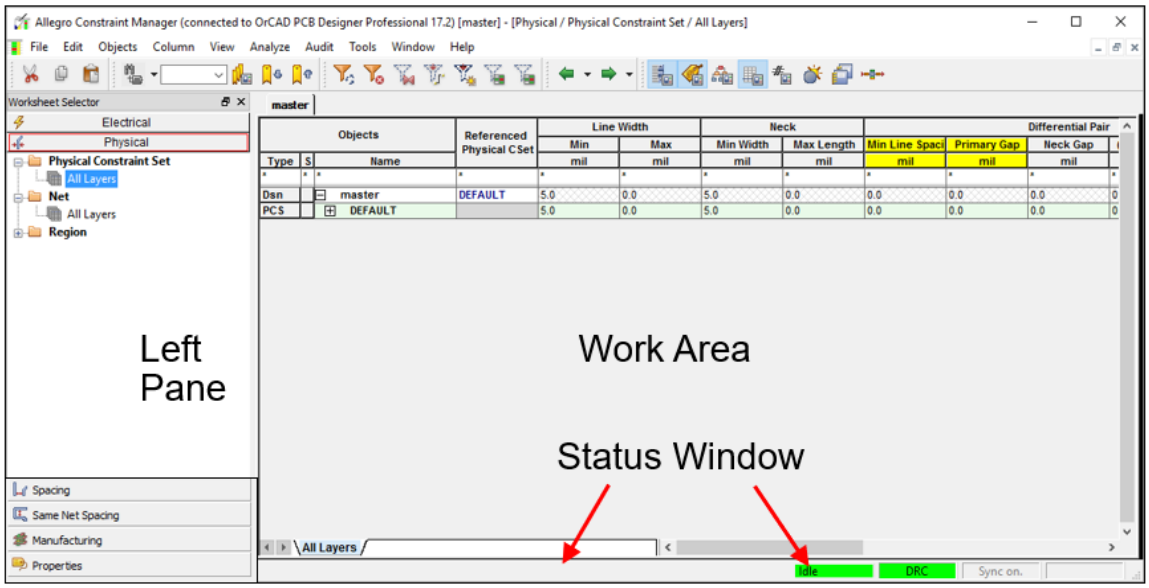
This rule 'bundling' is based upon the type of constraint set.

- **Electrical Constraints** - Constraints governing electrical behavior and performance 'of an entire net, (for example, Max Length and differential pairs).
- **Physical Constraints** - Constraints governing physical construction of a net (for example, minimum line width, via selection, and allowed etch layers).
- **Spacing Constraints** - Constraints governing the spacing between objects on different nets (for example, line-to-thru-pin spacing).
- **Same net Spacing Constraints** - Constraints governing the spacing between objects on the same net.
- **Design Constraints** - Setting or unsetting of package DRC checking, negative plane island constraints, and soldermask constraints.

There are two different categories of Physical and Spacing design rules. The **Default** category is used to specify the rules for the majority of the nets in your design, or nets that have no special routing requirements. Any nets that need specialized rules applied to them fall into the **Special** category. For these nets, you must identify the nets requiring the special rules, and also create/set the special rule values.

The Constraint Manager

Setup – Constraints … or … 



To set your design rules, use the ***Setup - Constraints*** command from the top menu or use the Constraint Manager icon. The **Allegro Constraint Manager** form is opened. You can access and create all of the required physical, spacing, same net spacing and design constraints from this form.

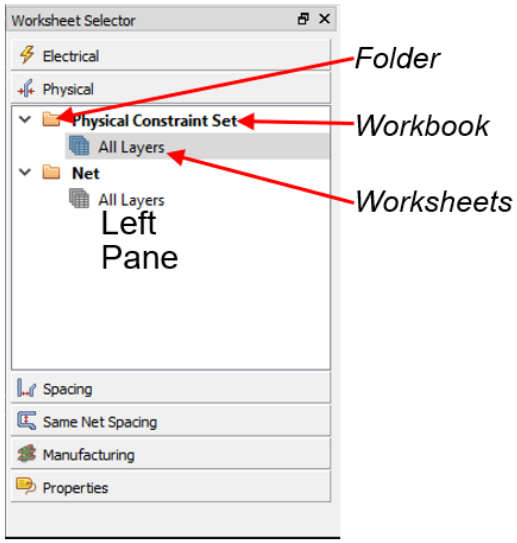
The Constraint Manager contains several different sections.

- The **Left Pane** contains different domain sections where you select which type of design rules you wish to set or view.
- The **Work Area** is the section where you will set the rules for your design or view the current rule values.
- The **Status Window** should always be checked for warning or error messages. If you attempt to set a value in a cell that cannot be modified, a message in the Status Window will identify this fact.

Constraint Manager - Left Pane

Left Pane Constraint Domains

- *Electrical*
- *Physical*
- *Spacing*
- *Same Net Spacing*
- *Manufacturing*
- *Properties*
- *DRC*



The Left Pane of the Constraint Manager is divided into six different domains. Each domain has several Folders available. Most of these folders may have just Worksheets but some may have a combination of Workbooks/Worksheets available. The Workbooks are expandable and contain individualized worksheets.

The six different domains available in the left pane are:

- **Electrical** - Electrical Constraints where electrical behavior and performance of a net is defined. Covered in the PCB Editor Professional Class.
- **Physical** - Physical Constraints where the physical characteristics of traces are defined. Includes line widths, allowable vias, etc. Referred to as Physical CSets.
- **Spacing** - Spacing Constraints where clearance between objects is defined. Includes line-to-line spacing, line-to-thru-pin spacing, via-to-thru-pin spacing, etc. Referred to as Spacing CSets.
- **Same Net Spacing** - Same Net Spacing Constraints where clearances between objects that are on the same net are defined. Includes line-to-line spacing, line-to-thru-pin spacing, via-to-thru-pin spacing, etc. Net Class-Class is not supported. Referred to as Same Net Spacing CSet.
- **Properties** - Allows for the assignment of properties to nets and components. Alternative method to the ***Edit - Properties*** command, discussed later in this section.
- **DRC** - Lists all DRCs in your design for Physical Worksheet, Spacing Worksheet, Same Net Spacing Worksheet, Design Worksheet, Assembly Worksheet, External Worksheet, Design for Fabrication Worksheet, and Design for Assembly Worksheet and Design for Test Worksheet.

Constraint Manager - Work Area

Sample Views

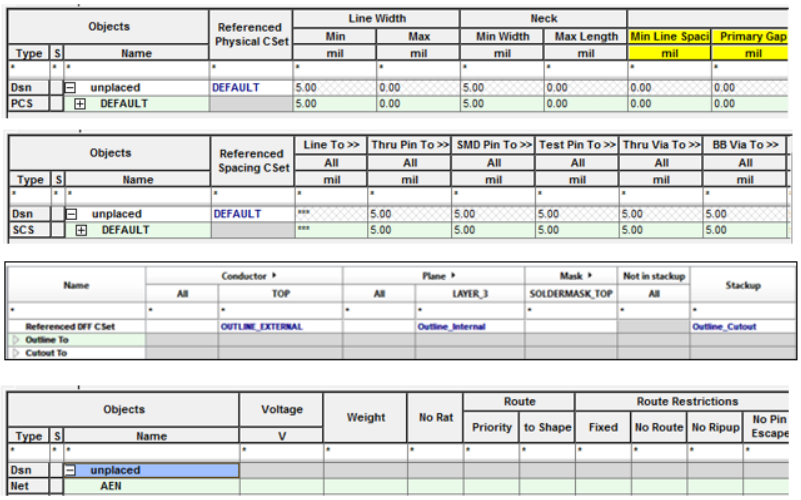
Physical

Spacing

Same Net Spacing

Manufacturing

Properties

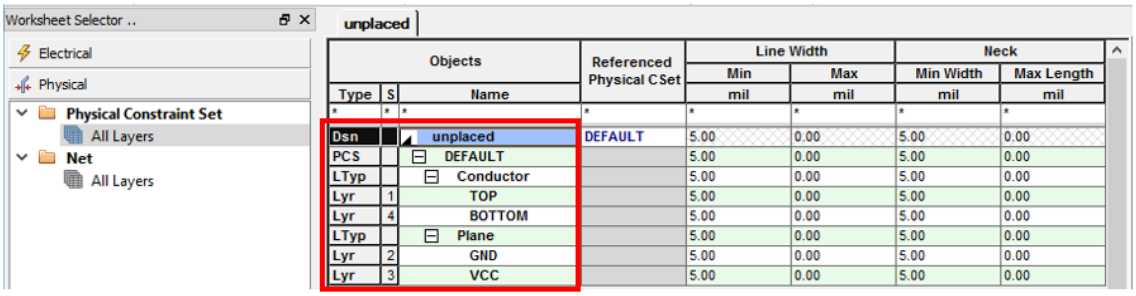


The Constraint Manager's work area is where you set or view all the design rules for your design. The work area will have the appropriate values that match the worksheet you have selected. The available values will be covered later in this section.

The Objects and Type columns will vary based upon the worksheet you have open. The objects and types can be items such as Electrical CSets, Physical CSets, Spacing CSets, Buses, Nets, etc. Hovering your cursor over an object or type will display a tool tip window identifying the object. The left end of the Status Window will also display the tool tip information.

You can turn on and off the row numbers by using the ***View – Views Options*** command and selecting or deselecting the Row Number option in the Workbooks section.

Setting Default Physical Constraint Values



Expanding the Constraint Set (CSet) displays the Layer Types (LTyp), Conductor and Plane. Expanding the individual Layer Types displays the layers associated with the respective Layer Type.

The first step in setting your design rules is make sure your default rules are set properly. These rules will be used for the nets that have no special routing requirements. You can set the same rules for all routing layers in your design by setting the values in the DEFAULT row of the Constraint Manager.

If you need to set different rules for different layers in your design, you can expand the DEFAULT row by selecting the "+" character. This displays Layer Type rows; Conductor and Plane. Expanding the Layer Types displays rows for each of the respective layers associated with the individual Layer. You can now set different values as required on any layer in your design.

The values you can set are:

- **Line Width, Min** - Minimum line width at which a connection can be routed. When you manually route a connection, this value will be used by default. If you route at a width less than this value, a DRC error will be created.
- **Line Width, Max** - Maximum line width at which a connection can be routed. If you use a line width greater than this value, a DRC error will be created.
- **Neck, Min Width** - Minimum line width at which a connection can be routed when using the neck mode. The neck mode option is available during routing by using the **Right-Mouse-Button** pop-up menu item **Neck**.
- **Neck, Max Length** - Maximum allowable length at which a connection can be routed at the neck width before returning to the minimum line width. Note that this value is the cumulative length of the necked sections across the entire net.
- **Vias** - List of via padstacks (`.pad`) that are allowed to be used with your default nets.
- **BB Via Stagger, Min** - Minimum center-to-center distance between the connect point of one pin or via and the connect point of another, where the two pins or vias are on the same net and have a single cline connecting them.

- **BB Via Stagger, Max** - Maximum center-to-center distance between the connect point of one pin or via and the connect point of another, where the two pins or vias are on the same net and have a single cline connecting them.
- **Allow Etch** - If set to True, routing is allowed on the subclass/layer. If set to false, routing is NOT allowed on the subclass/layer.
- **Allow Ts** - This specifies when and where T junctions (points where there are 3 or more segments of etch) are allowed.

  Values are:
  - **Not Allowed** – Prohibits all T junctions.
  - **Anywhere** – Allows all T junctions (pin, via, or on a cline). Default.
  - **Pins Only** - Allows T junctions on pins only.
  - **Pins Vias Only** - Allows T junctions only at a pin or via.

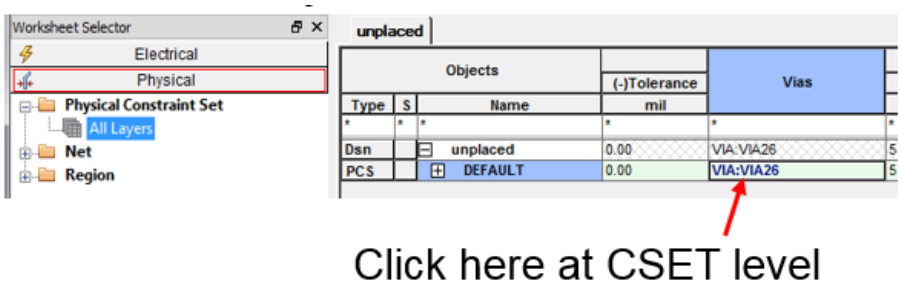
- **Allow Pad-Pad Connect** - Specifies whether a pin/via whose "connect point" lies within the extents of another pin/via forms a direct connection without the presence of an intermediate cline. For example, it would allow a fanout out via to be placed inside of a surface-mount pad without the need to draw a connect line.

  The choices are:
  - **All Allowed** - Specifies that direct connections can form anywhere. Default.
  - **Via/Pin Allowed** - Specifies that direct connections can only form between vias and pins.
  - **Via/Via Allowed** - Specifies that direct connections can only be formed between vias.
  - **Not Allowed** - Prohibits direct connections everywhere.

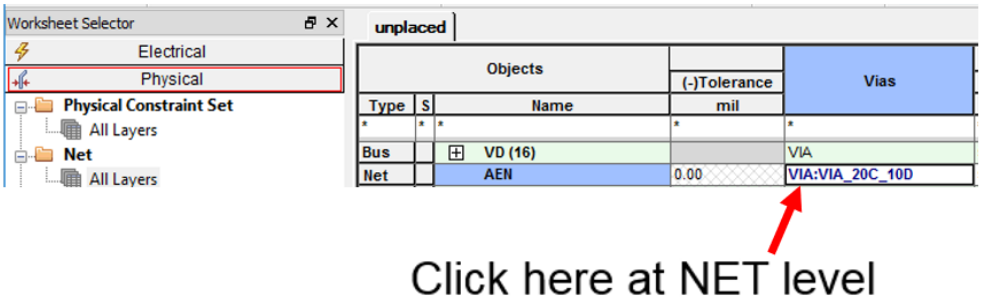
Add Via Selection to a Net or Constraint Set

When there is a requirement to include a selection of multiple vias, the multiple selection listing is added as a physical rule value in the Physical Constraints. This list of multiple vias can be applied to a Physical Constraint Set (CSet) or to an individual net.

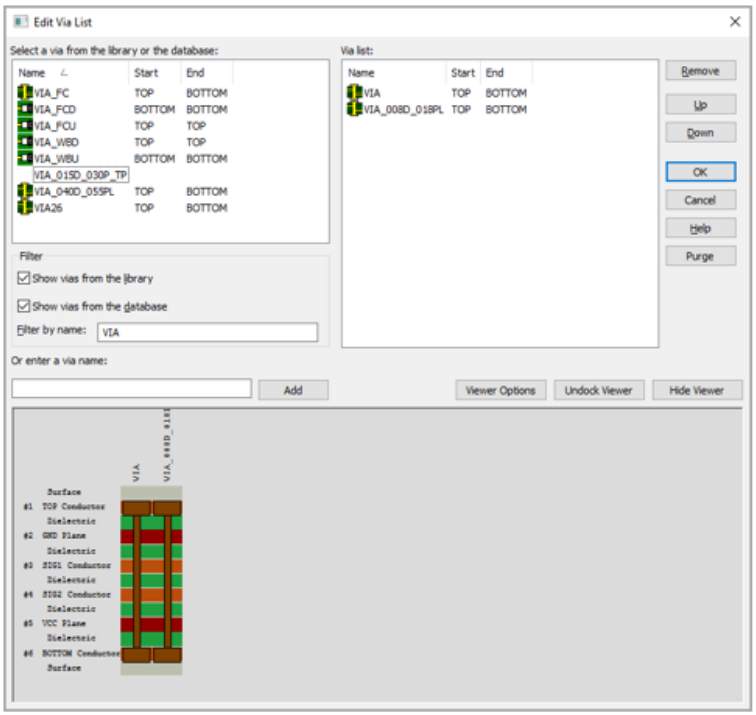
Adding Vias to a Physical CSET

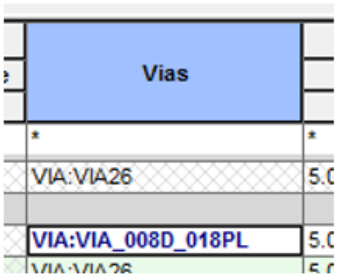


Adding Vias to a Net



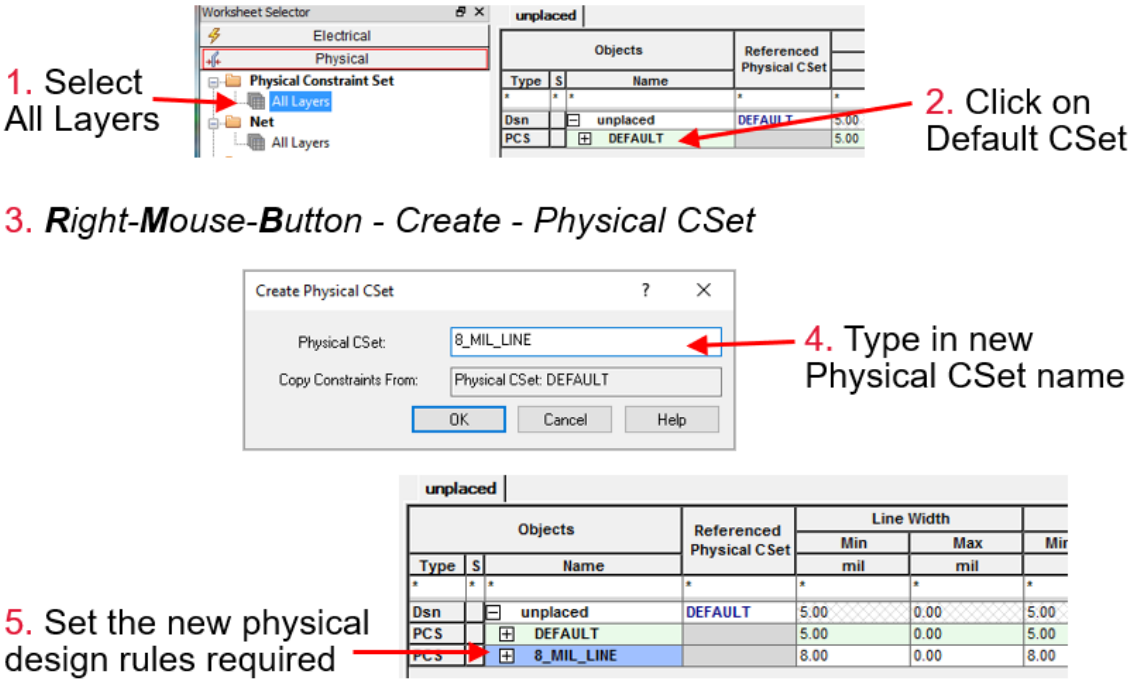
Clicking on the Vias column in either the CSet or the individual net opens an 'Edit Via List' form that provides a list of the available vias. From this list any padstack can be used as a 'via'.





Once the selection of vias have been made they will appear in the 'Via' category for either the CSET or net that you applied them to.

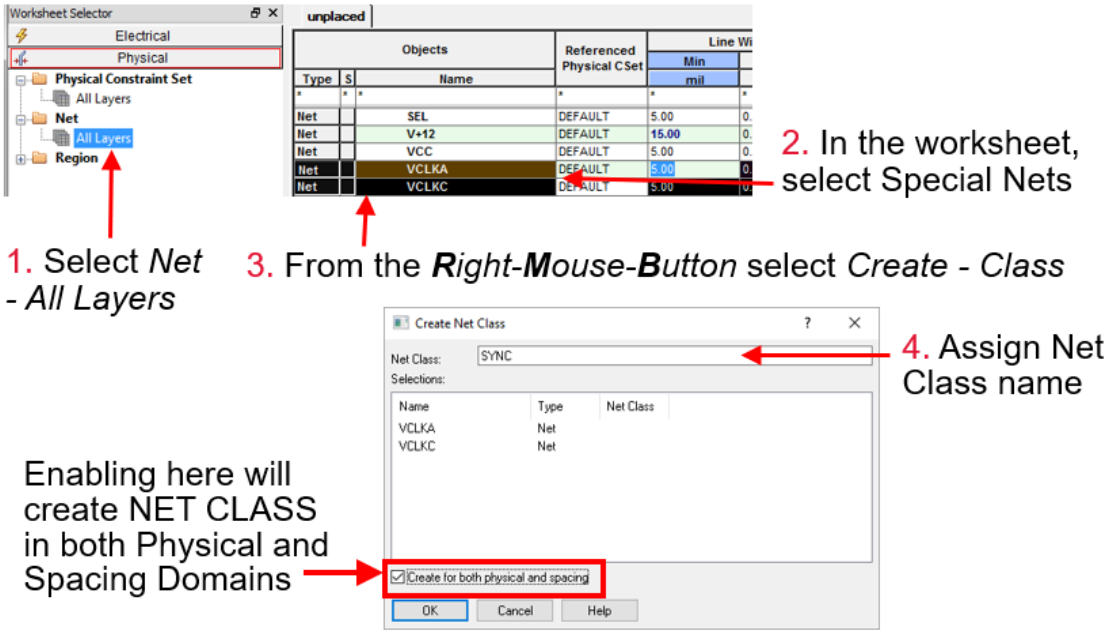
Creating a New Physical Constraint Set



You will probably have nets that require different physical rules than the default rules. These are your special nets. You need to create a new Physical CSet for these nets. You can create as many physical CSets as required for your design. To create a new CSet, perform the following steps:

1. Select the ***All Layers*** worksheet under the ***Physical Constraint Se***t folder.
2. Select the ***DEFAULT*** (or another similar Physical CSet) in the ***Objects Name*** column.
3. Click ***Right-Mouse-Button*** and select ***Create - Physical CSet*** from the popup.
4. Enter in a new ***Physical CSet*** name in the ***Create Physical CSet*** form.
5. Enter in the new values to match your special physical routing rules. If necessary, you can select the "+" character next to the physical CSet you just created. Remember that you will need to expand the Layer Types to set different values on different layers, if needed in your design.

Identify the Special Physical Nets

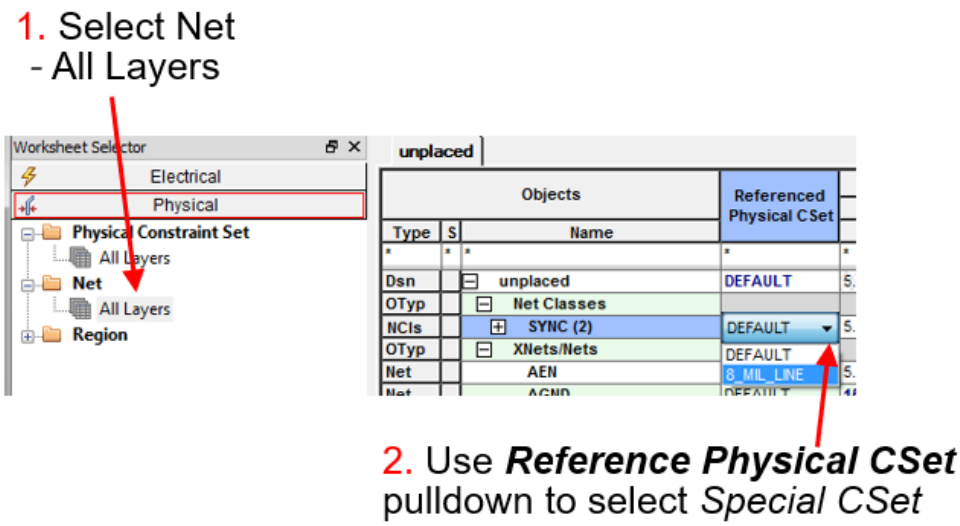


After you have created the physical rules for your special nets, the next step is to identify these nets. You perform this task by assigning nets into Net Classes. You can create as many Net Classes as are required within your design. To create a Net Class, perform the following steps:

1. Select the ***All Layers*** worksheet under the ***Net*** folder in the left pane.
   The worksheet displays all of the nets in the design.
2. In the worksheet, select the nets you want to assign to the new net class.
3. From the ***Right-Mouse-Button*** popup, select ***Create - Class***.
4. Type the new Net Class name in the **Create Net Class** form and click ***OK***.

Note You can create this new Net Class in both the physical and spacing domains by checking the ***Create for both physical and spacing*** box in the Create Net Class form.

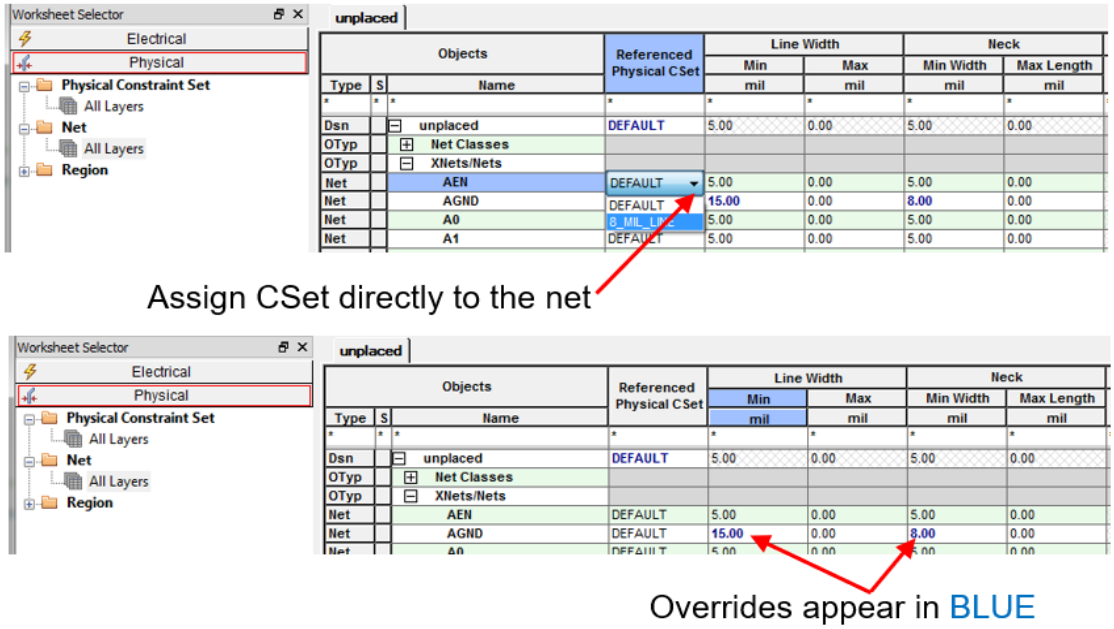
Assign the Physical Constraint Set to the Net Class



Now that you have created a net class, you need to assign the net class to the previously defined constraint set.

Select the **All Layers** worksheet under the **Net** workbook. Then, select the Net Class row (in this case, the Special net class) under the ***Referenced Physical CSet*** column. When you select this cell with the Left-Mouse-Button, a pull-down menu will appear with all of the defined Physical CSets listed. Select the appropriate CSet from the pull-down to make the assignment.

Assign Rules Directly to a Net



As an alternative to creating a net class, adding the nets to the net class, and assign a Physical CSet to the net class, you can assign rules directly to nets. In the Net Folder section, you can select on a net(s) and assign a Physical CSet directly, as shown in the top picture above.

You can also set values directly on a net(s) without assigning the net to a Physical CSet. Select on the net row and enter a new value, as shown in the bottom picture above.

In either case, note that when you change a value from the default value, the color of that value changes to blue. This is called an override and indicates that the rule in that cell does not match the default value assigned.

You can control the color used for these overrides by using the menu sequence ***View – Views Options***, in the ***Colors*** option set the ***Color Palette*** to ***Custom*** and setting the color of the ***Directly Set*** selection.

Also, in the Nets folder worksheet you can control whether or not you want the view to display the Object type separations or to just display the nets separated from the net class as in the previous versions. This is controlled in ***View – Views Options***, in the ***Worksheets*** option and enabling or disabling the ***Object Type Dividers*** selection.

Lab

Lab 7-1: Setting Physical Rules

- Define the Special Physical Rules
- Identify the Special Physical Nets
- Assign Physical CSet to Net Class

The following lab will allow you to familiarize yourself with the process required to set physical rules and create special physical design rules. You will learn how to create new design rules, identify the special nets, and apply the new design rules to the special nets.

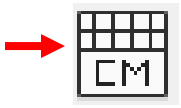
Lab 7-1: Setting Physical Rules

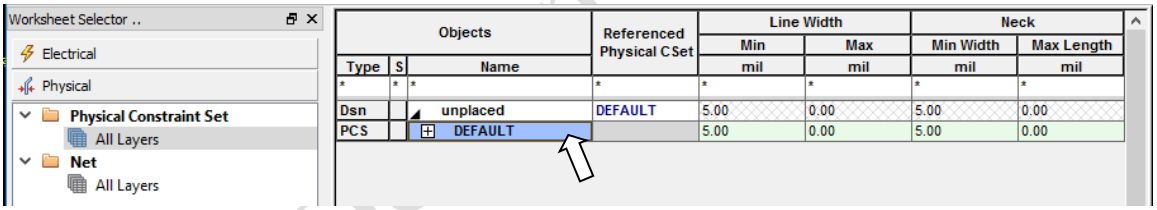
Objective: Define physical routing rules for special nets.

Defining the Special Physical Rules

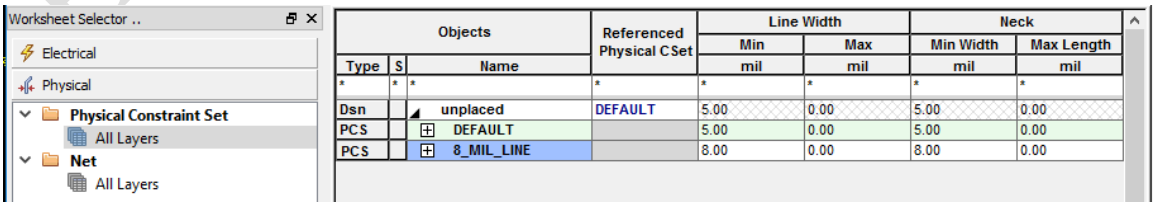
By default, all new designs have a 5-mil trace width assigned. If most of the nets in the new design require a different line trace width, that default constraint may be changed. We will use the 5-mil trace width for our design.

Assume the nets VCLKA and VCLKC require a larger line width (8 mils) than the default values. First, create the new rules by creating a new Physical CSet.

1. If you don't already have PCB Editor running, start the PCB Editor.
2. Choose ***File - Open*** and open the `unplaced.brd` design file you saved previously, if it is not currently open. An `unplaced.brd` file is also available in the ***PCB_Designer\solutions*** folder.
3. Select ***Setup - Constraints*** from the PCB Editor main menu, or 
   The ***Constraint Manager*** form opens.
4. Select the ***Physical*** domain.
5. Select the ***DEFAULT*** cell.



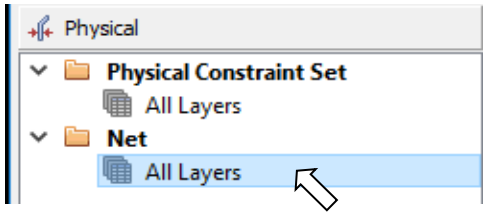
6. Click the ***Right-Mouse-Button*** and select ***Create - Physical CSet*** from the popup.
7. In the ***Create Physical CSet*** form, enter **`8_MIL_LINE`** and select the ***OK*** button.
8. In the ***8_MIL_LINE*** row, change the ***Min Line Width*** and the ***Min Neck Width*** to 8 mils
   Your Constraint Manager should look like the figure below:



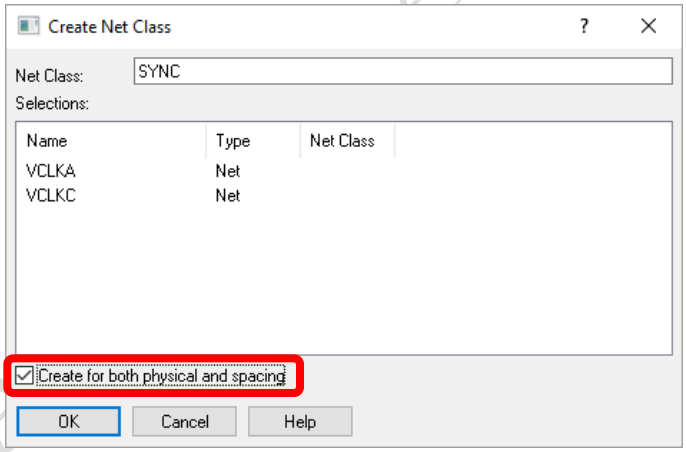
Identifying the Special Physical Nets

Now that you have created the physical routing rules for the special nets, you will identify the special nets and assign them to a net class. VLKCA and VCLKC nets will be assigned to a Net Class and then assigned the 8_MIL_LINE Physical CSet.

1. Select the ***All Layers*** worksheet under the ***Net*** folder as shown below.



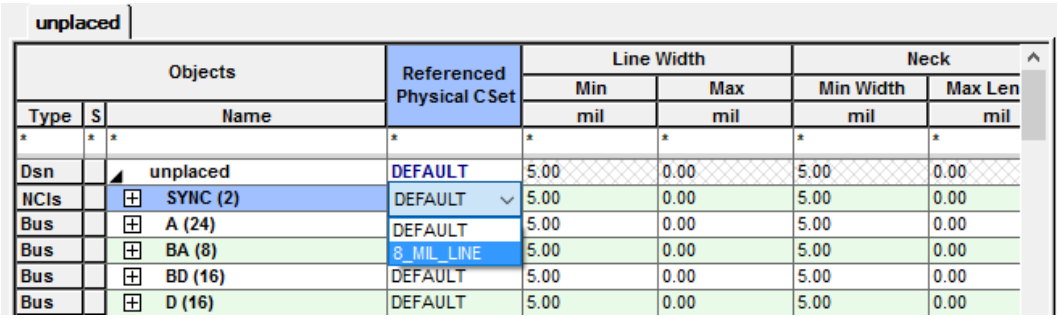
2. Scroll through the nets section so both the ***VCLKA*** and ***VCLKC*** nets are visible.
3. Select the net ***VCLKA***, and shift-select the net ***VCLKC*** so that both nets are selected.
4. Select with the ***Right-Mouse-Button*** and choose ***Create - Class*** from the pop-up.
   A Create Net Class form opens
5. In the ***Net Class*** field enter: **`SYNC`**.
6. Verify the "***Create for both physical and spacing***" option is checked and click ***OK***.



Assign the Net Class

You just created the new net class SYNC that contains the special nets VCLKA and VCLKC. Now you can assign the 8_MIL_LINE rule set to the SYNC net class.

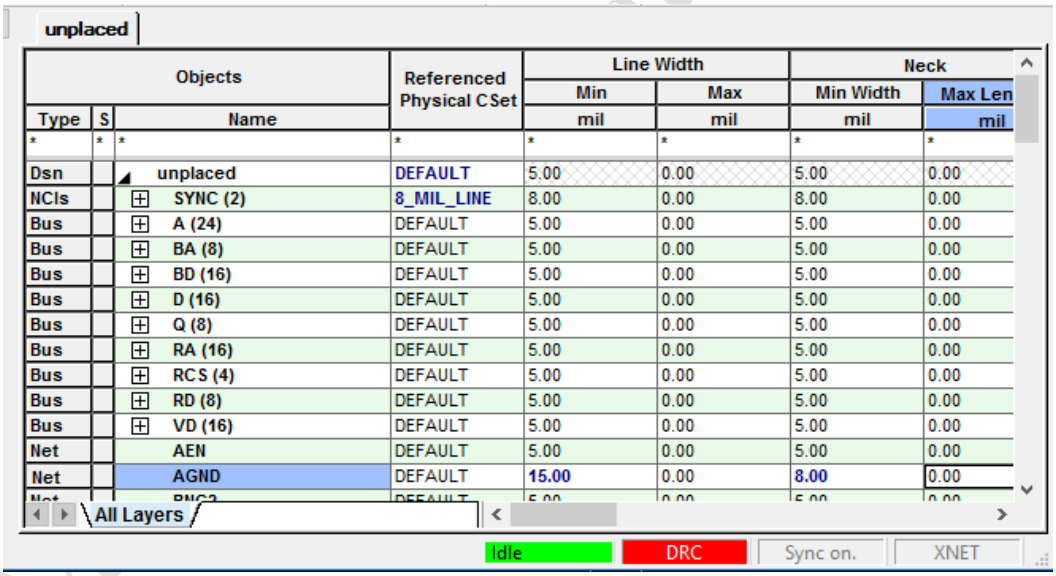
1. Select the ***Referenced Physical CSet cell*** in the ***SYNC*** row and select ***8_MIL_LINE*** from the pull-down menu as shown below.
   You will need to scroll to the top of the spreadsheet to locate the ***SYNC*** Net class.
   You will also notice that the ***SYNC*** net class is denoted as ***SYNC (2)***. The (2) denotes that there are two nets in the ***SYNC*** net class.



Now the SYNC net class, which contains the two special nets VCLKA and VCLKC, will use the 8_MIL_LINE rule such that when either of these two nets is routed, the line width used will be 8 mils instead of the default 5-mil-wide line.

Assign Min Line Width Directly to Nets

1. Next, assign a ***15 mil*** min line width and ***8 mil*** min neck width directly on the following ground nets ***AGND, GND, GND_EARTH*** by typing the required values in the ***Min Line Width*** and ***Min Neck Width*** fields.



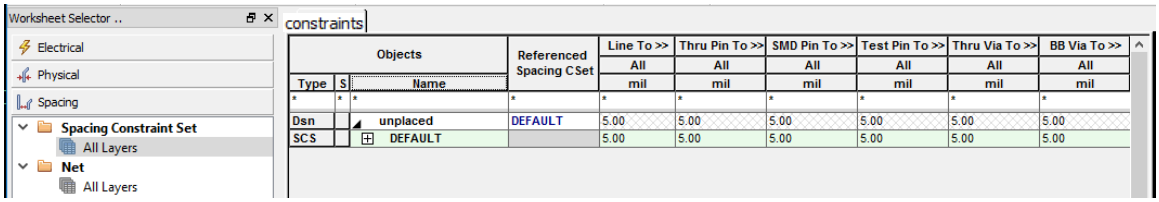
Notice that the 15 mil and 8 mil constraint "overides" show up in blue.

2. Select ***File - Close*** from the Constraint Manager's top menu.
3. In the PCB Editor, select ***File - Save As***. A ***Save As*** file browser form appears. Rename this drawing: **`constraints`**.
4. Make sure to save it in the ***PCB_Designer\project2\allegro*** folder.
5. Click ***Save*** to save the `constraints.brd` file.
   The `constraints.brd` file is saved to disk.

Note Do ***not*** exit PCB Editor. The next lab will continue from this point.

End of Lab

Setting Default Spacing Constraint Values

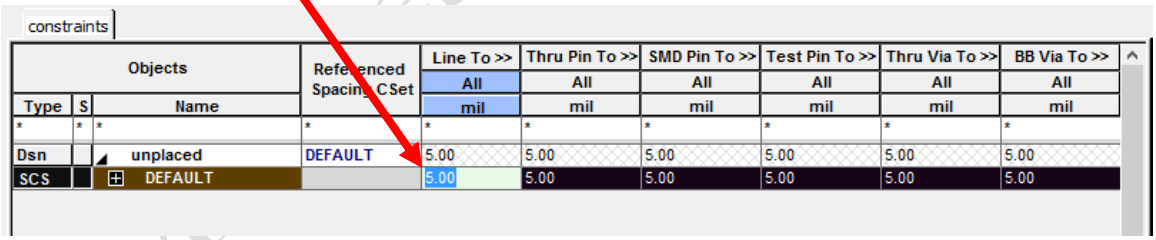


The first step in creating your spacing rules for your design is to set the default rules. These rules will be used for the nets that have no special routing requirements. You can set the same rules for all routing layers in your design by setting the values in the DEFAULT row of the Constraint Manager.

The Spacing Constraints are all in one worksheet and are separated into constraint categories that are either expandable or collapsible. To expand a constraint group, click on the ">>" next to the constraint category name. To collapse the constraint category, click on the "<<" next to the constraint category name.

To quickly populate a constraint category with the same value, click on the ***All*** cell for that category and type in the required value.

To quickly populate all constraint categories with the same value, select the constraint set name. This will highlight the entire row with the first category value selected. If you type a value in there and hit the Tab key, all values will be changed to that value.



The available Spacing Constraint categories are:

- Line To
- Thru Pin To
- SMD Pin To
- Test Pin To
- Thru via To
- BB Via To
- Test Via to
- Shape to
- Bond Finger To
- Hole To
- Min BB Via Gap

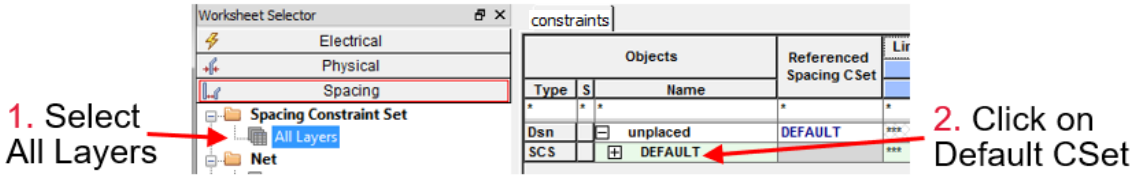
Note The Min BB Via Gap rules can be applied to the rule set but does not apply to individual layers.

If you need to set different rules for different layers in your design, you can expand the DEFAULT row by selecting the "+" character. This displays Layer Type rows; Conductor and Plane. Expanding the Layer Types displays rows for each of the respective layers associated with the individual Layer Type thus displaying each layer you have created in your board stack-up. You can now set different values as required on any layer in your design.

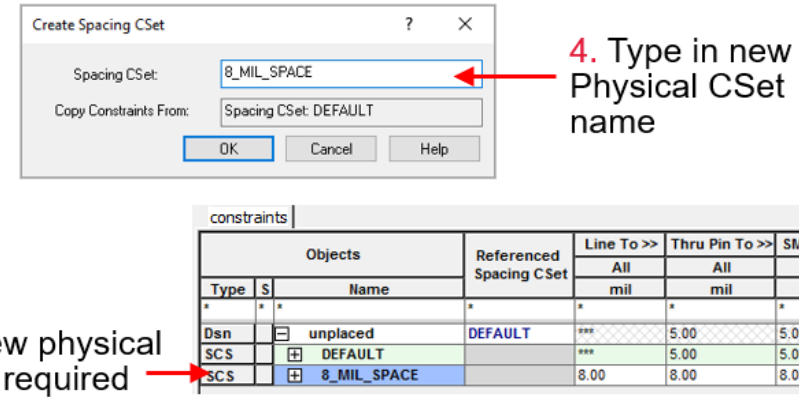
The spacing values you set are for edge-to-edge clearance, or the air gap between the two elements. You can specify different values for lines, pins, vias, shapes and holes. For pins, you can specify different values for thru pins, surface-mount pins, and test pins. For vias, you can specify different values for thru vias, blind/buried vias and test vias.

Note Populating a spacing constraint value in the element to element field in one spacing constraint category will automatically populate the same element to element field in the opposing spacing constraint category.

Creating a New Spacing Constraint Set



3. ***R**ight-**M**ouse-**B**utton - Create - Spacing CSet*



You will probably have nets that require different spacing rules than the default rules. These are your special nets. You need to create a new Spacing CSet for these nets. You can create as many Spacing CSets as required for your design. To create a new CSet, perform the following steps:

1. Select one of the worksheets under the ***All Layers*** workbook under the ***Spacing Constraint Set*** folder.
2. Select the ***DEFAULT*** (or any similar Spacing CSet) in the ***Objects Name*** column.
3. Click the ***Right-Mouse-Button*** and select ***Create - Physical CSet*** popup.
4. Enter a new ***Spacing CSet*** name in the ***Create Spacing CSet*** form.
5. Enter the new values to match your new spacing rule requirements. If necessary, you can select the "+" character next to the spacing CSet you just created. Remember that you will need to also expand the Layer Types to set different values on different layers in your design.

Identify Special Spacing Nets

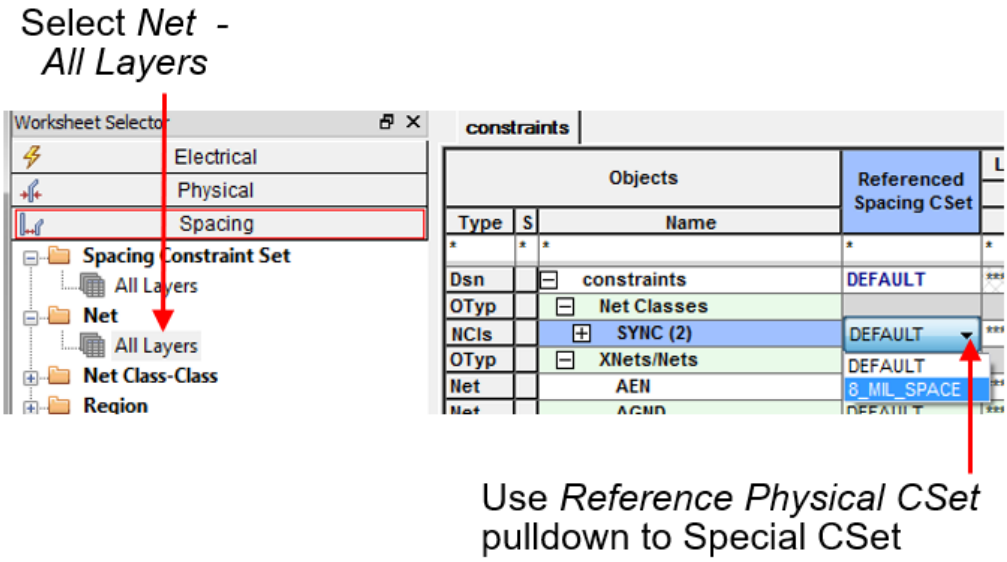
Now that you have created the spacing rules for the special nets, you will identify the special nets and assign them to a net class. In this case, the SYNC Net Class including the nets VLKCA and VCLKC have already been created in both the Physical and Spacing domains.

If you need to define more Net Classes, here is a quick overview of the steps we used to create the SYNC Net Class.

1. Select the ***All Layers*** worksheet under the ***Net*** folder as shown below.
2. Scroll through the nets until you find the nets you would like to define as a Net Class.
3. If the nets are in sequence, select the first net and shift-select the last net in the list. You can also hold down the Control key while selecting nets, if they are not in sequence.
4. Click the ***Right-Mouse-Button*** and select ***Create - Class*** from the pop-up.
   A Create Net Class form opens
5. In the ***Net Class*** field enter the name of your new Net Class.
6. If you want to create the Net Class in both the Physical and Spacing domains, verify that the "***Create for both physical and spacing***" option is checked.
7. Click ***OK***.

Your new Net Class is displayed towards the top of the Nets worksheet.

Assign the Spacing Constraint Set to the Net Class

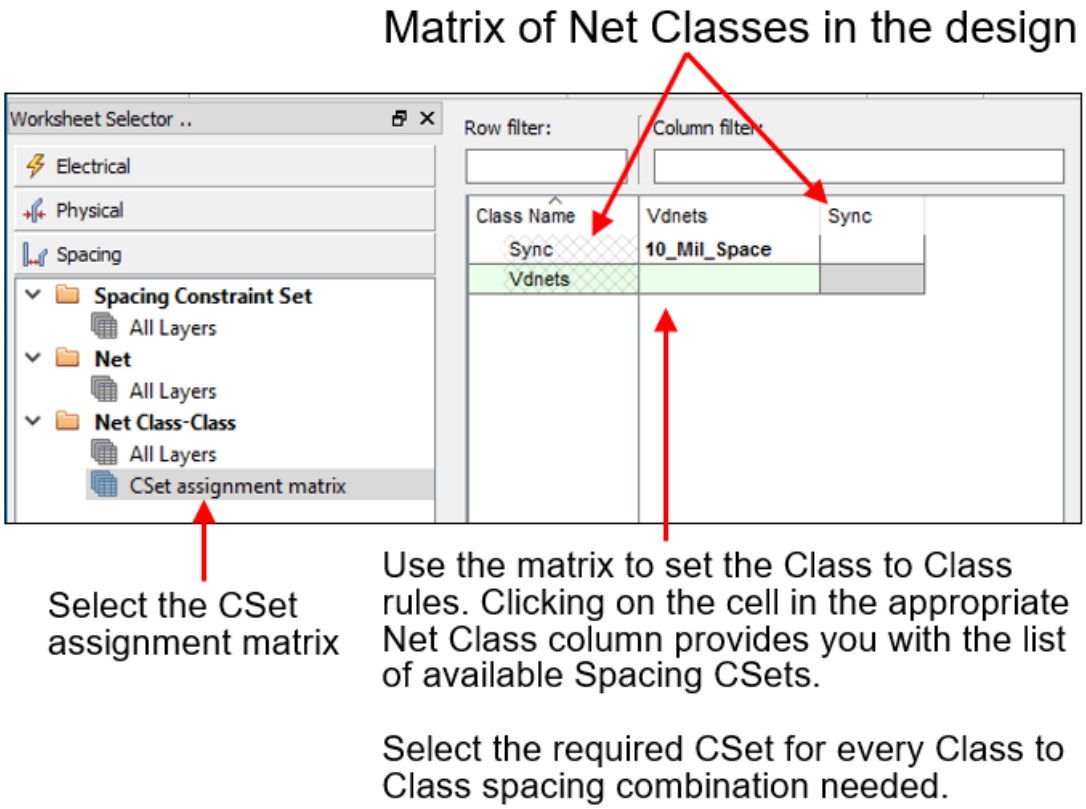


If you created your net class in both domains, all you will need to do is assign the net class to a previously defined constraint set. Select the ***All Layers*** worksheet under the ***Net*** folder.

Select in the Net class row (in this case, the SYNC net class) in the cell under the Referenced Spacing CSet column. When you select this cell (with the Left-Mouse-Button), a pull-down menu will appear with all of the defined Spacing CSets listed. Select the appropriate CSet from the pull-down menu to make the assignment.

Note that you can also assign rules directly to nets in the same manner as was shown in the Physical section under the topic “Assign Rules Directly on a Net”.

Net Class to Net Class Spacing



To set up your Class to Class rule pairing combinations. In the ***Net Class-Class*** folder select the ***CSet assignment matrix*** worksheet. The worksheet area displays a matrix with a column/row combination for every net class that you have in the design.

Clicking on the cell in the net Class column/row combination provides the list of Spacing Constraint Sets you have setup for the design. Select the appropriate Constraint Set.

You will find that if the Net Class to Net Class has already been assigned with a rule set in one Net Class column/row combination it will appear blank in the corresponding Net Class column/row field.

Labs

Lab 7-2: Setting Spacing Rules

- Define the Special Spacing Rules
- Assign Spacing CSet to Net Class

Lab 7-3: Setting Class-Class Rules

- Define a New Special Spacing rule
- Assign Nets to a New Net Class
- Create the Class-Class Rule

The following labs will allow you to familiarize yourself with the process and steps required to set spacing design rules in your design. You will learn how to identify the special nets, create new design rules, and apply the new design rules to the special nets. You will also proceed through the steps required to create a net class-class rule.

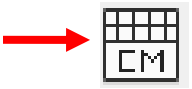
Lab 7-2: Setting Spacing Rules

Objective: Define spacing routing rules for special nets.

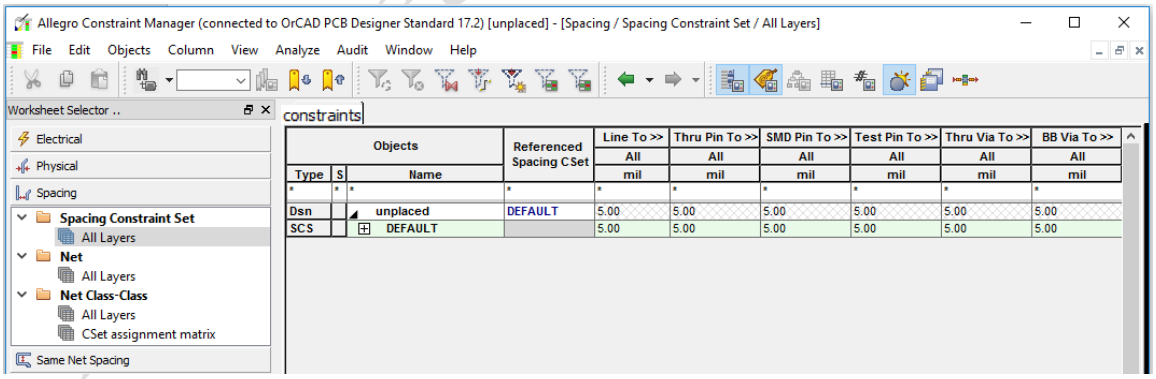
Setting the Special Spacing Rules

By default, all new designs have a 5-mil spacing rule assigned. If most of the nets in the new design require a different spacing, that default constraint may be changed. We will use the 5-mil spacing rule for our design.

Assume the nets VCLKA and VCLKC require a larger clearance (8 mils) than the default values. First, create the new rules by creating a new Spacing CSet.

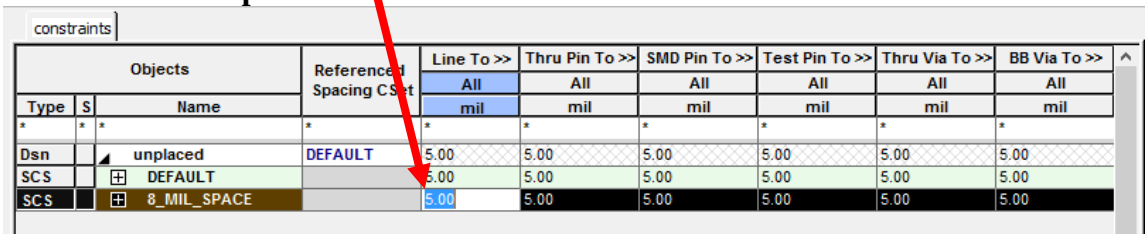
1. If you don't already have the ***PCB Editor*** running, start the ***PCB Editor***.
2. Choose ***File - Open*** and open the **`constraints.brd`** design file you saved previously if it is not currently open.
3. Select ***Setup - Constraints*** from the PCB Editor main menu, or 

The Constraint Manager form opens.
4. Select the Spacing domain from the left pane.
5. Select ***All Layers*** worksheet in the **Spacing Constraint Set** folder.
6. Select the ***DEFAULT cell*** in the worksheet in the ***All Layer*** workbook of the ***Spacing Constraint Set*** folder.

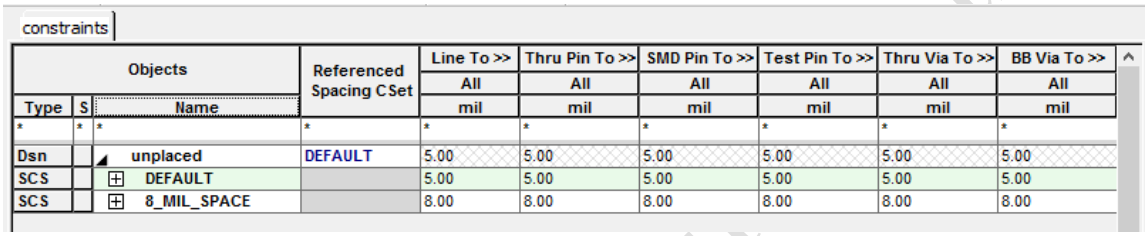


7. Click the ***Right-Mouse-Button*** and select ***Create - Spacing CSet*** from the popup.
8. In the ***Create Spacing CSet*** form, enter **`8_MIL_SPACE`** and select the ***OK*** button.
9. In the ***8_MIL_SPACE*** row, change all values to ***8***.
   - To quickly populate all constraint categories with the ***8 mil*** value, select the ***8_MIL_SPACE*** constraint set.
   - This will highlight the entire row with the first category value selected.

- If you type an 8 there and then the tab key, all values will be changed except **Min BB Via Gap**.



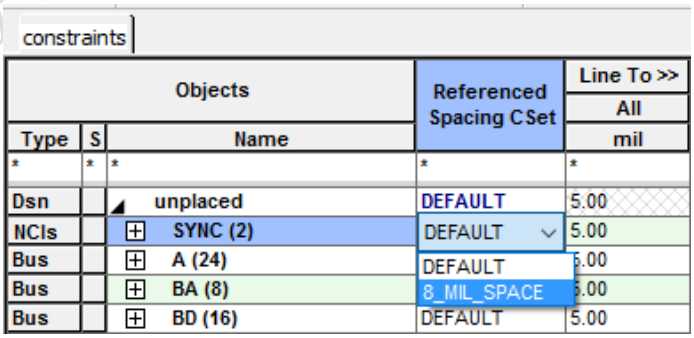
- Scroll across to the ***Min BB Via Gap*** field and type in **8**.
  Your Constraint Manager should look similar to figure below:



Assigning a Constraint Set to the Net Class

When you created the SYNC net class in the Physical Rule section, you created that class in both the physical domain and in the spacing domain. All that's left to do now is assign the 8_MIL_SPACE Spacing CSet to the SYNC net class.

1. Select the ***All Layers*** worksheet under the ***Nets*** folder.
2. Select the **Referenced Spacing CSet cell** in the ***SYNC*** row and select ***8_MIL_SPACE*** from the pull-down menu as shown below.



Now the SYNC net class, which contains the two special nets VCLKA and VCLKC, will use the 8_MIL_SPACE rule such that when either of these two nets is routed, all etch will remain 8 mils apart.

Note The SYNC Net class was created in the Spacing Domain when you checked the option “Create for both physical and spacing” option when you created the SYNC Net class in the Physical labs.

3. Save the drawing and continue by clicking ***File - Save*** from the PCB Editor main menu.
4. Click the “***Yes”*** button to confirm the file overwrite.
   The `constraints.brd` file is once more saved to disk.

End of Lab

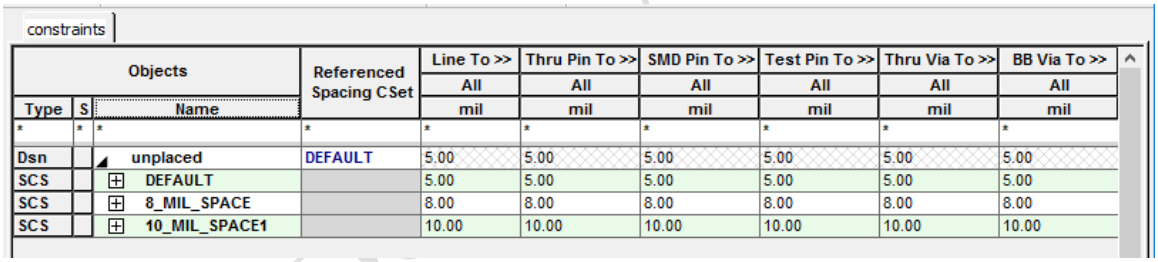
Lab 7-3: Setting Class-Class Rules

Objective: Create a new class of nets and set a class-class rule.

Assume the nets VD0....VD7 are critical and they must NOT interfere with the SYNC nets (VCLKA and VCLKC). The spacing required between these nets and the SYNC nets must be 10 mils at a minimum. You will create a new 10 mil spacing rule, assign the VD* nets into a new net class, and create a Class-Class rule between the VD* nets and the SYNC nets using the new 10 mil space rule.

Defining a New Spacing Rule

1. Select the ***All Layer***s worksheet in the ***Spacing Constraint Set*** folder.
2. Select the ***DEFAULT*** cell.
3. Click the ***Right-Mouse-Button*** and select ***Create - Spacing CSet*** *from the* popup.
4. In the **Create Spacing CSet** form, enter **10_MIL_SPACE** and select the **OK** button.
5. In the ***10_MIL_SPACE*** row, change all values to ***10***.
   Your Constraint Manager should look similar to the figure below:



Objects			Referenced Spacing CSet	Line To >>	Thru Pin To >>	SMD Pin To >>	Test Pin To >>	Thru Via To >>	BB Via To >>
				All	All	All	All	All	All
Type	S	Name		mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*	*	*
Dsn		unplaced	DEFAULT	5.00	5.00	5.00	5.00	5.00	5.00
SCS		DEFAULT		5.00	5.00	5.00	5.00	5.00	5.00
SCS		8_MIL_SPACE		8.00	8.00	8.00	8.00	8.00	8.00
SCS		10_MIL_SPACE1		10.00	10.00	10.00	10.00	10.00	10.00

Assigning Nets to a New Net Class

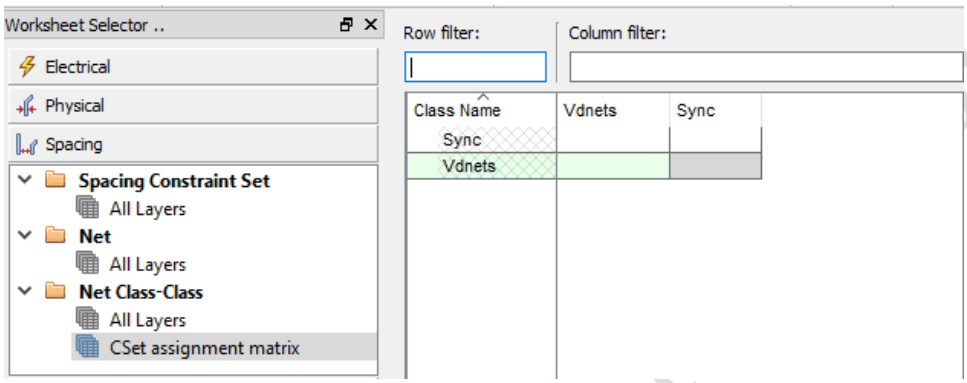
Now that you have created the spacing routing rules for the special nets, you need to assign the VD* nets to a Net Class and the power and ground nets to a Net Class.

1. Select the ***All Layers*** worksheet under the ***Net*** folder as shown below.
2. Expand the VD bus so you can see all the net associated with it (VD0 – VD7).
3. Select the first net in the bus, VD0 and then shift-select the last net, VD7 in the bus.
4. Click the ***Right-Mouse-Button*** and select ***Create - Class*** from the pop-up.
   A Create Net Class form opens
5. In the ***Net Class*** field enter the name VDNETS.
6. We only need to create this Net Class in the Spacing domain so, verify that the "***Create for both physical and spacing***" option is unchecked.
7. Click ***OK***.

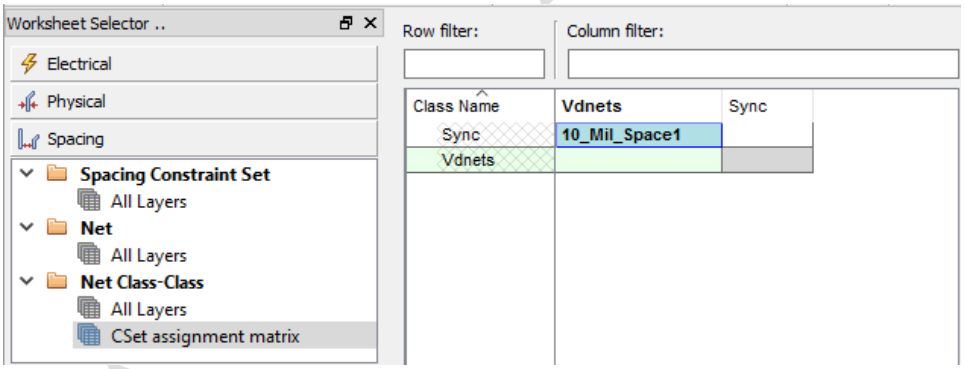
Creating the Class-Class Rule

The final step is to create class-class rules between the SYNC and VDNETS net classes.

1. Expand the ***Net Class-Class*** folder if it is not already expanded.
2. Select the **CSet assignment matrix** worksheet to display the Net Class matrix as shown below:



3. Click in the ***SYNC*** row in the ***VDNETS*** column and select the ***10_Mil_Space*** rule. The matrix should look as shown below:



The matrix defines that and if any of the SYNC nets are near any of the VDNETS, they must maintain a minimum clearance of 10 mils.

4. Select ***File - Close*** from the Constraint Manager window.
5. Select ***File - Save*** from the PCB Editor main menu.
6. Click **"Yes"** to confirm the file overwrite.
   The `constraints.brd` file is once more saved to disk.

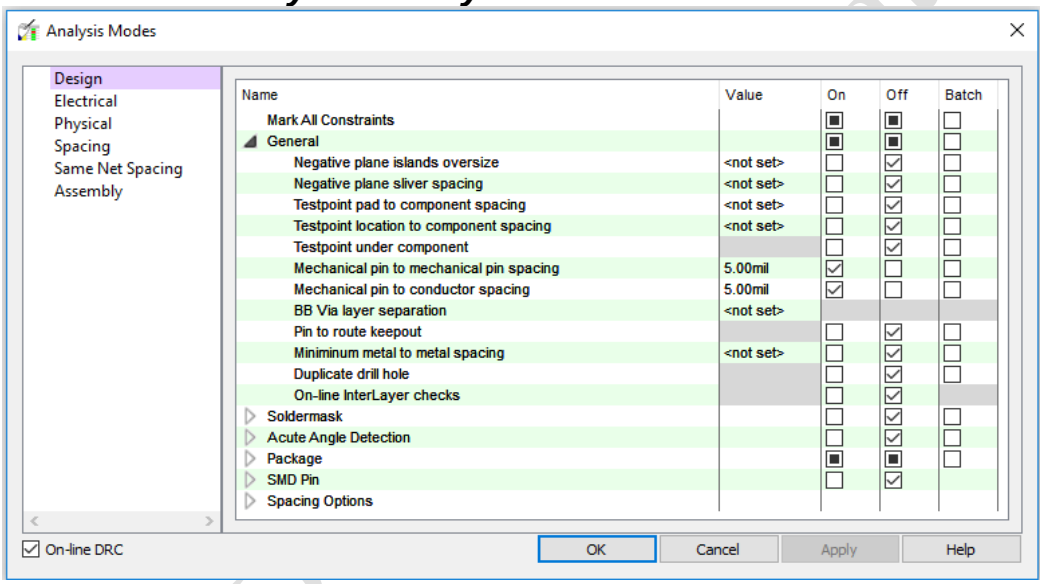
End of Lab

Analysis Modes

The *Analysis Modes* dialog box contains the modes and options for the *Design, Electrical, Physical, Spacing, Same Net Spacing, and SMA Pin* checks. These modes are accessible in the Constraint Manager from the *Analyze - Analysis Modes* menu command. In the PCB Editor they are also available from the *Setup - Constraints - Modes* menu command.

Design Options and Modes

Analyze - Analysis Modes - General



Design Options and Modes

The Design Options form specifies plane, testpoint, and mechanical-hole parameters for the enabled Design Modes checks.

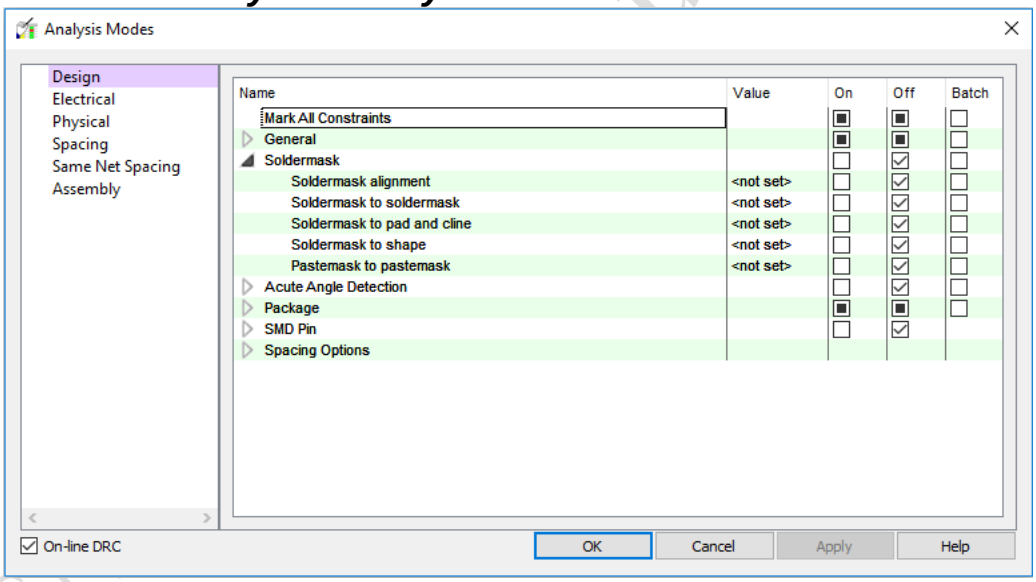
The Design Modes form controls whether specific design rule checks for planes, testpoint, and mechanical holes are triggered based on changes to the board layout.

- **Negative plane islands - C**heck for isolations when using a negative plane
- **Negative plane sliver** - Flags **"**slivers**"** or small undesired webs of copper between two objects, usually formed by placing antipads or thermal pads of pins or vias spaced too close to other padstack items or the negative plane boundary
- **Testpoint to component** - Specifies spacing checks between edges of testpoint pads and components

- **Testpoint location to component** - Specifies spacing checks between testpoint locations (center) and components
- **Testpoint under component** - Flags testpoints under components
- **Mechanical pin to mechanical pin** - Checks for a minimum spacing between mechanical holes
- **Mechanical pin to conductor** - Checks for a minimum spacing between mechanical holes and conductors
- **Pin to Route Keepout** – Checks to ensure that pins are not within a route keepout area
- **Minimum metal to metal** - Checks to ensure minimum metal to metal clearance is met
- **Duplicate drill holes** - Detects duplicate drill holes spanning the same layers
- **On-Line Inter Layer Checks** – Checks geometries between two different class/subclasses (More for Rigid Flex designs)

Design Options and Modes (Soldermask)

Analyze - Analysis Modes - Soldermask



Design Options and Modes

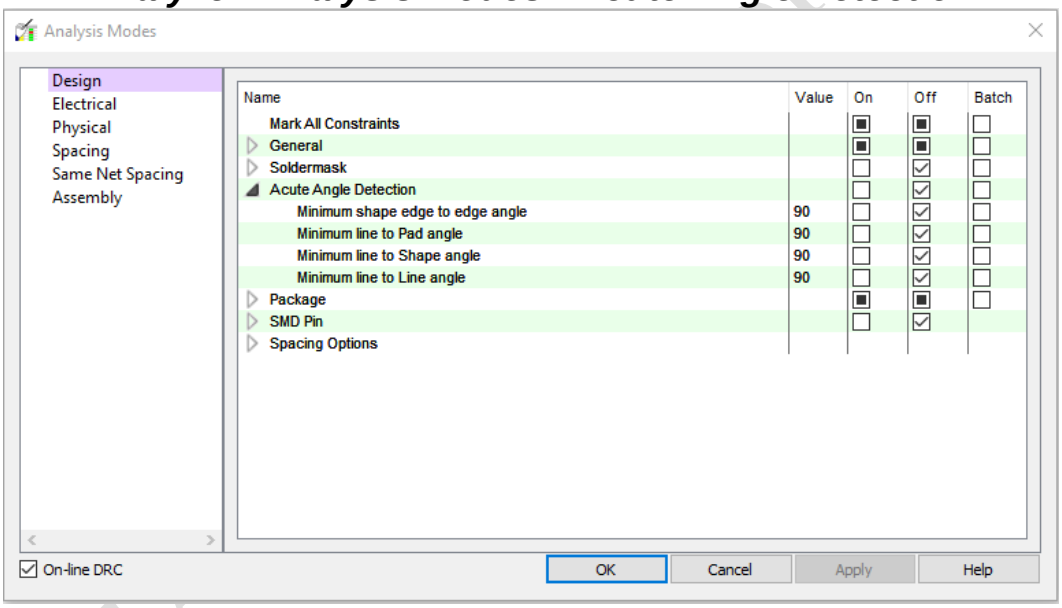
The Design Options (Soldermask) form specifies soldermask and pastemask parameters for the enabled Design Mode checks.

The Design Modes (Soldermask) form controls whether specific design rule checks for soldermask and pastemask are triggered based on changes to the board layout.

- **Soldermask alignment** - Specifies and checks the alignment tolerance required for the proximity of package soldermask to place_bound shapes and the pad soldermask to pad geometry
- **Soldermask to soldermask** - Specifies spacing checks for pad soldermask to pad soldermask, symbol soldermask to symbol soldermask, and symbol soldermask to pad soldermask
- **Soldermask to pad and cline** - Specifies spacing checks between the soldermask and pads and connect lines
- **Soldermask to shape** - Specifies spacing checks between the soldermask and shapes.
- **Pastemask to pastemask** - Specifies spacing checks for pad pastemask to pad pastemask and pad pastemask to package based pastemask

Design Options and Modes (Acute Angle Detection)

Analyze - Analysis Modes - Acute Angle Detection



Design Options and Modes

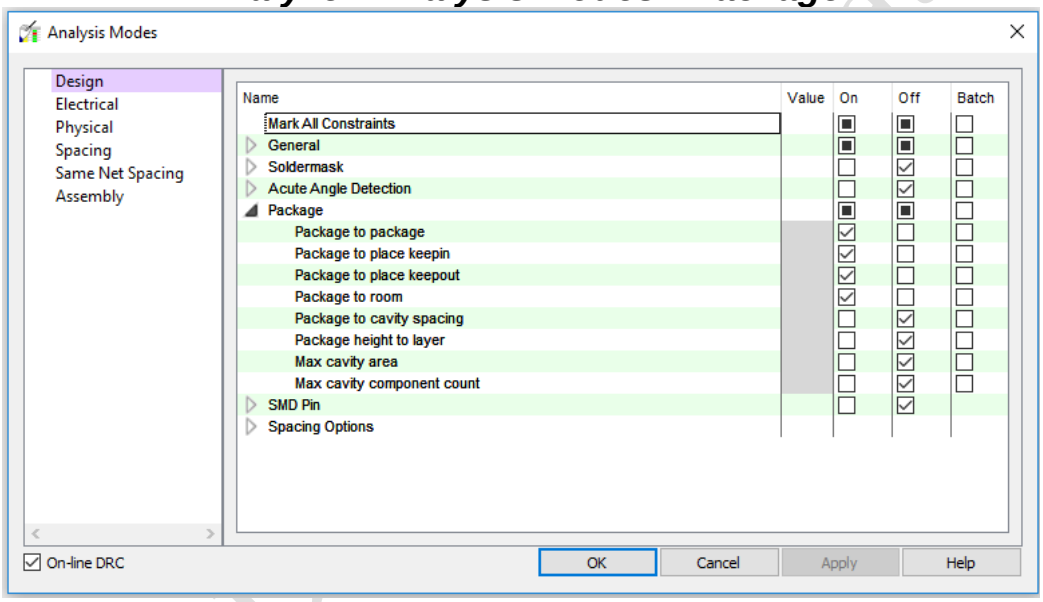
The Design Options (Acute Angle Detection) form specifies the allowed angle to be used to prevent an acute angle. The default angle for these checks is 90 degrees but may be set to any angle between 0 and 90.

The Design Modes (Acute Angle Detection) form controls whether specific design rule checks for acute angles are triggered based on changes to the board layout.

- **Minimum Shape Edge to Edge** – Checks whether the copper shape outline has an acute angle of less than the angle specified.
- **Minimum Line to Pad Angle** – Checks whether the connect line to pad entry has created an acute angle of less than 90 degrees.
- **Minimum Line to Shape Angle** – Checks whether the connect line to copper shape intersection has created an acute angle of less than 90 degrees
- **Minimum Line to Line Angle** – Checks whether the connect line to connect line intersection has created an acute angle of less than 90 degrees

Design Modes (Package)

Analyze - Analysis Modes - Package



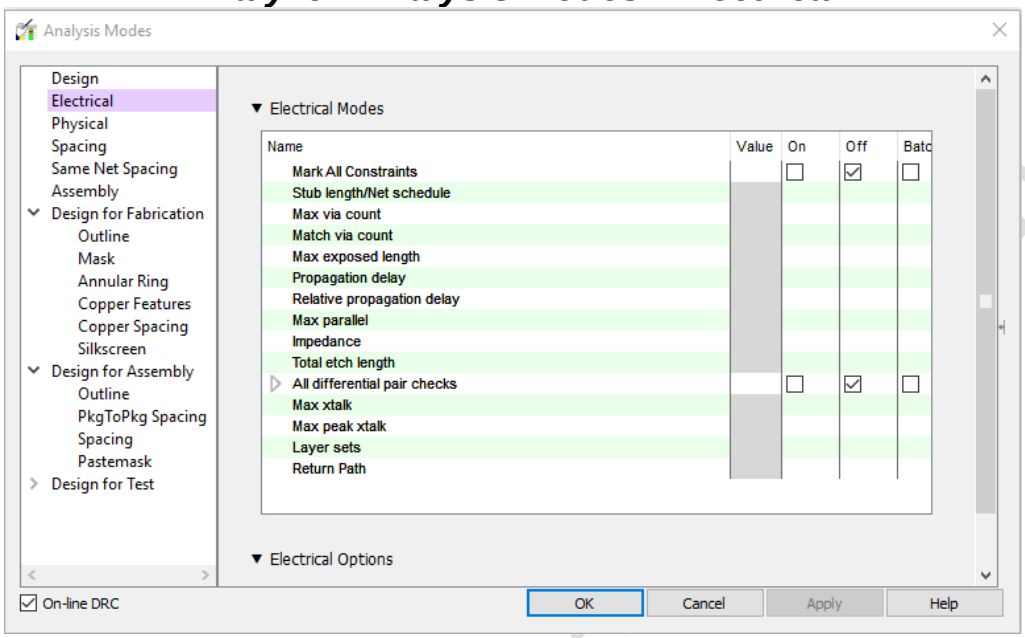
Design Options and Modes

The Design Modes (Package) window specifies whether the Package to Package, Package to Place Keepin, and Package to Place Keepout checks will be generated if there is any overlap between the appropriate type of shapes.

- **Package to package** - Flags packages that overlap one another
- **Package to place keepin** - Flags packages that extend beyond a place keepin
- **Package to place keepout** - Flags packages that extend inside a place keepout
- **Package to room** - Flags packages that are located in rooms to which they are not assigned
- **Embedded DRCs - Package height to layer** spec

Electrical Options and Modes

Analyze - Analysis Modes - Electrical



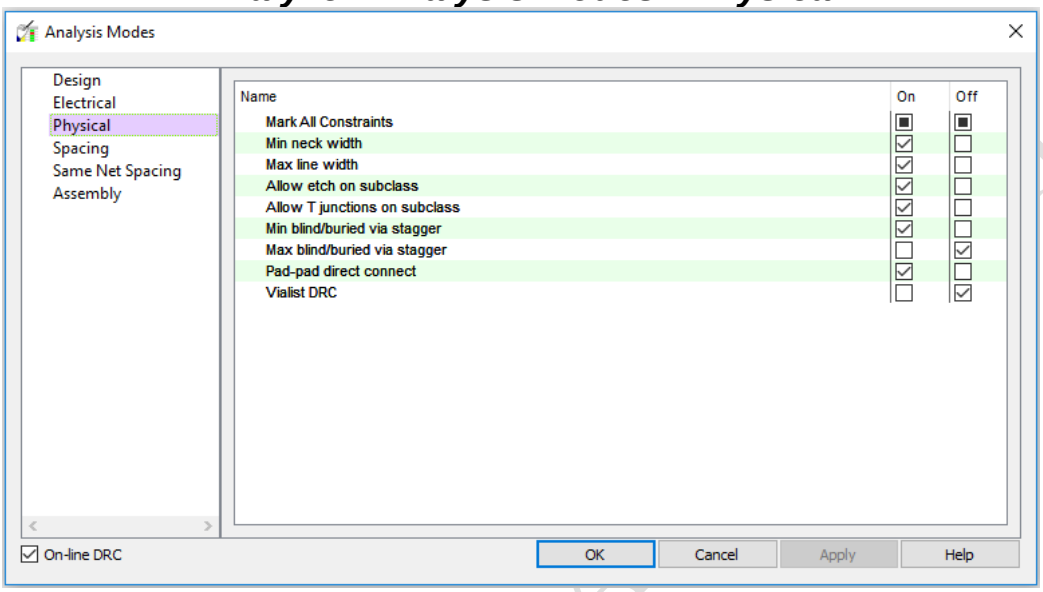
Electrical Options and Modes

The only Electrical Constraints included in the OrCAD PCB Designer Standard toolset are constraints for controlling the routing of Differential Pairs.

- **All differential pair checks** – Checks for phase control, uncoupled length, and minimum line spacing between the two differential pair nets.

Physical Modes

Analyze - Analysis Modes - Physical



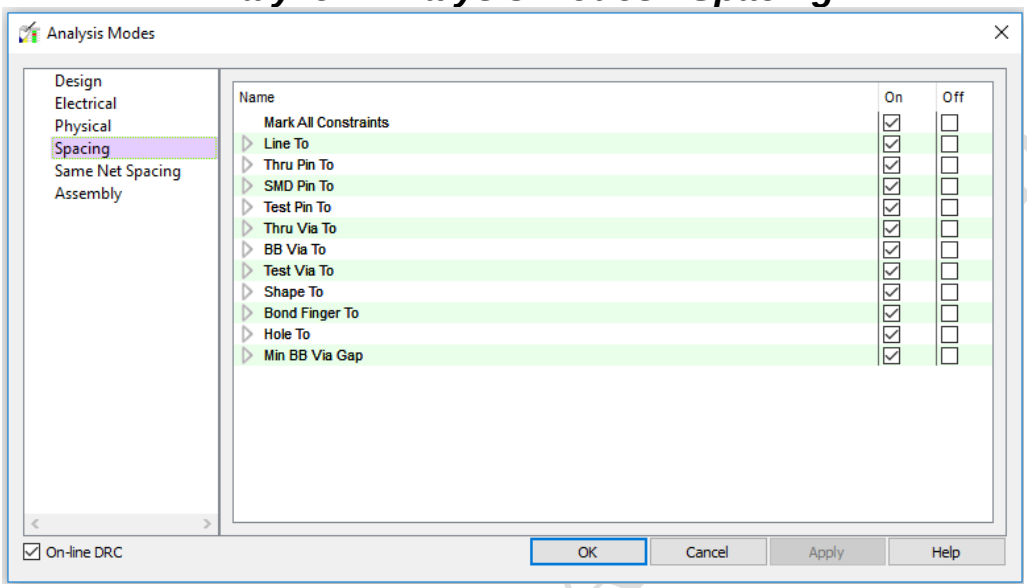
Physical Modes

The Physical Modes window specifies whether or not the respective physical constraints should be checked. Checks can be made for the following conditions:

- Min line width, Min neck width, and Max neck length
- Max line width
- Allow etch on subclass
- Allow T junctions on subclass
- Min and Max blind/buried via stagger
- Pad-pad direct connect, and Via list DRC.

Spacing Options and Modes

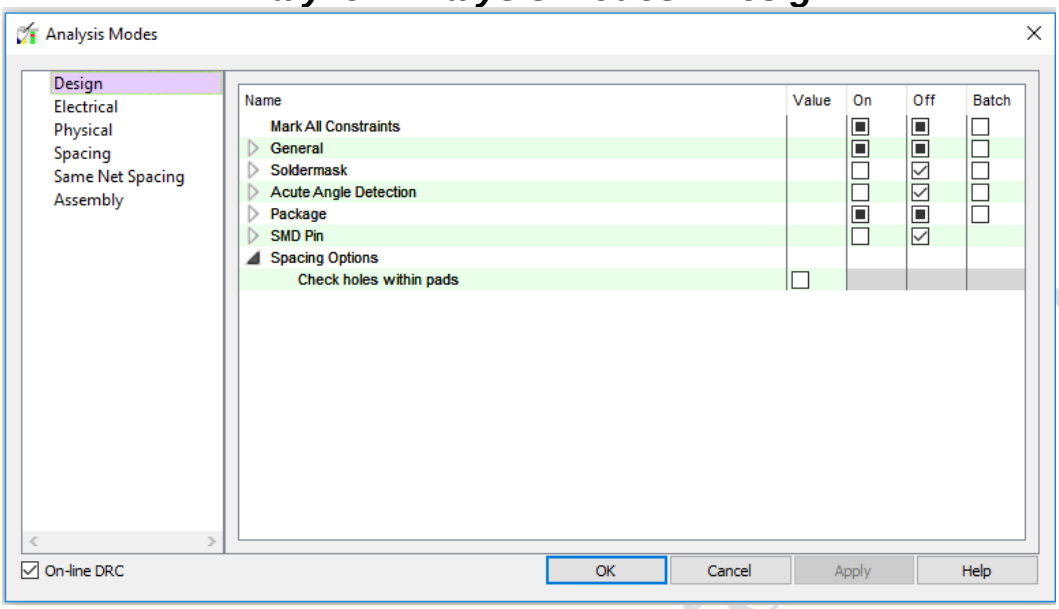
Analyze – Analysis Modes - Spacing



Spacing Modes

The Spacing Modes specify whether or not the respective spacing constraints should be checked. This mode enables or disables the testing of the exact spacing conditions between lines, pins, vias, shapes, holes, and blind and buried via gap.

Analyze - Analysis Modes - Design



Spacing Options

The Spacing Options form controls whether it is necessary to check the drill hole whether there are pads present or not.

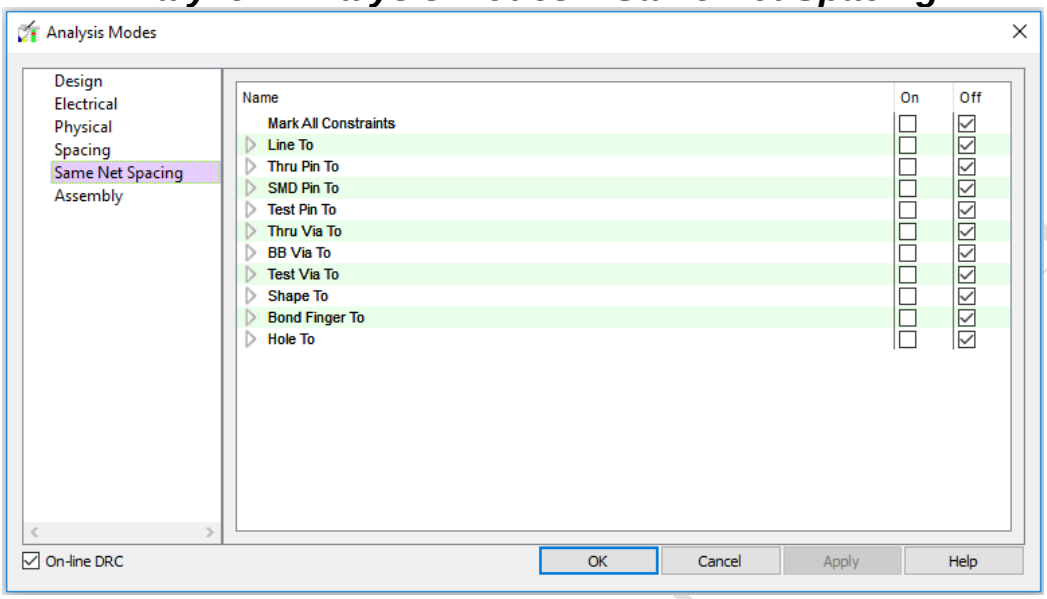
- **Check holes within pads** – When enabled drill-hole checks are run using the drill hole explicitly (the presence of pads associated with the drill hole is not relevant in this mode of the DRC calculation). In other words, the drill is checked whether a pad is present or notes.
- When disabled the drill-hole checks are only relevant when the pad is suppressed or undefined exposing the bare hole. This is the default configuration and is compatible with previous releases.

The Spacing Modes form specifies whether or not the respective spacing constraints should be checked. This mode enables or disables the testing of the exact same spacing conditions between lines, pins, via, shapes, bond fingers, holes, and blind/via gap.

The Spacing Modes cover these spacing conditions when they are applied to different nets. Example: an ENABLE via connect line near a RESET pin - spacing requirement of 8 mils.

Same Net Spacing Modes

Analyze – Analysis Modes – Same Net Spacing



Same Net Spacing Modes

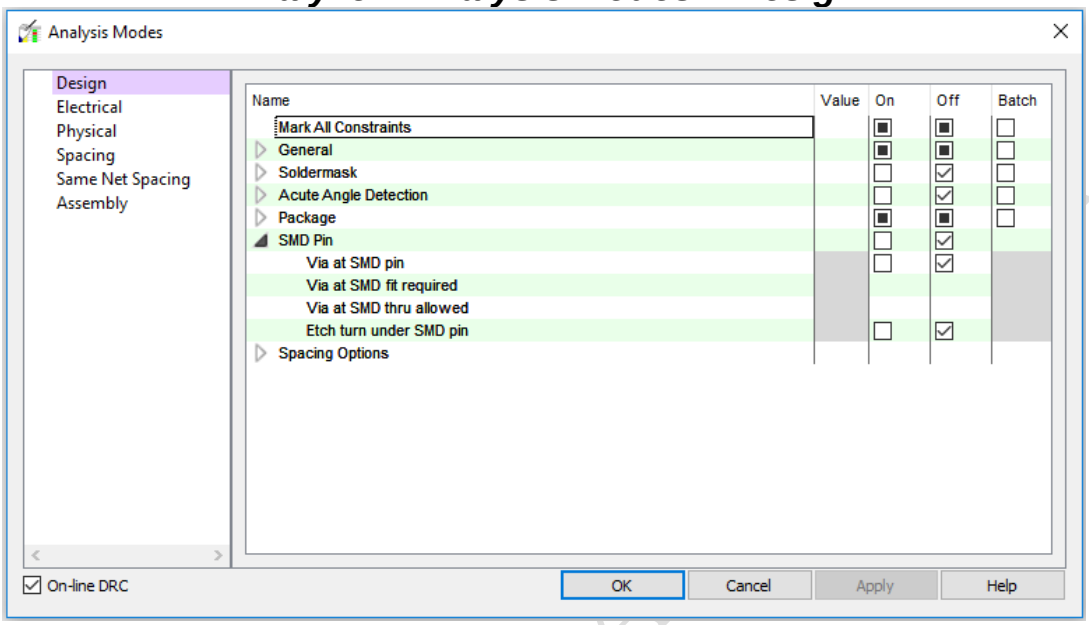
Like the Spacing Modes, the Same Net Spacing Modes specifies whether or not the respective spacing constraints should be checked. This mode enables or disables the testing of the exact same spacing conditions between lines, pins, via, shapes, bond fingers, holes, and blind/via gap.

The Same Net Spacing Modes cover these spacing conditions when they are applied to the exact same net so that you can place the elements closer to each other. Example: an ENABLE via close to an ENABLE pin - spacing requirement can be 4 mils.

Note If any of the spacing categories are blank then they are not being checked for. If any spacing category box has a gray square in it then not all selections in that category is enabled for checking.

SMD Pin Modes

Analyze – Analysis Modes – Design

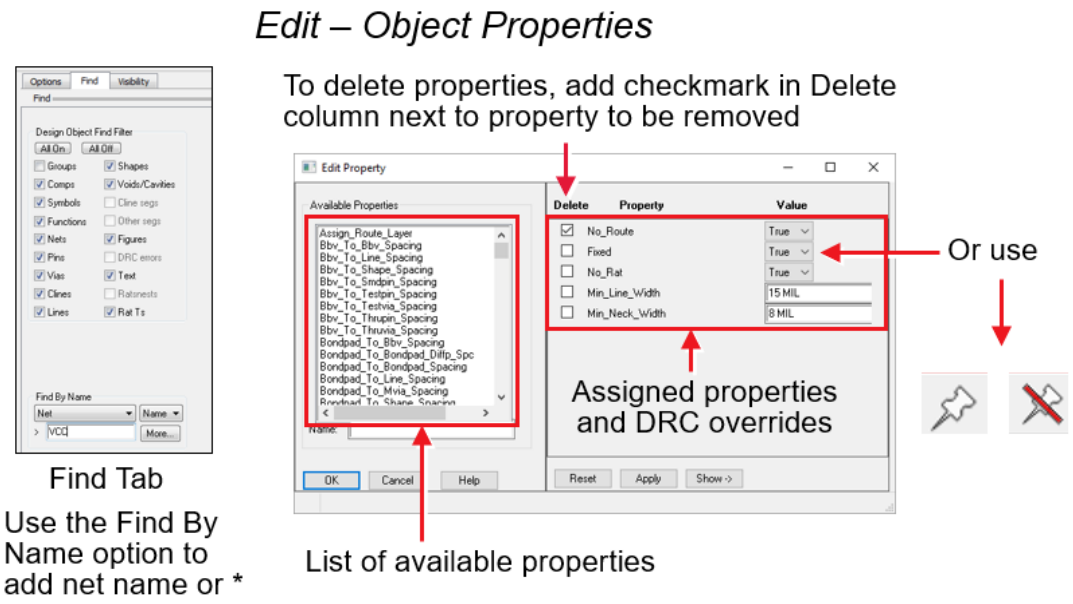


SMD Pin Modes

The SMD Pin Mode ensures that the placement of vias is properly contained within SMD pads.

- The Via at SMD fit
  - *On* denotes that the 'via' pad must be contained within the SMD pad.
  - *Off* denotes that the center of the 'via' cannot extend beyond the edge pad.
- The Via at SMD thru
  - *On* denotes that the thru vias are allowed in SMD pads.
  - *Off* denotes that the thru vias are not allowed in SMD pads.
  - The Etch turn under SMD pin checks to detect etch compensation buried within the pad.

Property Assignments and Changes



It is important to understand that there is overlap between properties and constraints. Properties override constraint values. For example, a design contains a special net class with an assigned physical rule set. This rule set calls out a Minimum Line Width of 8 mils. If the property MIN_LINE_WIDTH is set to 15 mils and is assigned to one or more nets in the net class, those nets will obey the property value rather than the physical rule set value. Therefore, in this case, the net will be routed with a 15-mil line rather than an 8-mil line.

Note A constraint override added in the Constraint Manager behaves the same as a property added using the ***Edit – Object Properties*** command. So, if the MIN_LINE_WIDTH property is added to a net using ***Edit – Object Properties***, it will be displayed in the Constraint Manager as an override. And, an override added in the Constraint Manager will be displayed as a property if that net is selected when in the ***Edit – Object Properties*** command.

When you select the ***Edit – Object Properties*** command, you must first identify the elements for property assignment. Use the ***Find Filter*** form to select elements either by pick or by element type plus name or list. You can use the ***Find by Name*** section of the Find Filter to identify elements with existing properties. The PCB Editor tool then displays the properties available for that element type.

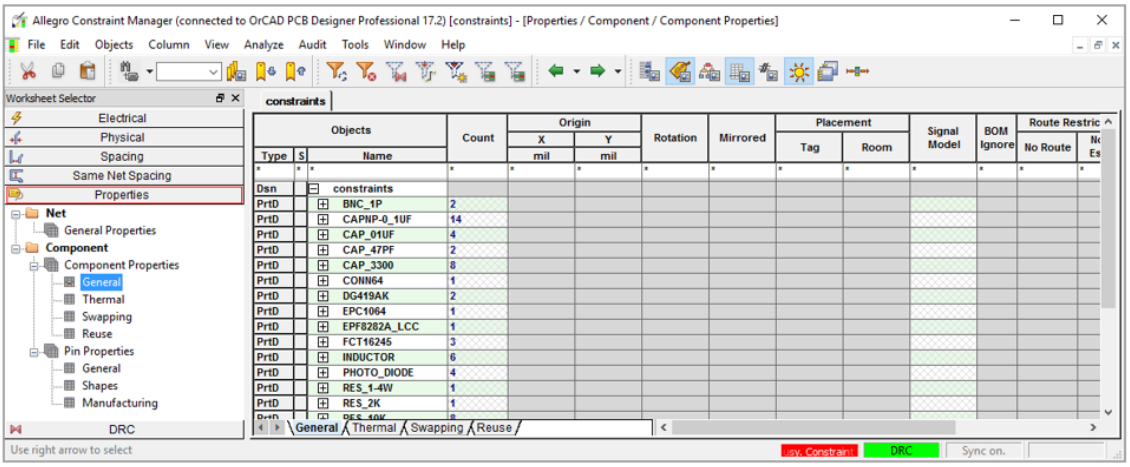
Once an element is identified, the ***Edit Property*** form appears. The ***Edit Property*** form lets you assign, delete or modify properties on design elements.

Select the properties you want to attach from the scroll list and click on the ***Apply*** button. Some properties require values (for example, min_line_width) while others do not. To modify existing property values, follow the same process. To remove an existing property, click the ***Delete*** button next to the selected property before applying.

The toolbar icons ***Fix*** and ***Unfix*** have been added as an aid in quickly adding and deleting the fixed property to any object.

Adding Properties in Constraint Manager

The Constraint Manager allows you to add properties to Nets and Components. In the Component folder it allows the properties to be applied as Component Properties or Pin Properties



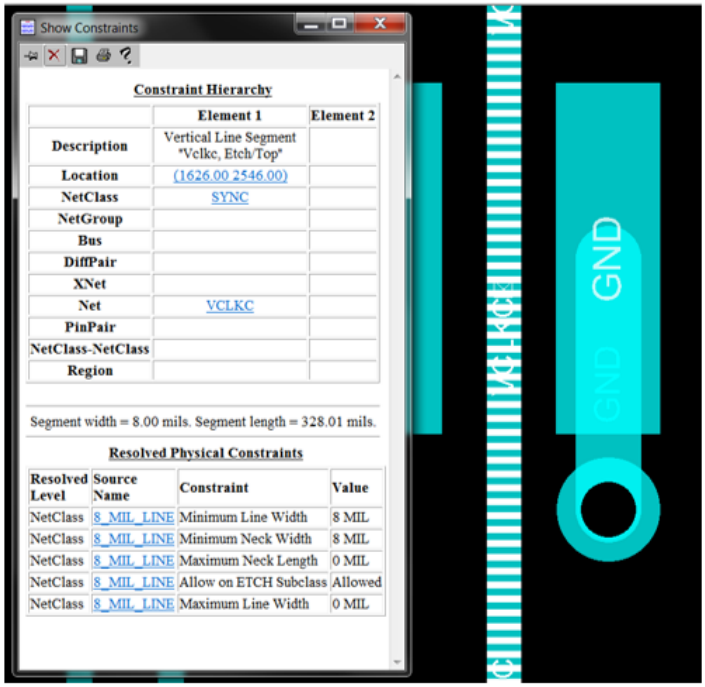
The Constraint Manager has a worksheet for the purpose of adding or editing properties on your Nets, Components and Pins. It contains a listing of all the available properties for each type of elements on one spreadsheet. You can use this one interface to add properties to these objects to help you manage design rules from front to back. You would use this form instead of going through the ***Edit – Object Properties*** command.

Physical Constraint Resolution

Check – Constraints (Single select)

Constraint Hierarchy
- Description
- X/Y location
- Net name

Resolved Physical Constraints
- Constraint set name
- Constraint set rules
- Constraint values



While routing your design, you may wonder why the routing of a net has certain physical characteristics, like why is it routed at the width displayed. You can use the ***Check - Constraints*** command to generate a report of the constraint information.

To show the physical attributes, execute a single select on an element. The information displayed will be in two sections:

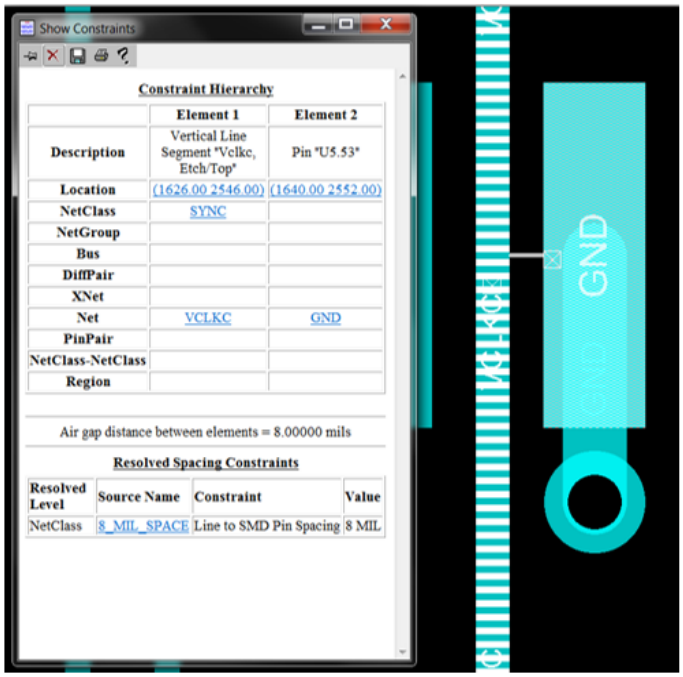
- The top or **Constraint Hierarchy** section will include information about the element picked, such as the x/y location, net name, and so on.
- The bottom or **Resolved Physical Constraints** section will display the Constraint rules used for the selected item such as the Constraint set name, constraint set rules, and the constraint values.

Spacing Constraint Resolution

Constraint Hierarchy
- Description
- X/Y location
- Net name

Resolved Spacing Constraints
- Constraint set name
- Constraint set rules
- Constraint values

Check – Constraints (Second Select)



While routing your design, you may wonder why the routing of a net has certain spacing characteristics, like why is the air gap between the route and a pin a certain value. You can use the ***Check - Constraints*** command to generate a report of the constraint information.

To show the spacing attributes, drag a window around the two elements. The information displayed will be in two sections:

- The top or **Constraint Hierarchy** section will include information about the elements picked, such as the x/y locations, net names, and so on.
- The bottom or **Resolved Spacing Constraints** section will display the Constraint rules used for the selected item such as the Constraint set name, constraint set rules, and the constraint values.

DRC Marker Display

DRC markers store the following information about a design rule violation:

- To display a filled DRC marker, enable ***display_drcfill*** variable in the ***Display folder – Visual subfolder*** of the ***User Preferences***
- DRC class, subclass, and location
- Type of constraint set (physical or spacing)
- Name of constraint set
- Constraint type being violated (for example, *Line to Route keepout Spacing*)
- Data concerning first element in violation (type of element, location, refdes, if a package/part, and so on)
- Data concerning second element (if there is one) in violation (type of element, location, refdes, if a package/part, and so on)

DRC markers have two characters, one in each side of the 'bow-tie', that identify the type of constraints violation being marked. Each character is a key as to what type of violation exists. In the example shown, the "L" represents a "Line." The "K" represents a "Route Keepout". So therefore, in this case, this is a line to routing keepout violation. In other words, a piece of etch exists in an area that has been identified as a routing keepout area.

To display the DRC filled, as shown in the example, enter on the PCB Editor command line "***set display_drcfill***" or use the ***User Preferences Editor***. The ***display_drcfill*** option can be found under the ***Display*** folder – ***Visual*** subfolder.

Lab

Lab 7-4: Working with Properties

Learn how to add, delete and modify property values using both the Edit Properties form and the Constraint Manager.

- Attach properties to components and nets
- Show existing properties on design elements
- Delete properties

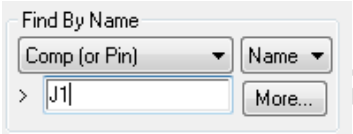
The following lab will let you familiarize yourself with the process required to work with the design constraints and add, modify and delete properties. You will learn how to modify the design constraints, attach properties to nets, components and areas, show existing properties, and delete properties from database elements.

Lab 7-4: Working with Properties

Objective: Attach, display, and delete properties in a design.

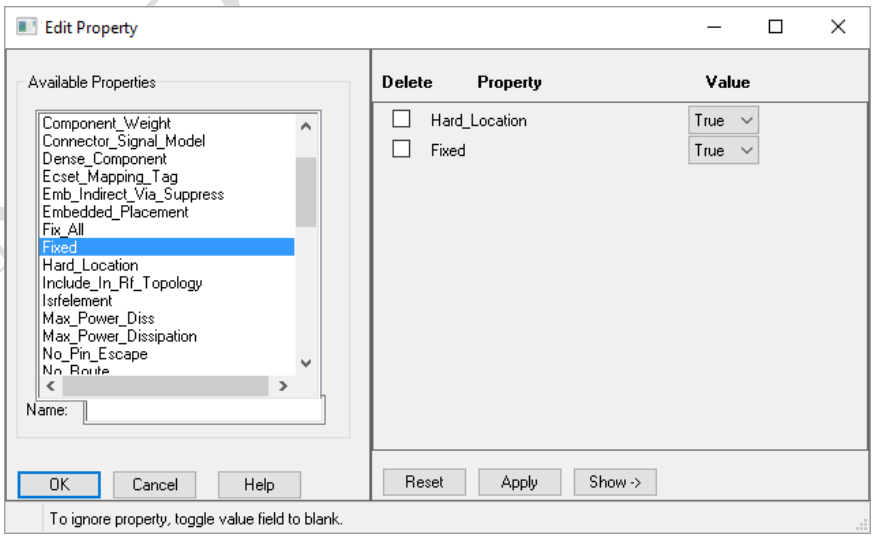
Attaching Properties to Components

1. Start the PCB Editor and open the `constraints.brd` file in your working directory if it is not already the open design.
2. Choose ***Edit – Object Properties*** from the top menu.
3. In the ***Find by Name*** section of the ***Find*** tab, click the scroll button to set the field description box to ***Comp (or Pin)***.
4. Click in the text entry field (>), and enter: **`J1`**



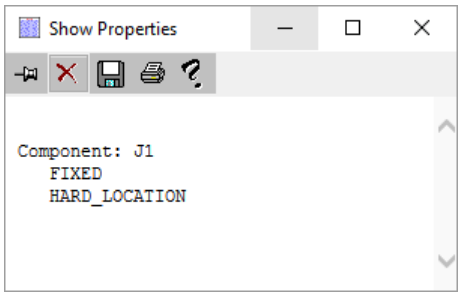
When you press the Tab key, the ***Edit Property*** and ***Show Properties*** forms appear. Notice that the J1 connector currently has no properties attached to it.

5. In the ***Edit Property*** form, select the ***Hard_Location*** and ***Fixed*** properties from the scroll list.
   These properties appear on the right.
6. Toggle the Property Values to ***TRUE*** if required.



7. Click ***Apply***.

In the ***Show Properties*** window, the properties ***HARD_LOCATION*** and ***FIXED*** are added to component J1.



Note The FIXED property prevents the component from being moved. The HARD_LOCATION property prevents the component reference designator from being changed during the automatic rename process.

8. Click ***OK*** to close the ***Edit Property*** form and ***Show Properties*** window.

Attaching Fixed Properties to Symbols Using Icons

In the last lab, you added properties by using a form. An easier way to add the FIXED property to an object is explained here. You will add a FIXED property to the two BNC connectors and the board outline. This step can also be done while you're defining the template board design.

1. Select the ***Fix*** icon.

2. In the Find Filter, select the "***All off***" button, then turn on only ***Symbols***.
3. Click on the two **BNC connectors** on the right side of the board and the board outline.
   This adds a FIXED property to these three objects, so they won't be inadvertently moved while placing other components.

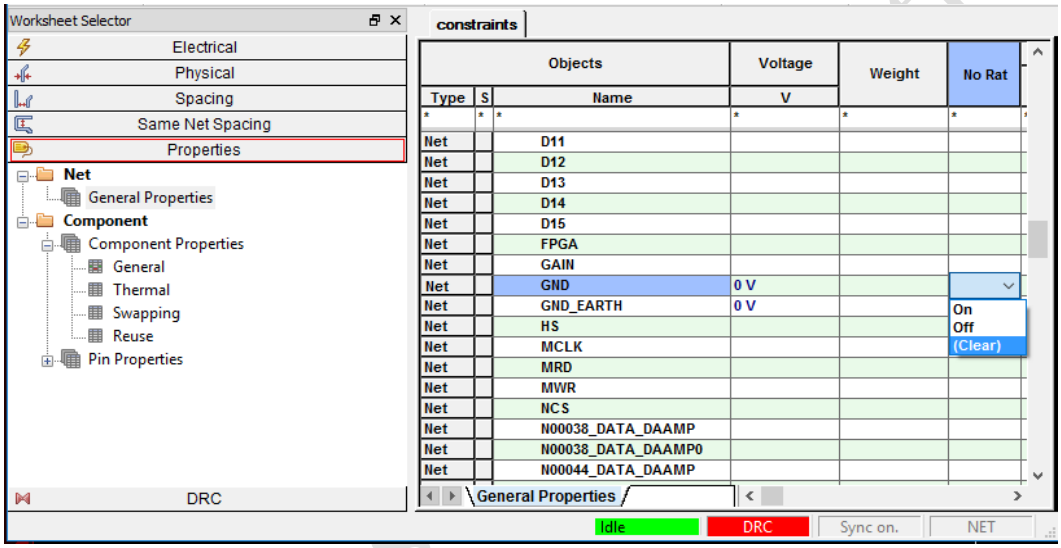
   If you used the ***Edit – Object Properties*** on any of these three objects, you will see that the ***FIXED*** property appears in both the ***Edit Property*** and ***Show Properties*** forms.

Note There is also an ***Unfix*** icon available to delete the FIXED property from symbols. If you select the Right-Mouse-Button while in the command, you will see a menu selection that will ***Unfix All***. We will not be using this command on our design at this time.

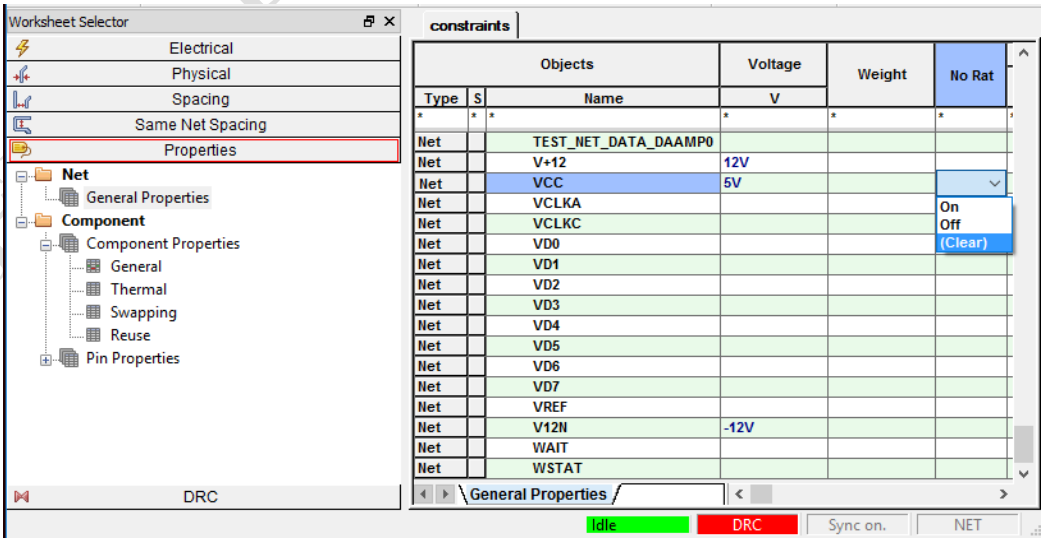
Attaching Properties to Nets in the Properties Domain of the Constraint Manager

In this section of the lab you will work with net properties in the Constraint Manager.

1. Choose ***Setup - Constraints*** from the top menu.
2. Click on the ***Properties*** domain in the ***Left Pane*** to open the ***Properties*** selections.
3. Select the ***General Properties*** workbook in the ***Net*** section of the ***Properties*** Domain.
4. Scroll down to the ***GND*** and ***GND_EARTH*** nets and add the value ***0V*** for their ***Voltage*** properties.
5. Using the pulldown in the ***No_Rat*** property column, select ***Clear*** to remove the ***No_Rat*** property from the GND net.



6. Scroll down to the ***V+12, VCC and V12N*** nets, add their Voltage properties as shown in the figure below and ***Clear*** the ***No_Rat*** Property from ***VCC***.



Note Ideally, the ***VOLTAGE*** properties would be added in the schematic. However, if not already present, they may be added in the ***Properties*** Domain of the ***Constraint Manager***, or by using the ***Setup – Identify DC Nets*** command that will be discussed later in this class.

Important

Another way to toggle the NO_RAT property 'Off' for the DC Nets is to use ***Setup – User Preferences***, select the ***Logic*** Category, and toggle '***On***' the ***dcnets_delete_norat*** variable. This will automatically turn off the ***NO_RAT*** property when you assign the Voltage property to the nets.

Saving the design

1. Choose ***File - Save*** from the top menu.
   A message window appears prompting you to decide whether you want to overwrite the existing `constraints.brd` file.
2. Click ***"Yes"***.
   The `constraints.brd` file is saved to disk.
3. Choose ***File - Exit*** from the top menu to exit the PCB Editor software.

End of Lab

Lesson 8: Component Placement

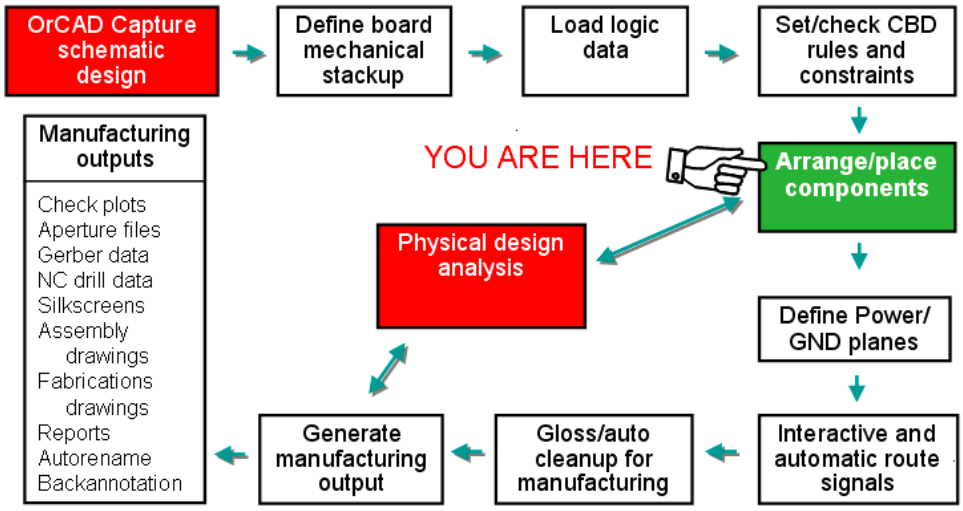
Learning Objectives

In this lesson, you will:

- Use floor planning to organize the placement of components with the ROOM property
- Assign reference designators to preplaced parts
- Interactively place components using various commands

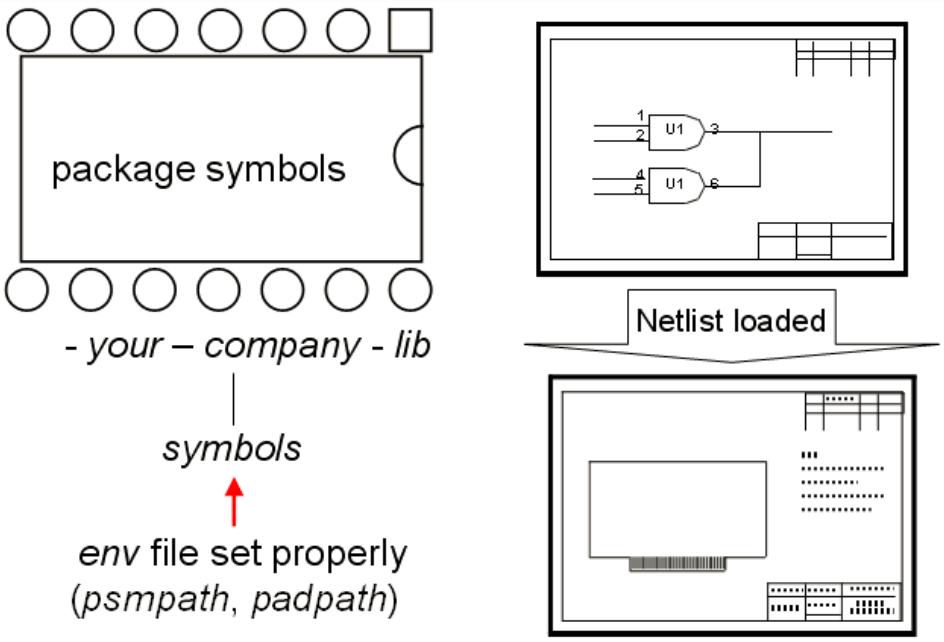
In this section, you will place components on your board. You will learn how to create Rooms and assign components to rooms, how to assign reference designators to preplaced symbols, and how to quickly place components. You will also learn the interactive commands available when working with placement.

Design Layout Process



This design flow is used throughout the course. Each box in this flow represents a common step in the design of a printed circuit board. As indicated in the flow, the Arrange/place components feature will now be discussed.

Placement Prerequisites

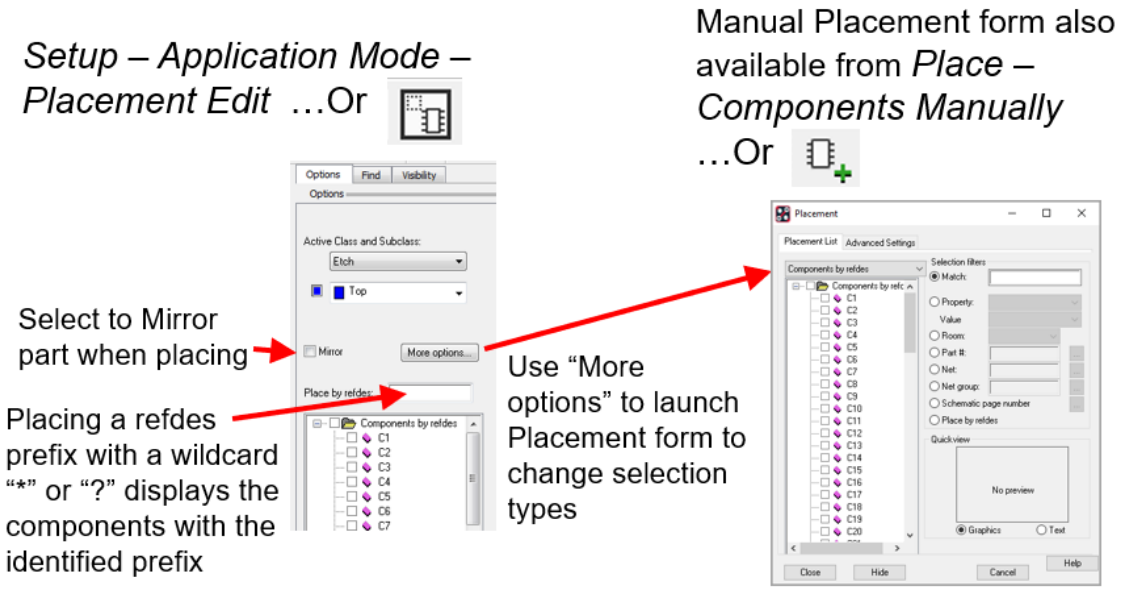


It is important to remember how the PCB Editor determines where the footprints and padstacks are located on disk. The variables PSMPATH and PADPATH are used to determine the locations on disk of the footprints and padstacks, respectively. These variables are defined in the *env* file and can be set and modified using the User Preferences Editor.

The prerequisites for manual placement are:

- **Symbols** - The package symbols and padstacks required for parts in the netlist must exist. Again, the PSMPATH and the PADPATH point to the locations of the symbols and padstacks.
- **Netlist** - You must load a schematic database into an PCB Editor design file.
- **Alternate Package Symbols** - If you plan to select alternative package symbols during manual placement, the alternate symbol definitions must be contained in the appropriate part definition files.
- **Floorplanning** - You can create a "block diagram" of the logical functions that need to be arranged on the board by using Rooms. Specify this part property within the schematic environment.
- **Package Keepouts** - If your template design file did not contain package keepouts, add them before you begin placing components, by selecting ***Outline - Package Keepout***. This step is also optional.

Placement Edit Application Mode



The Placement application mode is a tuned, high performance environment designed to increase efficiency during component placement sessions. Find filter settings are limited to those elements typically involved in placement such as symbols, pins and rat tees. This reduces unnecessary cycling of unwanted elements that do not contribute towards placement activity.

In this mode, it is still possible to perform non-placement functions like add connect or slide. However, context sensitive and auto executed commands are biased towards component placement functions.

The list of unplaced components is listed in the Options tab window. This form is an abbreviated version of the place manual user interface. You can toggle on the ***Mirror*** option so that all parts placed are automatically mirrored to the opposite side of the board. The ***Place by refdes*** field is used to enter in reference designators. Wildcard characters of "*******" and "***?***" are also accepted in this field.

The ***More options*** button launches the place manual form. You can use this form to further refine the parts that are selected to be placed. Upon selecting the Close button in this form, the parts populated in the Options window will be updated.

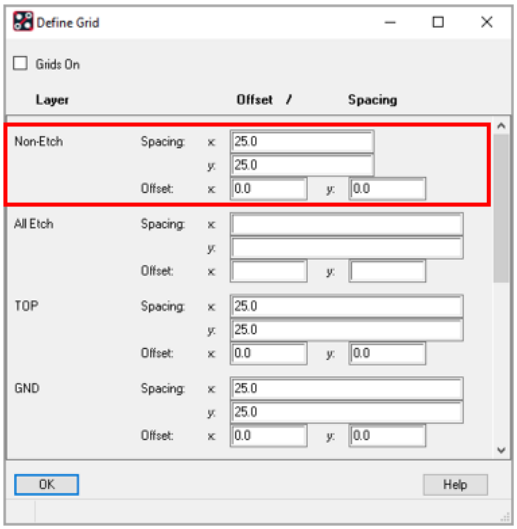
Placement Grid

When placing parts use the Non-Etch section of the Define Grid form

You can access the Define Grid form from numerous methods:

- *Setup – Grids*
- *Right-Mouse-Button – Quick Utilities – Grids*
- *Setup - Design Parameters - Display tab - Setup Grids*

Toolbar icon toggles Grid ON or OFF



The grid used for placement is the **Non-Etch** grid. The origin of the package symbol which is defined during symbol creation, snaps to the Non-Etch grid when placing parts with your mouse. The origin of the placement grid is the origin of the design file.

You can access the Define Grid form from a variety of methods:

- Select ***Setup - Grids*** from the top menu
- Use the ***Right-Mouse-Button*** to select ***Quick Utilities – Grids*** from the pop-up menu
- Select ***Setup - Design Parameters - Display tab - Setup Grids*** from the top menu

You can toggle the grid ON or OFF using either:

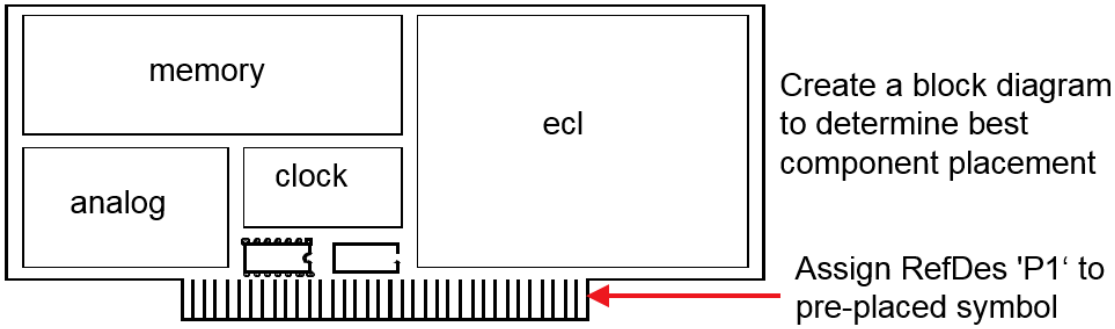
- ***Grids On*** option in the ***Define Grids*** form
- Using the ***Grid Toggle*** toolbar icon.

Remember, you can use the "x" command with the coordinates to place a part in your design that does not align with the grid, such as connectors; example x 2030 1562.

Placement Strategy

Placement Strategy:

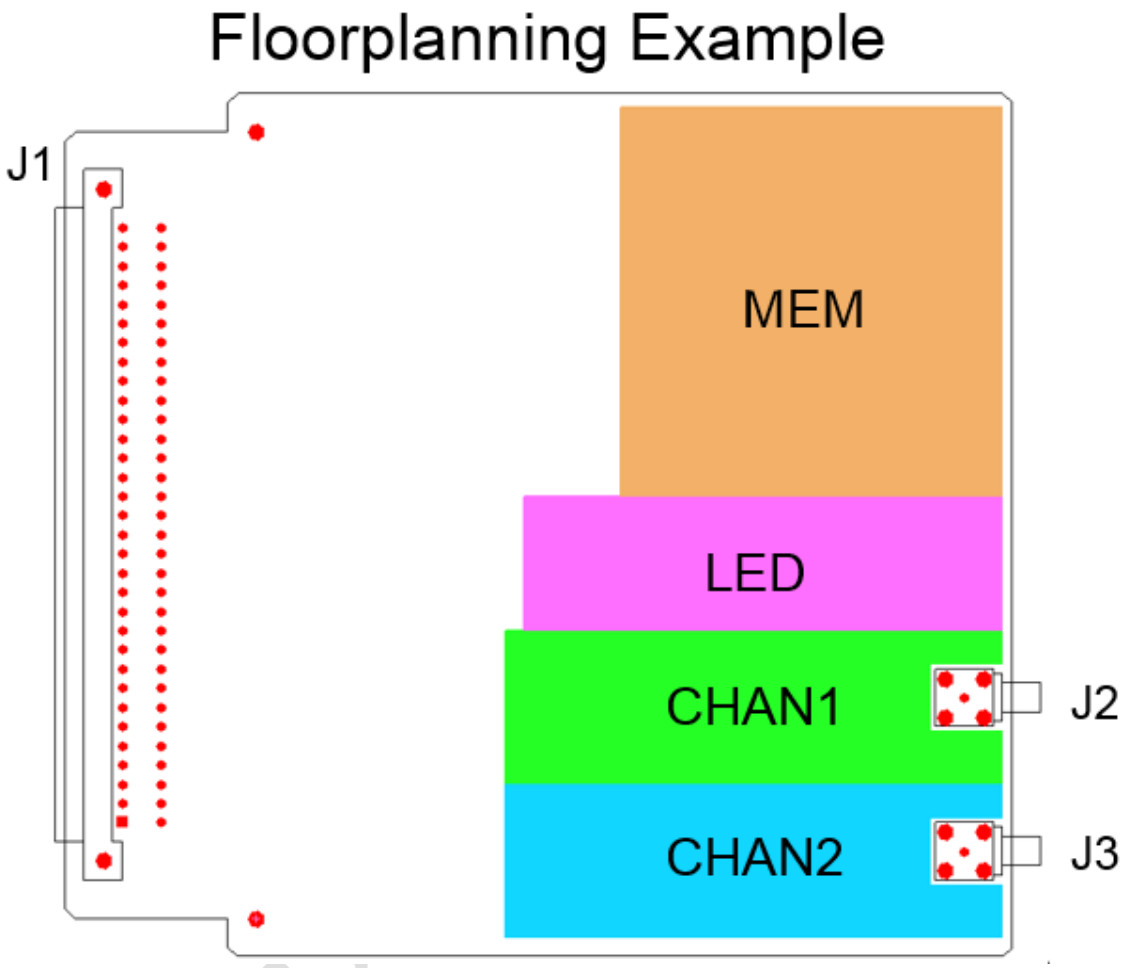
- Create rooms for floorplanning
- Assign reference designators to "preplaced" devices
- Place I/O bound devices
- Place critical logic functions
- Evaluate and revise placement
- Place bulk decoupling and bypass caps
- Use reports to aid placement process



1. **Floorplanning** - Create a "block diagram" of the logical functions using Rooms.
2. **Assign reference designators to any pre-placed devices** - Use the ***Place - Assign RefDes*** command to correlate any pre-placed package symbols within the logic in the database (such as J1, J2, etc.).
3. **Place IO bound devices** - Place any parts that send or receive nets from backplane connectors to minimize overall net length.
4. **Place critical logic functions** - Place clock circuits, memory arrays, buffers, controllers, and address buses. (See Floorplanning on the next page.)
5. **Place less critical circuits** - Place data buses and random logic, interactively.
6. **Evaluate and revise placement** - Use ratsnest display, net highlighting, gate and pin swapping, density evaluations, interactive net scheduling, autorouter, DFA, and Signal Analysis tools to evaluate the component placement.
7. **Place bulk decoupling caps** - Perform this step last. If embedded split planes are required for multiple voltages, place decoupling caps near associated ICs accordingly.

Note Some database reports may be useful during the placement process (for example, nets list, components list, bill of materials, and placed or unplaced components list). Also, you can use Etch Length by Net Report to flag potential net length problems prior to routing.

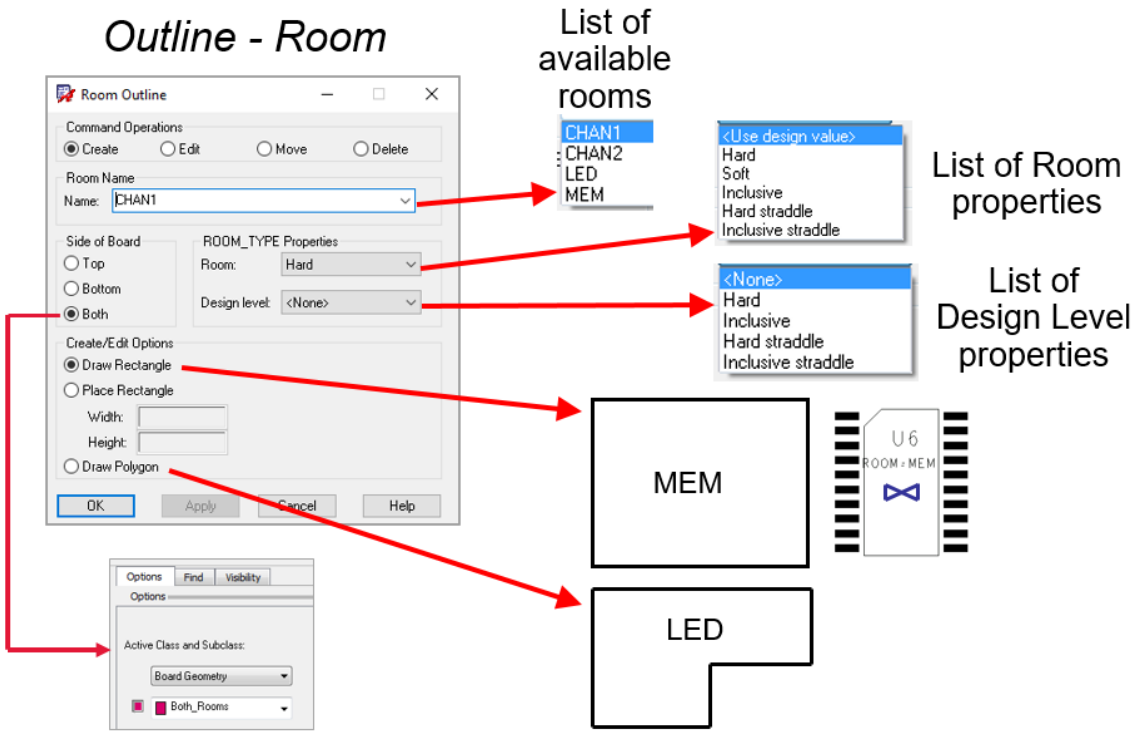
Floorplanning with Rooms



Rooms are confinement areas that provide a useful method for grouping components. You can force automatic placement to occur with specific components and cause them to be placed within specific rooms.

You can attach a room property to components during schematic creation, netlist creation, or at any time while in the PCB Editor design. Room boundaries are closed polygons on the TOP_ROOM, BOTTOM_ROOM, or BOTH_ROOMS subclasses of the BOARD GEOMETRY class.

Creating a Room



Use this Room Outline form to add rooms to your board for component placement.

Command Operations:

- **Create -** Allows you to create a new room.
- **Edit -** Edits an existing room.
- **Move -** Moves an existing room.
- **Delete -** Allows you to delete a room.

Room Name Area:

- **Name -** Provides the names of the rooms defined within the design in a drop-down list. When **Create** is active the list will contain the names of the new rooms. When active in **Edit**, **Move** or **Delete** modes, select from a drop-down list of available rooms to perform the task on. The room name matches the property name given to the symbols.

Side of Board:

- **Top, Bottom, Both -** Defines which side of the board the components assigned to a room will be placed on

ROOM_TYPE Properties

Component	Soft	Hard	Hard_straddle	Inclusive	Inclusive_straddle
Member in room	No DRC	No DRC	No DRC	No DRC	No DRC
Member straddling room	No DRC	DRC	No DRC	DRC	No DRC
Member outside of room	No DRC	DRC	DRC	DRC	DRC
Non-member in room	No DRC	DRC	DRC	No DRC	No DRC
Non-member straddles room	No DRC	DRC	DRC	No DRC	No DRC

Room Properties - The package boundary of the part is used for checking purposes

- **Hard -** DRCs are created when a part belonging to the room (member) is not placed entirely within the room boundary or if a part not belonging to the room (non-member) is placed within the room.
- **Soft** - No DRC errors are ever created. Use this option as a guide for placement.
- **Inclusive** - Like HARD, DRCs are created when a part belonging to the room (member) is not placed entirely within the room boundary but allows other components (non-member) to be placed in the room without a DRC.
- **Hard Straddle** – Member parts may straddle, but not be outside the room boundary. DRCs are also created if a non-member part is placed within the room boundary.
- **Inclusive Straddle** - Any components, members and non-members, may be placed in or straddle the room boundary.
- **Design Level** - Controls behavior for all rooms in the design without an assigning a ROOM_TYPE property to each room. If no ROOM_TYPE assigned SOFT behavior is used.

Note With the exception of the Soft property, all ROOM_TYPE properties will create a DRC when a part belonging to the room (member) is entirely outside the boundary of the room.

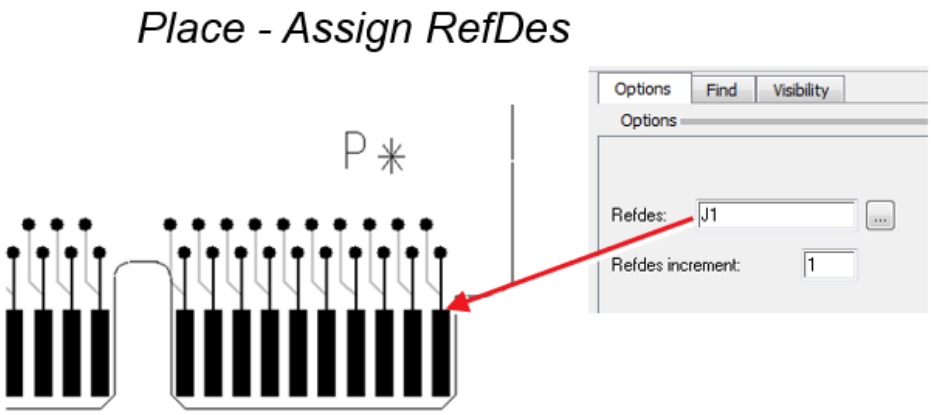
Create/Edit options:

- **Draw Rectangle -** Allows you to create and size a rectangular room
- **Place Rectangle -** Allows you to define and place a rectangular room per your specified dimensions
- **Draw Polygon -** Allows you to create a polygonal room

While in Edit mode:

- **Available room area used** - Shows the percentage of the area that the components will require
- **Autosize -** Automatically resizes the selected room to the percent specified

Assign RefDes Command



Associates a preplaced footprint with a logical part in the board database
Placeholder prefix does not have to match the prefix of the assigned reference designator

Use the ***Place*** **>** ***Assign RefDes*** command to map any package symbols to reference designators in the database. These are package symbols you previously placed manually with the Place - Manually command, such as the three connectors you placed in your `template.brd`.

Enter the reference designator you want to assign in the Refdes field of the ***Options*** tab or select the "browser" button to bring up a list of all the reference designators that still require placement and select a part from the list. Select the corresponding package symbol you wish to assign to the reference designator. When you select the part, you must select on some piece of graphics associated with the package symbol, such as one of the pins, a part outline, etc.

When you select on a part, the system will first determine which package symbol is defined in the schematic for the reference designator identified in the Options tab. It will then check to make sure the package symbol you selected in the design matches the package symbol specified in the schematic. If the two symbols are identical, the graphical reference designators will be updated, and the pins will be assigned to the appropriate nets. If the symbols do not match, an error will be reported in the command window and the reference designator will not be assigned.

After successful assignment of a reference designator, the reference designator in the Options tab is automatically incremented. For example, after you assign reference designator 'J1', the field in the Options tab will increment to 'J2', and so on, unless otherwise specified in the Options tab.

Labs

Lab 8-1: Floorplanning

- Organize areas of the board to place parts with the ROOM property
- Add rooms

Lab 8-2: Assigning Preplaced Packages

- Associate preplaced footprints with logical parts from the netlisted database

Lab 8-1: Floorplanning

Objective: Create a floorplan by adding two rooms for component placement.

Each design has unique placement requirements. For this reason, floorplanning is performed after the logic has been loaded into the template design file.

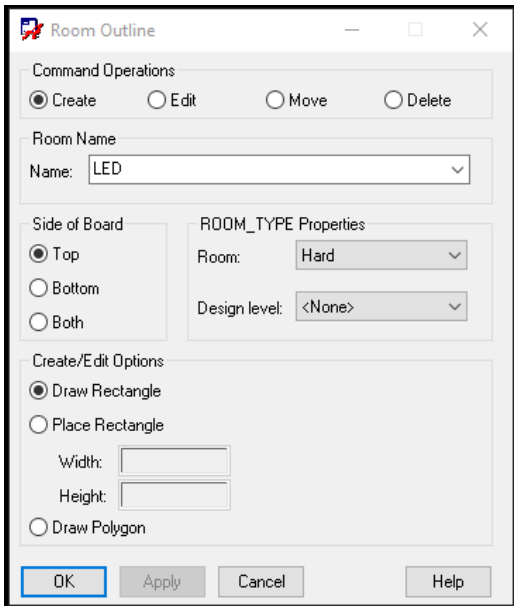
Opening Placement Board File

1. Start the PCB Editor if it is not already running.
2. Choose ***File - Open*** to open the `placement.brd` file located in the ***PCB_Designer/solutions*** folder.
3. Select ***File – Save As*** from the top menu and save the `placement.brd` in the ***PCB_Designer/project2 – allegro*** directory.
4. Use the ***Display - Zoom - Fit*** command to fit the board to your work area.

Adding Rooms

The placement.brd already has two rectangular rooms defined for placement on Both sides of the board. In the following exercise, you will add two more rectangular rooms, one for Top side and the other for Both sides. You will also assign them each a name that was read into the database from the schematic. Each set of coordinates you enter become the diagonal corner of a rectangle.

1. Choose ***Outline - Room*** from the top menu. The ***Room Outline*** form displays.
2. Fill out the form as you see in the figure to the right:



Note Do ***NOT*** click ***OK*** in this form until you have completed creating all of your rooms. The OK button closes out this command.

3. At the PCB Editor command line, enter the following:

```
x 1400 2200
x 3900 1500
```

Note This creates an LED room where the components that have the ROOM = LED property will be placed. When **ROOM_TYPE = HARD** is set and these parts are placed outside of or straddle the boundary of the assigned room, a DRC flag will be shown until the problem is resolved.

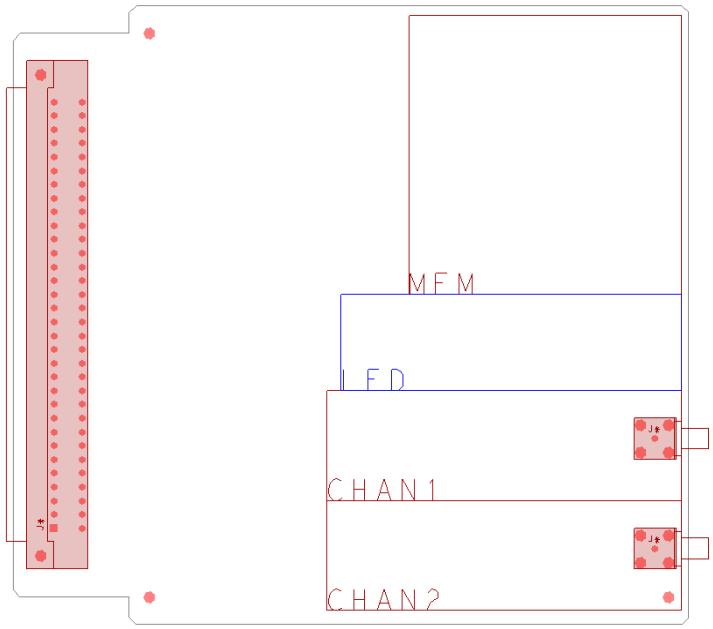
4. Use the pulldown in the Room Name and select the ***MEM*** room:
5. Set the ***Side of Board*** to ***Both*** and enter:

```
x 1900 4225

x 3900 2200
```

Four rectangles appear on the board with the labels attached to them.

6. Click ***OK*** to get out of the form.
You have just completed the floorplanning step of this design. Components that have an attached Room property equal to these name values will be placed in the rooms they belong in.



7. In the PCB Editor, select ***File - Save As***. A ***Save As*** file browser form appears. Rename this drawing: `floorplan.brd`
8. Make sure to save it in the ***PCB_Designer\project2\allegro*** folder.
9. Click ***Save*** to save the `floorplan.brd` file.
The `floorplan.brd` file is saved to disk.

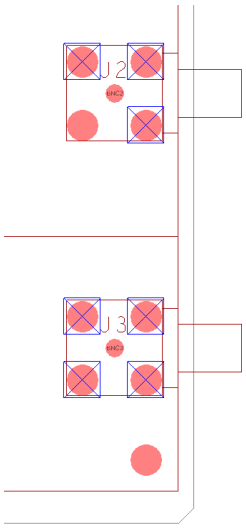
End of Lab

Lab 8-2: Assigning Preplaced Packages

Objective: Associate preplaced connectors to the logical database.

The mechanical template used to create this design file (`template.brd`) contained preplaced package symbols. In order for a preplaced part to have connectivity, it must be associated with a reference designator that exists in the design database.

1. From the top menu, choose ***Place - Assign RefDes***.
2. Open the ***Options*** tab and click in the ***Refdes*** field and enter: **`J1`**
3. Click on the ***edge connector symbol on the left side of the design***.
   The reference designator, previously ***J**** has changed to ***J1***.
   Notice that the ***Refdes*** field has incremented from J1 to J2.
4. Click on the ***upper BNC connector*** at the right side of the board.
   The reference designator, previously ***J**** has changed to ***J2***.
5. Click on the ***lower BNC*** connector at the right side of the board.
   The reference designator, previously ***J**** has changed to ***J3***.
   Both BNC connectors now have reference designators assigned and the ratsnest for the GND_EARTH net is displayed, as shown in the figure to the right:



You will notice that the ratsnest for GND_EARTH is not a point-to-point ratsnest, but rather a box with an X inside of it. This is caused by the addition of the VOLTAGE property. All nets with a VOLTAGE property assigned will display in this way.

6. Right-click and choose **"*Done*"** from the pop-up menu.
7. Choose ***File - Save*** from the top menu.
   A window appears and warns you that the `floorplan.brd` file already exists and asks you if you want to overwrite the file.
8. Click **"*Yes*"** to confirm the file overwrite.
   The file `floorplan.brd` is written to disk.

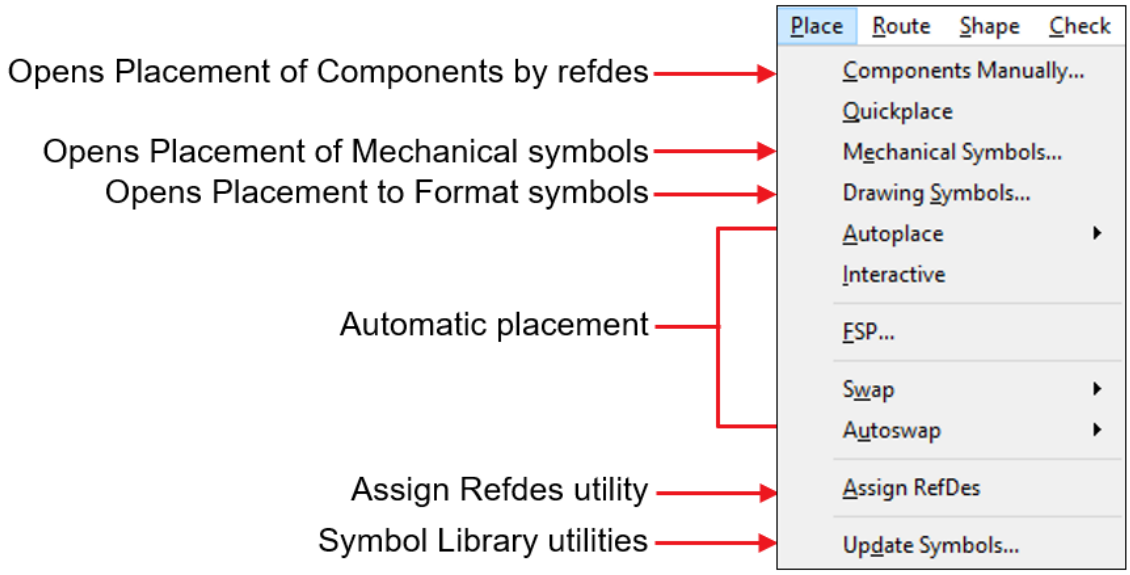
End of Lab

Placement-Related Properties

The following placement related properties control placement and swapability. They are typically placed on components in the schematic but may be placed at the board level.

- **ROOM** - Indicates that the component is to be located in a particular area, identified by the room name.
- **NO_SWAP_GATE** - Indicates that the functions, or gates within a component may not be swapped.
- **NO_SWAP_GATE_EXT** – Indicates that the functions, or gates may not be swapped with a function, or gate from another component. May only swap between functions or gates within the same component.
- **NO_SWAP_PIN** - Indicates that pins on a component may not be swapped.
- **FIX_ALL** - Declares that components having this property will not be eligible for any pin or function swapping.
- **FIXED** - Component is locked down and may not be moved or deleted.

Placement Commands

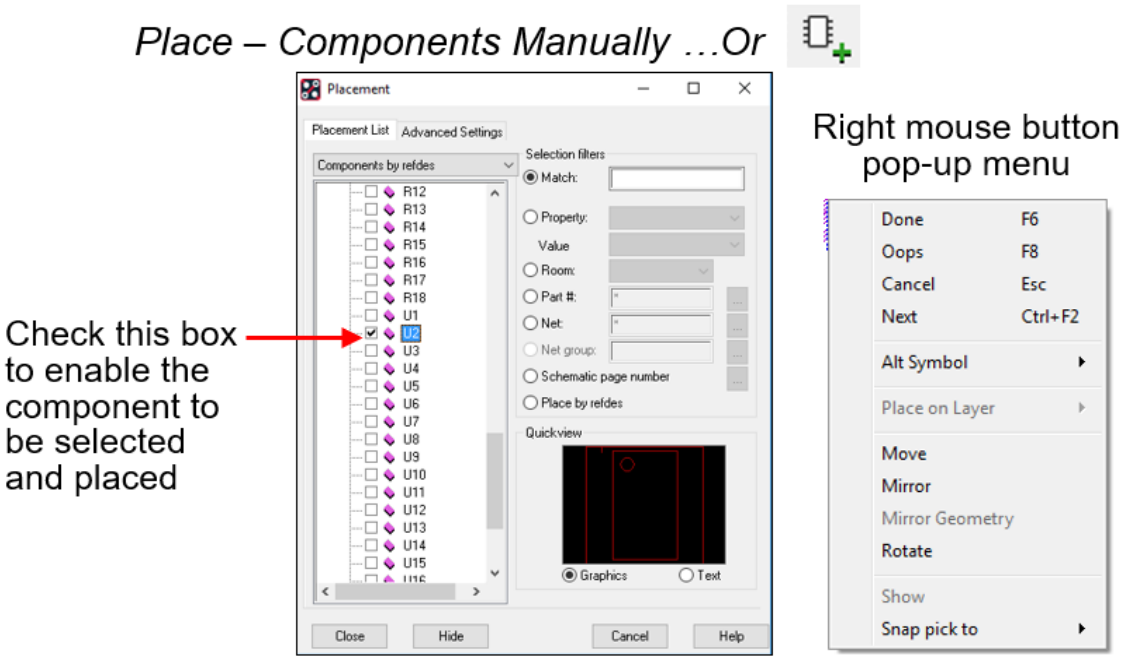


The PCB Editor's placement commands include the following and will be discussed in this or the next segment of the class:

- **Components Manually** - Opens the Placement form directly to the place ***Components by refdes*** with a list the reference designators that still need placing.
- **Quickplac**e – Automatic, but unintelligent placement program which will automatically place parts outside the board outline, or inside their designated rooms. The parts may then be placed interactively in their final location.

- **Mechanical Symbols** - Opens the Placement form directly to the **Mechanical symbols** with a list of the mechanical symbols in the library.
- **Drawing Symbols** - Opens the Placement form directly to the **Format symbols** with a list of drawing format symbols in the library.
- **Swap** – Allows for the interactive swapping of pins, gates or components.
- **Assign RefDes** – Allows the assignment of a reference designator from the schematic to a pre-placed footprint in the board design.

Manual Placement - Placement List Tab



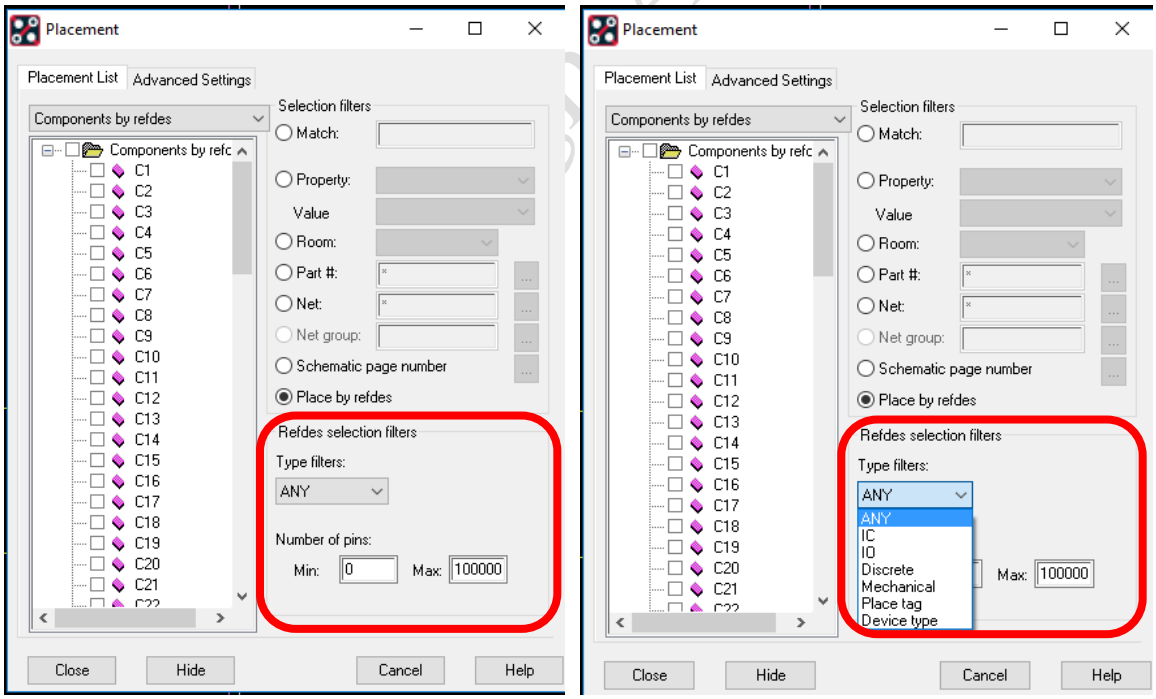
The ***Place – Components manually*** command lets you specify a component or group of components to be placed. When you click on the box to the left of the reference designator the PCB Editor attaches that component to your cursor. Click in the graphics window to place the part on the board.

The following selection options are available in the **Placement List** tab.

- **Components by RefDes** - Lets you specify one or more reference designators
- **Components by net group** – Displays all of the components associated with a net
- **Package Symbols** - Lets you place package symbols in the design WITHOUT containing any logical information
- **Mechanical Symbols** - Lets you place mechanical symbols such as a board outline or non-logical mounting hole in the design
- **Format Symbols** - Lets you place format symbols such as drawing formats and assembly or fabrication notes in the design

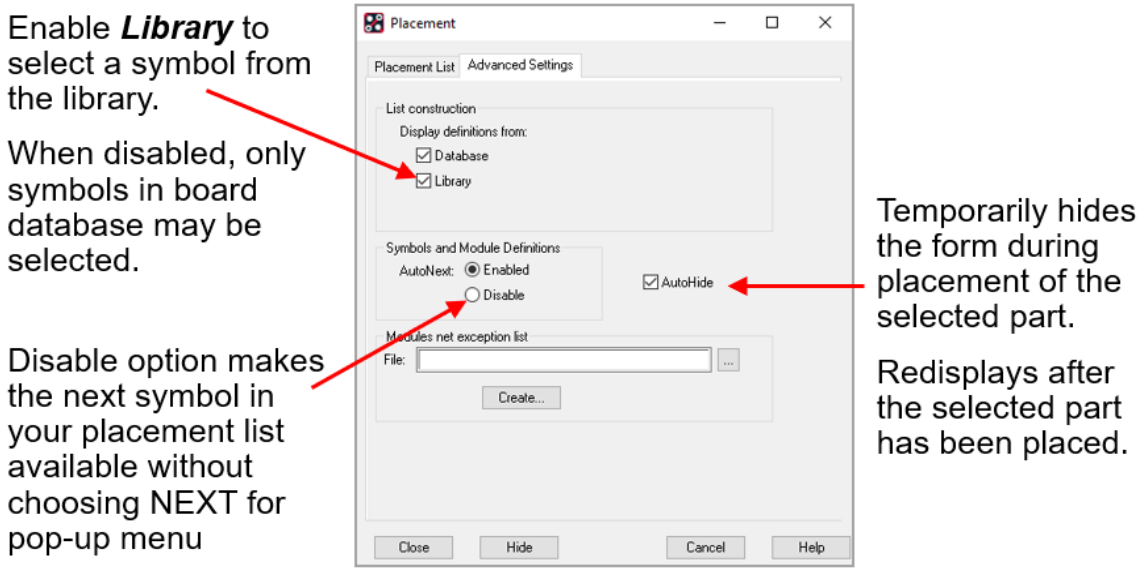
The Selection Filters section lets you further refine the elements that are available for selection. The following filters are available:

- **Match** - Lets you select the elements that match the name you enter. You may use the wildcard character of "*" to select a group of components, such as "U*
- **Property** - Lets you select the elements that match a certain property name attached to components and can be further refined by matching the property value
- **Room** - Lets you place components that are to be placed in a certain room, or all components that are to be placed in any room
- **Part #** - Lets you place components with a given part number. The wild card character "*" may be used
- **Net** - Lets you place all components that are associated with a net. The wild card character "*" may be used
- **Net group** - Lets you place all components that are associated with a net group
- **Schematic page number** - Allows you to place all the parts from a particular schematic page
- **Place by refdes** - Changes the Quickview section of the form so that you may select components by class (IC, IO, Discrete, or Mechanical), by the Place tag property, or by device type. You can also search for parts based on minimum and/or maximum number of pins (see figures below).



While a part is attached to the cursor, click right to access options for rotating the part or mirroring the part to the opposite side of the board.

Manual Placement - Advanced Settings Tab



By default, the Placement List tab will be displayed at all times. The parameter settings for this command are located in the **Advanced Settings** tab.

List Construction

- **Display definitions form** - Lets you choose from where symbol and module definitions are displayed; the **Database** of the current design, the **Library**, or both.

Symbols and Module Definitions

- **AutoNext**
  - **Enabled** (Default) - Puts the next symbol in your placement list on your cursor without the need to choose 'Next' from the Right-Mouse-Button popup
  - **Disable** - Requires you to choose 'Next' from the Right-Mouse-Button popup to put the next symbol on your cursor for placement

  The behavior of AutoNext differs somewhat when placing non-component symbols or module definitions. For these elements, only one copy of the element is placed when AutoNext is enabled.

- **AutoHide** – Automatically hides the Placement dialog box once a part is on your cursor and re-displays it once the part has been placed. To manually redisplay the Placement dialog box, right-click and choose Show.

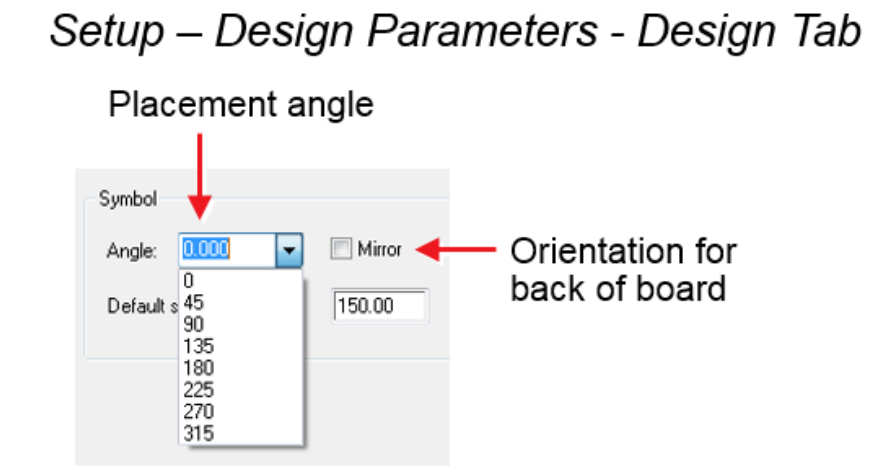
Modules net exception list - Lets you create or use an existing exception list for renaming nets when you are about to place a module instance previously created in your design. When a module is added to a design, all components and nets in the module are given unique names so that they do not conflict with any other design objects already present.

- **File** - In most designs, you want to make an exception to this general rule in the case of power and ground nets, which you would normally want to merge with the design. The nets you want to merge with the existing board can be added to a module net exception list, an ASCII file containing net names that are not changed when a module is added to the design. You specify this file in this field. You can either enter the list file name or use the Browse button to locate the file.
- **Create** - Creates list files and brings up the Select Nets dialog box from which you can create an exception list. You can also create list files typing them in with an external text editor or by using the define list command.

Buttons

- **Close** - Saves any changes made during the session and closes the dialog box.
- **Hide** - Causes the Placement dialog box to disappear. To re-display the Placement dialog box, choose ***Show*** from the pop-up menu.
- **Cancel** – Will undo any changes made during the session and close the form.

Changing the Default Orientation



The angle and mirror options eliminate the need to use the Right-Mouse-Button during placement of groups requiring rotation or mirroring to place on the back side

When you place parts manually, they are by default placed as created in the library. If you have several parts that require placing at a different angle, rather than using the ***Right-Mouse-Button*** and selecting ***Rotate*** from the popup, you can change the default rotation angle. To set this behavior, use ***Setup - Design Parameters***, select the ***Design*** folder tab and change the ***Angle*** field to the desired rotation. You can change the rotation to any of those available in the pull-down, or you can type in any value you need.

By default, all parts are placed on the top side of the board. However, if you have a series of parts that you want to place on the bottom or back side of the design, such as standard surface-mount decoupling capacitors, you can change the default to Mirror. To place each part on the bottom side of the board, WITHOUT manually using the Right-Mouse-Button and selecting "Mirror" from the popup, set the ***Mirror*** toggle in the ***Design*** folder tab under ***Setup - Design Parameters***. After you set this toggle, all parts that are manually placed will be placed on the bottom side of the board.

Lab

Lab 8-3: Manual Placement

- Place parts by reference designator
- Use the Move and Rotate commands
- Coloring the GND and POWER Nets
- Change Default Orientation
- Move groups of parts

The following lab will allow you to familiarize yourself with some of the commands required to manually place parts on the board. You will learn how to rotate parts, mirror parts, move parts and other manual placement options.

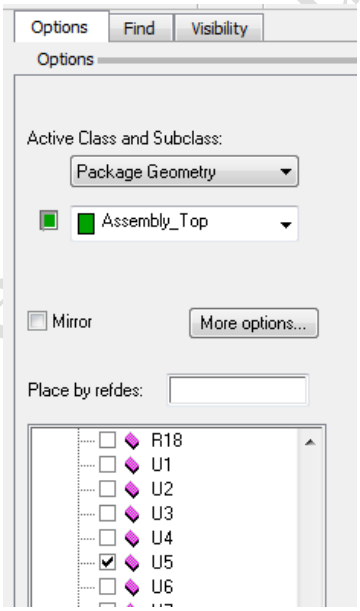
Lab 8-3: Manual Placement

Objective: Select, place, and move components interactively.

Placing Parts by Reference Designator

1. Start the PCB Editor if it is not already running.
2. Choose ***File - Open*** to open the `floorplan.brd` file that we were working with in the last lab.
   If you did not finish the last labs, you will find a copy of the `floorplan.brd` located in the ***PCB_Designer/solutions*** folder.
3. From the top menu, choose ***Setup - Application Mode - Placement Edit***.
4. Open the ***Options*** tab and in the ***Place by refdes*** list scroll through the list and enable the check box to the left of ***U5***.
   The PCB Editor's command area states:

   ```
   Placing U5 / EPF8282A_BGA / BGA_84.
   ```

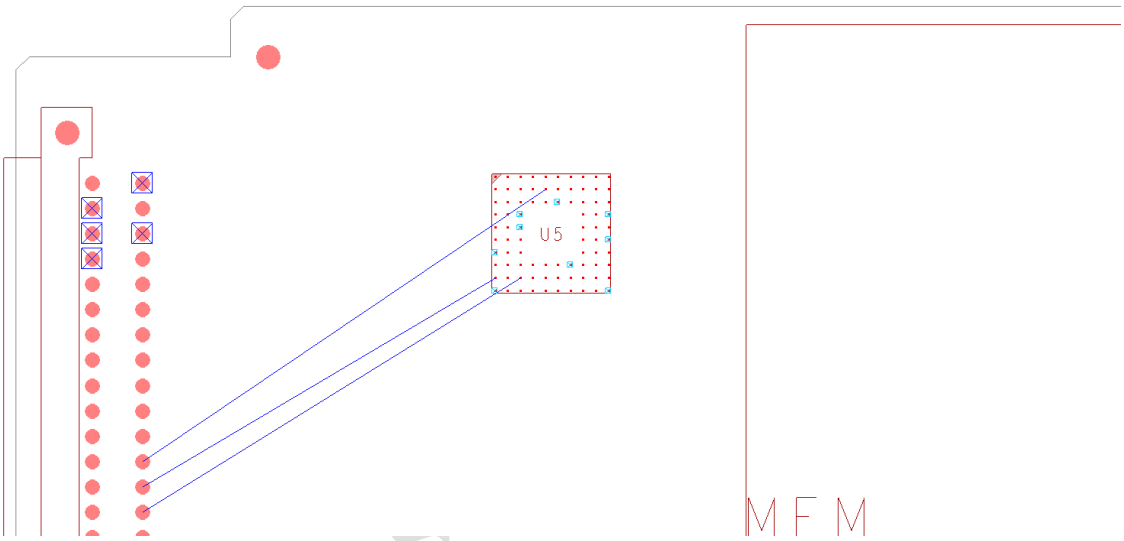


5. Move your cursor into the main PCB Editor graphics window.
   U5 is attached to your cursor. Next, practice rotating U5.

Note By default, parts will be attached to your cursor in 0-degree rotation. This is the orientation of the part when it was created.

6. Right-click and choose ***Rotate*** from the pop-up menu.
   A "handlebar" extends between the part and your cursor.

7. Use the handlebar to spin the component.
   Notice that the angle of rotation appears in the status bar at the bottom of your window (to the right of the P and A buttons).
8. Spin ***U5*** to ***180 degrees***.
   Notice the angle reading in the Status area of your screen.
9. Go ahead and set ***U5*** at a ***0-degree*** rotation, click left to accept the current orientation. You are no longer in rotate mode, but you are still in move mode. U5 is still attached to your cursor.
10. Click to place ***U5*** in the design at the location shown in the figure below.

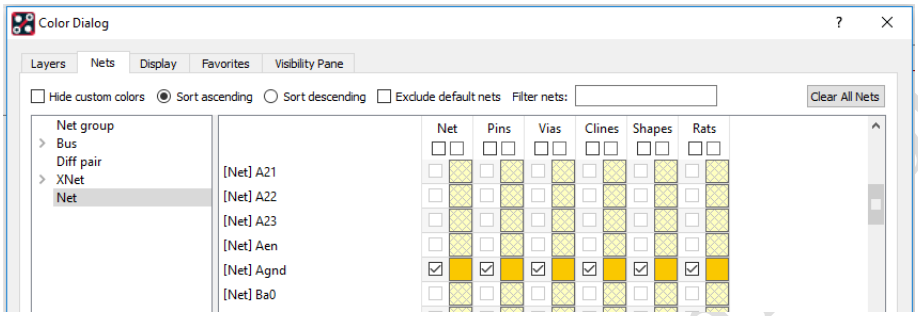


11. Right-click and choose "***Done***" from the pop-up menu.

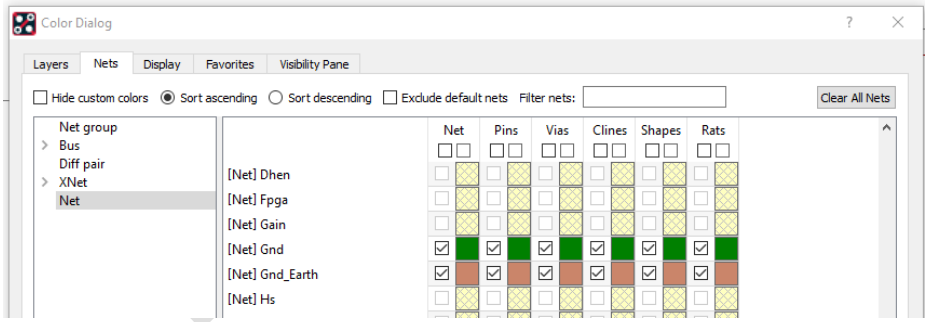
Coloring the GND and POWER Nets

As mentioned in the last lab, the ratsnest for any nets with the VOLTAGE property, generally Power and Ground nets, do not show a point-to-point ratsnest. This is done as a visual aid, assuming that these nets will most likely be routed to their respective internal planes. It is helpful however, to have these nets set in different colors so you will know where to place the discrete components that are often assigned those nets.

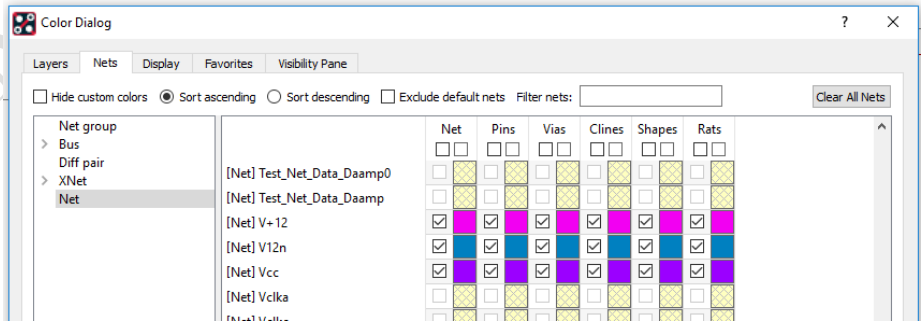
1. Select ***Setup - Colors*** in the top menu or select the ***Color192*** icon.
2. In the ***Color Dialog*** form select the ***Nets*** tab.
3. Click on the ***Mustard*** colored chip (or another color you have not used previously in your color setup) in the ***Available colors*** area.
4. Scroll down to ***AGND***
5. Select the ***Net column*** chip for the ***AGND*** net as shown below.



6. Select a ***Green*** chip (a shade of green you have not used previously in your color setup) in the ***Available colors*** area.
7. Scroll down the list of nets to find ***GND***.
8. Select in the ***Net column*** on the chip for the net ***GND*** as you did for the ***AGND*** net.
9. Now, select a ***Brown*** chip and set the color for the net ***GND_EARTH*** as you did for the ***AGND*** and ***GND*** nets (See figure below).



10. Finally, using what you learned in steps 3 through 8, color the VCC Purple, V+12 Magenta and V12n Blue as you see in the figure below.

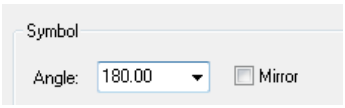


11. Select ***OK*** to close the ***Color Dialog*** form.
    This will color all the pins, vias, clines, and shapes that are part of those nets, the selected colors.

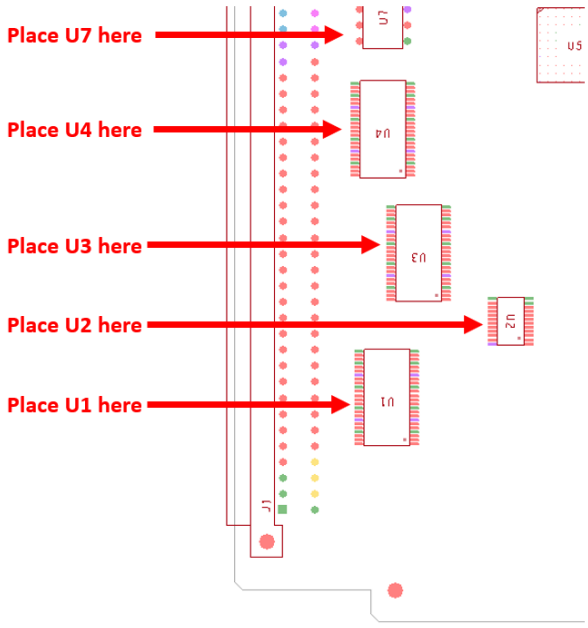
Changing the Default Orientation

Rather than using the "***Rotate"*** command from the pop-up menu each time you place an individual compo**nent, you can override the default orientation using the** *Design Parameter Editor* form.

1. Choose ***Setup - Design Parameters*** in the top menu.
2. Click the ***Design*** tab to bring it forward.
3. Set the ***Angle*** field to ***180***, as shown:



4. Click ***OK*** to exit from the ***Design Parameter Editor*** form.
   Now the default orientation is 180 degrees (instead of zero).
5. From the ***Place by refdes*** list in the ***Options*** tab, scroll through the list and enable the check box to the left of ***U1***.
6. Move your cursor into the PCB Editor' design window.
   U1 attaches to your cursor in a 180-degree rotation. The dynamic ratsnest lines appear between the component on your cursor and any currently placed components.
7. Click to place the ***U1*** component on the board at the location indicated in the next figure.



8. Place components ***U2***, ***U3***, ***U4*** and ***U7*** using the method you just tried. Refer to the above figure for where to place the components and in what rotation. Do **NOT** align them in a column or equally space them. We will use the alignment command to align and equally space them later.

Moving Groups of Parts

1. Choose ***Edit – Move*** from the top menu.
2. In the ***Find Filter***, toggle the ***All Off*** button and then enable just ***Symbols***.
3. Click and hold the ***Left-Mouse-Button*** as you drag the mouse to stretch a frame around the desired group of components you want to move.

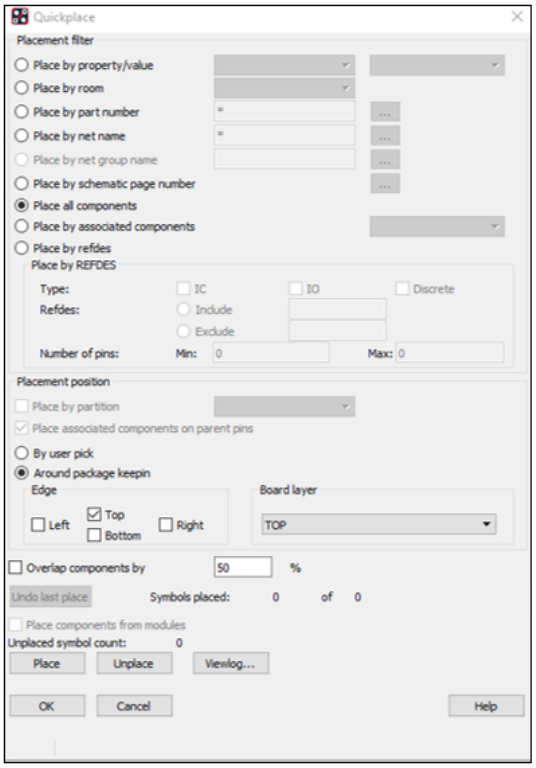
Note The graphics of these parts do not need to be entirely within the window to be selected. Do not include any part of the board outline in your selection window. The board outline, keepins, and keepouts were created as one board symbol, so this symbol should NOT be moved.

If you make a mistake creating the selection window, right-click and choose **Oops** from the popup menu. Then use the Left-Mouse-Button to stretch a frame around the desired components.

4. When the parts you want to move are highlighted, click left (but do not drag) to define an origin, or reference point, for the group to move. The group is now attached to your cursor.
5. Move the group around and click on a new grid location to place the group.
6. Right-click and choose **"*Done*"** from the pop-up menu.
7. Selecting ***File – Save As*** from the top menu, save the board as **`partplaced.brd`**.

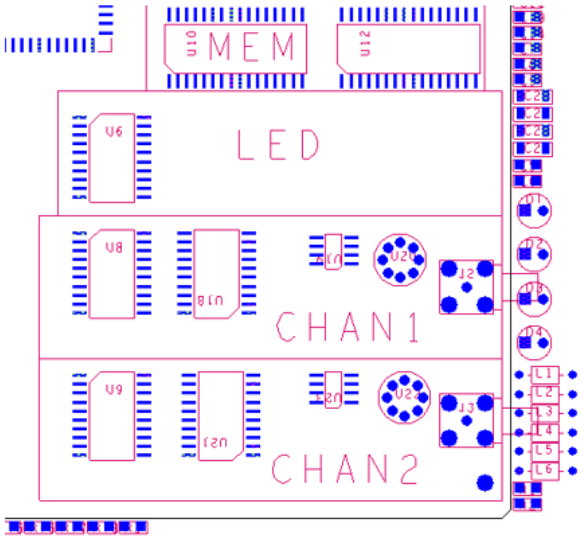
End of Lab

Quickplace Command



Place - Quickplace

Components placed along the right and bottom edges of the board



The **Quickplace** command is an unintelligent placement too that will place unplaced parts outside the board outline, or for those parts assigned a room property, they will be placed inside the assigned room. The command will not place any parts outside the drawing extents. Parts that are already placed in the design will not be affected by the **Quickplace** command.

Placement Filter

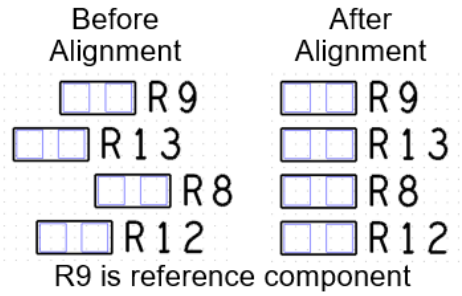
- **Place by property/value** - Places components by their component property and value
- **Place by room** - Places components into a single room or all rooms simultaneously.
- **Place by part number** - Places components in groups by part number around the board outline (i.e. EMA-00006556V22, AX88178LF)
- **Place by net name** - Places components that have a common net name between them. Useful for boards that have multiple voltages and will need to set up placement for a resulting split plane
- **Place by net group name** - Places components that have a common net group name between them.
- **Place by schematic page number** - You can place components by page. The Browse button displays the schematic hierarchical blocks or individual pages or sheets that still have unplaced components
- **Place all components -** This option will attempt to place all currently unplaced parts in the next execution of the command.
- **Place by refdes –** This section is used to refine the parts for placement. You can specify components by Class property; IC, IO or Discrete, or any combination of the three. Remember, these three classifications of parts are controlled by the library definition in OrCAD Capture or by the device files from third-party netlists.

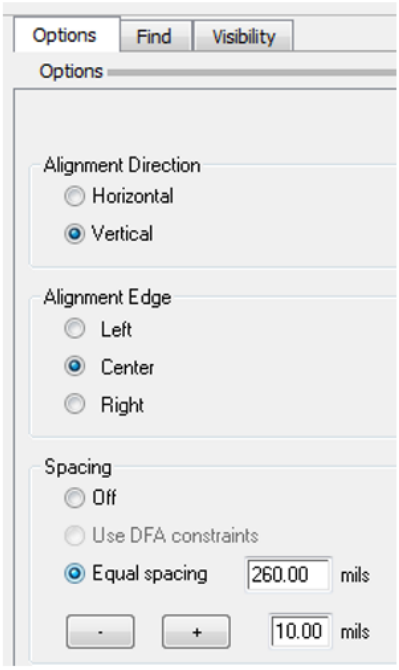
Placement Position

- **By user pick -** Allows you to place anywhere on the drawing. Use in combination with Edge and Board Side.
- **Edge** section - Controls whether parts are placed outside the left, right, top or bottom edge of the board outline. The option can be changed at any time and the command rerun multiple times to achieve almost any desired placement pattern.
- **Board Side -** Controls whether parts are placed on the top or bottom side of the design. The option can be changed at any time and the command rerun multiple times to achieve almost any desired placement pattern.
- **Symbols placed** field - Displays the number of components placed, as well as the number of unplaced components.
- **Undo last place** button - Removes only the most recent parts placed, as specified by the Filters settings. The Unplace button will repeatedly remove parts placed for as many times as a place option was run during the current session.
- **Unplaced symbol count** field - Displays the current number of unplaced parts.

Aligning Components

- Must be in Placement Edit application mode
- Parts must exist on the same subclass/side
- More than one component must be selected
- Components must not be FIXED
- Steps required to align components
  - Select all components to be aligned
  - Hover over reference component
  - RMB – Align Components
  - Set the alignment options





The Align Components command is available in the Placement edit application mode from the Right-Mouse-Button popup. To use the alignment command, the components must be on the same subclass, or side of the board, you must select more than one component and components must NOT be FIXED.

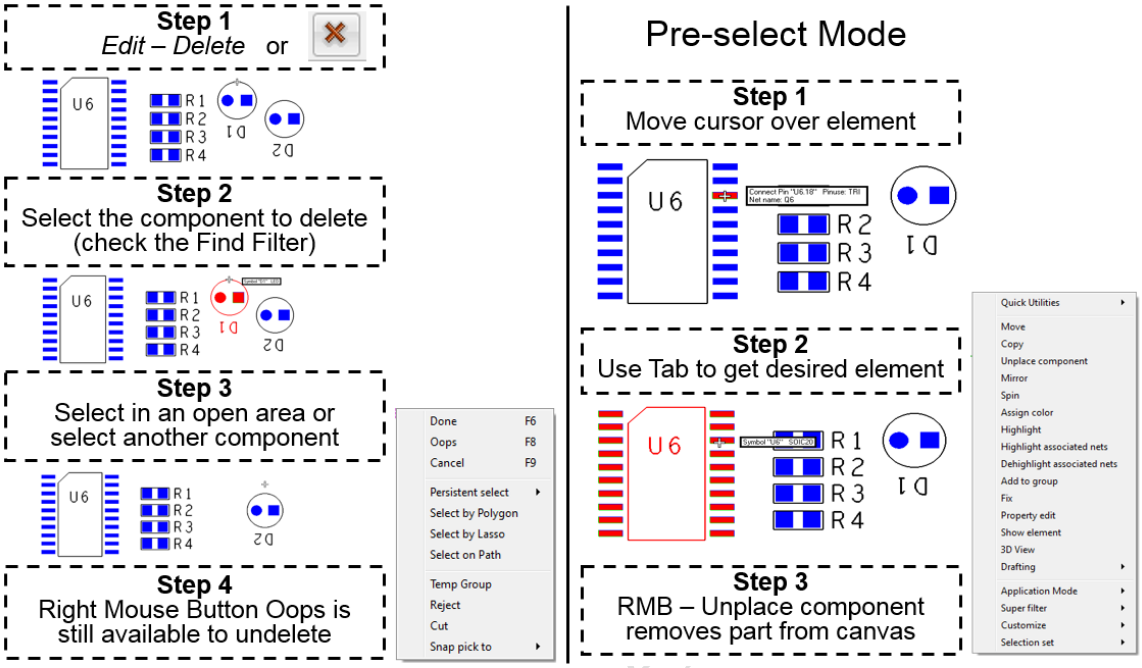
Steps required to align components:

- Must be in the Placement Edit application mode
- Select all components to be aligned
- Hover your mouse over the reference component
- Use the Right-Mouse-Button pop-up menu option Align Components
- Set the alignment direction, alignment edge, and spacing in the Options tab

Alignment Direction - Horizontal or Vertical
Alignment Edge – Sets the edge of the component to align by (right, left, or center).
Spacing

- **Off** - Aligns the components at their current spacing.
- **Use DFA Constraints** - compresses components in the selection set to the minimum DFA spacing distance (***NOT available in the PCB Editor***).
- **Equal Spacing** - Uses an algorithm to compute distances between the first and last component in the selection set then divides by the number of components resulting in an equalized spacing gap between each component. Use the increment/decrement controls to adjust component spacing real time.

Deleting/Unplacing Components



There are two different methods to delete a component from a design. Note that when you delete a component, you only unplace the component. Deleting a component does not remove it from the logic or from the Bill of Material.

One method to delete a component is to use the standard ***Edit - Delete*** command. You can delete individual parts from the board or delete a group of components by dragging the mouse and forming a rectangle around a series of parts. When using this method, the selected component(s) will highlight but will not be removed until you verify whether you want to delete additional components or are finished with the command. Also remember that parts that have the ***FIXED*** property will not be deleted.

Note Make sure to check your Find Filter when attempting to delete parts from your design. If Symbols is not checked, you will not be able to delete the parts desired.

A second method to delete a component is to use the Pre-selection mode. Hover your mouse over the part you want to delete and tab through until the Symbol is selected. You can then use the Right-Mouse-Button pop-up menu and select the ***Unplace component*** command to delete the part. Note that when you first move your cursor over the part, if the Symbol is not selected, you can use the Right-Mouse-Button pop-up menu, then use the Symbol option, and then select **Unplace component**.

Lab

Lab 8-4: Using the Quickplace Command

- Use the **Quickplace** command to place parts in rooms
- Automatically align the previously placed ICs U1, U3 and U4

The following lab will allow you to:

Familiarize yourself with the Quickplace command. You will also use the placement skills you have already learned to place the design.

Lab 8-4: Using the Quickplace Command

Objective: Use the Quickplace command to place all the components onto a partially placed board.

The **Quickplace** command can be used to place parts on the board and into their assigned rooms.

1. Be sure you are working on the board file **`partplaced.brd`**.
   It is the board we saved in the previous lab. If you did not finish the last lab, you can find a **`partplaced.brd`** in the solutions folder.
2. Select ***Display - Zoom - Fit*** from the top menu such that all of the rooms on the board are visible.
3. If the grids are displayed, turn them off by clicking the ***Grid Toggle*** icon.

Quickplacing Components into their Assigned Rooms

First you will quickplace the parts with room assignments into their respective rooms. Then you can start moving parts in the selected rooms to create your final placement.

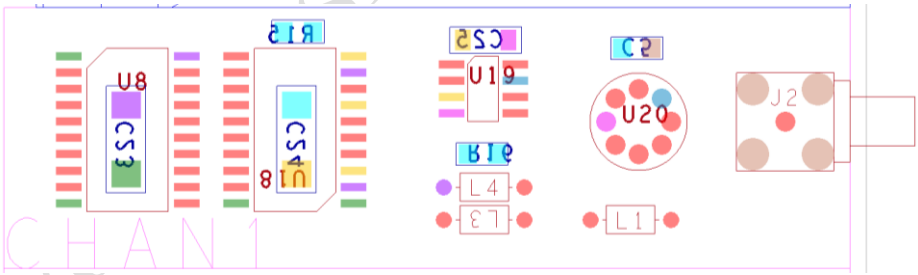
1. Choose ***Place - Quickplace*** from the top menu.
2. In the ***Quickplace*** form, select the ***Place by room*** placement filter and set the room to ***MEM***.
   This will flag each component with the MEM Room property and place it in its appropriate room. By default, the Board Side **Top** was selected as the side of the board that would be placed. So, even if the room was defined as BOTH, Quickplace only places one side of the board at a time.
3. Click the ***Place*** button at the bottom of the form.
   This will place all the parts with the ***MEM*** Room assignment.
4. In the ***Place by room*** placement filter, set the room to ***LED***.
   This will flag each component with the LED Room property and place it in its appropriate room.
5. Click the ***Place*** button.
   This will place all the parts with the ***LED*** Room assignment.
6. In the ***Place by room*** placement filter, set the room to ***CHAN1***.

This will flag each component with the CHAN1 Room property and place it in its appropriate room.

7. Click the ***Place*** button.
   This will place all the parts with the ***CHAN1*** Room assignment.
8. In the ***Place by room*** placement filter, set the room to ***CHAN2***.
   This will flag each component with the CHAN2 Room property and place it in its appropriate room.
9. Click the ***Place*** button.
   This will place all the parts with the ***CHAN2*** Room assignment.
10. Change the ***Placement Filter*** from ***Place by room*** to ***Place all components***.
11. If the ***Edge*** option is not currently set to Right, set it to ***Right*** now.
12. Click ***Place***.
    This will place all of the remaining parts along the bottom outer edge of the board.
13. Click ***OK*** to close the ***Quickplace*** form.
14. You can use the **Mirror**, **Move**, **Group Move**, and **Rotate** commands to rearrange the locations and orientation of the parts as needed.

Note If you had a problem with the Quickplace command and could not quickplace your components, there is a **`quickplaced.brd`** file in the solutions folder that you may use for the rest of this lab.

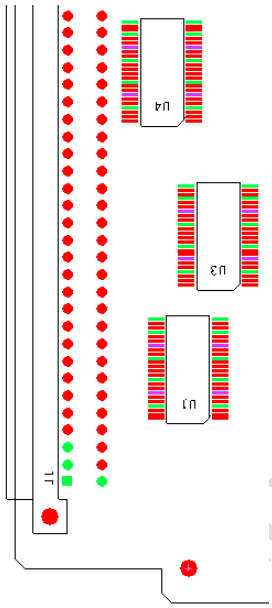
15. Place the parts in the ***CHAN1*** (and if you have time ***CHAN2***) room in a more logical manner. We have given you a suggested placement below.



16. Save the board as **`partplacedroom.brd`**.

Align Components

1. If you are not still in the ***Placement Edit*** application mode, then ***reactivate*** it.
2. Zoom around the ***U1***, ***U3*** and ***U4*** ICs on the left side of the board as shown below.



3. Window select *the 3 ICs to the right of the connector (**U1, U3,** and **U4**).*
4. Hover over ***U1*** and from the ***Right-Mouse*** popup select ***Align Components***.
5. In the ***Options*** tab, set the ***Spacing*** option to ***Equal Spacing***.
   U3 and U4 should now be aligned with U1 and the Equal Spacing option set the IC's calculated equal distance spacing between U1 and U4.
6. Choose ***File - Save As*** for the top menu.
7. Rename this drawing by entering the following in the *File Name* field: **`placed`**
8. Click Save to save the `placed.brd` file to disk.

End of Lab

Lesson 9: Additional Placement Features

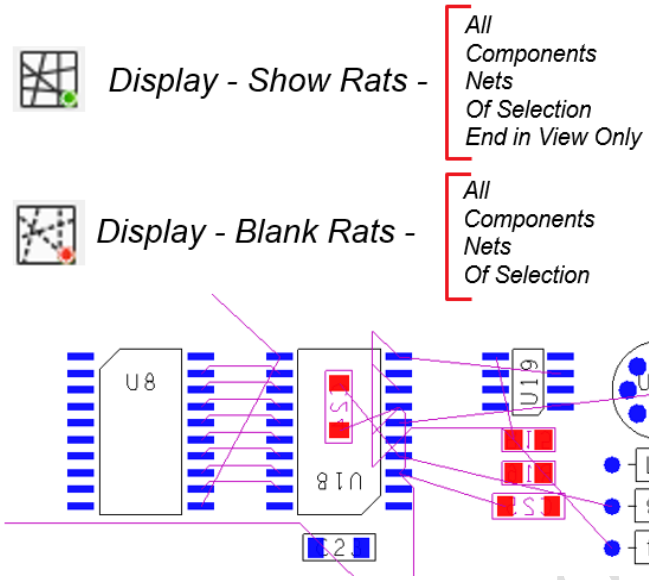
Learning Objectives

In this lesson, you will:

- Turn ratsnests on and off selectively
- Update symbols and padstacks that have been changed
- Modify padstacks within a board design
- Create and copy fanouts
- Create a library from a board design
- Perform cross placement between the schematic capture environment and the PCB Editor environment

In this section, you will learn some placement techniques that can be used to aid you in the placement and ultimately the routing of your design. These techniques include controlling the display of ratsnests, selecting alternate footprints for parts, modifying a padstack in a design and cross probing between the OrCAD Capture Schematic and the PCB Editor board file. You will also learn how to assure that your schematic and board file are in sync. Additionally, you will learn the steps required when a physical library part or padstack has been modified in the library and the board must be updated with these changes.

Ratsnest Display



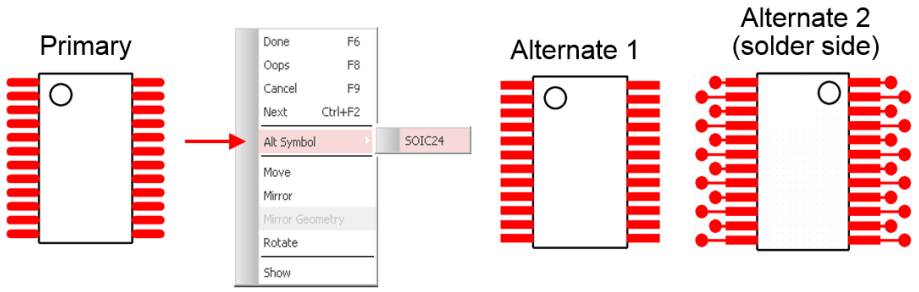
Ratsnests are lines displayed between the pins of an unrouted net. They show a relationship between pins having the same net name. They can be very useful placement aids. Displaying ratsnests can help identify congested areas. Ratsnests can also help evaluate the 'flow' within and between functional blocks of logic.

To display ratsnests, select **Display** from the top menu. The following sub-menus are available:

- Show Rats
  - **All** - Displays ratsnest lines for all nets, except those having a NO_RAT property attached.
  - **Components** - Displays all ratsnest lines associated with a particular part. Select the parts with your LMB or use the Find by Name section of the Find Filter to enter a reference designator or a file of reference designators.
  - **Net** - Displays all ratsnest lines on a net(s) you select. Select pins with your Left-Mouse-Button or use the Find by Name section of the Find Filter to enter a net name or a file of net names.
  - **Of Selection** - Displays all ratsnest lines on the net(s) you preselected.
  - **End in View Only** - Reduces the density of the ratsnest display. This command filters out the rats from the display that are either pass-through or those not terminating at a pin in the view (use with **All**).
- Blank Rats
  - **All** - Blanks all ratsnest lines currently displayed.
  - **Components** – Turns off ratsnest lines for a specified part(s).
  - **Net** – Turns off ratsnest lines for a specified net(s).
  - **Of Selection** – Turns off preselected ratsnest lines.

Selecting Alternate Packages

JEDEC_TYPE = SOIC24_OB
ALT_SYMBOLS = '(TOP: SOIC24; BOTTOM: SOIC24_PE)'
ALT_SYMBOLS_HARD = TRUE



If the property ALT_SYMBOLS_HARD is set for a part AND the JEDEC_TYPE specified also appears in ALT_SYMBOLS property then the JEDEC_TYPE footprint will only be available for placement on the side specified in the ALT_SYMBOLS property

It is important to remember that you will only be able to use alternate symbols when they are defined by your schematic capture tool. You cannot add the ALT_SYMBOLS property inside the PCB Editor. If this property is not defined as part of the schematic symbol or in the device file, you will not be able to use alternate symbols when placing your parts. A good candidate that works well for Alternate symbols is when you have larger sized pad capacitors to be placed on the solder size of the board for solder reflow.

When you place a part, the primary package symbol is attached to your cursor by default. This primary package symbol is contained in the part definition file (`pstchip.dat` for OrCAD Capture or a device file for Third Party).

To select an alternate package symbol for the part being placed, click the Right-Mouse-Button and select to the **Alt Symbol** option. All available alternate symbols will be displayed in a separate pop-up menu for the side of the board currently active. (If no alternate symbol statement exists in the part definition file, the **Alt Symbol** option will appear "greyed out" in the right mouse pop-up menu.)

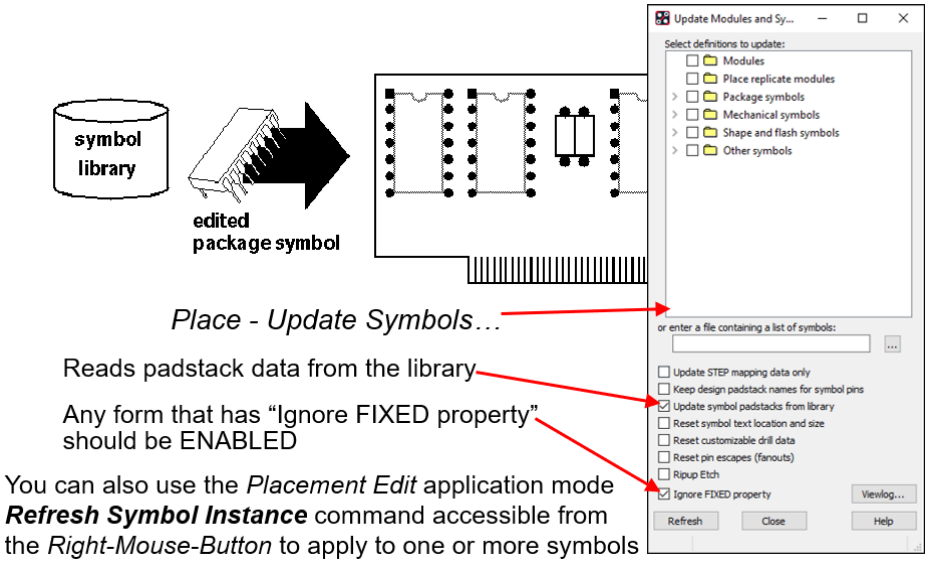
You can specify alternate packages for the top and bottom of the board (see example). When placing a part on the top side, the **Alt Symbol** option displays the package symbols listed for the top. When alternate symbols are defined for the bottom side, the **Mirror** command also changes the package symbol popup accordingly (or the current package is mirrored). Setting the **Mirror** switch in the Design Parameters form also allows access to any alternate symbols for bottom side placement.

By default, the footprint specified in the JEDEC_TYPE property is available for both the Top side and Bottom side when using Alternate Symbols. If the property ALT_SYMBOLS_HARD is set for the part AND the JEDEC_TYPE specified also appears in the ALT_SYMBOLS property, then the JEDEC_TYPE footprint will only be available for placement on the side specified in the ALT_SYMBOLS property.

Alternate symbol functionality lets you toggle between different package or mounting styles. It also allows you adjust pad sizes for surface-mount discrete components to accommodate different assembly processes for the top (vapor phase or infrared reflow) or bottom (wave solder). To specify multiple alternate symbols per side, use a comma to separate them. For example:

```
alt_symbols='(T:soic24,soic24_pe;B:soic24_pe)'
```

Updating Symbols in a Design



When you place a part in your design, a copy of the package symbol is stored in the PCB Editor database. This means that any changes made to the footprint in the library after placement are NOT reflected in the design. When you select the ***Update Symbols*** command, the form shown above is displayed. You can then specify through the different symbol folders which type of symbols need to be updated, such as package symbols, mechanical symbols, and so forth. The folders may also be expanded to allow the selection of a specific symbol name.

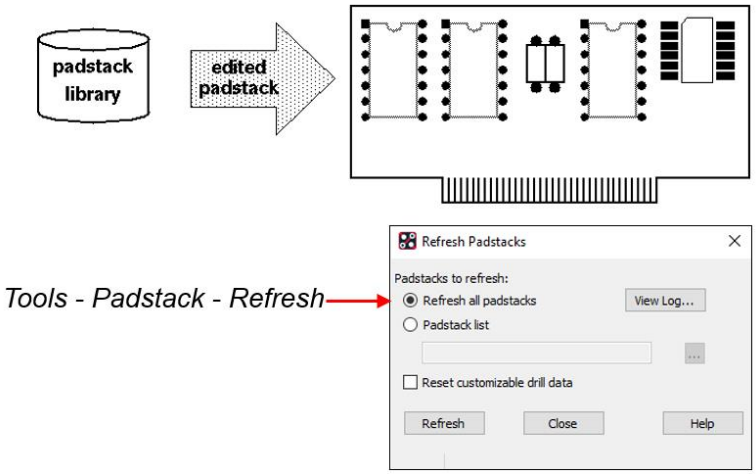
When you select the ***Refresh*** button, the update symbol routine is run. This routine will update the requested symbols from the library using the current PSMPATH, resulting in the board design now matching the library.

Various options let you control which symbols *get updated.*

- **Enter a file containing a list of symbols** – Use if you have a list file with specific symbols to update
- **Keep design padstack names for symbol pins** – Maintains the name on the symbol's pins that have had instance modifications made to them
- **Update symbol padstacks** – Use to replace padstacks in your design with padstacks found in the library
- **Reset symbol text locations** – Use to have the text return to its original symbol location if it had been altered
- **Reset customizable drill data** – Use to refresh the Drill Customization spreadsheet during subsequent updating of padstacks (Tolerance, Symbol Figure and so on).
- **Reset pin escapes (fanouts)** – Use to reset predefined pin escapes from the symbol.
- **Ripup Etch** – Used to allow etch associated with symbol pins be removed during refresh symbol.
- **Ignore FIXED property** – Use to replace a symbol with a FIXED property.

The *Placement Edit* application mode has the ability to refresh a symbol instance. Hover over one or more symbols and then use the Right-Mouse-Button pop-up menu to select ***Refresh Symbol Instance***. A typical application of using this in the Placement Edit application mode would be to restore text or outlines to symbols.

Updating Padstacks



When you place a part in your design, a copy of the padstack is also stored in the PCB Editor database. This means that any changes made to the padstack in the library after placement are NOT reflected in the design. When you select the ***Refresh Padstac*k** option from the top menu, the form shown above is displayed. You specify to update all padstacks in the design, or only padstacks whose names appear in a disk file. When you select the ***Refresh*** button, the Refresh Padstack routine is run. This routine will update the requested padstacks from the library using the current PADPATH variable, resulting in the board design now matching the library.

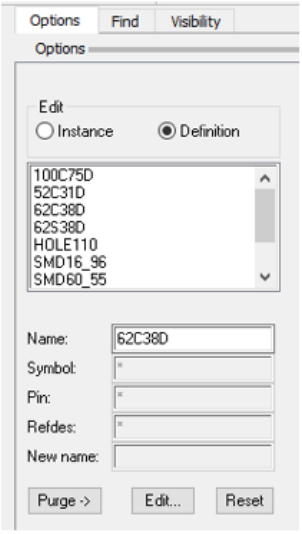
Various options let you control which padstacks get updated.

- **Refresh All Padstacks** - Indicates you want to update all padstacks in the design to match the library padstacks.
- **Padstack List** - Indicates you want to update only the padstacks in the named list to match the library padstacks. The padstack list can be stored in an ASCII text file that has an `.lst` file extension.
- **Reset customizable drill data** – Used to refresh the Drill Customization spreadsheet during subsequent updating of padstacks (Tolerance, Symbol Figure and so on).

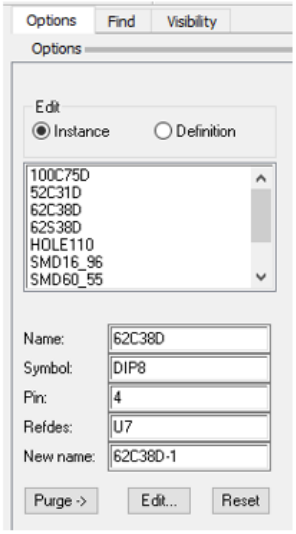
Modifying Padstacks in a Design

Tools - Padstack - Modify Design Padstack

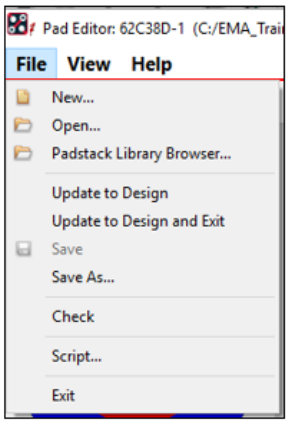
Definition applies to selected padstack everywhere used within the entire design



Instance applies to selected padstack only on designated symbol, pin, and/or refdes



After modifying padstack in the Pad Editor select *File – Update to Design* to just update the padstack in the board design



You can modify a padstack within a design if the original values need to be changed. The standard Pad Editor form is used to update the padstack within the design.

- **Definition** - Every occurrence of this padstack found in the design is modified.
- **Instance** - You edit the padstack description for a certain pin(s) within the design.

  Wildcards may be used in any/all of the Symbol/Pin/Ref Des fields. The New Name field will contain a new padstack name automatically generated by the software. This is to differentiate the new padstack definition from the original padstack definition.

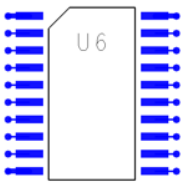
Once the changes have been made, use the ***File - Update to Design*** command from the top menu in the Pad Editor form. This saves the modified padstack "inside" the design only. To save the modified padstack to disk, use the ***File - Save*** or ***File - Save As*** command from the Pad Editor form.

The ***Tools - Padstack - Modify Library Padstack*** command is used to update the library padstack. A browser is presented for choosing which padstack to be modified. You must have write permissions for the library in order to update the padstack.

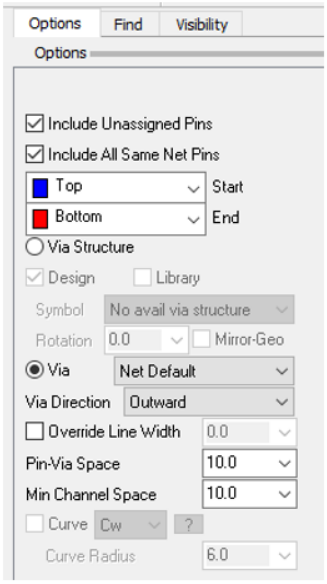
Create Fanout Command

Route – Create Fanout

Setup in Options tab to control line width, spacing and style of fanout pattern.



- Available elements
  - symbols
  - pins
- Replaces any existing fanout on chosen element
- If connection is routed, route is preserved and no fanout is added
- Fanout is applied to a single package symbol
- Command is not DRC aware. Parameter adjustments or interactive editing may be required to comply with DRC value.



The PCB Editor offers several interactive and automatic controls for component fanout, or pin escaping. You can route interactively within the layout editor, build fanouts into your library symbols, or use the suite of fanout commands located in the ***Route*** menu. The interactive suite includes four commands to create, copy, define via structures, and convert cline/via extensions to fanouts.

Route - Create Fanout is applied to a package symbol, or pin. There are several options available in the ***Options*** tab to customize the style and physical characteristics of the resulting fanout pattern. ***Route - Create Fanout*** is not DRC aware and may result in conflicts. Running additional passes with parameter adjustments may be required to reach a DRC free result.

Generating a fanout automatically replaces any existing fanout on the chosen elements. If the connection is routed, existing route is preserved and no fanout is created.

The command does not create:

- Shared vias
- Multiple vias for voltage pins
- Fanouts for thru-hole pins
- Fanouts for pins whose padstack name contains FID, assumed to be fiducials

If multiple via padstacks are associated with a net, then fanout does not occur, and a warning message is displayed. In this case, you must select a specific via padstack from the via drop-down menu.

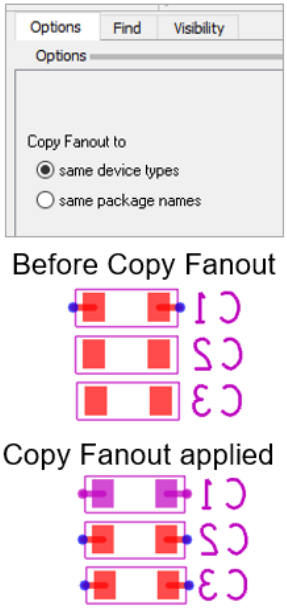
Fanout options available in the Options tab:

- **Include Unassigned Pins** - Results in the fanout of all pins on a component. Pins not assigned a logical connection are considered unassigned
- **Include All Same Net Pins** – This means that every pin on the component assigned to a net will each have their own individual fanout.
- **Via Structure** - Lets you capture complex fanout patterns that may include multiple vias or clines, or even blind and buried vias.
- **Via** - Chooses the type of via from a list of those stored in the database that span specified subclasses.
- **Via Direction** – Specifies the direction of the fanout via relative to the pin location. Directions available are Via in Pad, BGA Quadrant Style, North, South, East West, NE, NW, SE, SW, Inward, Outward and In/Out.
- **Override Line Width** - Overrides the inherited constraint value and applies to all pins. Selective override at the net level can be accomplished by enabling the *Include all Same Net Pins* option. For example, you may want all logical nets to be 6 mils, but DC nets to be 10 mils. After using Route - Create Fanout with override line width set to 6 mils, change the override line with to 10 mils, enable the same pin option, set the Find Filter to pins, then select a DC pin to fanout all pins on that net.
- **Pin-Via Space** - Defines the distance between the edge of the pin-pad and the edge of the via-pad. Zero or negative numbers are valid entries.
- **Min Channel Space** - Used to maintain a minimum space between adjacent fanout vias. The distance spans the edge of a via-pad to the edge of a via-pad on the diagonal, and as the distance increases, so does the stagger effect. The value defaults from the via-to-via space in the default constraint set and is available when you set Via Direction to Inward, Outward, or In/Out.

Copy Fanout Command

Route – Copy Fanout

- Replicates instantiated fanouts across all common package names or device types
- Replication is limited to the same side of the board where the origin component is placed
- Copying a fanout automatically replaces an existing fanout on the chosen component unless the FIXED property has been assigned, or the fanout net is routed
- Copied fanouts replicate the origin symbol attributes such as line width, via type, direction, or via structure
- DRC unaware, so DRCs errors may occur



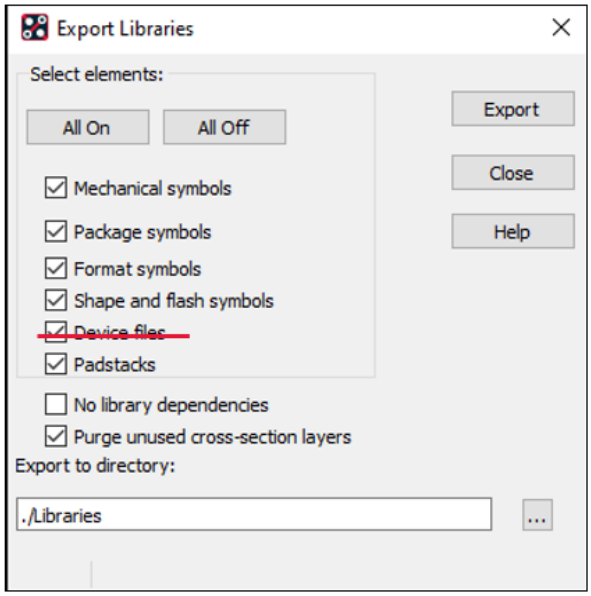
Route - Copy Fanout replicates instantiated fanouts across all common package names or device types. Replication is limited to the same side of the board where the origin component is placed. For symbols on the opposite side, you can create a fanout for one instance using ***Route - Create Fanout***, and then copy it to the remaining symbols on that subclass.

Copying a fanout automatically replaces any existing fanout on the chosen component unless the ***FIXED*** property has been assigned, or the fanout is routed to a different component. A copy occurs even if you have modified a symbol pin's padstack on one instance, as long as the pin location remains unchanged.

Copied fanouts replicate the origin symbol attributes such as line width, via type, direction or via structure. DRC errors may occur after the command is completed; for example, the copied fanout via may conflict with an adjacent pad or may not meet minimum line width requirements.

Creating a Library from a Design

Export - More - Libraries



Note: Device files are not required for designs generated from an OrCAD Capture, or DE HDL Schematic

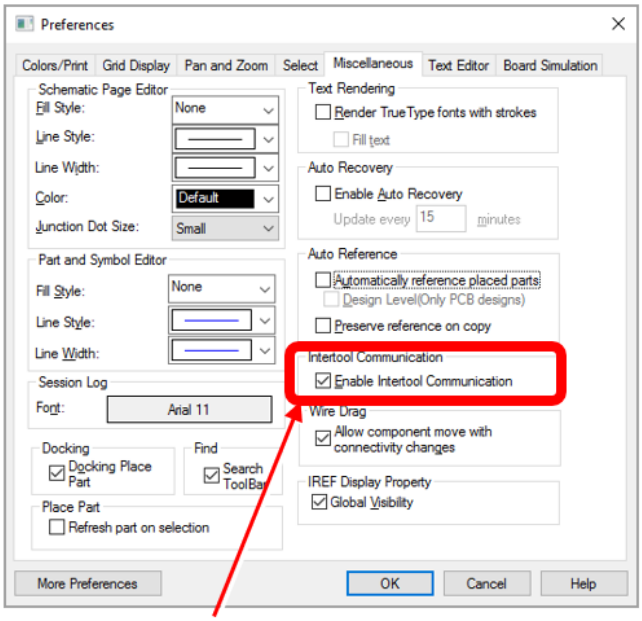
Select ***Export – More - Libraries*** to create library definitions from a .brd file. The Export Libraries program can create mechanical symbols, package symbols, format symbols, shape symbols, flash symbols, device files, and padstack files. It also creates all symbol-related drawing files.

- **No library dependencies** - If you have modified padstacks in your design and want to dump them to the current directory, toggle this to ON.
- If you use an OrCAD Capture Schematic to generate your PCB Editor netlist files, you will not need Device Files.

By default, all files are written into your current working directory. You can use the ***Export to directory*** field to have all the library parts saved to a different location.

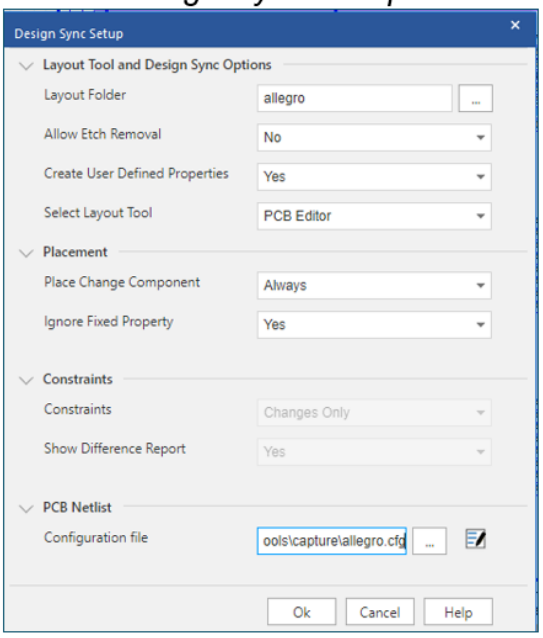
Cross Selection with OrCAD Capture – Prerequisites

Options - Preferences

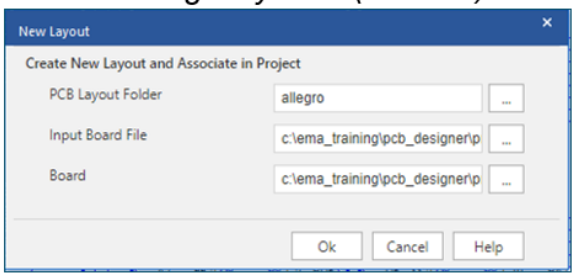


NOTE: *Intertool Communication* must be Enabled

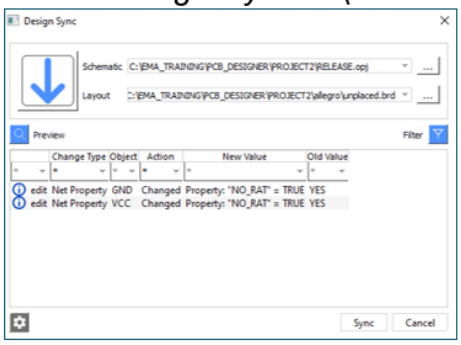
PCB – Design Sync Setup



PCB – Design Sync… (1st time)



PCB – Design Sync… (after 1st time)



NOTE: *Intertool Communication* requires that the Schematic and Board Files be in Sync

If you use OrCAD Capture to create your schematics, you have the ability to cross-probe with PCB Editor. To perform cross probing between the two environments:

- First, you will need to enable ***Intertool Communication*** option. To enable ***Intertool Communication*** from OrCAD Capture, select ***Options - Preferences***, select the ***Miscellaneous*** tab, and check the ***Enable Intertool Communication*** option.
- Next, you will need to make sure that your OrCAD Capture Schematic is in sync with your PCB Editor Board file. To do this you will need to run the ***Design Sync*** program. If you have not run ***Design Sync*** before, you will first need to run ***Design Sync Setup*** by selecting ***PCB – Design Sync Setup*** from the top menu in OrCAD Capture. Then, you will be able to run ***Design Sync*** by selecting ***PCB – Design Sync*** from the top menu in OrCAD Capture. The first time you run ***Design Sync*** on a design, you will select an allegro folder, the input board file and the output board file. After that, ***Design Sync*** will automatically compare your schematic to the last board you ran the ***Design Sync*** on and report any differences. You may then select a different board file to compare your schematic to.
- Once Intertool Communication has been enabled and Design Sync has assured that the schematic and board files are in sync, you are ready to cross probe.

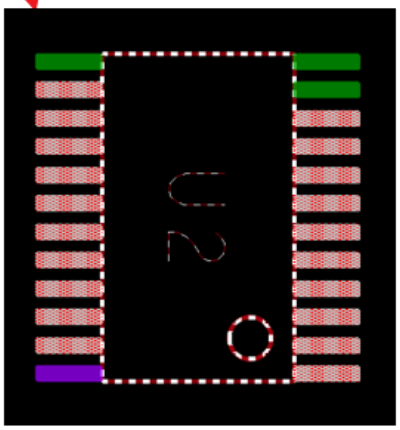
Important

Remember that you must first start a PCB Editor command, such as place, delete, move, etc. ***BEFORE*** selecting the object in the OrCAD Capture schematic. If no PCB Editor command is active and you select an object in OrCAD Capture, the default command is the PCB Editor ***Highlight*** command. If the object selected is not yet available, you will get an error message in PCB Editor.

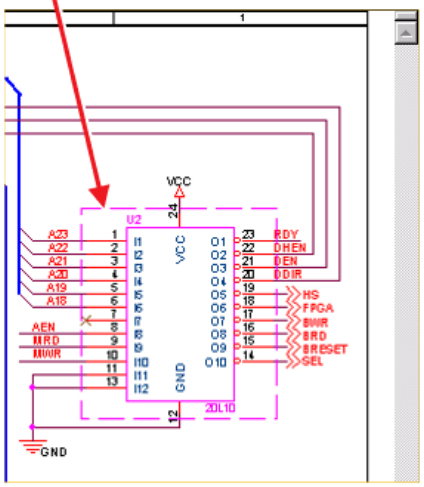
Cross Highlight between Board and Schematic

Display - Highlight

Highlight this part in PCB Editor…



This component is selected in OrCAD Capture



Remember: The command must be activated first in the PCB Editor

Once the link has been made as previously described, you can work with these tools in close relationship. It helps when troubleshooting problems to locate specific components or nets on the schematic or board.

Labs

Lab 9-1: Displaying Ratsnests

- Turn ratsnest on and off to view and hide selected nets and components

Lab 9-2: Creating and copying Fanouts

- Create a fanout
- Copy the created fanout to similar devices

Lab 9-3: Using the OrCAD Capture Schematic for manual Placement (Optional)

- Place, move and highlight parts using the cross probing and cross highlighting between OrCAD Capture and PCB Editor

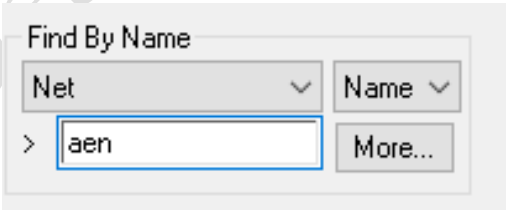
Lab 9-1: Displaying Ratsnests

Objective: Turn ratsnests on and off to selectively view and hide nets while interactively routing individual nets.

1. Start the PCB Editor, open the **`PlacementDone.brd`** file in the ***Solutions*** folder and save it to the ***project2/allegro*** folder.
2. To blank all ratsnest lines, choose ***Display - Blank Rats - All***.
3. To display rats by component, choose ***Display - Show Rats - Components***.
4. Click on a component.
   Ratsnest lines appear for all signals that are connected to the component you picked. The appearance of the ratsnests is cumulative as you select more components.
5. Choose ***Display - Blank Rats - All*** from the top menu.

Note You can also use the **Unrats All** and **Rats All** icons for turning ratsnests on and off.

6. To display ratsnest lines for a particular signal, choose ***Display - Show Rats - Net***.
7. In the ***Find*** tab, go to the ***Find By Name*** section, select ***NET*** from the drop-down list, make sure the next field is set to **Name**, and enter **`aen`** (not case sensitive) in the > field as shown below.



   The AEN rat is displayed and the window will zoom around the ratsnest. You could have also clicked on a pin if you knew the location of the net.
8. Right-click and choose **"*Done*"**.
9. Choose ***Display - Blank Rats - All*** from the top menu.

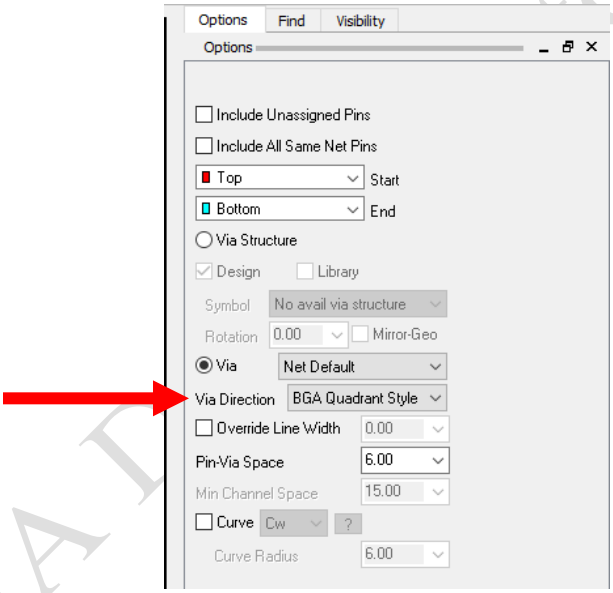
End of Lab

Lab 9-2: Creating and Copying Fanouts

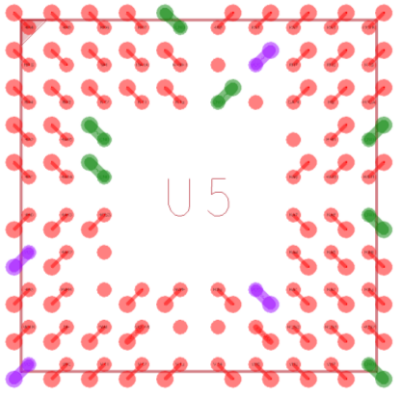
Objective: Create a 'via' fanout on a part and copy the fanout to similar devices types.

Create Fanout

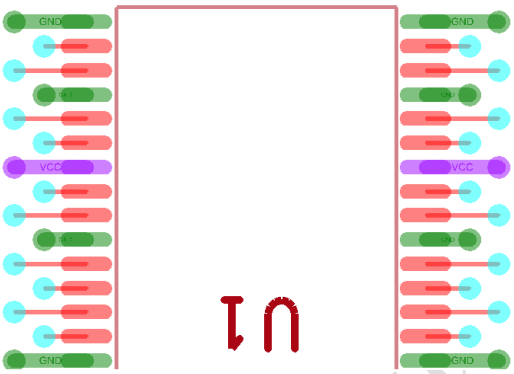
1. Start the PCB Editor if you don't already have it running and open the **`part_fanout.brd`** from the ***Solutions*** directory.
2. Select ***File - Save As*** and save to the ***Project2/Allegro*** directory.
3. If required, resize the PCB Editor to fit your screen.
4. Use the ***Display – Zoom – Window*** to zoom in around the ***BGA*** towards the top center of the board.
5. Select ***Route – Create Fanout*** from the top menu.
6. Select ***BGA Quadrant Style*** in the **Via Direction** section of the **Options** tab



7. Click on the U5 **BGA**

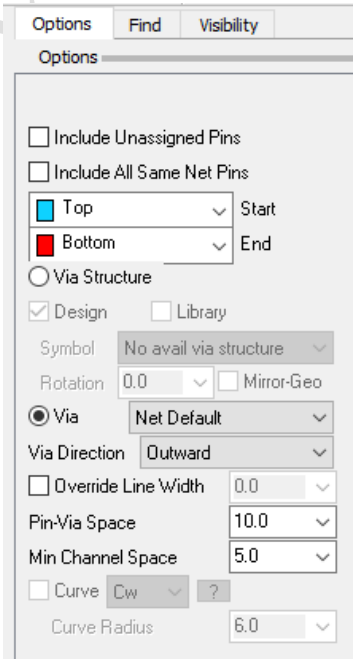


8. Now, use ***Display - Zoom - Window*** to zoom around C3, the decoupling capacitor that is just above U1.



Note The order of the capacitors and resistors may be different than the order shown above.

9. Select ***Route - Create Fanout*** from the top menu, if you are not still in the command.
10. In the ***Find*** tab, make sure that ***Symbols*** and ***Pins*** are both enabled.
11. In the ***Options*** tab set the options as displayed below:



12. Click on C3.
    The capacitor will have a 'via' fanout extending outward from each pad with a spacing between the pad and the 'via' of 10 mils.

Note If you only had "Pins" enabled in the Find Filter you could have had to click on each pin of C3 to add the fanouts.

Copy Fanout

1. Select ***Route - Copy Fanout*** from the top menu.
2. In the ***Options*** tab set the "***Copy Fanout to***" option to ***same device type***.
3. Click on the C3.
   Notice that the decoupling capacitors above U2, U3 and U4 and all of the decoupling capacitors in the memory section now have fanouts.
4. Right click and select **Done** from the popup.

Save the Design

1. Choose ***File - Save As*** from the top menu.
2. Rename this drawing by entering the following in the File Name field: **`fanout`**.
3. Select **Save** to save the **`fanout.brd`** file.

End of Lab

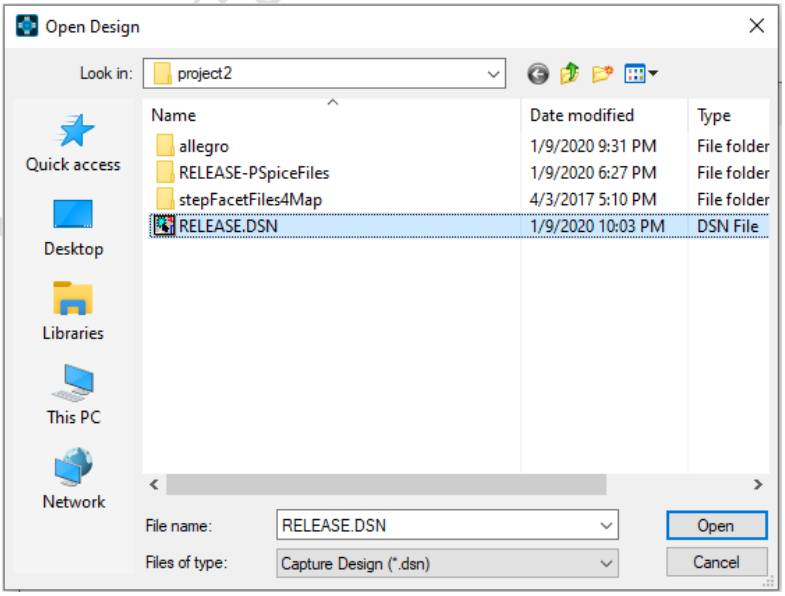
Lab 9-3: Using the OrCAD Capture Schematic for Manual Placement

Objective: Use the OrCAD Capture schematic to select and place components in the physical layout.

In this lab, you will use the OrCAD Capture schematic to place and move components in the PCB Editor design. Do ***not*** save the results of this lab.

Opening OrCAD Capture

1. Make sure PCB Editor is **closed** before you start this lab.
2. To start the OrCAD Capture tool, choose ***Start - All Apps - Cadence Release 17.4-OrCAD Capture CIS***.
3. The ***Cadence Product Choices*** form will appear, prompting you for which tool you want to check out. Select ***OrCAD PCB Designer Standard*** and press ***OK***.
   The OrCAD Capture or OrCAD Capture CIS window displays with no projects open.
4. Choose ***Open Design*** from the ***Getting Started*** window displayed when you open OrCAD Capture.
   A file browser window opens.
5. Navigate to the *C:- EMA_Training - PCB_Designer - project2* working directory, select **`release.dsn`**, and click ***Open***.

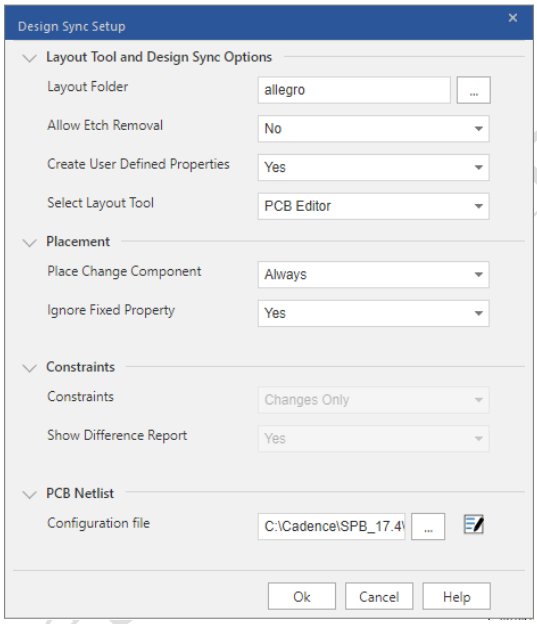


6. Next, choose ***Options - Preferences***.
7. In the ***Options - Preferences - Miscellaneous*** tab, make sure the ***Enable Intertool Communication*** option is checked, then click ***OK***.

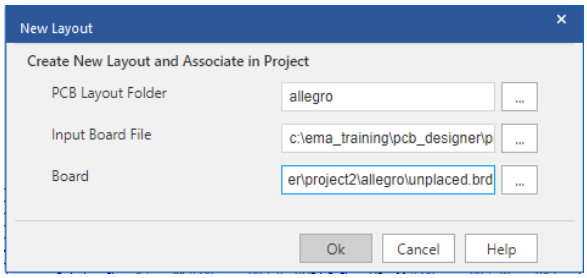
8. Click the + ***symbo***l on the left side of **`release.dsn`** to expand the design.
9. Click the + ***symbol*** on the left side of ***Release Root Schematic*** to expand the drawings in the design.
10. Double-click ***Page 1*** of the Root Schematic to open that drawing.

Running Design Sync

1. Select ***PCB – Design Sync Setup*** from the top menu in OrCAD Capture.
   The **Design Sync Setup** form appears.
2. Fill in the form as you see in the figure below and click ***OK***.



3. Select ***PCB – Design Sync*** from the top menu in OrCAD Capture.
   The **New Layout** form opens.
4. Fill in the fields in the **New Layout** form as follows:
   - PCB Layout Folder = ***C:\EMA_Training\PCB_Designer\project2\allegro***
   - Input Board File = ***C:\EMA_Training\PCB_Designer\project2\allegro\unplaced.brd***
   - Board = ***C:\EMA_Training\PCB_Designer\project2\allegro\unplaced.brd***



5. Click ***OK***
6. The ***Cadence Product Choices*** form will appear, prompting you to select a tool.
   Select ***OrCAD PCB Designer Standard*** and press ***OK***.

Cross placement between OrCAD Capture and PCB Editor

1. PCB Editor will open with the `unplaced.brd` file from ***project2 - allegro*** folder.
2. Arrange the OrCAD Capture and PCB Editor so that they each occupy half of your screen, one on the left side, the other on the right.
3. In the PCB Editor window, choose ***Display - Zoom - Fit*** to see all of the PCB Editor board.
4. In the PCB Editor's top menu, select ***Setup - Application Mode - General Edit***.
5. In the PCB Editor's top menu, select ***Place - Components Manually***.
6. Click the ***Hide*** button to temporarily close the ***Placement*** form.
7. Move your cursor into the schematic project's ***Page 1*** schematic window, select one of the ***FCT16245*** (U1, U3 and U4) components and move your cursor into the PCB Editor graphics window.
   The component you selected in the schematic is attached to your cursor in PCB Editor.
   If the components were previously placed on the board, you can delete them from the board and replace them.
8. Practice cross selecting components in the schematic and moving them into PCB Editor. When you are finished, right-click and choose "***Done***" from the pop-up menu in PCB Editor.

Cross Highlighting and Dehighlighting Between PCB Editor and OrCAD Capture

Now that you have several components placed on the board, you can do cross highlighting between the PCB Editor board file and the OrCAD Capture schematic.

1. Choose ***Display – Highlight*** from the top menu in PCB Editor.
2. Click on one of the newly placed parts in PCB Editor.
   The corresponding component in the schematic is selected.
3. Click on a couple more parts in PCB Editor.
   The corresponding components in the schematic are selected. The selection in the schematic is cumulative. If a different schematic page contains the component you've selected in PCB Editor, the appropriate page opens in the schematic.
4. In PCB Editor, choose ***Display - Dehighlight***.
5. Click one of the previously highlighted parts in PCB Editor.
   The corresponding component in the schematic is unselected.
6. If you have time, you can try highlighting and dehighlighting some Nets as well.
7. ***Exit*** OrCAD Capture and ***Exit*** the PCB Editor. Do ***not*** save these designs in either tool.

End of Lab

Lesson 10: Interactive Routing and Glossing

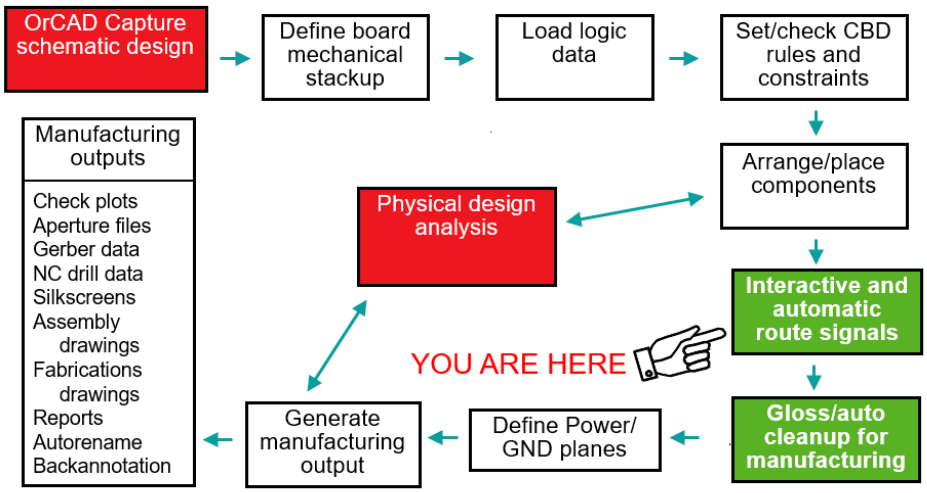
Learning Objectives

In this lesson, you will:

- Define and display etch grids used for routing
- Add and delete connect lines (clines) and vias
- Use Slide and Replace Etch to improve routing
- Use the Cut option in conjunction with other editing commands
- Use the Gloss to automatically clean up the routed etch in the design

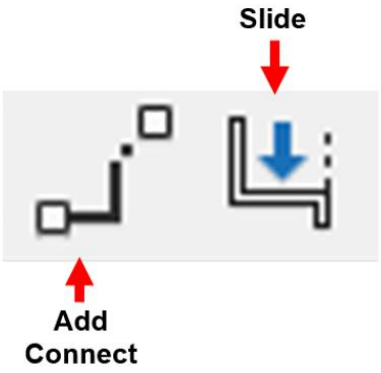
In this module, you will learn how to interactively route your printed circuit board. You will learn how to add etch to make signal connections and will also learn the commands used to edit existing etch on the board.

Design Layout Process



At this point in the design process, the logic has been loaded, the board mechanical has been defined, the design rules or constraints have been set and the components have been placed. You will now route the design using interactive techniques.

Accessing Interactive Routing Modes



Use a **Route** command to access interactive route mode quickly. When you use routing commands, the etch grid is displayed.

Icons associated with routing are:

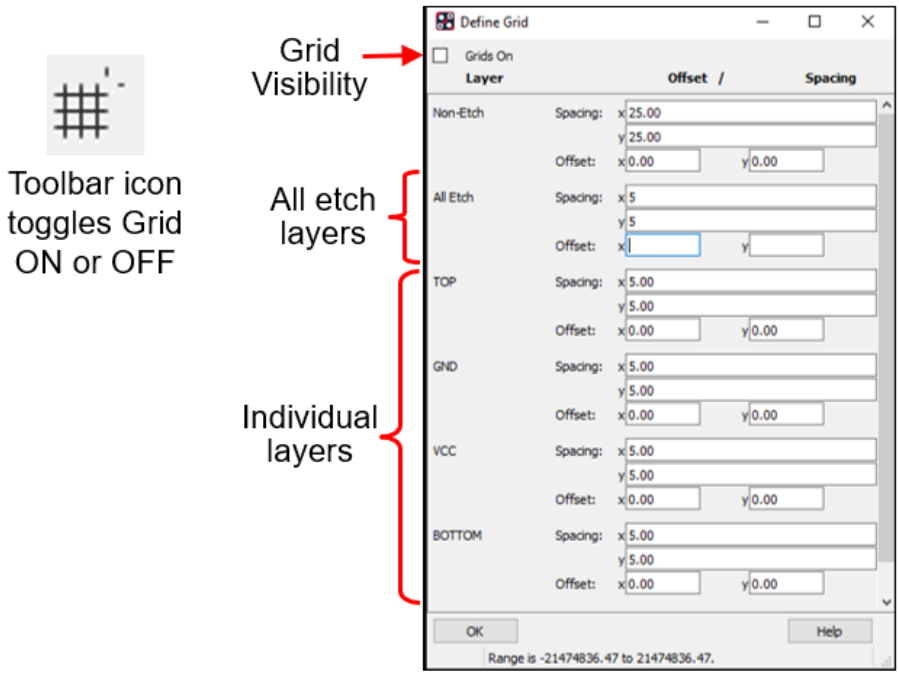
- **Add Connect -** Used to make electrical connections between pins.
- **Slide -** Used to move existing traces.

Other commands available from the **Route** pulldown menu are:

- **Custom Smooth -** Used to smooth or remove extra jogs in individual nets after interactively routing traces.
- **Create Fanout -** Allows you to create fanouts (pin-escapes) automatically. You can fanout parts or nets, either by window or selecting them individually.
- **Copy Fanout –** Allows you to copy fanouts to other components with like packages, or device types on the same layer.
- **Convert Fanout** – Allows you to Mark a trace and via combination as a fanout, so that is can be moved with its associated component. You can also unmark an existing trace and via combination.
- **Via Structure** – Allows you to create complex via and line combination structures that may be used as fanouts, etc.
- **Resize/Respace – Via-Via Line Fattening –** Fattens lines between vias that are a specified maximum distance apart.
- **Gloss Line Parameters** – Use to smooth or remove extra jogs in lines and maximize the length of the 45-degree segments. Can also remove floating lines.

Routing Grids

*Setup - Grids **OR** RMB - Quick Utilities - Grid*



Access to the ***Define Grid*** form can be made using one of the following:

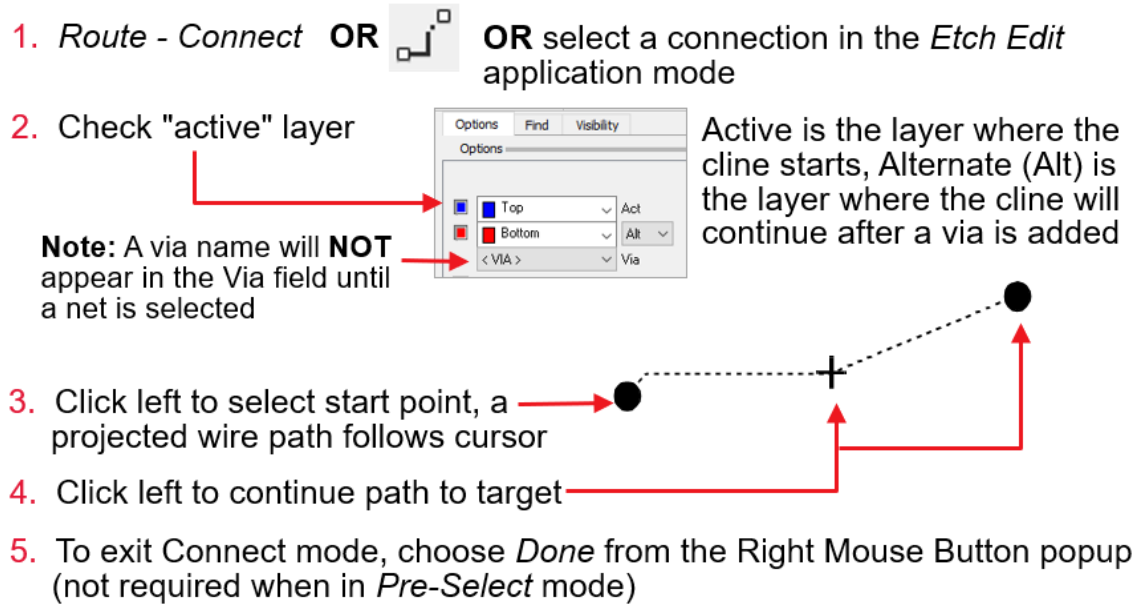
- Select ***Setup - Grids*** from the top menu
- Use the ***Right-Mouse-Button*** to select ***Quick Utilities - Grids*** from the pop-up menu

Much like the grid used when placing parts manually; a grid is also used when you are routing interactively. However, it is a different grid. The etch grid is the section starting from "All Etch" and traversing to the bottom of the grid form. The origin of the routing grid is the origin of the design file. You can use the **Grid Toggle** icon to turn the grid display ON or OFF.

The form shows a fixed routing grid of 5 on all layers. A fixed grid system uses a consistent increment or spacing between grid lines in the x and y direction. Entering the route grid in the **All Etch** section defines the same grid on all the etch layers at once. If you want to use a different route grid on a certain layer, enter it into the individual layer's section. Use the scroll bar on the right side of the form to see all the individual layers.

The etch grid is automatically displayed, if grids are visible, whenever a **Route** command such as ***Route - Connect*** is executed. This is the snap grid that is used when you graphically route a trace in your design. If you set the routing grid and your grid is displayed, but you still cannot see the routing grid, set the Active Class in the Options tab to an Etch layer.

Adding Signal Connections



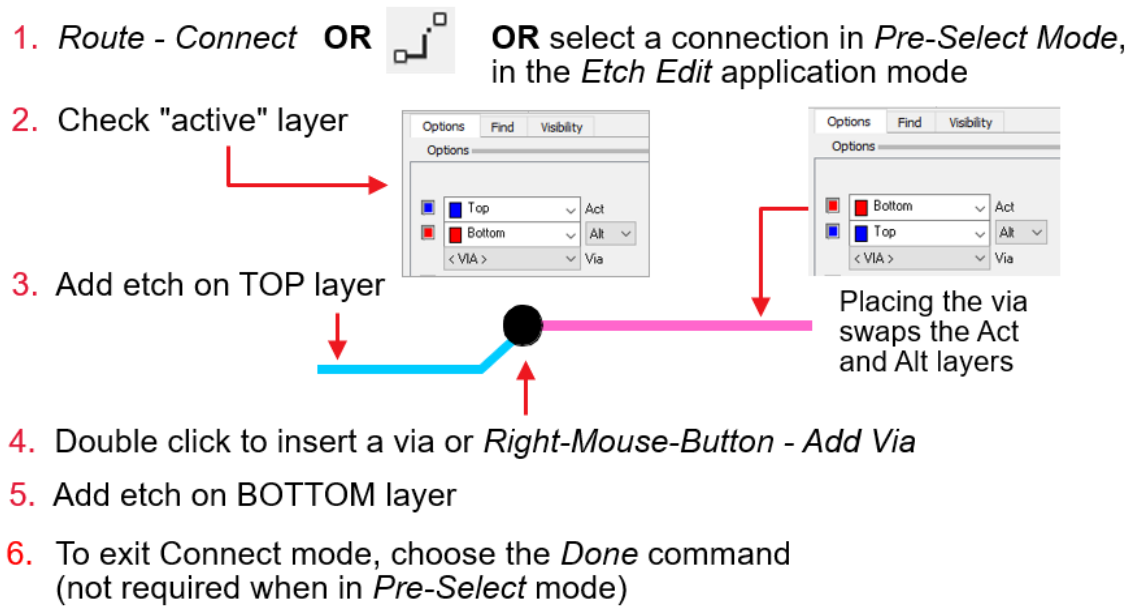
To add signal connections, select ***Route - Connect*** from the top menu, or use the ***Add Connect icon***. This puts you into add connect mode, ready to add connect-lines (or clines). Clines differ from other graphic lines in that they have signal name intelligence and adhere to design rules for width and spacing.

Next, verify that all settings are correct in the ***Options*** tab. It is very important to check the settings of the ***Act***ive and ***Alt***ernate layers in the ***Options*** tab when adding etch. If the routing does not appear on the etch subclass that you expected, it is probably due to an incorrect ***Act***ive layer setting. We will give a detailed description of these settings later in this lesson.

Next, select a point where you wish the routing to start from. This can be a pin, via, ratsnest line, or at a point where there is nothing. Once you have selected a start point, a projected wire path follows your cursor. This is the wire segment or connection that will be added to the design. Between your cursor and the target pin is a target line that acts as a directional guide that shows you where you must go to complete the connection. Once you have reached the destination point, select "Done" from the Right-Mouse-Button popup to end the command.

You can also use the Pre-Select mode to manually route connections. If you are in the *Etch Edit* application mode, when you select a pin, via, or ratsnest, you will automatically be placed in the ***Add Connect*** command.

Inserting Vias

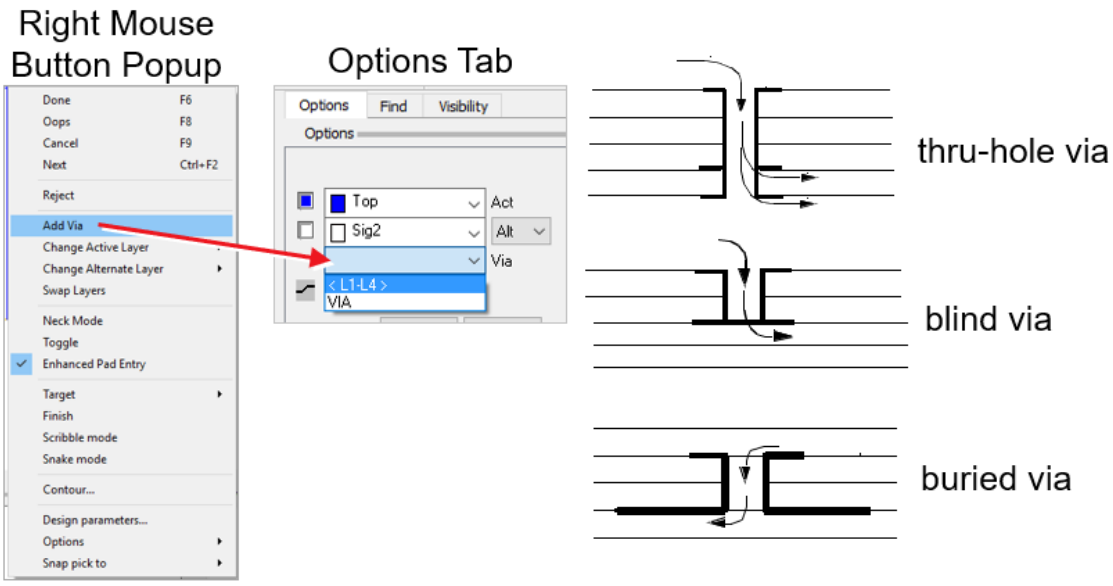


This section explains how to use the **Add Connect** command to add vias to a design.

1. Select ***Route - Connect*** from the top menu. Notice that the *Options* window changes. In the Pre-Select mode, if you are in the *Etch Edit* application mode, selecting a pin, via, or ratsnest, will automatically place you in the ***Add Connect*** command
2. Verify all settings in the *Options* window.
3. Begin adding the connection by picking vertex points, using the Left-Mouse-Button in your PCB Editor's work area.
4. To add a 'via', check the *Alternate* layer in the *Options* window (and change if necessary). Then double-click the Left-Mouse-Button. You can also use the ***Right-Mouse-Button - Add Via*** option from the popup.
5. Notice that the **Act**ive and **Alt**ernate layers have swapped. You can continue adding your connection on the currently active layer.
6. Click right and select **"*Done*"** to complete the ***Connect*** command. If you started routing using the ***Pre-Select mode***, once a connection is finished, the ***Add Connect*** command is automatically terminated.

Remember that the 'via' padstack that is used will be the 'via' you defined as the default via in the Physical Constraints form of the Default Rules.

Selecting Via Types



The PCB Editor attempts to use the most "conservative" via. When using blind and buried vias, this means that the PCB Editor will attempt to use the blind or buried vias before using a through-hole via

In the case shown, since the Active layer was set to Top, the Alternate layer was set to Sig2, and there was a buried via defined between these two layers, the PCB Editor will by default select this via. However, you can always override this by selecting a different via. Remember, the available vias are defined in the Physical domain of Constraint Manager.

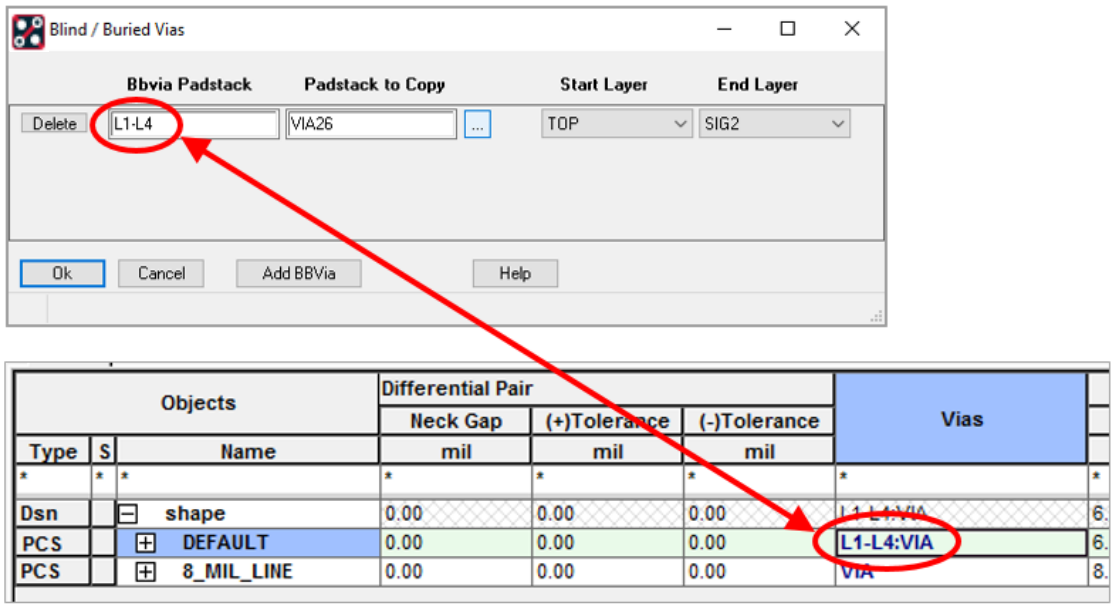
In order to add vias that differ from the default via padstack you defined, you must add them to the list of available vias in the physical constraint rules. There are two types of vias: through-hole or blind/buried. You can add either type as part of a connection.

- A ***through-hole*** via is a plated hole that passes through all layers of your design. Through-hole vias are the most common. They are easier and cheaper to manufacture than blind or buried vias, but block routing channels on all layers of the board.
- A ***blind*** via is a plated hole that starts from an external layer but is not drilled through all layers.
- A ***buried via*** is a plated hole that starts from an internal layer and extends to another internal layer but never reaches the external surface of the fabricated board.

Note Blind and buried vias do not block routing channels on all layers and thus allow more connections to be made on very compact designs. These types of vias require separate drilling files for the various drill stages required by manufacturing and are therefore more expensive to produce.

Define Blind/Buried Via

Setup - Define B/B Via



Once the Blind/Buried Via has been defined it has to be added to the appropriate Physical Constraint Set(s) in order to be used

Blind and buried vias (bbvia) are padstacks that do not have a regular pad on both the top and bottom layers but do span at least two conductor layers. Bbvias may be created using *pad_designer* and imported into the Physical domain of the Constraint Manager, or in PCB Editor by selecting ***Setup - Define B/B Via*** from the top menu.

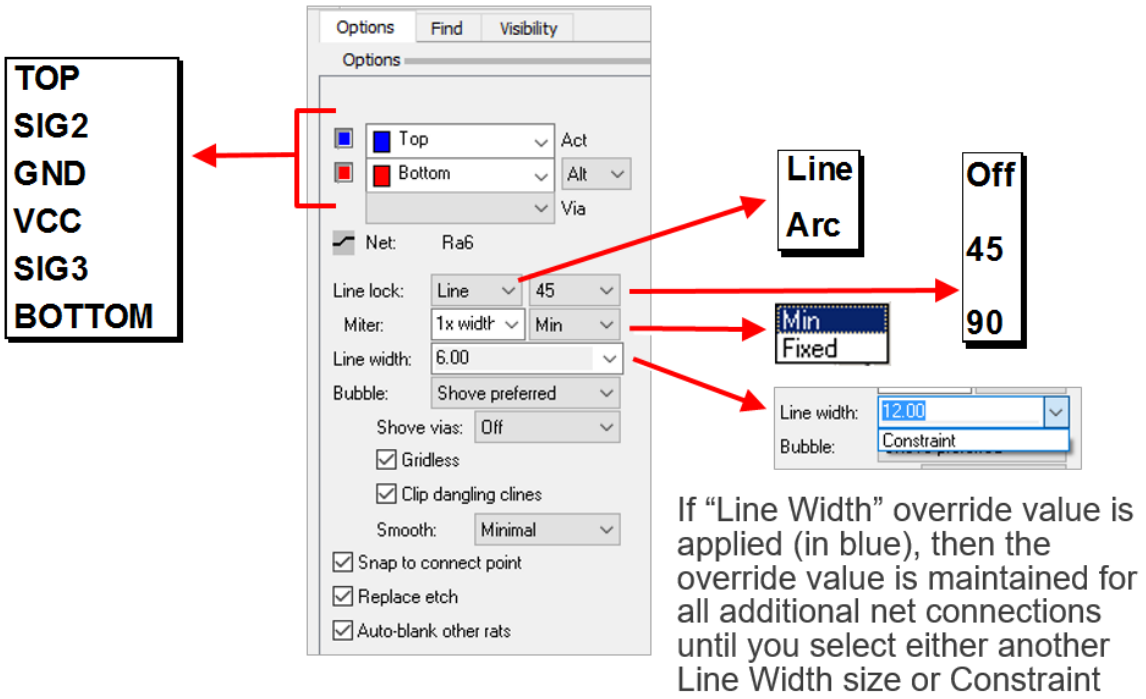
Options and Buttons

- **Add BBVia -** Creates a new entry block for a padstack to be created.
- **Delete:** Removes its entry block and removes the associated padstack from the PCB Editor database.
- **Bbvia Padstack -** Enter the name of the new padstack to be created.
- **Padstack to Copy -** Indicates the source padstack to use as a template in creating the new bbvia. This may be a padstack in the design or from the library.
- **Start Layer -** Displays a popup listing each conductor layer in the design. Select the name of the conductor layer that begins the new padstack.
- **End Layer -** Displays a popup listing each conductor layer in the design. Select the name of the conductor layer to end the new padstack.

Using B/B Vias in the Design

After the blind/buried vias are defined, their names are entered in the Physical Rule Set under the Vias column. Select which Physical Constraint Set will include the blind/buried vias. Then select which blind/buried via padstacks you want to route with in that Constraint Set by adding then to the list of vias. Separate via padstacks with the ":" (colon) character.

Routing - Options Tab

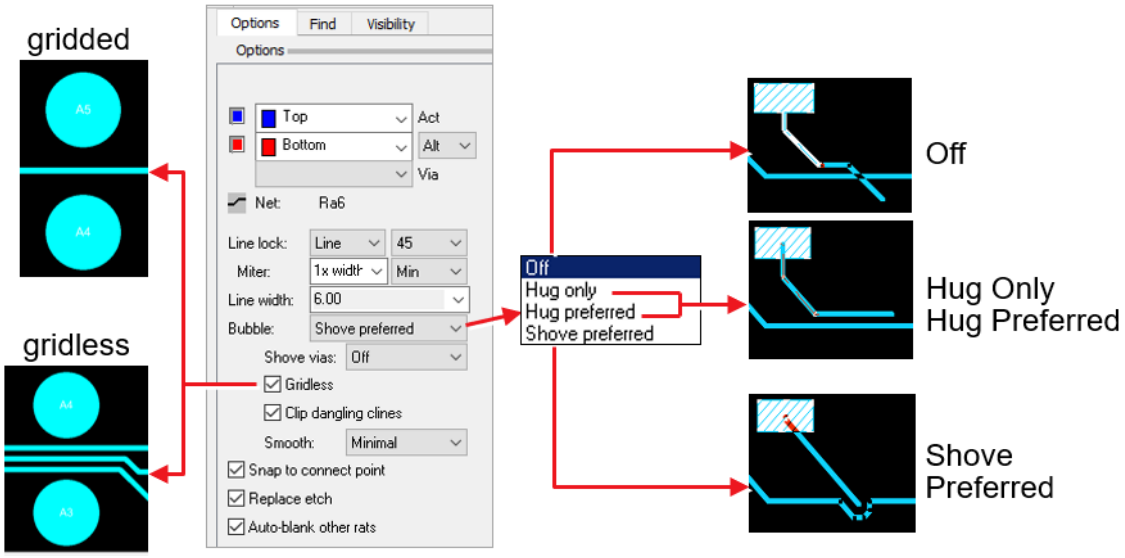


When you select the ***Add Connect*** command, the *Options* tab displays the possible settings. You can change any of the parameters here or by using the RMB popup.

- **Act** and **Alt** - The **Act**ive and **Alt**ernate subclass fields define a pair of layers to be used for the current connection. The **Act**ive and **Alt**ernate layers are swapped if you select ***Swap*** from the RMB popup or add a 'via'. When selecting a surface-mount pin or a piece of existing etch, the **Act**ive layer will automatically be set to the appropriate subclass.
- **Line Lock** - These settings control the type of line, either Line or Arc, and the angles allowed for turns. Off implies that "any-angle routing" is allowed.
- **Miter** - Defines the value for the miter size. This can be set to a certain length, miter value (i.e. 5), or it can be set to a relative value of the current line width (i.e. 3x width) to get *n* times the line width. In general, the resulting segment length will be the (square root of 2) times the miter value.
  - **Min** - The resulting corner length is not restricted.
  - **Fixed** - The length entered in the field is used to add a corner at that length.
- **Line Width** - The line width value is based on the Physical Constraints. When you select a pin for routing, the PCB Editor program recognizes the net, and automatically displays the Net Name and required line width size in the Options tab. You can also type an override value into this field.

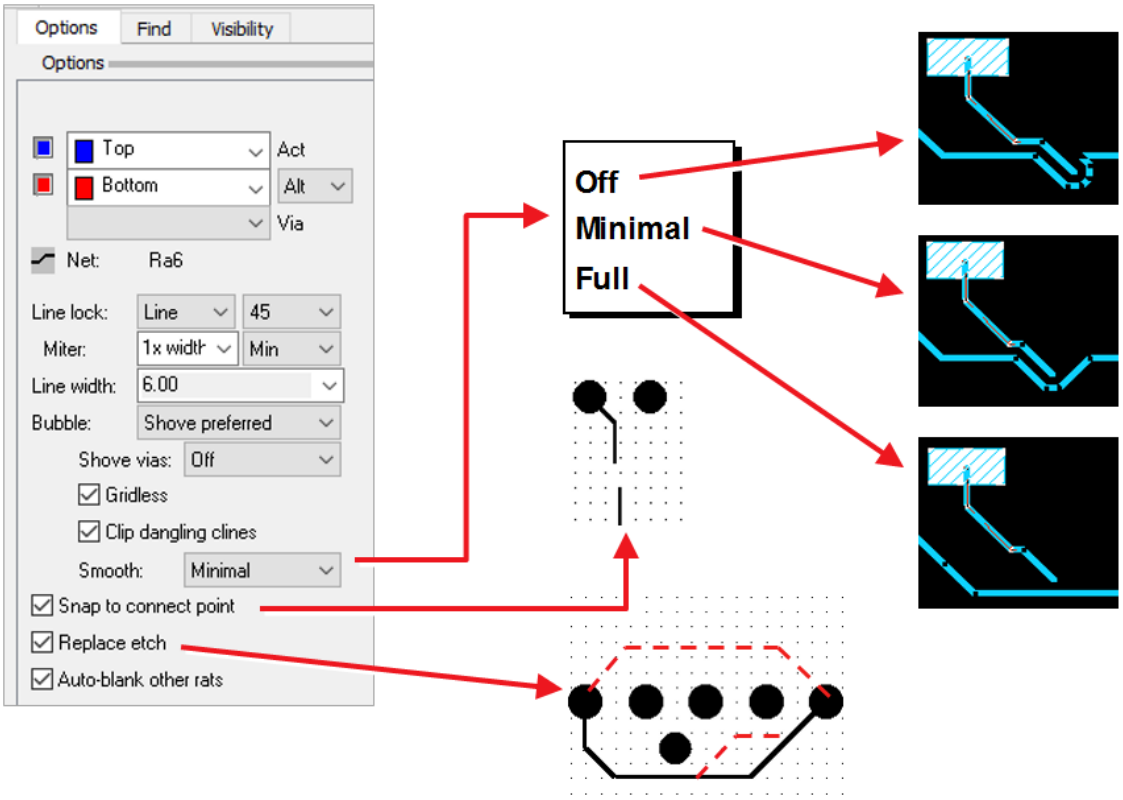
Note If you override the line width, the override value is maintained until you change it to another override or select "Constraint" from the pull-down arrow.

Routing - Options Tab - Bubble/Gridless



- **Bubble** - The Bubble field provides these choices:
  - **Off** - Means the route follows your cursor picks exactly, regardless of the potential for DRC errors.
  - **Hug Only** - Means the routed cline contours around other etch objects to avoid spacing DRCs. Other etch remains unchanged.
  - **Hug Preferred** - Means the new route attempts to hug around existing etch objects, if possible. If not possible, it will attempt to shove.
  - **Shove Preferred** - Means other etch objects are shoved and moved out of the way, if possible, to correct for spacing violations.
- **Gridless** - This feature determines whether the added etch is snapped to the routing grid or not. Gridless is only available if Hug Preferred or Shove Preferred is enabled. This option offers two choices:
  - **Off** - Pushes etch to the next available free grid.
  - **On** - Shoves just enough to reach a legal minimum DRC clearance.
- **Shove Vias** – Used to shove vias when adding or sliding connections. Requires that Bubble is NOT set to 'Off'.
  Choices here are based on how Bubble is set:
  - **Off** - Never moves an existing via.
  - **Minimal** - *Hug-Preferred Mode* - Clines hug the vias unless there is no room, then shoving occurs; *Hug-Only* - Clines hug the vias. Other etch remains the same; *Shove- Preferred Mode* - Clines hug the vias unless there is no room, then shoving occurs.
  - **Full** - *Hug-Preferred Mode* - Clines hug the vias unless there is no room, then shoving occurs; *Hug-Only* - Clines hug the vias. Other etch remains the same; ***Shove-Preferred Mode*** - Vias are shoved. If a 'via' cannot be shoved, the PCB Editor goes around it.

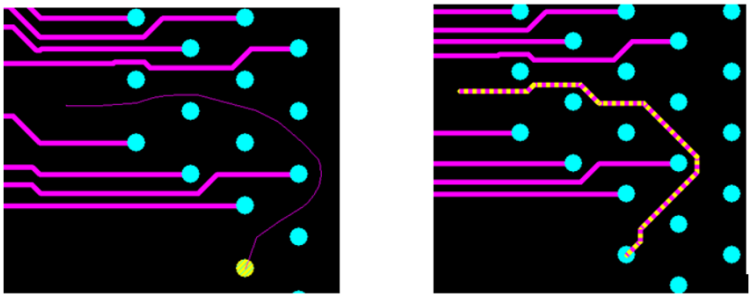
Routing - Options Tab - Smooth



- **Smooth -** This feature automatically smooths or cleans up routing as it's being added. This is required, since the interactive router performs real-time push and shove etch. Smooth is only available if Hug Preferred or Shove Preferred is enabled.
  The Smooth option offers three choices:
  - **Off** - Means this feature is disabled. Existing etch affected by the current route may end up with more vertices and bends.
  - **Minimal** - Will eliminate only a few extra segments.
  - **Full** - Will eliminate more segments similar to the **Custom Smooth** command.
- **Snap to Connect Point -** This option lets you connect to the center of off-grid pads, vias, or dangling endpoints. This option is preferred.
- **Replace Etch -** Etch lets you change the path of an existing trace, without extra delete and add steps. When you add a loop into an existing trace, the older portion of the loop is recognized and automatically deleted.

Scribble Route Mode

Scribble Routing Mode lets you scribble a route path between two points using smart shove and push techniques. Once the routing is completed the etch solution is generated by the application for the scribble path.



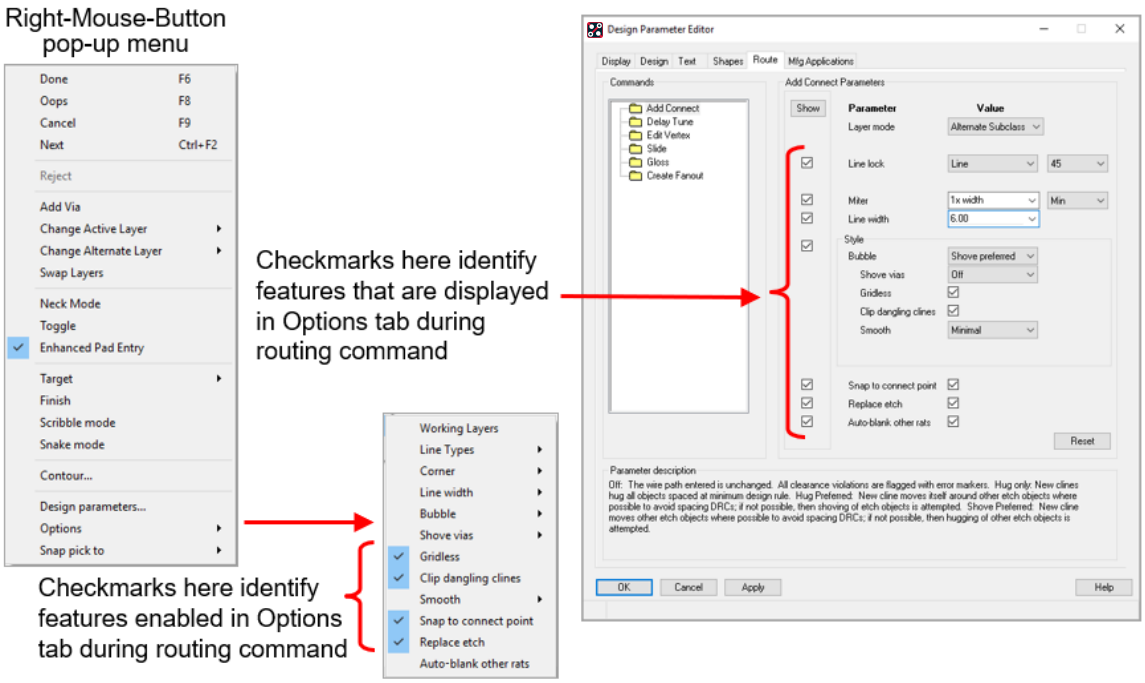
Scribble mode is designed to route in complex routing areas using the ***Add connect*** command. Once a route has been started in the ***Add connect*** command, you can select ***Scribble mode*** from the **RMB** popup.

Scribble mode creates an off-angle path through pinch points, keeping the rest of the route path at 45 degrees. It moves the existing routes only when necessary to avoid a DRC violation.

Note Use the ***Tab*** key to toggle between scribble mode and the normal add connect mode.

To avoid conflicts during interactive routing Clip dangling lines is disabled when using scribble mode.

Setting Interactive Route Parameters



All the parameters that affect interactive routing can be set in the ***Route*** tab of the ***Design Parameters*** form. These will be the default values when starting command. These values may be changed in the ***Options*** tab of the ***Control Panel*** if required during interactive routing.

The ***Show*** column is used to make the parameters visible or invisible in the ***Options*** tab. For instance, if you always have Clip dangling connect lines set to yes, and you never change it, you can uncheck the box to the left of this parameter, so it does not appear in the Options window.

To change the parameters while in the Add Connect command, you can also use the ***Right-Mouse-Button - Options*** selections. When you change the parameters while interactively routing, the values are remembered from one Add Connect command to the next. If you change the parameters while interactively routing, the Design Parameters form is also updated.

Labs

Lab 10-1: Defining Etch Grids

- Define and display a grid suitable for routing traces

Lab 10-2: Adding and Deleting Connect Lines and Via

- Learn how to add and complete a connection
    - Add a connect line (cline)
    - Delete etch
    - Inset vias
    - Use the bubble option

Lab 10-1: Defining Etch Grids

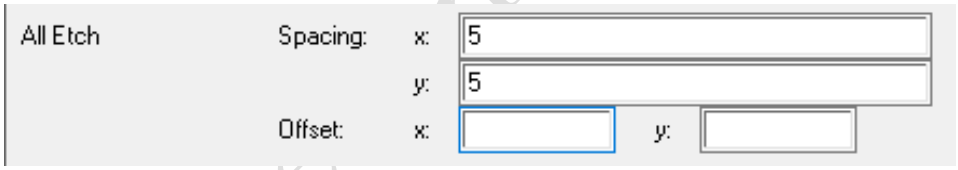
Objective: Define and display a grid suitable for interactively and automatically routing traces.

Defining Grids

1. Start the PCB Editor if you don't already have it running and open the `fanout.brd`. If you did not finish the previous labs, you may find the `fanout.brd` in the ***solutions*** folder.
2. Select ***Setup – Grids*** from the top menu
   The ***Define Grid*** form appears.
3. In the ***Grids On*** option in the upper left corner of the form, toggle the grids to ***ON***.

Note Before you proceed to the next step, please note: To advance to the next field in any PCB Editor menu, use the ***Tab*** key. Do ***not*** press the ***Enter*** key to advance fields. The ***Enter*** key has the same result as clicking the ***OK*** button, closing and executing the form.

4. Locate the section marked **All Etch** and set the **X** and **Y s**pacing values to ***5*** as shown in the figure: The settings automatically change for all other etch layers.



5. Click ***OK*** at the bottom of the ***Define Grid*** form.
6. Select ***Setup – Application Mode - Etch Edit*** from the top menu.
   This will ensure that we are viewing the Etch, or routing grid.
7. The Etch grid displays. You can **Zoom In** to get a closer look at the etch grid.

Note If you had set the grid to alternating 8 9 8 mil intervals instead of a straight 5 mil grid, you would see a distinct repeating grid pattern, showing a larger dot every 25 mils with smaller dots at 8 9 and 8 mil intervals.

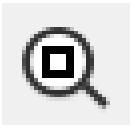
End of Lab

Lab 10-2: Adding and Deleting Connect Lines and Vias

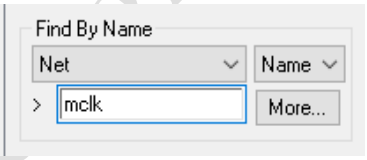
Objective: Add a signal connection with and without vias to become familiar with the various etch editing commands.

Adding a Connect Line

1. Click the ***Zoom Fit icon*** to fit the entire design in your view.

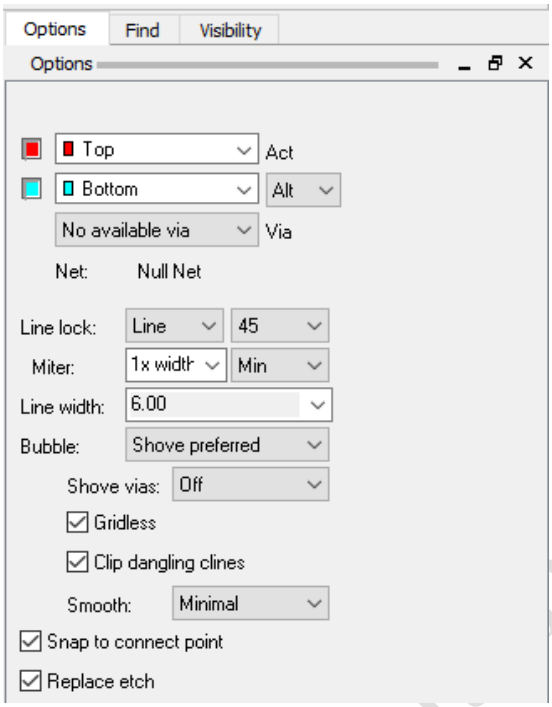


2. If ratsnests are currently displayed, choose ***Display - Blank Rats - All*** from the top menu to turn off all ratsnests.
3. Choose ***Display - Show Rats - Net*** from the top menu.
4. In the **Find by Name** section of the ***Find*** tab, select ***NET*** from the drop-down menu.
5. In the value (>) field, enter the following net name: **`mclk`**



The ratsnest line for the MCLK signal is displayed.

6. If the display has not automatically zoomed around the MCLK rat line, choose ***Display - Zoom - Window*** and zoom in around the MCLK rat line going between J1, and U5.
7. Click the ***Add Connect*** icon  (same as ***Route - Connect*** command)
8. Open the ***Options*** tab to display the window before you select a pin to start from, all settings should match the following illustration.

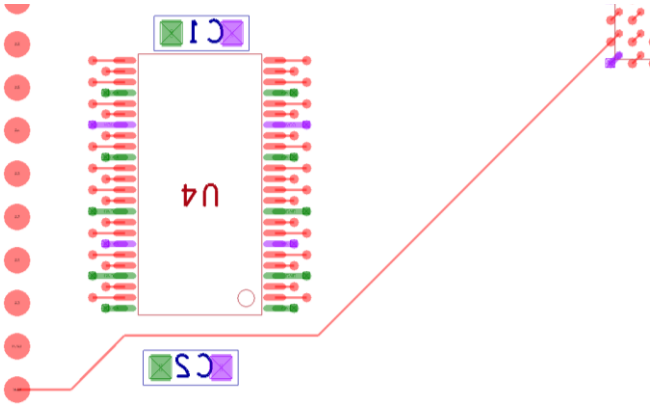


9. Click on the ***pin of the J1 connector***, which is the endpoint of the ***MCLK*** ratsnest line.
   Since the TOP layer is active and the pin is a through-hole pin, you are adding a connection on the top layer of the board. If this were a surface-mount pin, the connection would be added to the layer on which the SMD pin was defined.

   After you select the start point, you see a ratsnest line stretching from the cursor to the nearest destination pin. As you move your cursor, the route appears.

   Notice also that the net name and the correct line width for MCLK are now displayed in the ***Options*** tab when visible. Also, notice that the MCLK net name is embedded in the pins and the trace as you connect it.

10. Continue to click points for the line until you reach the destination pin/via. You can make your trace look similar to the figure:



If you make a mistake while picking points, right-click and choose ***Oops*** from the popup. This allows you to backup while staying in the command.

When you reach the destination pin, the ratsnest line disappears, denoting the completion of that connection.

If the destination pin was on the bottom side of the board and was not previously fanned out, you would need to add a 'via' in order to connect to the pin. You will learn how to add vias shortly.

11. Right-click and choose "***Done***" from the popup menu.

Deleting Etch

The PCB Editor program provides several ways to delete etch lines. You can delete lines, segments of lines, and sections within segments. Be sure that you set the ***Find*** tab and the ***Options*** tab so that only the desired items are deleted. You can also delete etch in a Pre-Select mode.

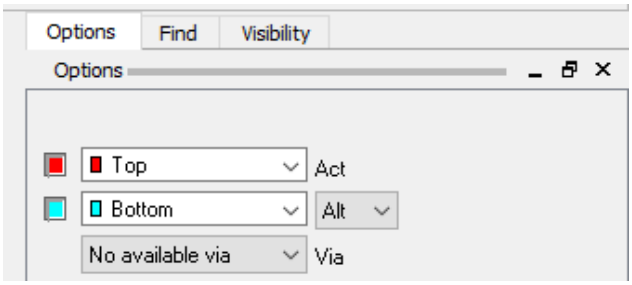
1. Click on the ***Delete icon*** in the toolbar.

Note Default settings in the Find tab may show all items toggled ON. This can be dangerous while in delete mode. As a general rule, you should turn all items OFF, then select only the items you want to delete.

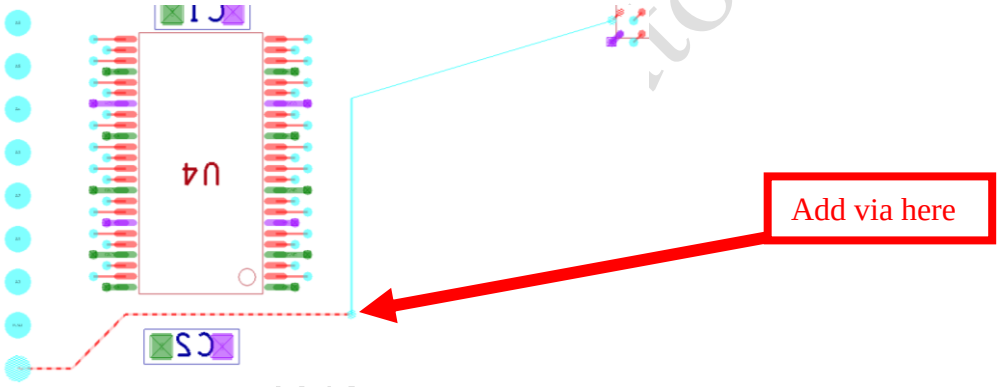
2. In the ***Find*** tab, click the ***All Off*** button and then click the **Clines** (connect lines) box to '***ON***'.
3. Click on the ***MCLK*** net.
   The connection becomes highlighted. This gives you the opportunity to right-click and choose ***Oops*** from the popup if you accidentally selected the wrong element.
4. Right-click and choose "***Done***" from the popup.
   The etch you added previously disappears. Using Clines in the Find Filter lets you delete the entire connect line (all segments from pin to pin, or pin to via).

Inserting Vias

1. Click the ***Add Connect icon*** in the toolbar.
2. In the ***Options*** tab, set the active and alternate layers as shown in the figure below:

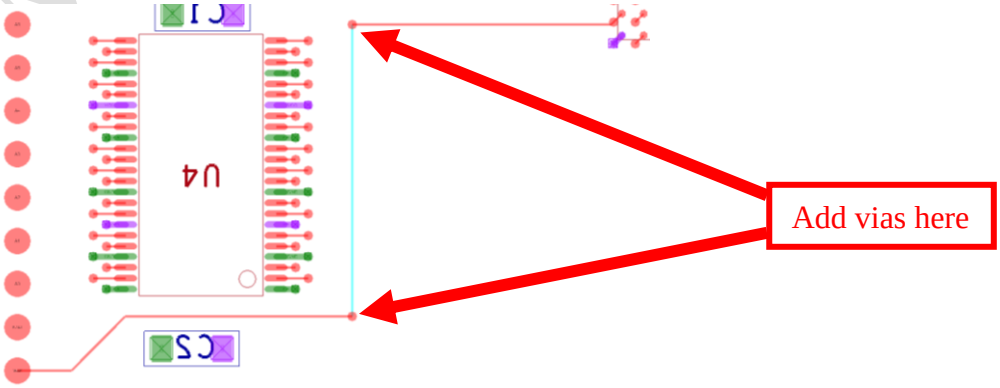


3. Click on the ***J1 pin*** of the ***MCLK*** net, the pin connected to one end of the ratsnest.
4. Once again, begin adding segments from that pin toward its destination.
5. When you have reached a point where you would like to add a 'via', ***double-click*** with the ***Left-Mouse-Button***. See the figure.



You have just added a 'via', and the Active and Alternate layers in the Options tab have been swapped. You are now routing on the BOTTOM side of the board.

6. Finish the connection all the way to the fanout on the ***pin of the U5*** component. Since there is already a fanout via on the destination pin, we can route the net on either layer of the board. See the figure below.

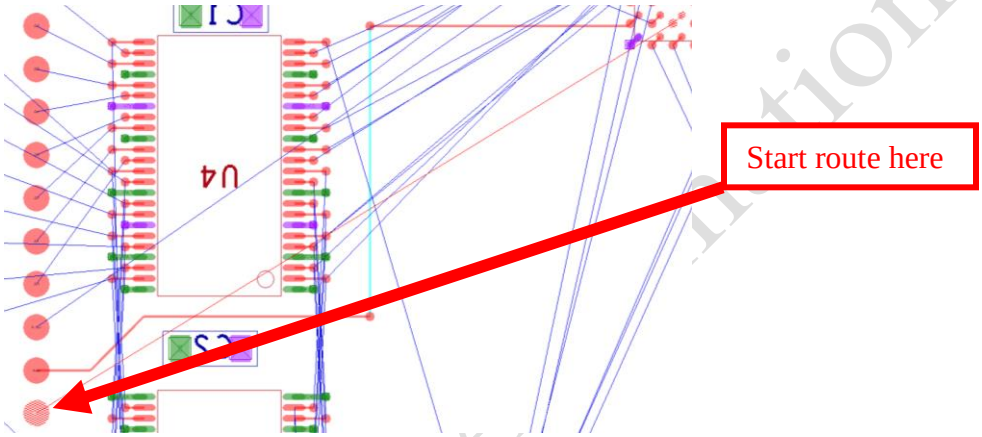


7. Right-click and choose "***Done***" from the pop-up menu.

Using the Bubble Options

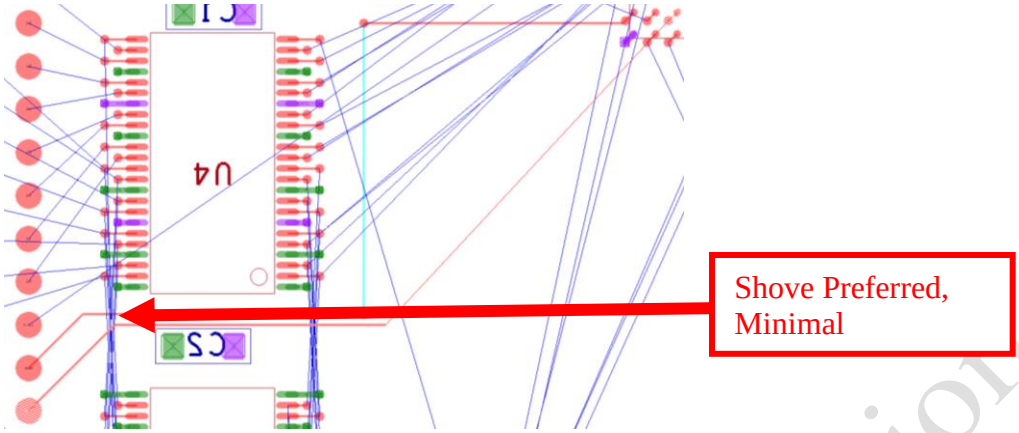
1. Click the **Rats All** icon to turn on all ratsnests.
2. Zoom into the area to view the ratsnest connection between the ***J1*** connector and the ***U5*** component ***just below the MCLK*** net. See the figure below.

Note Your view may differ slightly, depending on your component placement.



3. Click the ***Add Connect icon*** in the toolbar.
4. In the ***Options*** tab, set the ***active layer*** to ***TOP***, ***Bubble*** field to ***Shove Preferred*** and set the ***Smooth*** field to '***Minimal***' if these options are not already selected.
5. Click on the ***pin*** just ***below the MLK*** pin of the ***J1*** connector. This is the ***WAIT*** net. See figure above. Start moving your cursor toward the existing etch of the MCLK net. The existing etch will be "shoved", or moved, as the new etch becomes closer than the DRC "line to line" value.
6. Experiment with the different ***Smooth*** options of '***Off***', '***Minimal***' and '***Full***' that are available in the ***Options*** tab, and with the different ***Bubble*** options of '***Off***' and '***Hug Preferred***'. Also experiment with the ***Shove vias*** option.

Note While you are in this mode, there may be some instances when the trace to be added will create a DRC. When this happens, your cursor will appear as a DRC marker to warn you.



7. Finish routing the ***WAIT*** net.
8. Right-click and choose "***Done***" from the pop-up menu.
9. Choose ***File - Save As*** from the top menu.
   A browser form appears.
10. In the File Name field, enter: `mclk_route`
11. Choose **Save**.
    The file `mclk_route.brd` has been saved to disk.

End of Lab

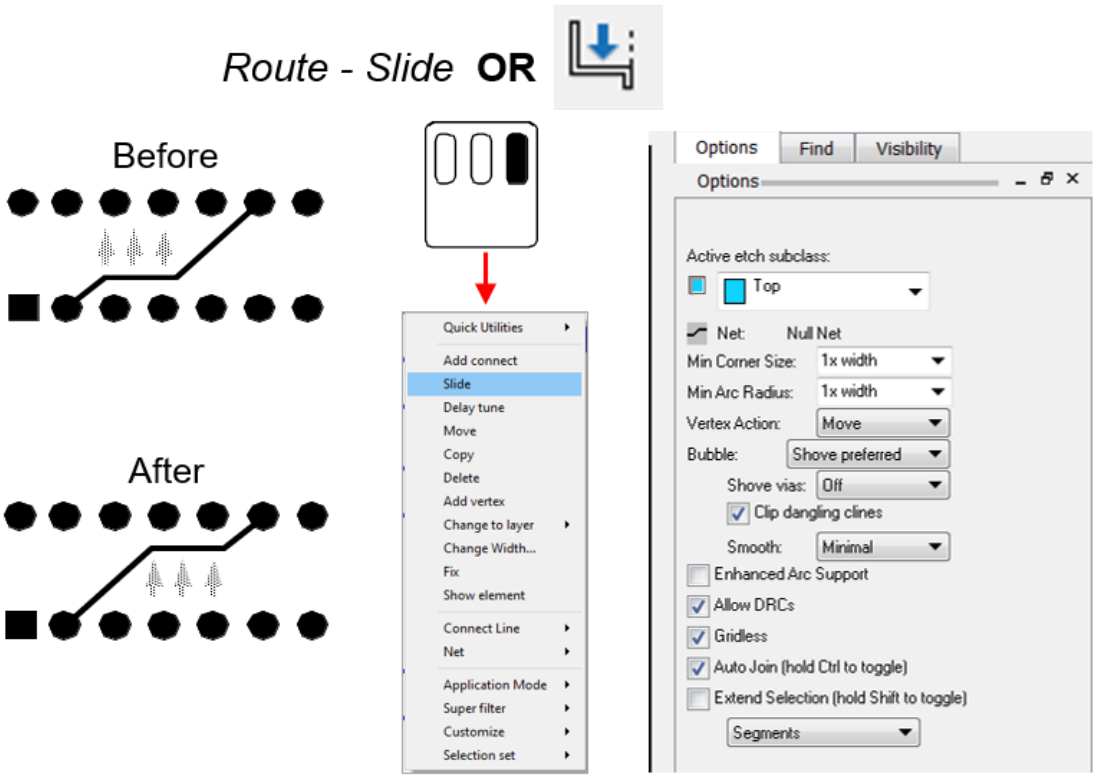
Editing Existing Etch

This section explains various editing options available while in ***Edit Etch*** mode. The ***Options*** tab plays a very important role during etch editing. The ***Options*** tab changes to match different types of editing needs and is an integral part of editing control.

Some examples of editing existing etch:

- Sliding connections and vias
- Editing vertices
- Moving a connection to another layer
- Deleting connections

Moving Etch with the Slide Command



The Slide command lets you move a segment of a connection with or without moving the associated vias. The moved segments do not become disconnected.

Follow these steps to slide a segment of etch:

1. Select the ***Route - Slide*** command on the top menu.
2. Click on the etch line segment, or via with the ***Left-Mouse-Button*** and move your cursor in the desired direction. Notice, in the ***Options*** tab, the net name of the connect line segment you are sliding.
3. Position the line and click the ***Left-Mouse-Button*** once more.

You can also use the Pre-Select mode to slide connections. If you are in the ***Etch Edit*** application mode, select with the ***Left-Mouse-Button*** on a segment of etch and move you cursor with the line segment to the desired location and click again.

Settings in the *Options* tab affect the resulting etch:

- **Min Corner Size -** Sets the minimum 45-degree corner length allowed between two non-parallel cline segments. This field also supports [N] x width values.
- **Min Arc Radius –** Sets the minimum arc size allowed between two cline segments. This field supports [N] x width values. This value prevents arcs from completely collapsing during slide operations.
- **Vertex Action -** Controls the action when you select a vertex between two segments during the slide operation or when running the Slide command. A special vertex cursor is shown as an indication when a pick gets the vertex rather than a segment.
  The choices are:
  - **Line Corner -** Causes the current angle at the vertex to be split and a new segment is created. The new segment is then active on the cursor and can be modified using the Slide command. This would allow you to change a 90-degree corner into a 45-degree or split any other existing angle. This is very useful to cleanup 90-degree corners, adjust off-angle corners, or reduce lengths of existing routes.
  - **Arc Corner -** Causes an arc to be created at the selected vertex. The new arc is then active on the cursor and it can be modified using the Slide command. This is very useful to convert 90 or 45 corners to arcs.
  - **Move (default) -** Causes the vertex to move as both adjacent segments are modified using the Slide command. This is essentially a 2-segment operation.
  - **Edit -** Edits the vertex similarly to the *Edit - Vertex* command.
  - **None -** Prevents any special action when a vertex is selected.
- **Bubble**: Controls automatic bubbling (moving of existing connections) to resolve DRC errors. Enabling either of the hug modes or shove-preferred bubble mode sets the Line lock field to Line to prevent you from adding arcs while in shove-preferred or hug-preferred mode. Bubble mode does not support arcs.
  The choices are:
  - **Off -** Flags all clearance violations with error markers.
  - **Hug Only -** Where possible, the routed cline contours to other etch/conductor elements to avoid creating spacing DRCs. Other etch/conductor elements remain unchanged.

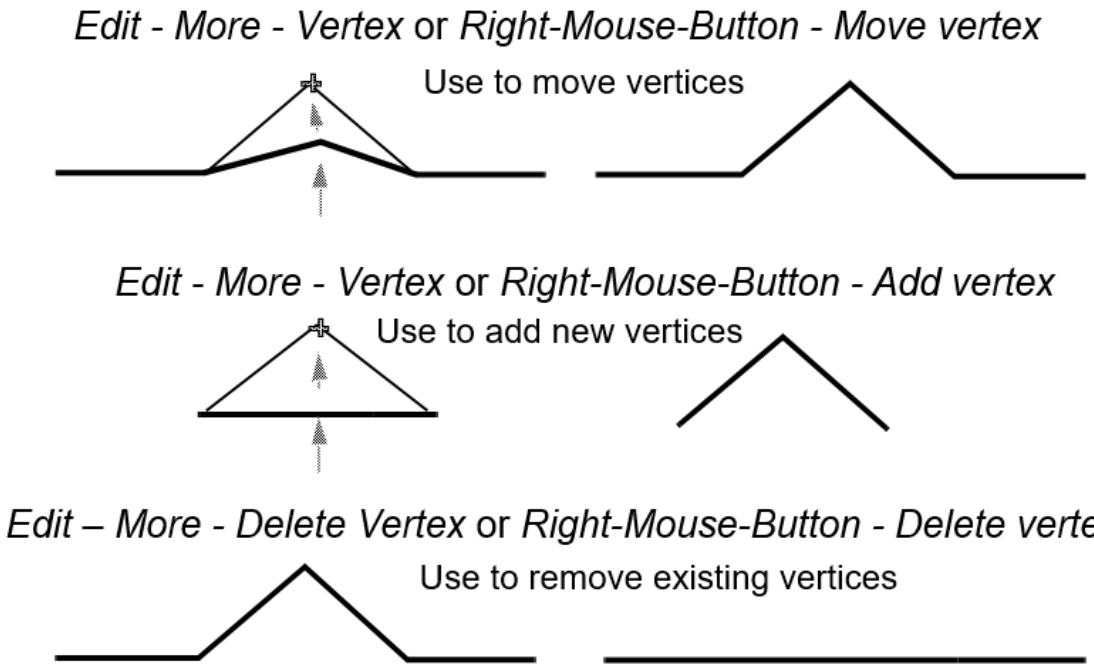
    - **Hug Preferred -** Where possible, the routed cline contours to other etch/conductor elements to avoid creating spacing DRCs. If not possible, shoving of other etch/conductor elements to open routing paths is attempted. **Note:** This method is more aggressive than Hug Only.
    - **Shove Preferred -** Where possible, the routed cline pushes and shoves other etch/conductor elements to avoid creating spacing DRCs. If not possible, the layout editor tries hugging other etch/conductor elements.
- **Shove Vias -** Allows the bubble functionality in shove mode to move vias when you are editing etch. It is only active when the bubble functionality is enabled.
  Choices are:
    - **Off -** Vias are not shoved.
    - **Minimal -** Vias are shoved in a hug-preferred manner. Vias are not moved unless there is no way to draw a connect line around them.
    - **Full -** Vias are shoved in a shove-preferred manner. Any new or edited etch always shoves vias out of the way.
- **Clip dangling clines -** This option clips dangling clines that are too close (violate spacing constraints) to any line segments you are editing. It is active only when bubble functionality is enabled in shove mode.
- **Smooth -** Controls whether smoothing occurs on the cline to minimize segments between the start and finish points. Smoothing occurs dynamically as you move the mouse on cline segments close to the segment you chose. Only segments changed by sliding or bubble options are smoothed. Performance with the Smooth option active may be somewhat slower than when it is inactive.
  The choices are:
    - **Off -** Choose to disable smoothing
    - **Minimal -** Executes dynamic smoothing to minimize unnecessary segments.
    - **Full -** Executes more extensive smoothing to remove any unnecessary jogs. An additional segment on each end of the changed segments can be included.
- **Allow DRCs – Enabled:** The layout editor can violate design rules to make the edit. The violations are flagged with DRC markers.
  Allow DRCs – Disabled: If DRCs exist, or if the layout editor determines that DRCs will be introduced to the design, the layout editor does not slide the connection.
- **Gridless -** Specifies whether, or not the connect line or via you are sliding must adhere to the routing grid. When you enable gridless routing, the layout editor can slide connections at maximum density while accommodating the minimum spacing design rules. This affects your connections only if bubble is active.
- **Auto Join –** When 'ON' (Default), this option causes same-direction cline segments to join as they line up during the slide operation, allowing the user to continue the current operation on larger sections of the cline. When 'OFF', this option does not join same-direction cline segments when they line up unless a click is made.
- **Extend Selection -** When 'ON', this option extends the original selection made during the slide operation to include the two cline segments at each end of the selection. The 'OFF' (Default) behavior does not affect the original selection.

Arc Corners - Extend selection can be used when sliding a 45/90-degree segment that has arc corners and you want to maintain the arcs while the selected segment slides. This option is similar to the arcs with segments option.

The choices are:

- **Segments -** Extends selection to adjacent segments. This is the default option.
- **Vias -** Extends selection to adjacent vias.
- **Segments and Vias -** Extends selection to both segments and vias.

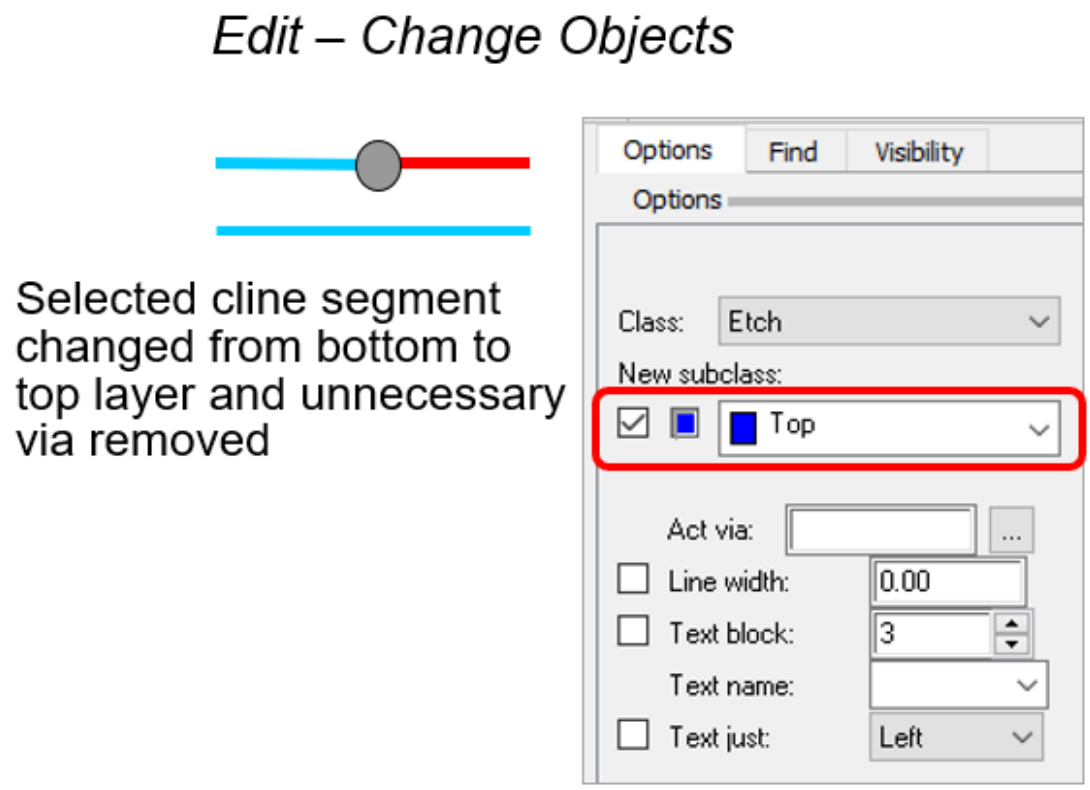
Editing Vertices



A vertex in an etch line is a point at which the line changes direction or creates a corner.

- To ***Move*** an existing vertex, use either the ***Edit – More - Vertex*** from the top menu or the ***Move vertex*** from ***Right-Mouse-Button*** popup, click on the vertex and place it in the new position
- To ***Add*** a vertex, use either the ***Edit – More - Vertex*** from the top menu or the ***Add vertex*** from ***Right-Mouse-Button*** popup, click on a point in the existing cline segment and place the point in the new position
- To ***Delete*** an existing vertex, use either the ***Edit – More – Delete Vertex*** from the top menu or the ***Delete vertex*** from ***Right-Mouse-Button*** popup and click on the vertex to remove it

Changing the Layer of a Connection

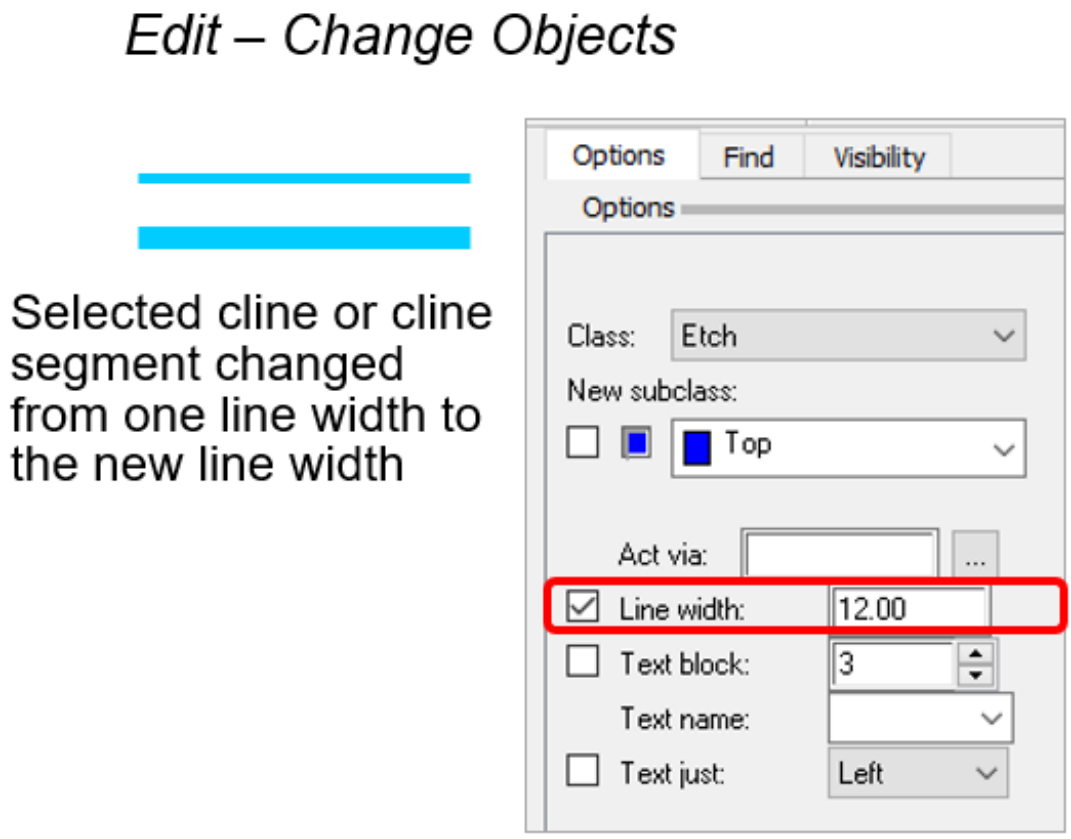


Use the ***Edit – Change Objects*** command from the top menu to change the layer of an existing connect line. From the ***Options*** tab, use the ***New Subclass*** drop-down menu to select the appropriate etch layer for the change. When you select any visible connect line in your work area, it immediately changes to the layer that you designated in the New Subclass field.

Note Vias are added or deleted automatically if the layer change dictates.

In Pre-Select mode, if you are in the ***Etch Edit*** application mode, when you move your cursor over a cline, the ***Right-Mouse-Button*** pop-up menu will have a ***Change Layer*** option where you can select the new etch subclass.

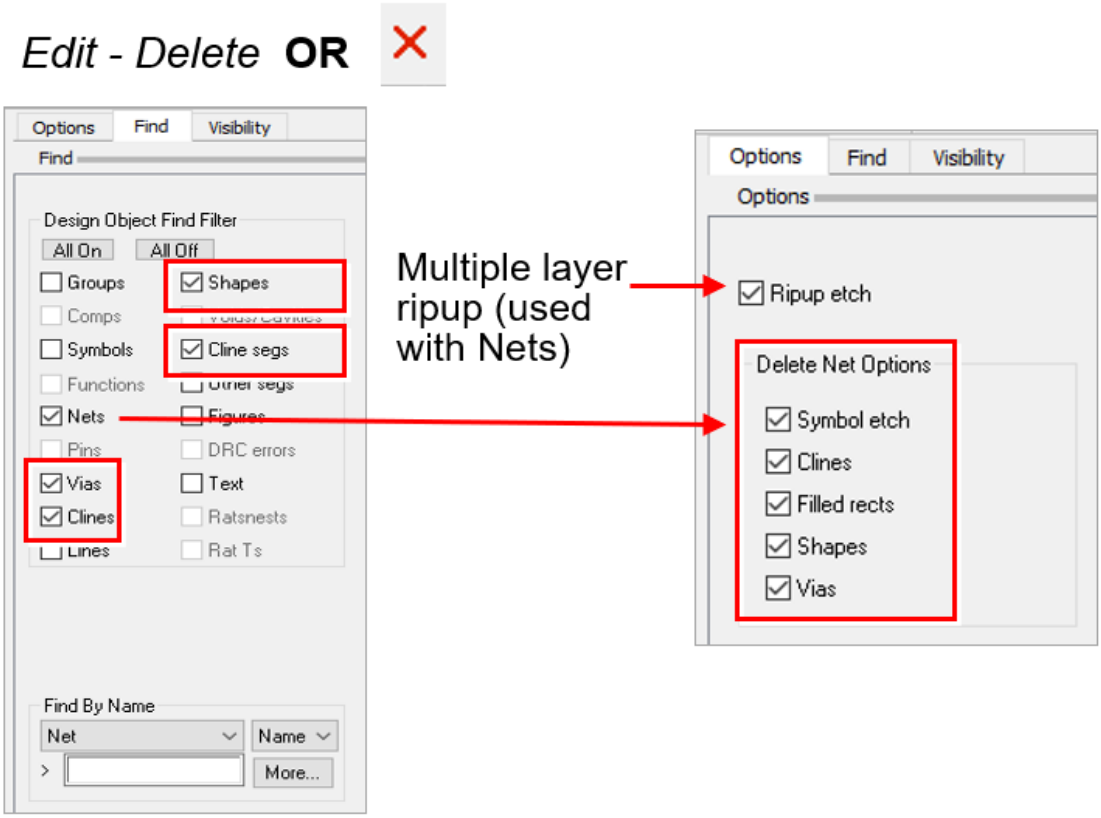
Changing the Line Width of a Connection



Use the ***Edit - Change*** command from the top menu to change the line width of an existing cline or cline segment. From the ***Options*** tab, set the ***Line Width*** field to the new line width. When you select any visible connect line or connect line segment in your work area, it immediately changes to the line width that you set in the Line Width field.

In Pre-Select mode, if you are in the ***Etch Edit*** application mode, when you move your cursor over a piece of cline, the ***Right-Mouse-Button*** popup menu will have a ***Change Width*** option that will open a Change Width form where you type in the new width.

Deleting Etch



To delete etch lines and vias, select ***Edit - Delete*** from the top menu. The ***Find Filter*** and the ***Options*** tab control the actions of this command. In the ***Find Filter*** turn all items '***Off***', then toggle '***On***' only the items you want to delete. Most often this would include Clines, Cline Segs and/or Vias. Select the desired options in the ***Options*** tab next and specify which types of etch you want to delete.

By manipulating the ***Find Filter*** and the ***Options*** tab, you can define which portions of a net to delete.

You can choose the following combinations:

- Use **Cline Segs** to delete a single segment of a net.
- Use **Clines** to delete all segments, excluding vias.
- Use **Vias** to delete vias.
- Use **Clines** and **Ripup Etch** to delete all segments and vias between pins (multiple layer ripup).
- Use **Nets** and **Delete Net Options** (**Clines** and **Vias**) to perform a multiple layer ripup for all etch on a net.

Select "***Done***" from the popup to complete the deletion process.

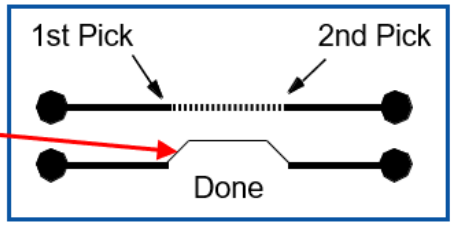
You can also use the Pre-Select mode to delete etch. First, make sure you are in the ***Etch Edit*** application mode. You can use the ***Tab*** key to either select a cline segment, an entire cline, or a 'via'. After selecting the desired etch, use the ***Right-Mouse-Button*** popup and select ***Delete*** to remove the selected etch.

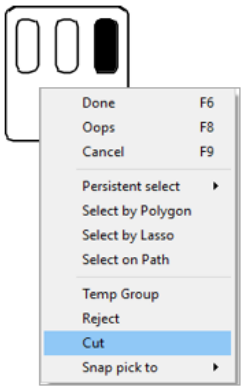
Using the Cut Option

- Activate the command first
- ***RMB - Cut***
- Click two points in the SAME segment
- ***RMB - Done***

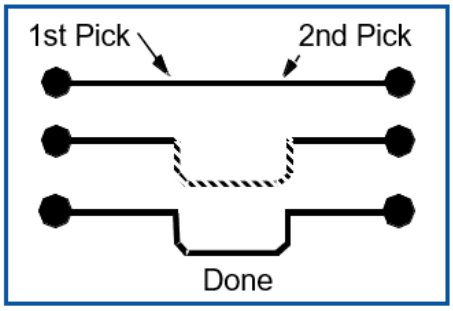
Edit - Delete

Places ratsnest between break

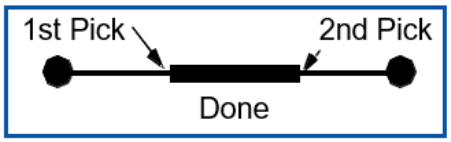




Route - Slide



Edit – Change Objects
(width and/or layer)



You can use the ***Cut*** option to edit specific sections within a line segment. Use the ***Cut*** option with the ***Edit - Delete***, ***Route - Slide***, and ***Edit – Change Objects*** commands. The Cut option is not available in the Pre-Select mode.

Access the **Cut** option through a popup menu available in all three of these commands. By selecting the **Cut** option with the Right-Mouse-Button, you can define a start and end point within a single line segment. Once you define this section of line, you can delete, slide, or change its width and or layer, depending on which command you started with.

Interactive Routing Properties

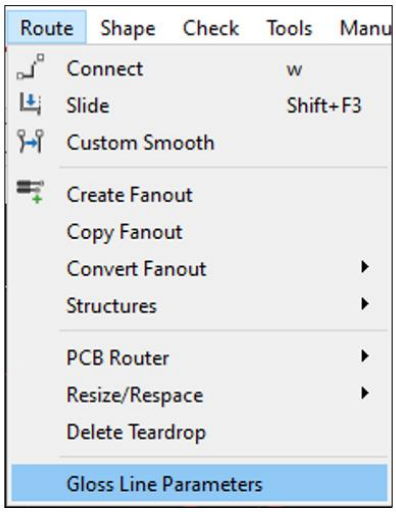
- Net properties affect not only the autorouter actions but also DRC checking while in interactive route mode
- Define net constraints and properties before adding etch
- Common net properties used with interactive route are:
    - **MIN_LINE_WIDTH** – May be added as a Physical Constraint override in the Constraint Manager, Physical domain
    - **MIN_NECK_WIDTH** – May be added as a Physical Constraint override in the Constraint Manager, Physical domain
    - **MAX_LINE_WIDTH** – May be added as a Physical Constraint override in the Constraint Manager, Physical domain
    - **NO_RAT** – May be added as a Net Property in the Constraint Manager
    - **FIXED** – May be added using the Fix icon

Note  Trace Width Properties are automatically populated when Constraint Overrides are added in the Constraint Manager.

- The **MIN_LINE_WIDTH** and **MIN_NECK_WIDTH** properties determine default trace widths for specific signals
- The **MAX_LINE_WIDTH** is a property you can set to specify a maximum width the trace can be.
- The **NO_RAT** property prevents the display of ratsnest lines. Most often used on GND and VCC nets
- The **FIXED** property can be attached to nets immediately after adding etch. This property prevents future modification.

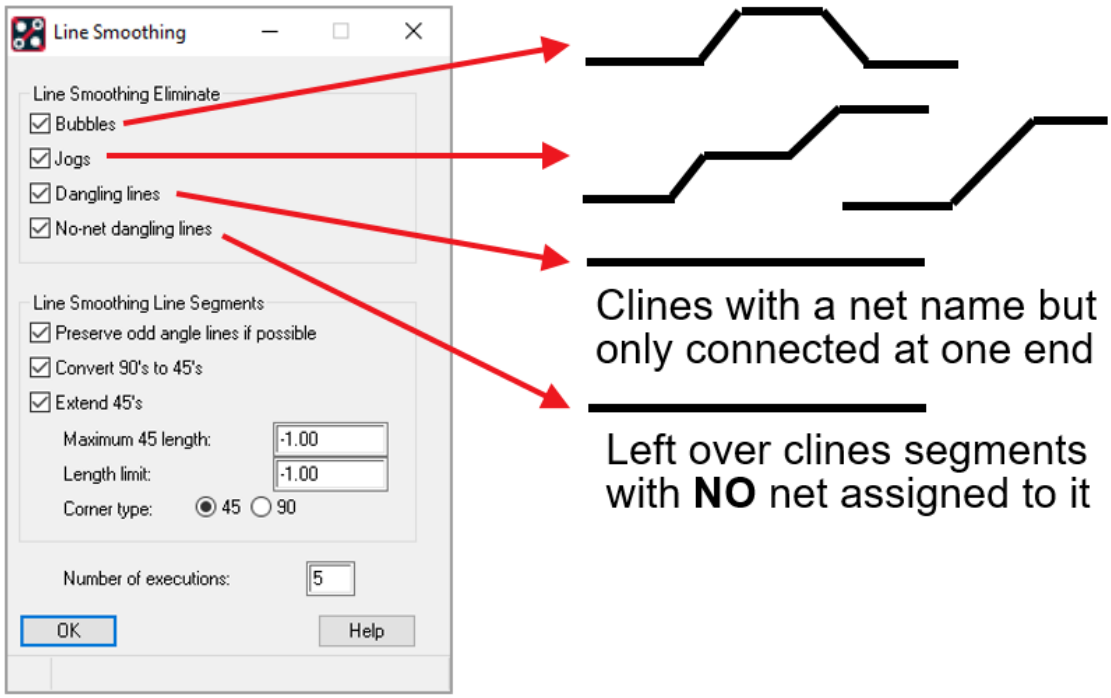
Gloss Line Parameters

Route – Gloss Line Parameters



PCB Editor Standard includes ***Gloss Line Parameters***. This program runs the ***Line Smoothing*** utility which cleans up extra jogs and vertices in clines created during routing by the push and shove features.

Line Smoothing



Line Smoothing removes extra jogs and line segments in the design. It also converts orthogonal corners to diagonal corners. Line smoothing is a good tool to help open channels during routing.

- **Bubbles** - Line Smoothing is a tool that smooths bubbles configured around pads that are no longer in the design.
- **Jogs** - Specifies the elimination of repeated jogs or "stair steps."
- **Dangling Lines** - Indicates whether Line Smoothing eliminates connect lines without two owners (pins or vias). These lines are usually connected to a pin, via, or T junction on one end and unconnected on the other. The default is 'ON'.
- **No-net dangling lines** - Indicates whether Line Smoothing eliminates connect lines not associated with any net.
- **Preserve odd angle lines if possible** - Specifies Line Smoothing preserve odd angle lines (unless removing them shortens the connection).
- **Convert 90's to 45's** - Changes orthogonal 90-degree angles to 45-degree diagonals.
- **Extend 45's** - Attempts to extend the 45-degree segment so that either the horizontal or the vertical segment can be eliminated.
    - **Maximum 45 Length** - Specifies the maximum orthogonal distance to which a 45-degree angle segment will be extended.
    - **Length Limit** - Limits the maximum length of line segments that are to be considered by Line Smoothing.
        - Bubbles are processed if the orthogonal segment in the bubble is less than or equal to the value of this parameter. Diagonals whose orthogonal length of the diagonal is longer than this value are skipped. The default value is -1 and indicates no length limit.
        - Jogs are only considered if the orthogonal segment in the jog is less than or equal to this limit. The default value is -1 and indicates no length limit.
    - **Corner Type** - Specifies whether corners are diagonal (45) or orthogonal (90). The default is 45.
- **Number of Executions** - Specifies the number of times that Line Smoothing is executed. It is recommended that you run multiple passes. The default value is 1.

Labs

Lab 10-3: Improving Routed Connections

- Learn how to improve etch paths using the Slide function and other techniques for adding, deleting, and moving vertex points on existing etch

Lab 10-4: Using the Cut Option

- Learn how to use the Cut option in conjunction with other editing commands

Lab 10-5: Running Gloss

- Learn to run the Line Smoothing routine

Lab 10-3: Improving Routed Connections

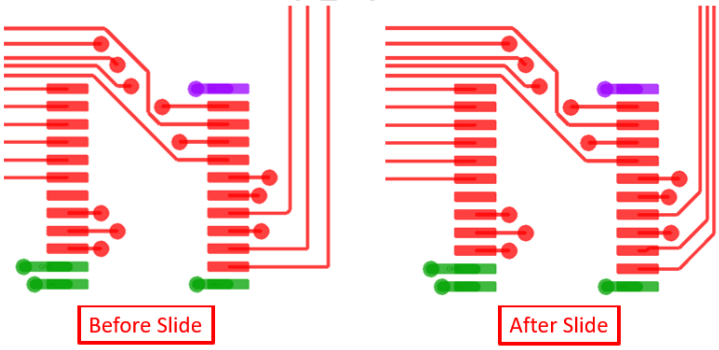
Objective: Improve etch paths to partially clean up the traces using the Slide command, the replace etch function, and other techniques for adding, deleting, and moving vertex points on existing etch.

Using Slide

Thus far you have been adding new etch. This next lab exercise focuses on editing or moving existing etch.

1. Open the **`routed.brd`** file in the ***solutions*** folder and save it to the ***project2 – allegro*** folder
2. Zoom in around U2 and its surrounding traces.
3. Click the ***Slide icon*** in the left side ***Route toolbar***.

4. The ***Find Filter*** should already be set for ***Vias*** and ***Cline Segs*** only.
5. Set the ***Visibility*** tab to just have the ***Top layer visible***.
6. Click any segment of etch in your display.
   The segment you picked travels with the cursor.



7. Choose a location for the moveable etch and click to define the new location.
8. Experiment by changing the Options for ***Bubble***, ***Shove Vias*** and ***Smooth*** settings and sliding other etch segments.
9. Also try combinations with the ***Gridless*** and ***Allow DRCs*** options checked and unchecked to get a feel for how these choices restrict or change the slide behavior.
10. Right-click and choose "***Done***" from the pop-up menu.
11. Now go to an area where there are lots of traces that are routed together, either horizontally or vertically.
12. Make sure you are in the ***Etch Edit*** application mode.
13. Select on a cline segment. Notice that you are now in the ***Slide*** command. When you have moved the 'etch' to where you wish, click Left-Mouse-Button again to place the 'etch' at the new location. Now, notice you are no longer in the ***Slide*** command.

Moving, Creating, and Deleting Vertices

You can move vertex points or create new vertices to quickly edit existing etch.

1. Choose ***Edit – More - Vertex*** from the top menu.
2. Click a vertex on a cline.
   Notice that the cursor changes as you see in the figure to the right.

   The corner of the cline is now attached to your cursor and can be moved to a new location.
3. Choose a new location and click at that point.
   Now we will add a vertex to an etch segment.
4. Select a point anywhere in the middle of a cline segment.
   This causes a new vertex to be added.
5. Click a location for the new vertex.
6. Now, click on an existing vertex on a cline.
7. Right-click and choose ***Delete Vertex***.
   The vertex is deleted, and the new trace path is shown.
8. Right-click and choose "***Done***" from the pop-up menu.

End of Lab

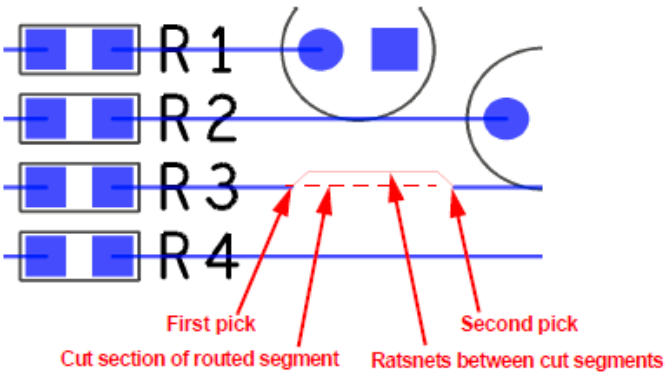
Lab 10-4: Using the Cut Option

Objective: Use the Cut option in conjunction with other editing commands.

You can use the **Cut** feature to define specific sections within line segments. You can use ***Cut*** with the ***Edit - Delete***, ***Edit - Change Objects*** and ***Route - Slide*** commands.

Using Cut with Delete

1. Select the ***Zoom Points icon*** to zoom in to any area of the design so that only two or three components fill the PCB Editor display, and trace thickness is apparent.
2. Choose ***Edit - Delete*** from the top menu.
3. Set the ***Find*** tab so that only ***Cline Segs*** is toggled '***ON***'.
4. Right-click and choose ***Cut*** from the pop-up menu.
5. Click ***two points within a single segment*** where you want the cut to occur. The selected section is highlighted.
6. Right-click and choose "***Done***" from the pop-up menu. The highlighted portion is deleted, leaving a ratsnest in its place. Add the connection back using the skills you have learned for manual routing.

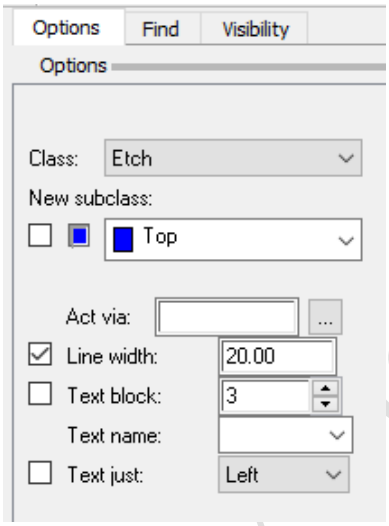


Using Cut with Slide

1. Click the ***Slide icon*** in the toolbar.
2. Set the ***Find*** tab so that only ***Cline Segs*** is toggled '***ON***'.
3. Right-click and choose ***Cut*** from the pop-up menu.
4. Click ***two points within a single segment*** where you want to define a section. As soon as you make the second click you will notice that the section is now moveable.
5. Click on the new location or position for the section of etch you are sliding.
6. Right-click and choose "***Done***" from the pop-up menu.

Using Cut to Change Width

1. Choose ***Edit – Change Objects*** from the top menu.
2. Set ***Find*** tab so that only ***Cline Segs*** is toggled '***ON***'.
3. In the ***Options*** tab set the options to match the figure. Change the value in the ***Line Width*** field to ***20***.



4. Right-click and choose ***Cut*** from the pop-up menu.
5. Click ***two points within a single segment*** where you want to define a section to be changed.
   The new section is highlighted and changes width immediately.
6. Right-click and choose "***Done***" from the pop-up menu.
7. Do ***not*** exit out of the board. We will use it in the following lab.

End of Lab

Lab 10-5: Running Gloss

Objective: Run Line Smoothing to automatically clean up the routes to make the design more manufacturable.

Note The Line Smoothing program may significantly modify the routes in your design. For this reason, you may want to fix critical nets before running it.

Using Gloss

1. Reopen the ***routed.brd*** by typing `reopen` in the Command window.
2. Select ***Route - Gloss Line Parameters*** from the top menu.
   This will open and the ***Line smoothing*** parameters form.
3. In the ***Line Smoothing*** form leave all settings to their defaults, except set the ***Number of Executions*** to ***5***.
4. Select ***Gloss*** from the ***Line Smoothing*** form.
   The Glossing routine is run. You will see the traces being moved, and corners will change from orthogonal to diagonal.
5. After Gloss has finished, you may view the gloss log file by selecting ***File – Viewlog*** from the main menu.
   If you opened the **`gloss.log`** file, close the log file.
6. Select ***File - Save As*** from the top menu.
   A browser form appears.
7. In the ***File Name*** field, enter **`gloss`**.
8. Choose ***Save.***
   The file `gloss.brd` is saved to disk.

End of Lab

Lesson 11: Copper Areas and Positive Planes

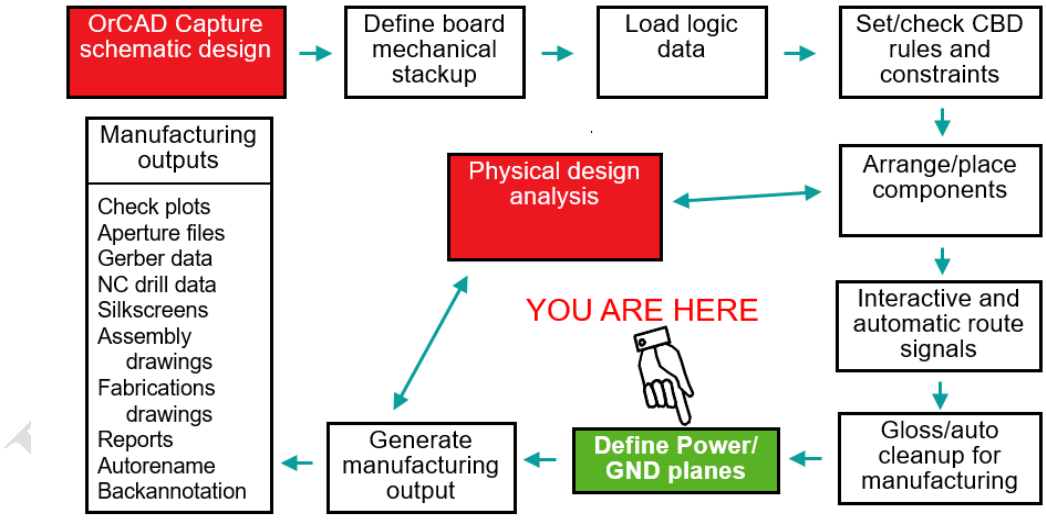
Learning Objectives

In this lesson, you will:

- Learn how to generate positive planes, split planes, and copper pours for artwork
- How to work with the Shape Edit application mode

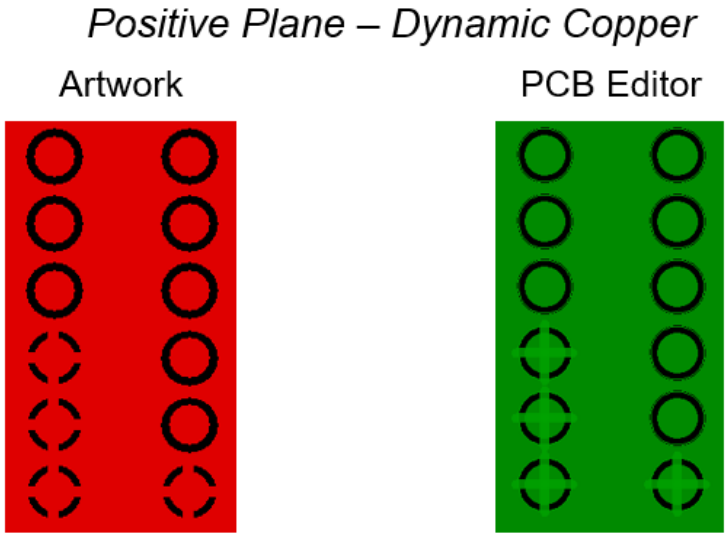
In this section, you will learn about shapes. Shapes are used to represent copper areas, among other things. Shapes can be added to routing layers as well as plane layers. This lesson will focus on using shapes to represent an internal planes and copper areas/pours on routing layers.

Design Layout Process



This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. As indicated in the flow, the define power/gnd planes box will now be discussed.

Copper Area Images

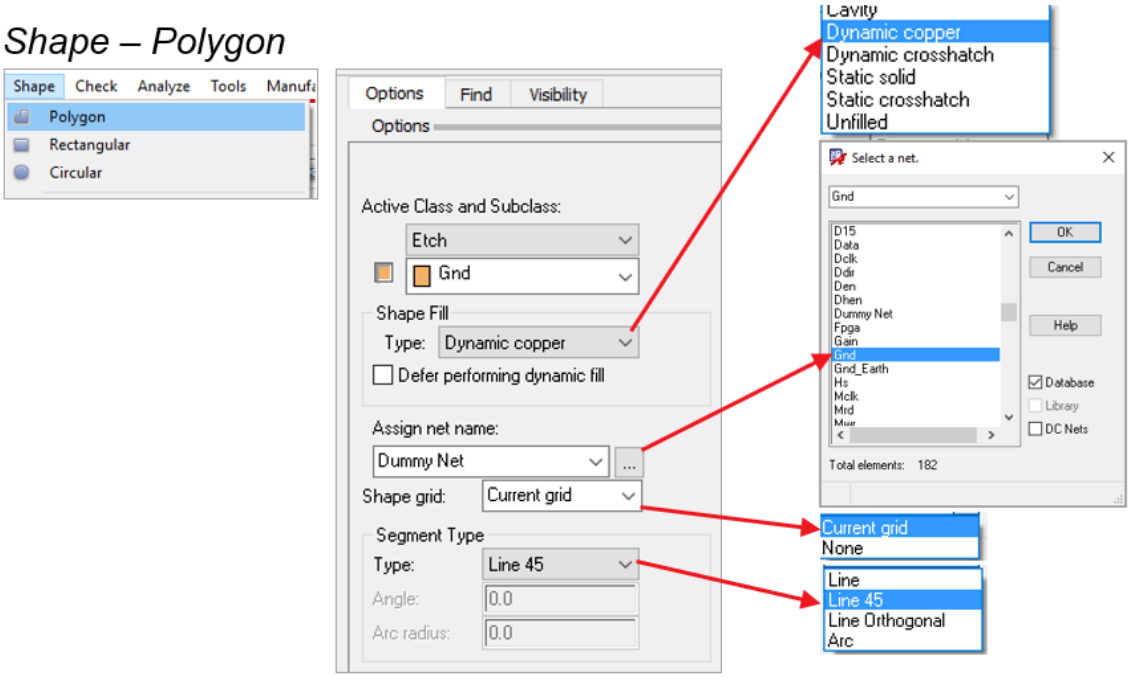


Creating copper areas:

- Advantages to Positive Shapes:
    - The PCB Editor displays the actual positive copper fill, as well as the anti-pad, or plane opening and thermal relief features. No special flash symbols are required
    - As can be seen on the right-hand side of the figure above, the PCB Editor display matches the final artwork
    - Clearances are based on various DRC values in the Constraint Manager rather than the anti-pad and thermal flash information embedded in the padstack

- Viewing of Dynamic vs Static Shapes:
    - A copper shape drawn as Dynamic Copper will display in the workspace as a filled in solid image.
    - A copper shape drawn as Static Solid will display as a see-through dot filled image. This allows the user to distinguish between a dynamic shape and a static solid shape.

Adding a Copper Area



There are two different types of fill styles to choose from:

- **Dynamic** - Once the shape boundary is defined and the fill is set to either dynamic copper or dynamic crosshatch, the fill will automatically void where needed, add thermal straps where needed to create connectivity and run DRC checking to produce artwork quality output.

    - **Example for Dynamic Positive Shape** - This type of shape fill may be used for internal power and ground planes and most copper pours on routing layers. With all but the very largest boards, performance is not an issue.

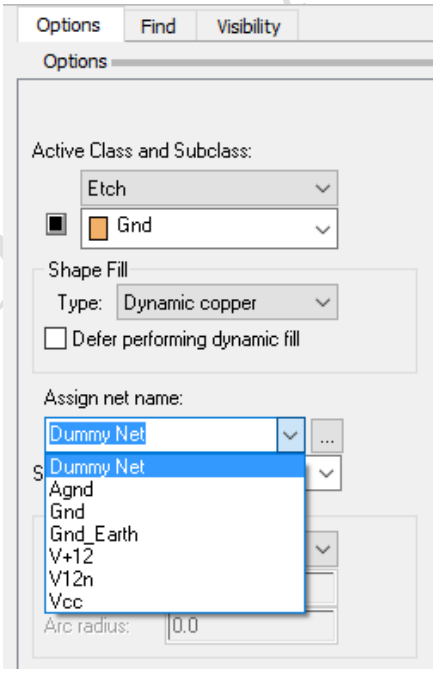
- **Static** - Once the shape boundary is defined and the fill is set to solid or crosshatched, you will need to perform manual voiding as NO automatic voiding takes place with this fill style.

    - **Example for Positive Static Shape** - These shapes may be used for RF circuits or when defining a Chassis ground area around some critical circuitry. (Use when you don't want the shape to be inadvertently modified.)

Add Shape Options:

- **Select a subclass** - Change the setting to the etch layer the shape will be added to.
- **Shape Fill Type:**
  - **Dynamic Copper** - Select if auto-voiding upon each edit to the boundary or elements within the shape boundary is desired
  - **Dynamic Crosshatch** - Acts the same as Dynamic Copper except the fill pattern is crosshatched
  - **Static Solid** - Select if automatic updating of shape during editing elements or boundaries is NOT desired
  - **Static Crosshatch** - Acts the same as Static Solid except the fill pattern is crosshatched
  - **Unfilled** - Defines areas on the board such as constraint regions, route keepins, rooms, etc. These types are not allowed on etch layers

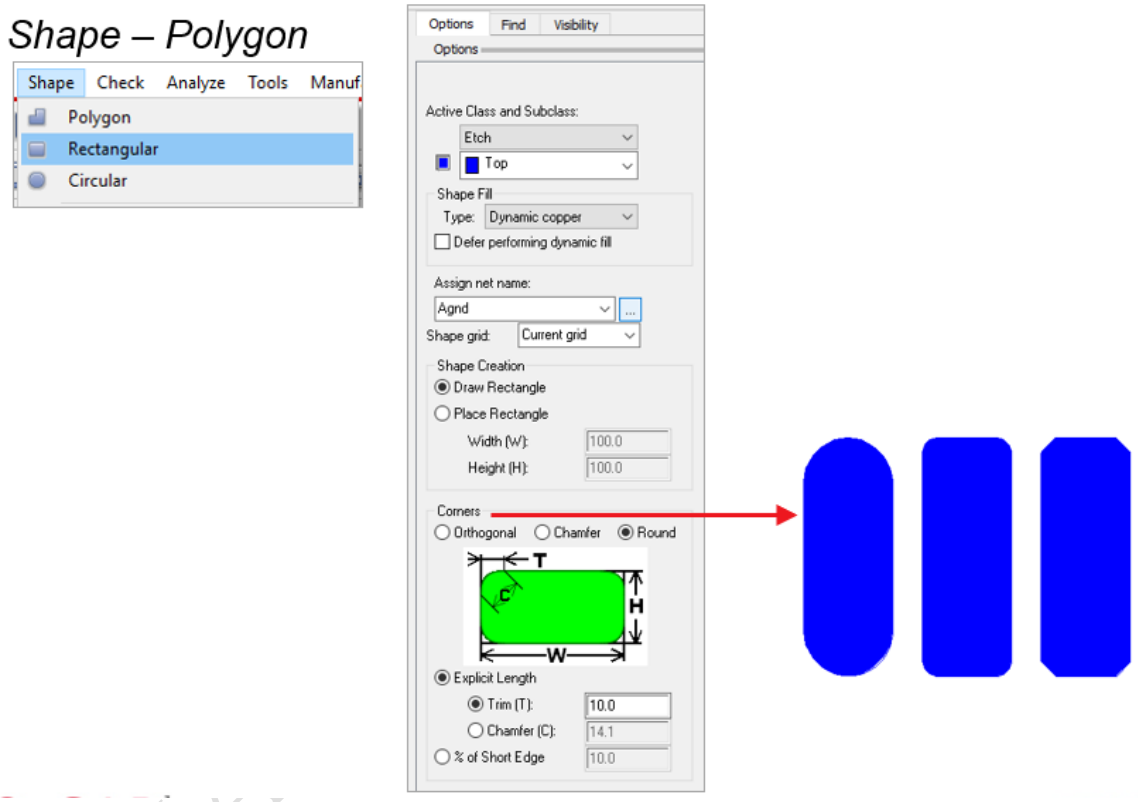
- **Defer Performing Dynamic Fill** - Pushes the dynamic voiding and plowing of a currently added shape off until a later time. Artwork will not be generated if this setting is present.
- **Assign Net Name** - Select net name from the ***Options*** tab browser menu. All nets with a ***VOLTAGE*** property will be available from the ***Assign net name*** pulldown, or the net may be selected from a list button ***(...)*** of all the nets in the design.



- **Shape Grid** - The grid increment used to construct shapes or void outlines.
  - **Current Grid** - Uses the current subclass grid.
  - **None** - Creates shapes off grid in user units.

- **Segment Type** – Line or corner type used when defining a polygon shape boundary.
  - **Line** - Any angle
  - **Line 45** - Miters corners to 45-degree angles
  - **Line Orthogonal** - Corners will be at 90-degree angles
  - **Arc** - Choose to create an arc in the shape boundary
    - **Angle** - Creates an arc from a start point with the specified angle
    - **Arc Radius** - Enters the next arc with the given radius

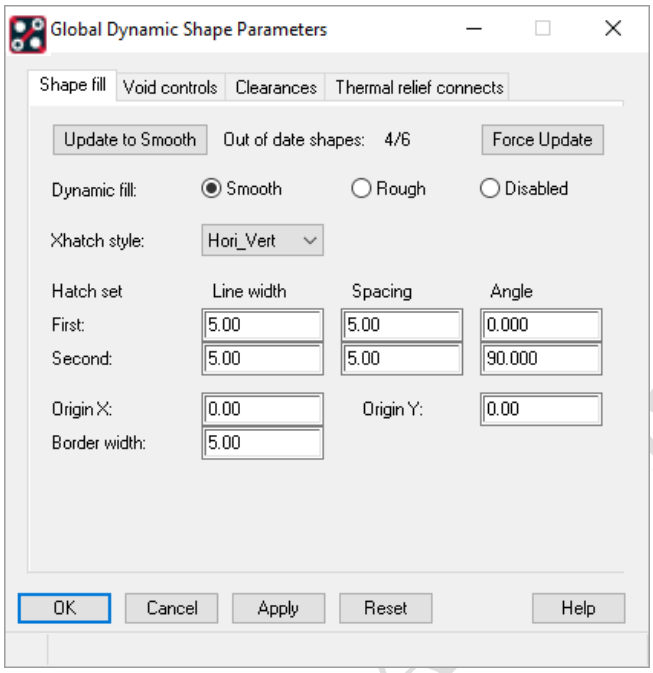
Rectangular Shape Options



Shape - Rectangular - Provides the option to interactively draw the rectangle or "Place Rectangle" of a specific width and height. It is also possible to specify cornering options, such as "Orthogonal", "Chamfered", or Round". You may control the corner length or radius by using either "Explicit Length" or the "Percentage of Short Edge" options.

- **Explicit Length** – Controls the Trim or Chamfer sizes
  - **Trim (T)** – Specifies the distance in from the corner to add either the chamfer or round
  - **Chamfer (C)** – Specifies the length of the mitered segment of the chamfer
- **% of Short Edge** – Specifies the percentage of the short edge of the rectangle that the chamfer or round is to be applied. The specified percentage is the total trim length of both side corners when compared against the width of the short edge of the rectangle.

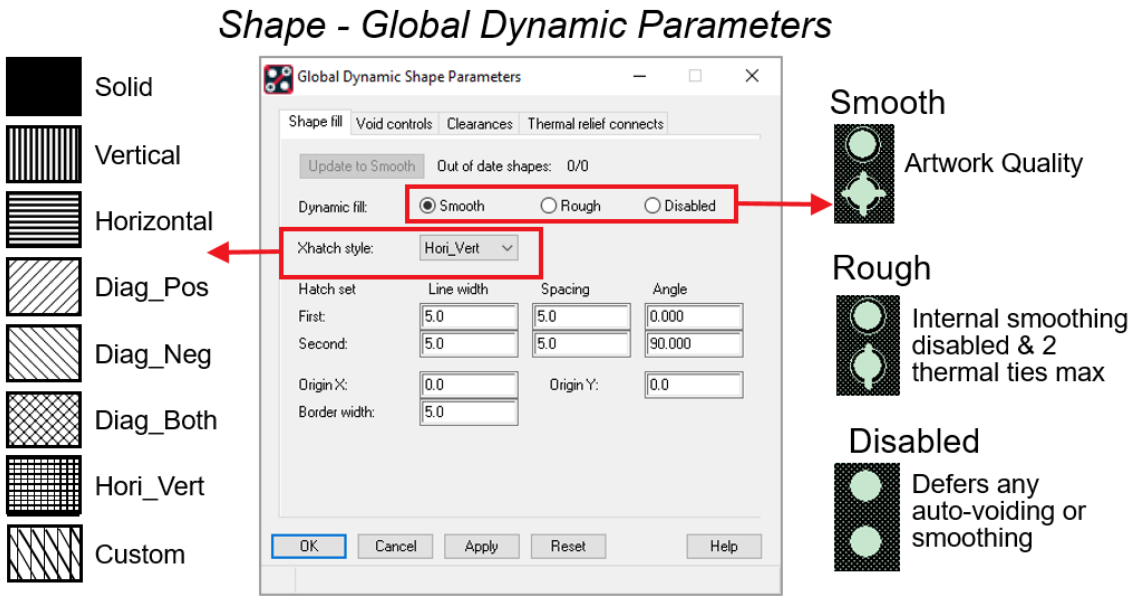
Global Dynamic Parameters



The Global Dynamic Shape Parameters form controls settings for all dynamic shapes. Updates will be made when either the ***Apply*** or ***OK*** buttons are selected. These parameters may be overridden by Dynamic Shape Instance Parameters on a shape-by-shape basis.

- **Global** - Select ***Shape - Global Dynamic Parameters***
- **Shape Instance** - Select the shape then select ***Parameters*** from the ***Right-Mouse-Button*** popup
- **Object Level - (pin, via, cline)** – Select ***Edit – Object Properties*** from the PCB Editor top menu (see CDSDoc for properties available. All dynamic shape properties begin with DYN.)

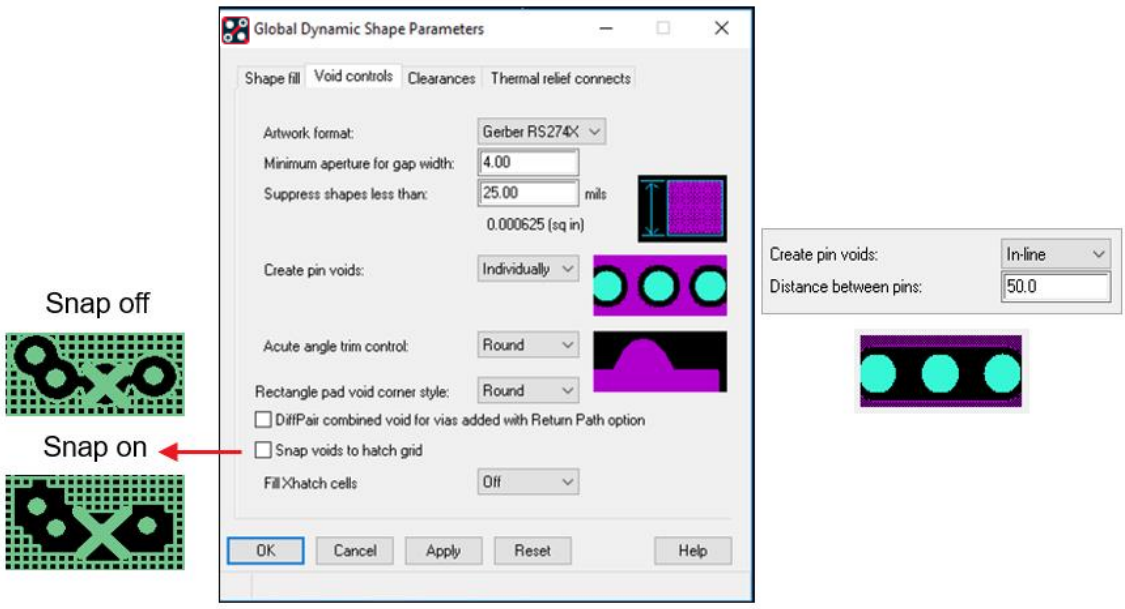
Global Dynamic Parameters - Shape Fill



In the Global Dynamic Parameters form under Shape Fill the settings are:

- **Dynamic Fill:**
  - **Smooth** - Produces artwork quality film. (Shapes with no DRCs).
  - **Rough** - Internal smoothing disabled and maximum of two thermal ties added. Used during editing of very large boards with complex shapes.
  - **Disabled** - Defers any auto-voiding or smoothing. Use during editing of very large boards with many complex shapes or if rough mode is unacceptable.
- **Xhatch Style** – Specifies the crosshatch style to be used on the shape. The hatch set, line width, spacing, and angle settings determine the crosshatch orientation.

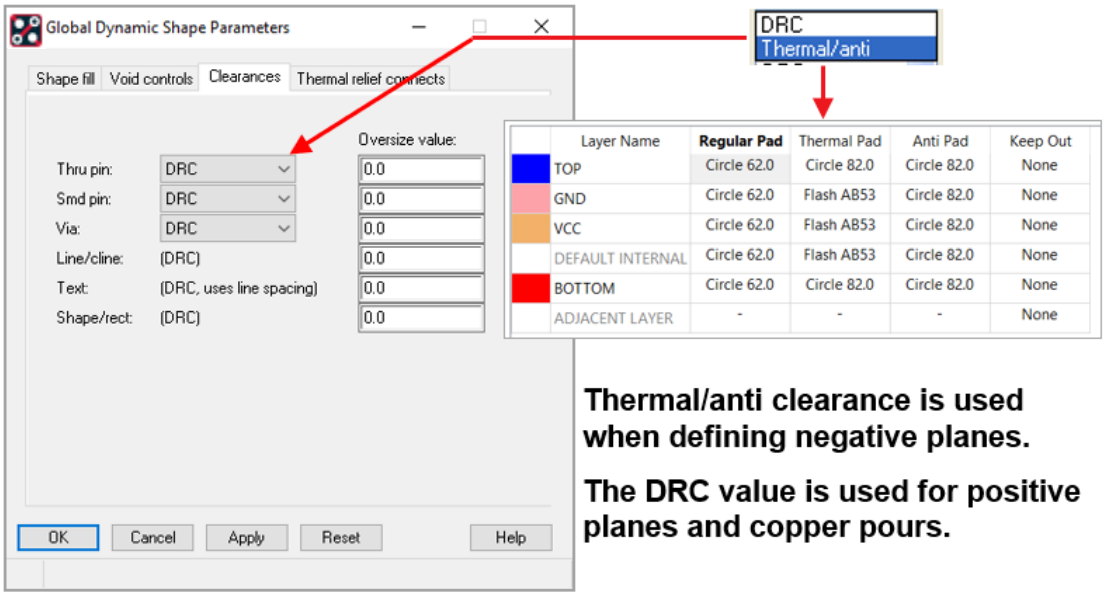
Global Dynamic Parameters - Void Controls



In the Global Dynamic Parameters form under Void Controls the settings are:

- **Artwork Format** - Will optimize the shape fill for vector or raster processing. Default is raster-based RS274X.
- **Minimum aperture for gap width** - Used for vector-based Gerber output only.
- **Suppress shapes less than** - Eliminates unconnected shapes less than the area value specified when voiding shapes.
- **Create pin voids** - Inline or individual options for voiding around pins.
    - **Distance between pins** - Used when inline is selected.
- **Acute angle trim control** - Used only when raster processing is selected. Round, chamfered, and Full Round are the options.
- **Snap voids to hatch grid** - Attaches created voids to the hatch grid rather than following the voided element edge.

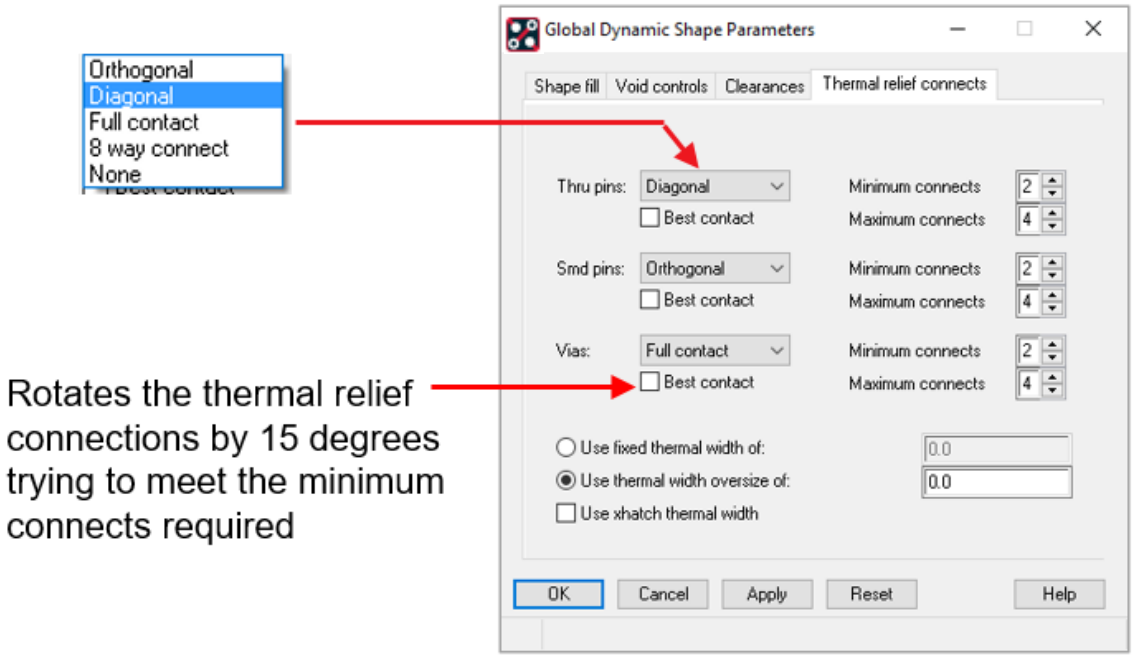
Global Dynamic Parameters – Clearances



The Clearances tab specifies how far the copper shape is recessed from any conductive object within the copper shape in order to prevent shorting.

- **DRC** - Uses the DRC spacing rules setup in the Constraint Manager as the clearance. The DRC clearance is typically used when defining positive planes and copper pours.
- **Thermal/Anti** - Uses clearance size from thermal relief and antipad definition in the padstacks of pins or vias as long as the thermal relief and antipad definition is NOT smaller than the DRC spacing rule for the shape to the conductive object. The Thermal/anti clearance is typically used when defining negative planes.
- **Oversize** - Increases the clearance of the specified DRC or thermal/antipad value.

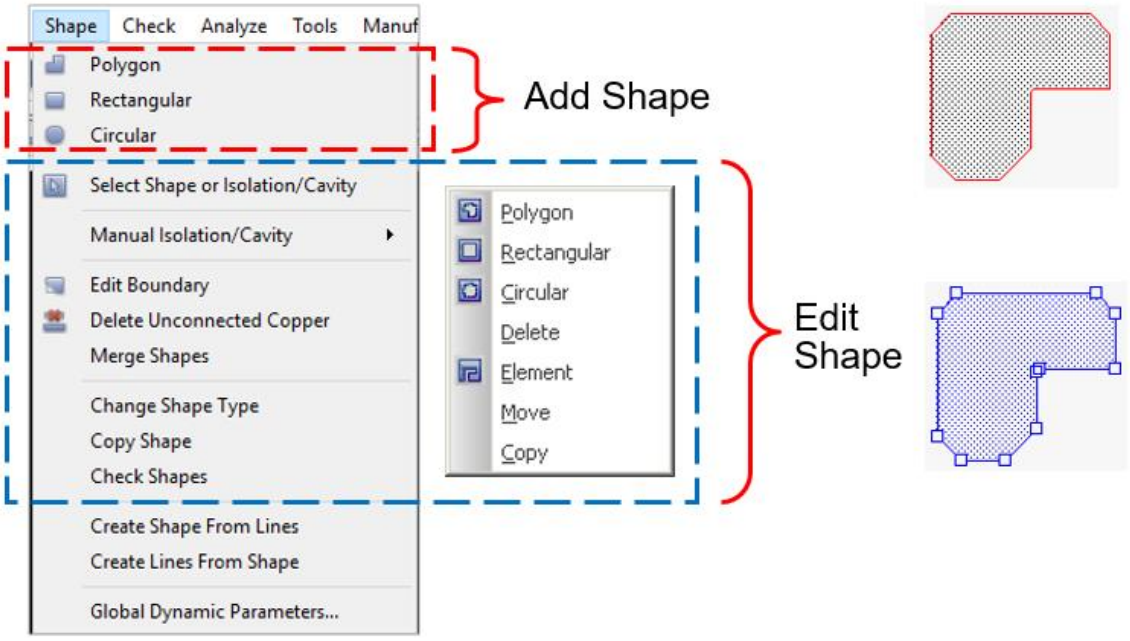
Global Dynamic Parameters - Thermal Relief Connects



Thermal Relief Connects tab specifies how pins and vias with the same net name as the shape should be connected to the shape.

- **Orthogonal** - Connect lines are added straight up and down or left and right to connect to the shape.
- **Diagonal** - Connect lines are added upper left to lower right and lower left to upper right to connect to the shape.
- **Full contact** - A solid connection to the shape is made to the pin/via. No voids. Typically set for vias.
- **8 way connect** - Connect lines added orthogonally and diagonally.
- **None** - Thermal relief connect lines are not added.
- **Best Contact** - Rotates the thermal relief connections by 15 degrees trying to meet the minimum connects required.
- **Use fixed thermal width of** - Overrides the Physical Constraint Set value.
- **Thermal width oversize value** – Increases default thermal connect line width by the specified value.
- **Use xhatch Thermal Width** - Allows cross-hatched dynamic shapes to generate thermal connect line widths based upon the shape's cross hatch width.

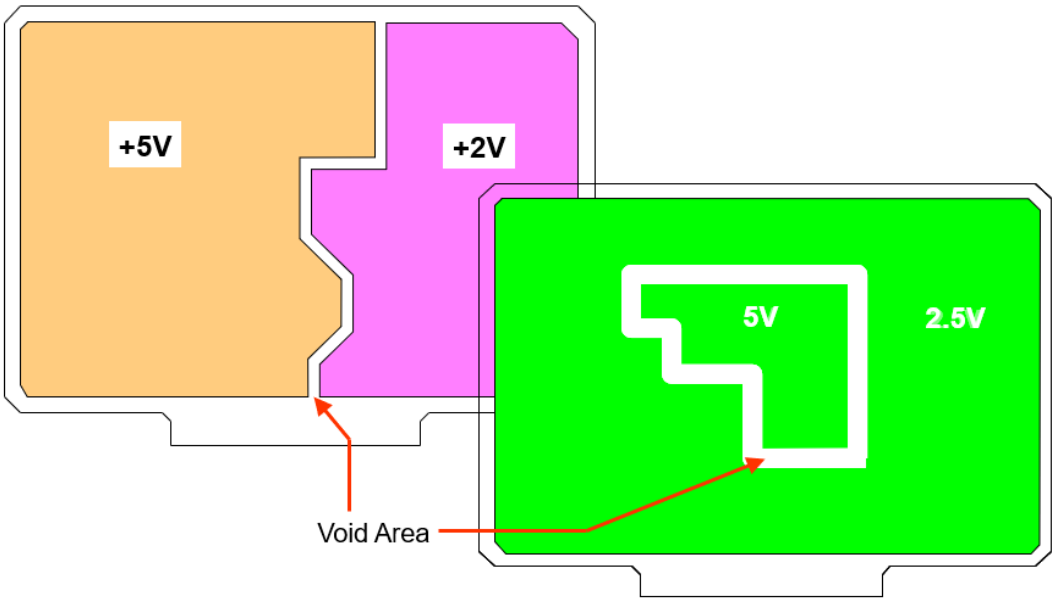
Editing Copper Shapes



This is the ***Shape*** - pull-down menu. The first three commands allow you to add shapes to the board. The remaining commands allow you to edit shapes.

- **Select Shape or Insulation/Cavity** - To interactively edit an existing shape or void, you must first select it. Then use the Right-Mouse-Button popup, or the top pull-down menu to make changes to the assigned net, parameters, etc.
- **Manual Insulation/Cavity** - Use this submenu to interactively add or edit the voids in a shape. You must also use this command to delete voids within shapes.
- **Edit Boundary** - Used to draw a new boundary to an existing shape. After defining a new boundary to a shape, the old boundary is automatically removed.
- **Delete Unconnected Copper** - Used on dynamic shapes to highlight isolated areas of copper for you to delete or connect as you wish.
- **Merge Shapes** - Merge shapes that overlap and are assigned to the same net. The shapes to be merged will take on the properties of the primary shape.
- **Change Shape Type** - Changes shape type from Static Solid to Dynamic Copper or vice versa.
- **Copy Shape** – Works the same as the ***Outline - Z-Copy*** command but is used to copy copper shapes from one layer to another.
- **Check Shapes** - Necessary only when creating vector-based artwork. Checks the shape for narrow areas where the smallest specified aperture cannot fill.
- **Create Shape from Lines** - Converts a group of lines and arcs into a shape. The lines may have come from a DXF file.
- **Create Lines from Shape** - Converts a shape to a group lines and arcs.

Split Planes



Split planes are multiple copper areas that share the same etch layer. To help plan the geometry of each copper area, it is best to color the various nets that will be attached to the planes. Then you will be able to examine how pins are distributed on the layout. This will also guide you while defining where the various splits will occur.

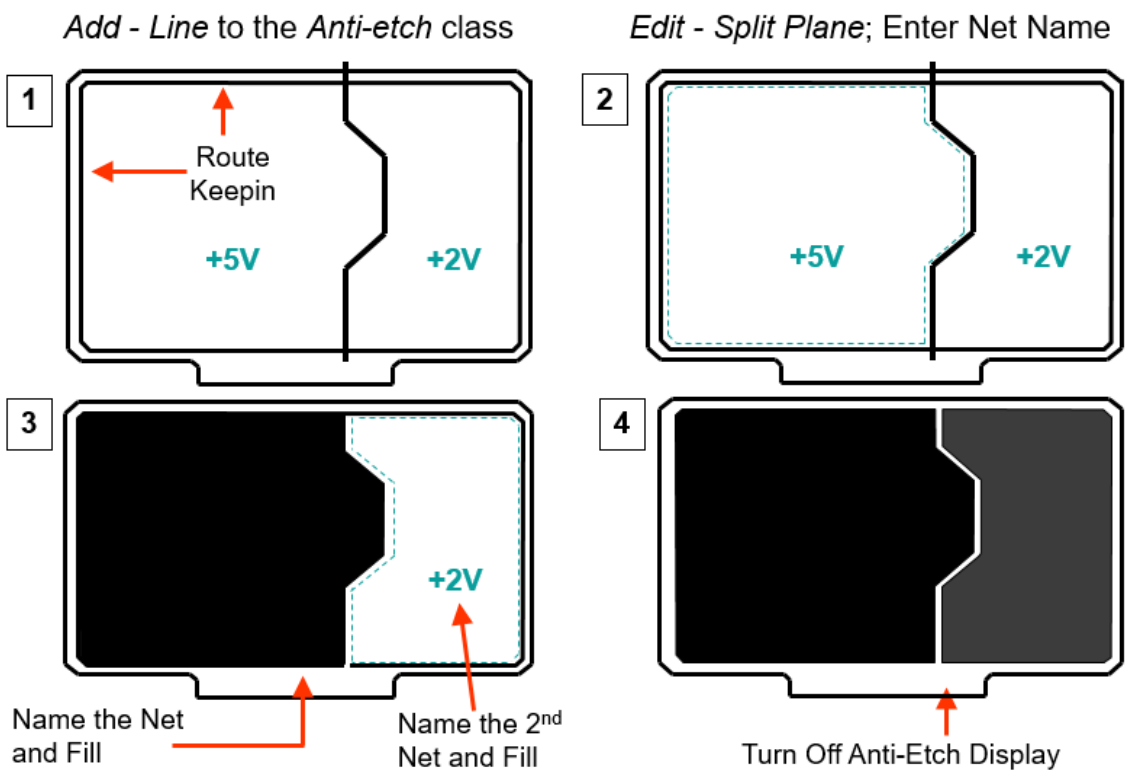
> **Hint**: It is helpful to color the nets before placement and then dissect the design for the different voltage areas that will be needed. That way you have a visual display of approximately where the edges of the shapes will be defined while placing components.

Colors may be assigned to nets using one of the following methods:

- Select the ***Setup - Colors*** command from the top menu. In the Color Dialog form select the **Nets** tab at the top and then set the color of the required nets.
- Hover over a net in the PCB Editor window and click with the ***Right-Mouse-Button*** and select ***Assign Color*** from the pop-up menu and select a color from the resultant color pallet.
- Select the ***Assign Color*** toolbar icon and then select a net and then select a color from the resultant color pallet in the ***Options*** tab.

Note Use one of these methods of displaying pins with different colors to determine where to draw the line(s) that will become the gap or split between the two areas of copper.

Strategy for Split Planes



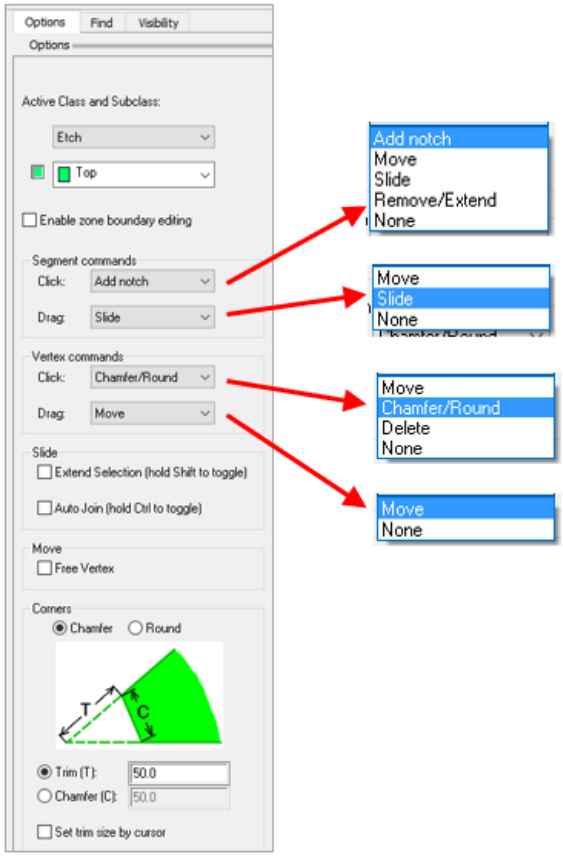
The plane shown in this example has two different shapes. There is no limit to how many different splits you can make in a plane.

You may have noticed a class called ***Anti-Etch***. There is an ***Anti-Etch*** layer for every Etch layer in your design. It is used to define the location of the separation of each of the planes in the split-plane process. You will do a lab exercise later that details this process.

The following are the phases of split plane process.

1. Draw a line on the ***Anti-Etch*** class where you want the gap between the shapes to occur. Make the width of this line the size of the gap required. ***The Anti-Etch line must either be one contiguous line creating a closed polygon or begin and end outside the Route Keepin***.
2. Select ***Edit - Split Plane*** from the top menu.
3. Select the type of shape and the etch layer on which to create the plane in the ***Create Split Plane*** form.
4. Enter the net name for the first and second shape when prompted. The separate shapes are automatically defined and filled.
5. When all of the shapes have been assigned a net and filled, turn ***off*** the ***Anti-Etch*** visibility to see the shape splits more clearly.

Shape Edit Application Mode



The parameters set in the Options tab allow you to customize for the mouse-click, drag and vertex operations without having to access the main toolbar or top-level menu for the following operations:

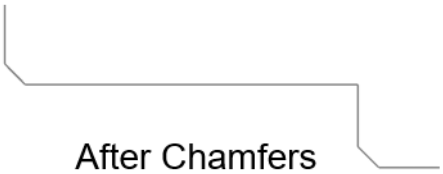
- Add a notch to a shape segment
- Extend or shrink a segment of a shape
- Add chamfered or rounded corners to a shape

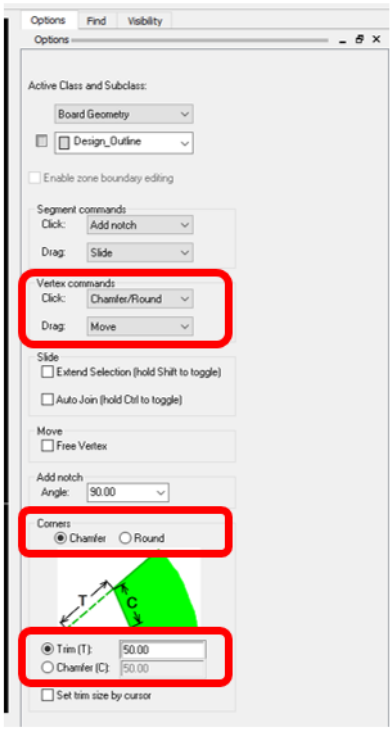
The Shape Edit application mode is a tuned editing environment primarily designed to increase efficiency with shape boundary editing. This object-action environment simplifies the actions of sliding a shape edge, adding a notch to a shape edge, or chamfering/rounding the corners of a shape. You will notice similarities with other application modes but also find new functionality that allows customization of single pick and drag operations.

Chamfers

Shape Application Mode

- Set the Vertex commands to Chamfer/Round
- Set Corners to Chamfer
- Set Trim to length of 45 degree line





Since the board outline is a shape, you will need to use the Shape Application Mode to chamfer or round the corners.

Once you are in the Shape Edit Application Mode, the ***Options*** tab allows you setup the required options for chamfering the corners of your board outline:

- First, you need to set the ***Vertex commands*** for ***Click*** to ***Chamfer/Round***.
- Then, you can set the ***Corner*** to ***Chamfer***.
- Lastly, set the ***Trim*** to the desired length of the 45-degree line (i.e. 50 mil).
- All you need to do now is click on each corner you wish to chamfer.

If you need rounded corners:

- Set the ***Vertex commands*** for ***Click*** to ***Chamfer/Round*** as before.
- Set the ***Corner*** to ***Round***.
- Set the ***Trim*** to the desired ***Radius*** for the rounded corner (i.e. 50 mil).
- All you need to do now is click on each corner you wish to round.

Labs

The following labs will instruct you on how to create shapes.

Lab 11-1: Creating an Internal GND Plane

- Create the GND plane shape

Lab 11-2: Creating a Split Plane for VCC Layer

- Creating plane separations
- Creating the split plane shapes on VCC layer

Lab 11-3: Copper Pour Areas

- Setting Parameters for Rectangular Shapes
- Creating the GND_EARTH copper pour area

Lab 11-4: Shape Edit Application Mode

- Work with the Shape Edit application mode options

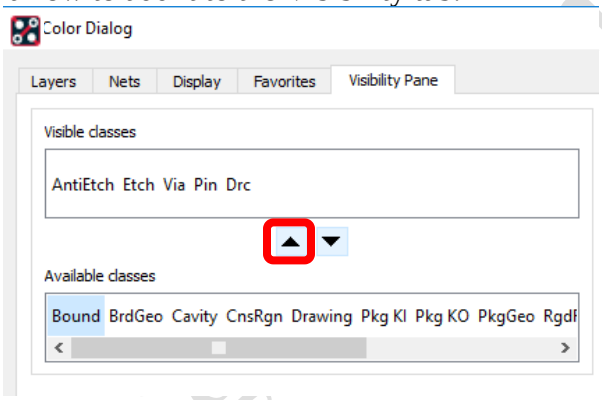
Lab 11-1: Creating an Internal GND Plane

Objective: Create an internal GND plane on an unrouted board.

Adding Classes to the Visibility Pane

To make the split planes and shapes easier to work with, we will add the ***Anti Etch*** and ***Boundary*** Classes to the ***Visibility Pane***.

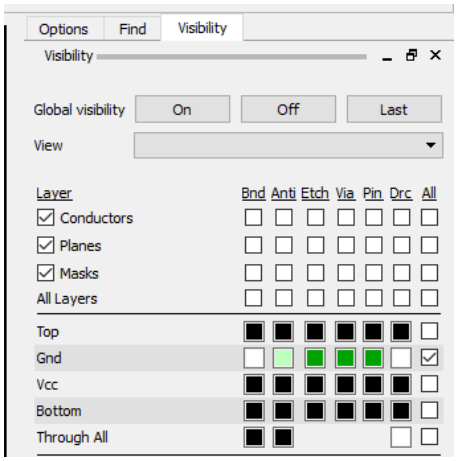
1. Start the PCB Editor if the software is not already running and open the **`planes.brd`** file in the ***solutions*** folder and save it to the ***project2/allegro*** folder.
2. Select ***Setup - Colors*** from the top menu and go to the ***Visibility Pane*** tab.
3. In the ***Visible classes*** section, select ***AntiEtch*** class from the Available classes and then click on the up arrow to add it to the Visibility tab.



4. Do the same for the Bound class.

Making the GND Plane Layer Visible

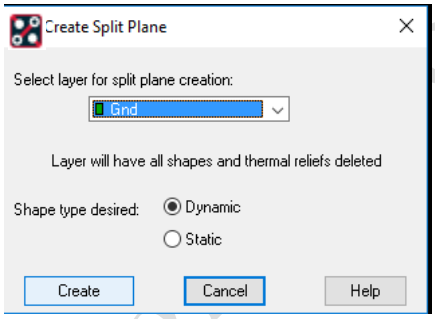
5. Select the **Visibility** tab and set the check box options to match the figure below by checking the ***All*** in the ***GND*** layer:



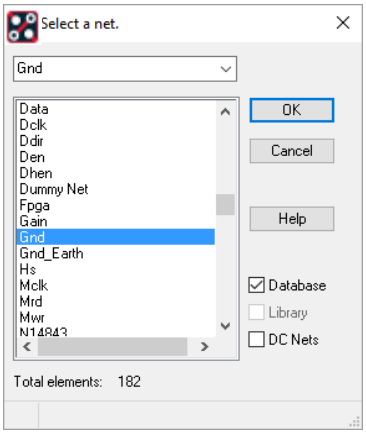
6. Choose ***Setup - Colors*** from the top menu.
7. Select the ***Layer*** tab at the top if it is not already selected.
8. Select and expand the ***Areas*** category and then the ***Route Keepin*** selection.
9. Toggle the ***Through All*** check box to ***ON***.
   The Route Keepin will be used to automatically specify the extents of the GND plane shape.
10. Click ***OK*** to confirm your settings.
    The ***Color Dialog*** form closes.

Creating the GND Plane Shape

1. Select ***Edit - Split Plane*** from the top menu.
2. Using the pulldown in the ***Create Split Plane*** form select the ***GND*** layer.
3. Check to make sure ***Shape Type*** is set to ***Dynamic***.

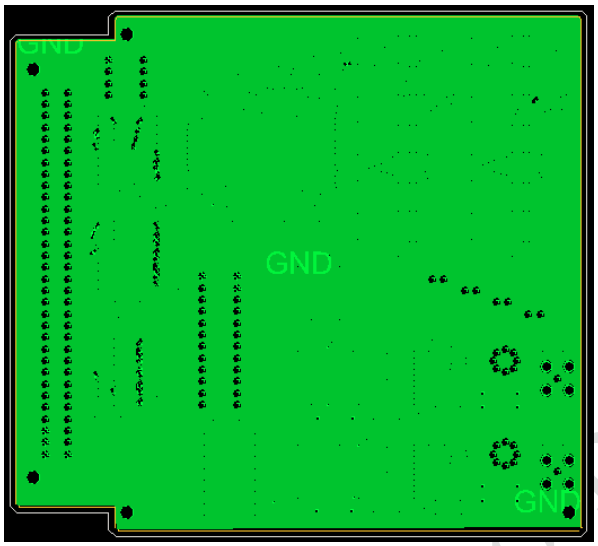


4. Click ***Create***.
5. Select the ***GND*** net from the ***Select a net*** form.



Note Rather than browse for the GND net you could type g* in the filter field at the top of the "*Select a net"* form to filter out all nets except those beginning with the letter g.

6. Click ***OK*** to complete the shape and dismiss the form.



Saving Your Work

1. Choose ***File - Save As*** from the top menu.
2. In the ***File Name*** field of the resultant form, enter `planes_gnd.brd`
3. Choose ***Save***.

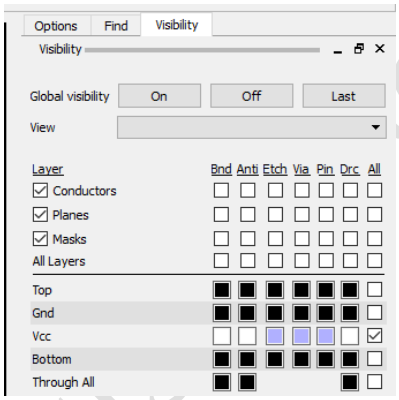
End of Lab

Lab 11-2: Creating a Split Plane for VCC Layer

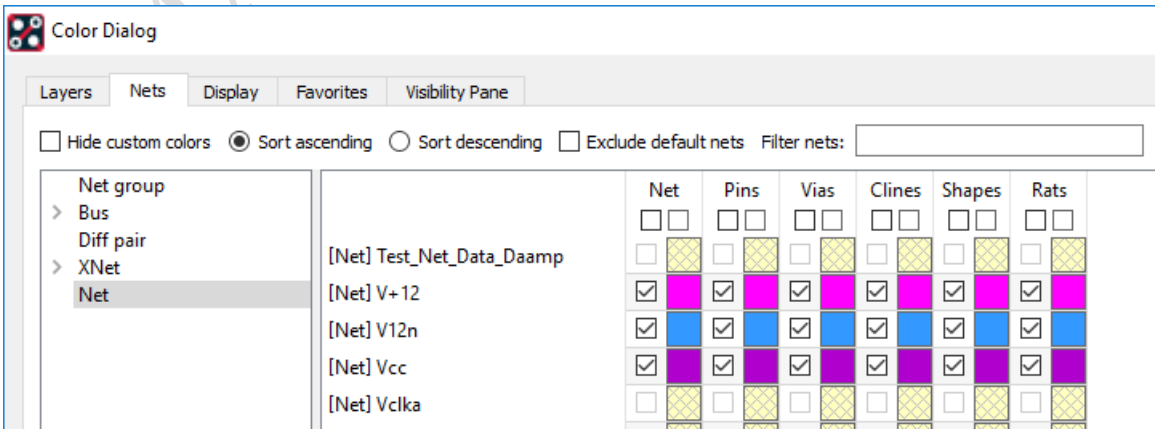
Objective: Create internal split plane for V+12, V12N, and VCC on the VCC layer.

Making the VCC Plane Layer visible

1. Start the PCB Editor if the software is not already running and open the **`planes_gnd.brd`** file.
2. Open the **Visibility** tab and set the check box options to match the figure below by checking the ***All*** in the ***VCC*** layer:



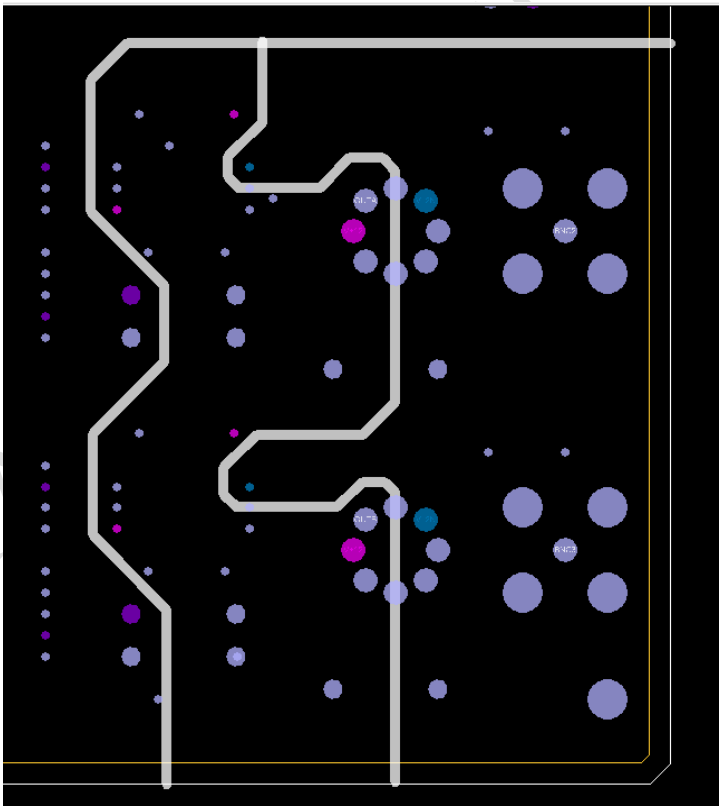
The Power and Ground nets are still colored from when we did our component placement. As a refresher, the power nets are colored as follows:
V+12 = Magenta
V12N = Blue
VCC = Purple
These colors will guide us as we split the VCC layer plane.



Creating Plane Separations

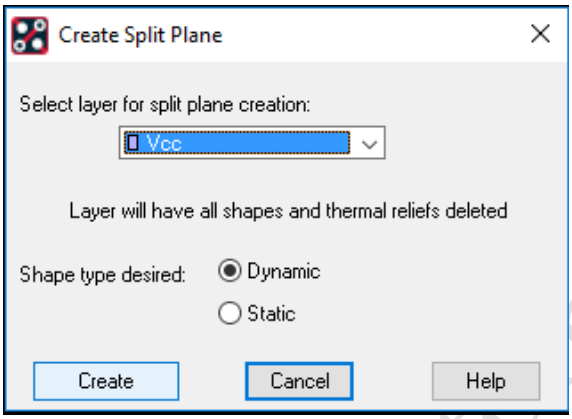
1. In the ***Visibility*** tab of the Control Panel, turn on the VCC layer.
2. Zoom into the lower right corner of the board.
3. Select ***Add - Line*** from the top menu.
4. In the ***Options*** tab set the class to ***Anti Etch*** and the subclass to ***VCC***.
5. Set the ***Line width*** to ***25***.
   This will create a 25 mil clearance between the plane sections.
   We have already added one line that separates V+12 and V12N from VCC (the rest of the board).
   Now, you will add the line that separates V+12 from V12N.
6. Draw the split between V+12 (Magenta) and V12N (Blue) as seen in the figure below making sure that the magenta pads are on one side of the anti-etch line going through the circular ICs and the blue pads are on the other side of the line.

Note If the split plane starts and ends at a board edge, the Anti Etch line MUST cross the Route Keepin area.



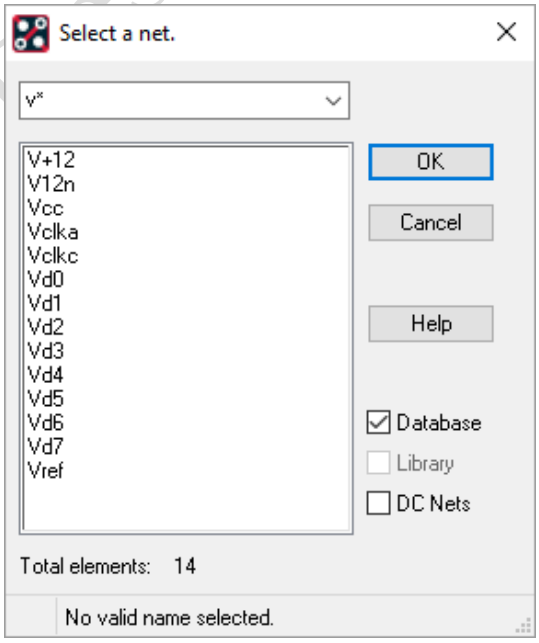
Creating the Split Plane Shapes on VCC Layer

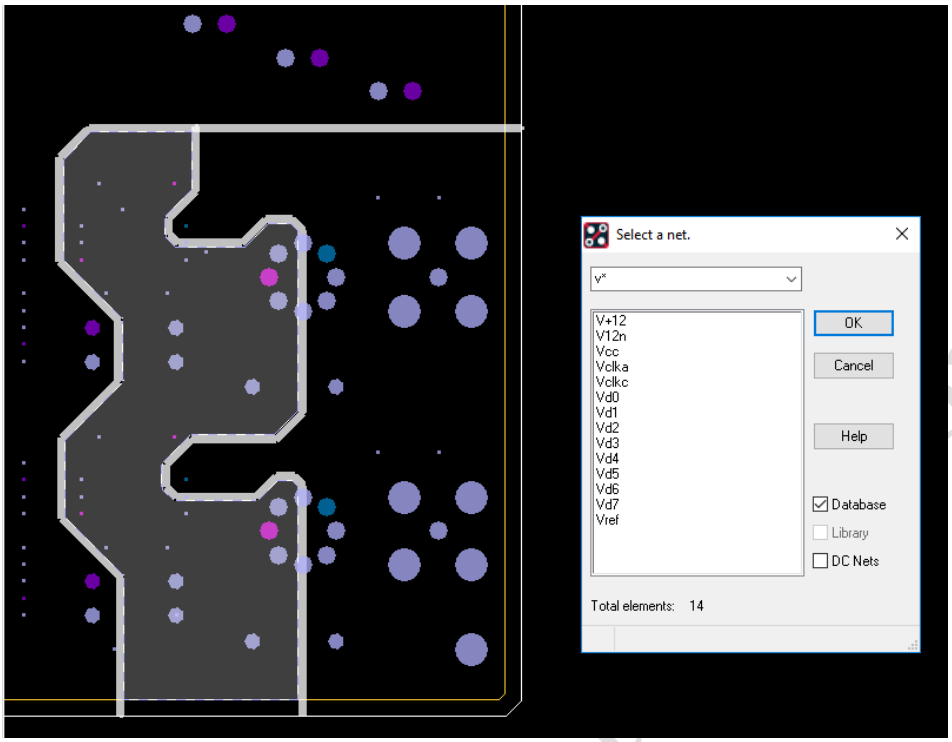
1. Select ***Edit - Split Plane*** from the top menu.
2. Using the pulldown in the ***Create Split Plane*** form select the ***VCC*** layer.
3. Check to make sure ***Shape Type*** is set to ***Dynamic***.

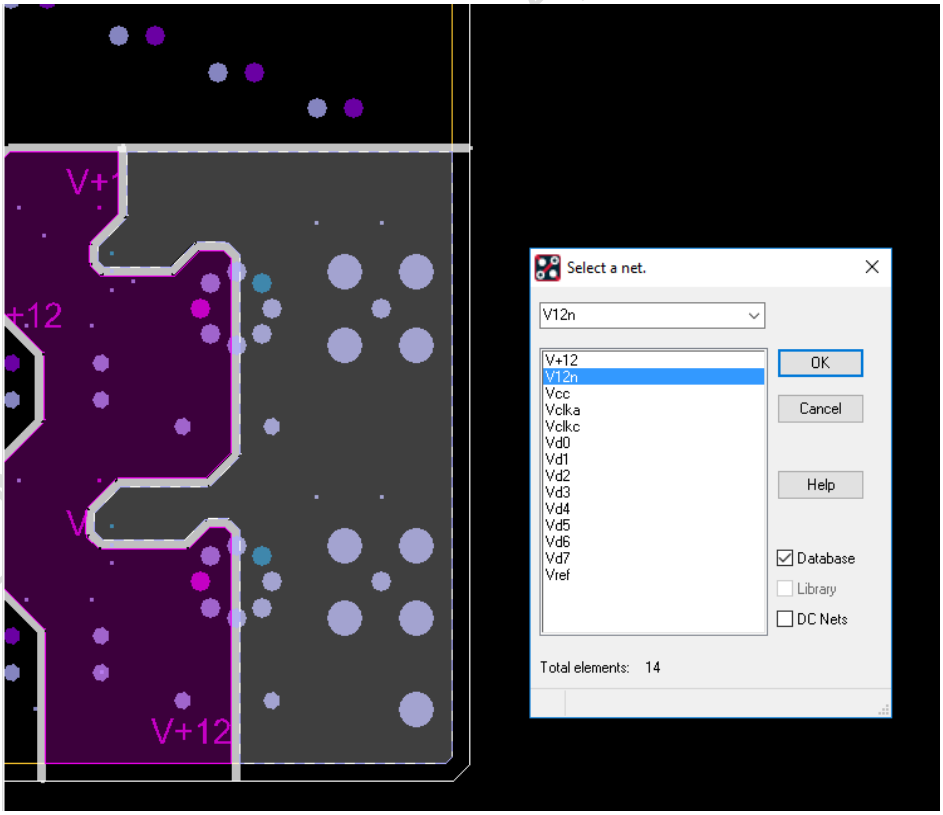


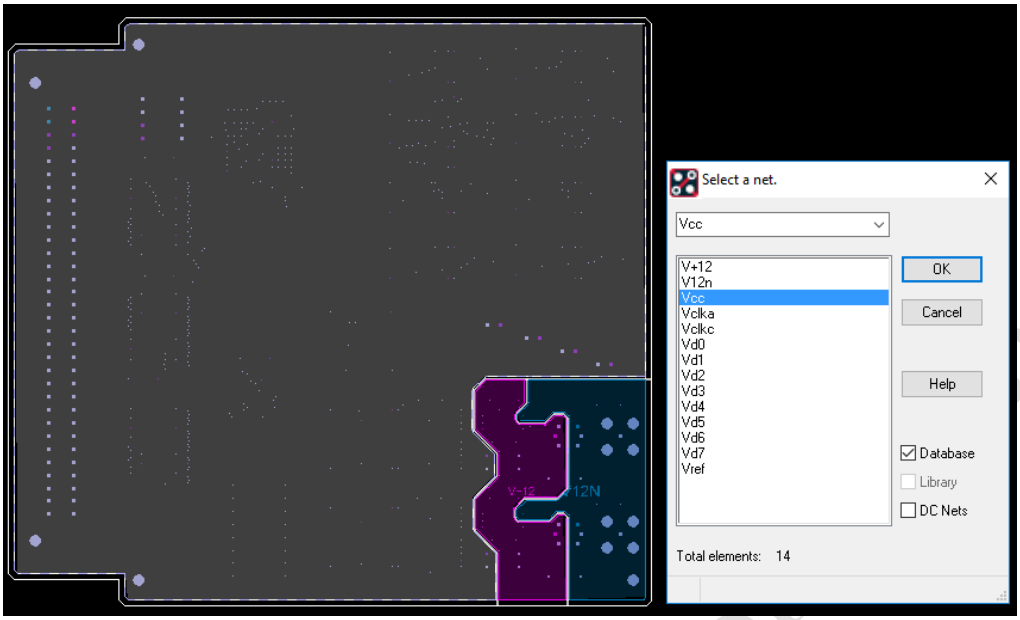
4. Click ***Create***.
5. One at a time when prompted, select the ***V+12, V12N***, and ***VCC*** nets from the ***Select a net*** form and click ***OK*** for each

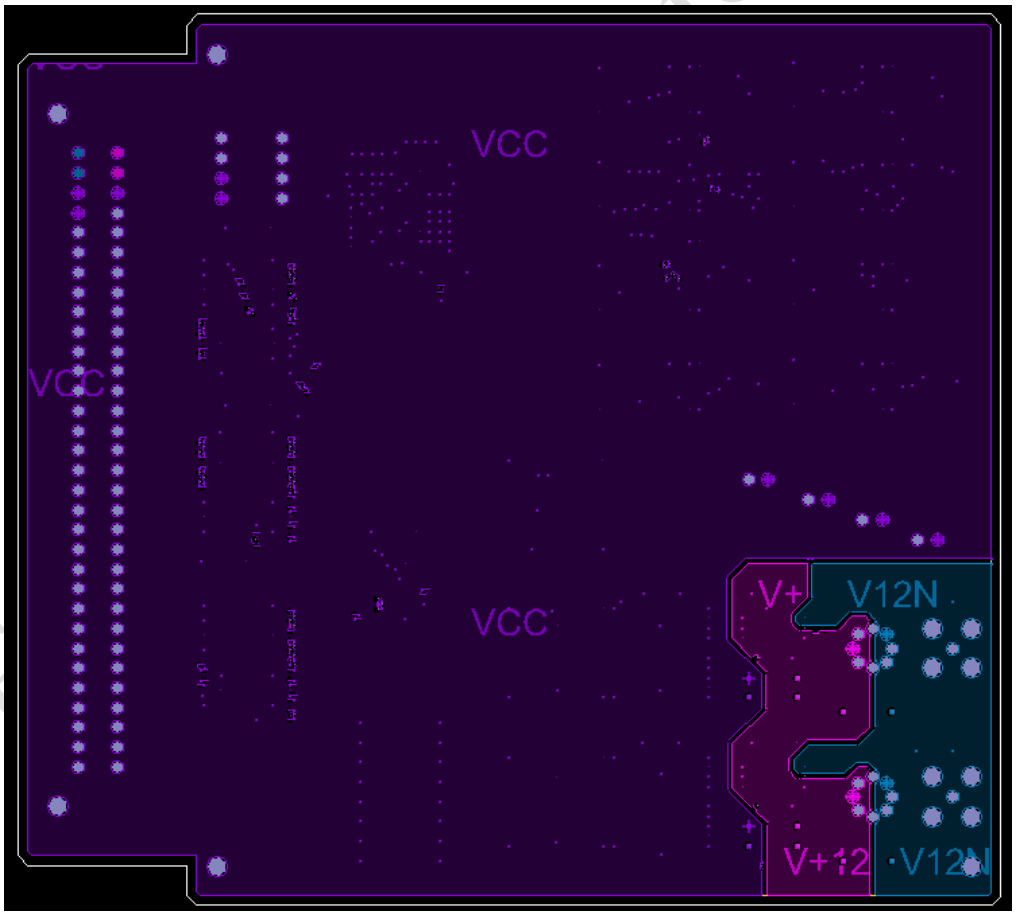
Note As you did with the ground plane, you may type v* to filter out all nets except those beginning with the letter v.




Select a net.
v*
V+12
V12n
Vcc
Vclka
Vclkc
Vd0
Vd1
Vd2
Vd3
Vd4
Vd5
Vd6
Vd7
Vref
OK
Cancel
Help
Database
Library
DC Nets
Total elements: 14


V+12
Select a net.
V12n
V+12
V12n
Vcc
Vclka
Vclkc
Vd0
Vd1
Vd2
Vd3
Vd4
Vd5
Vd6
Vd7
Vref
OK
Cancel
Help
Database
Library
DC Nets
Total elements: 14





6. In the ***Visibility*** tab, you may now turn ***OFF*** the ***Anti Etch*** and ***Boundary*** classes for the ***VCC*** subclass.

Saving Your Work

1. Choose ***File - Save As*** from the top menu.
2. Enter `planes_vcc` in the ***File Name*** field and click ***Save.***
   The file `planes_vcc.brd` has been saved to disk.

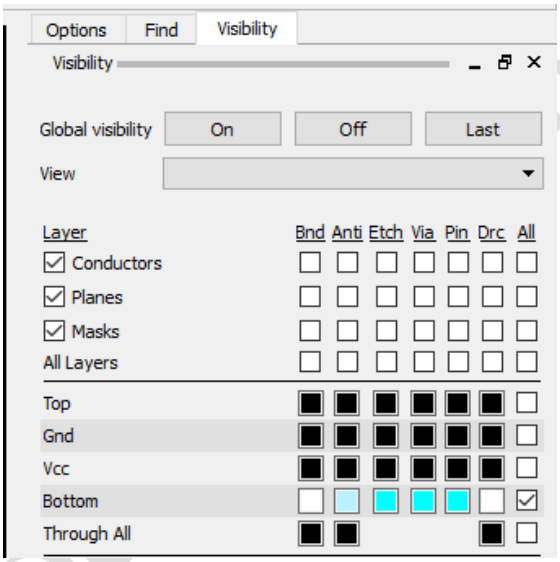
End of Lab

Lab 11-3: Copper Pour Areas

Objective: Create a copper pour area for the GND_EARTH net on the bottom layer.

Making the Bottom Layer visible

1. Start the PCB Editor if the software is not already running and open the `planes_vcc.brd` file.
2. Open the **Visibility** tab and turn on the ***BOTTOM*** layer by checking the ***All*** in the ***BOTTOM*** layer as you see below:

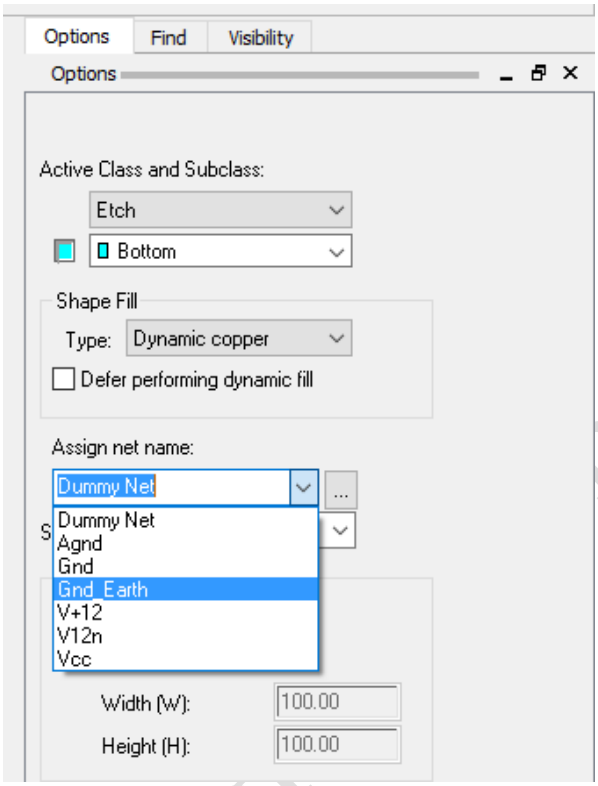


Again, the nets are still colored from before. As a refresher, the ***GND_EARTH*** net is colored **Brown**. This will guide us when we create the ***GND_EARTH*** copper pour.

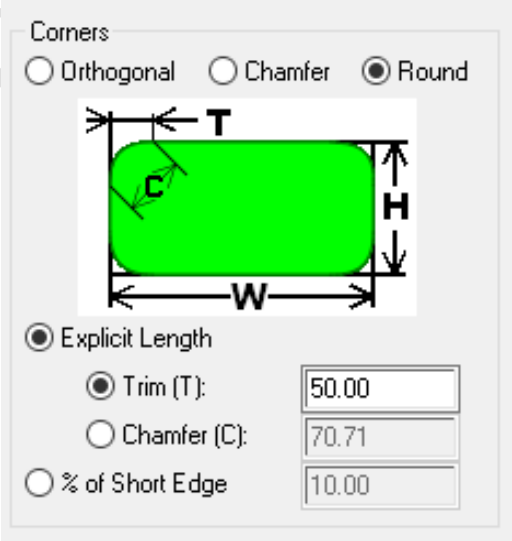
Creating the GND_EARTH Copper Pour Area

1. Zoom into the bottom right hand corner of the board where ***GND_EARTH*** is located.
2. Select ***Shape - Rectangular*** from the top menu.
3. In the ***Options*** tab, select ***Etch*** for the class and ***Bottom*** for the subclass.
4. Set the ***Shape Fill type*** to ***Dynamic copper***.

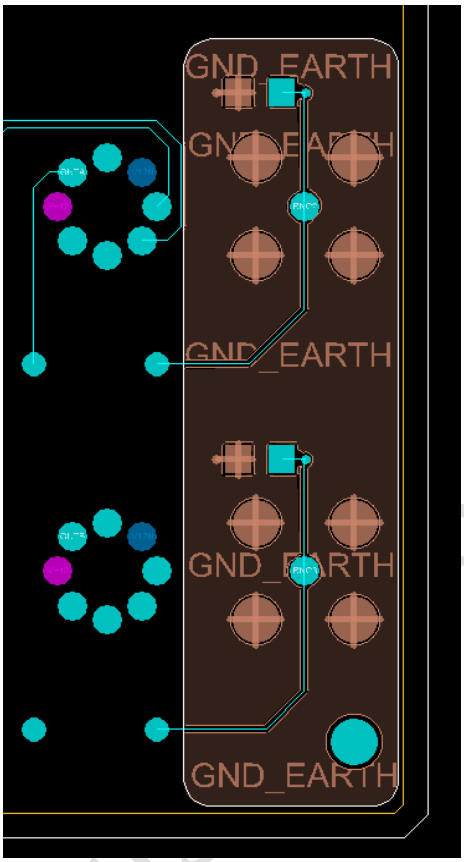
5. Since all power and ground nets in this design have the VOLTAGE property attached, you may select the ***GND_EARTH*** net by simply using the ***Assign Net*** pulldown as shown below.



6. Select ***Draw Rectangle*** and set the corners to ***Round*** and the Trim to ***50***.



7. Draw the GND_EARTH rectangular shape in the lower right corner of the board similarly to what you see in the figure below by clicking at the upper left corner, then the lower right corner.



8. Click the Right-Mouse-Button and click **"Done"** in the popup menu.

Saving Your Work

1. Choose ***File - Save As*** from the top menu.
2. Enter `shapes_all` in the ***File Name*** field and click ***Save.***
3. The file `shapes_all.brd` has been saved to disk.

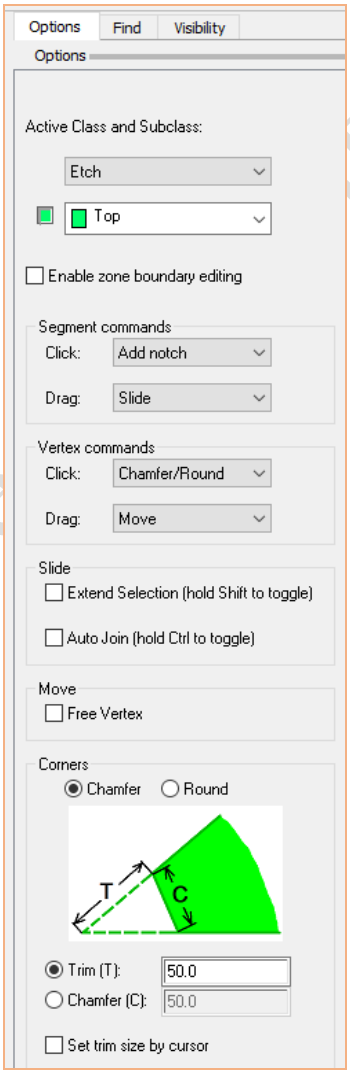
End of Lab

Lab 11-4: Shape Edit Application Mode

Objective: Work with the various functions to modify shapes with the Shape Edit application mode.

Shape Edit Option Tab Default Parameter Settings

The parameters that you set in the Options tab allow you to customize the mouse-click, drag, and vertex operations without having to access the main toolbar or top-level menus for basic shape boundary editing.



Hovering over a shape segment produces a popup menu listing shape commands you can apply to the selected element.

Slide Segment

1. Open the `shape_edit.brd` file in the ***project2 - allegro*** directory.
2. Select ***Setup - Application Mode – Shape Edit*** from the top menu.
3. Zoom in around the ***Slide Segment*** rectangular and circular shapes.
4. Hover over the bottom edge of the rectangular shape and from the ***Right-Mouse-Button*** select ***Slide Segment*** and drag your cursor down to increase the size, or up to decrease the size.
5. Now, hover over the edge of the circular shape and using the same ***Right-Mouse-Button – Slide Segment*** command drag your cursor outward or inward to increase or decrease the diameter of the circle.

Adding an Inward or Outward Notch

1. Use the ***Display – Zoom – Fit*** command to display the complete size of the board again.
2. Zoom in around the ***Add Notch*** shape and hover over the longer segment of the shape's bottom edge.
3. From the ***Right-Mouse-Button*** select ***Add notch***.
4. Click on two points on this edge to define the picks and drag your cursor inside the shape and you will define a notch.
5. Now, click on two new points on the same edge and drag your cursor outward to add a new material to the shape.
   The ***Add Notch*** shape may now look something like this:

Move Vertex

1. Use the ***Display – Zoom – Fit*** command to display the complete size of the board again.
2. Zoom in around large shape in the ***Move Vertex*** section and hover over the inside corner on the right end.
3. Hover over the internal corner on the right end and from the ***Right-Mouse-Button*** select ***Move vertex***.
4. Drag your cursor to the left and down to add more material to the shape or right and up to remove material from the shape.
   The ***Move Vertex*** shape may now look like this:

Chamfer Corners

1. Using the same shape, hover over any inside or outside corner and from the ***Right-Mouse-Button*** select ***Trim corner***.
2. Single click on the corner and this corner will be chamfered to the trim size set in the ***Options*** tab.
3. To chamfer all corners of the shape, hover over the shape and from the ***Right-Mouse-Button*** select ***Trim corners***.
   All inside and outside corners will now be chamfered.

Note To convert a corner back to orthogonal, in the ***Segments commands*** section of the ***Options*** tab change the "***Clic***k" option to ***Remove/Extend*** and then click the chamfered segment.

Alternatively, you can hover over the chamfered edge and from the ***Right-Mouse-Button*** select ***Remove/Extend segment(s)***.

Round Corners

1. Use the ***Display – Zoom – Fit*** command to display the complete size of the board again.
2. Zoom in around the ***Round All Corners*** shape.
3. In the ***Segments commands*** section of the ***Options*** tab change the "***Corners***" option to ***Round***.
4. Hover over any inside or outside corner and from the ***Right-Mouse-Button*** select ***Trim corner***.
5. Single click on the corner and this corner will be rounded to the trim size set in the ***Options*** tab.
6. To round all corners of the shape, hover over the shape and from the ***Right-Mouse-Button*** select ***Trim corners***.
   All inside and outside corners will now be rounded.

Note  To convert a corner back to orthogonal, in the ***Segments commands*** section of the ***Options*** tab change the "***Clic***k" option to ***Remove/Extend*** and then click the rounded segment.

Auto-Join Option

1. Use the ***Display – Zoom – Fit*** command to display the complete size of the board again.
2. Zoom in around the ***Join Segments*** shape.
3. In the ***Options*** tab enable the "***Auto Join***" option.
4. Hover over the farthest right edge and from the ***Right-Mouse-Button*** select ***Slide segment***.
5. Drag your cursor to the left until you are to the left of the innermost step segment.
   All of the step segments are now all on the same plane.

End of Lab

Lesson 12: Preparing for Post Processing

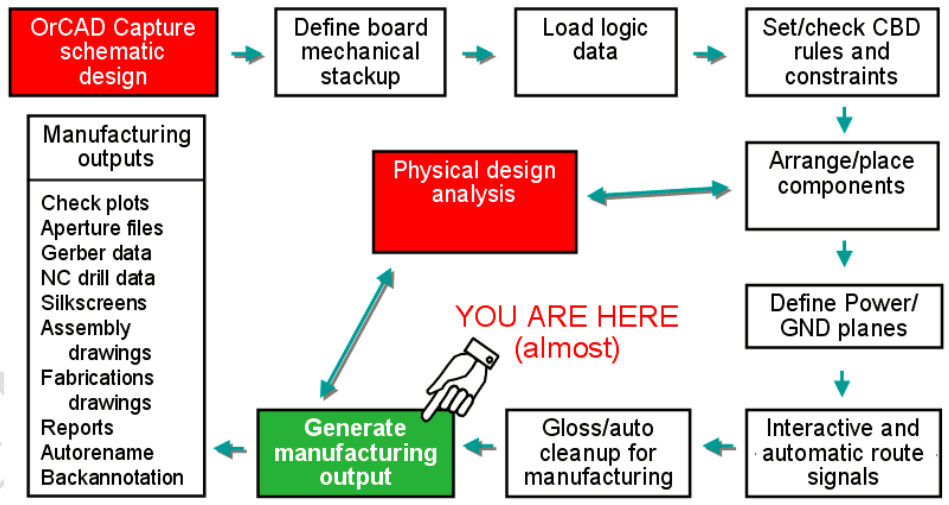
Learning Objectives

In this lesson, you will:

- Check design for DRCs and unconnected pins
- Ready shapes for final artwork
- Rename reference designators on the board design
- Back-annotate changes made in the PCB Editor to DE CIS

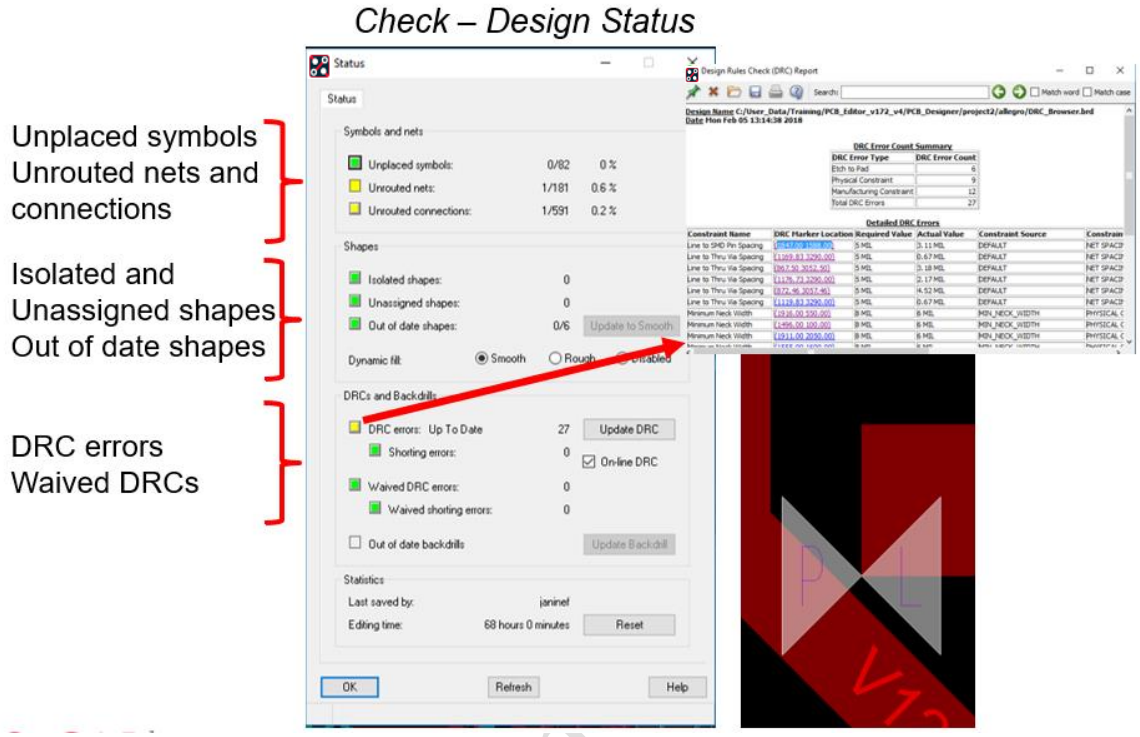
In this section, you will learn about preparing your design for post processing. This will include checking the design for unconnected nets and DRCs, renaming of reference designators, and back-annotating your design changes to your schematic.

Design Layout Process



This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. The items about to be discussed are sometimes included in the manufacturing output area.

Checking for DRCs and Unconnected Pins



Once you have finished adding all of your planes and copper pours, the design should be completely connected. It would also be nice to think that, at this point there are no DRC errors. To make sure our design is complete and error free, we will use the ***Check - Design Status*** command.

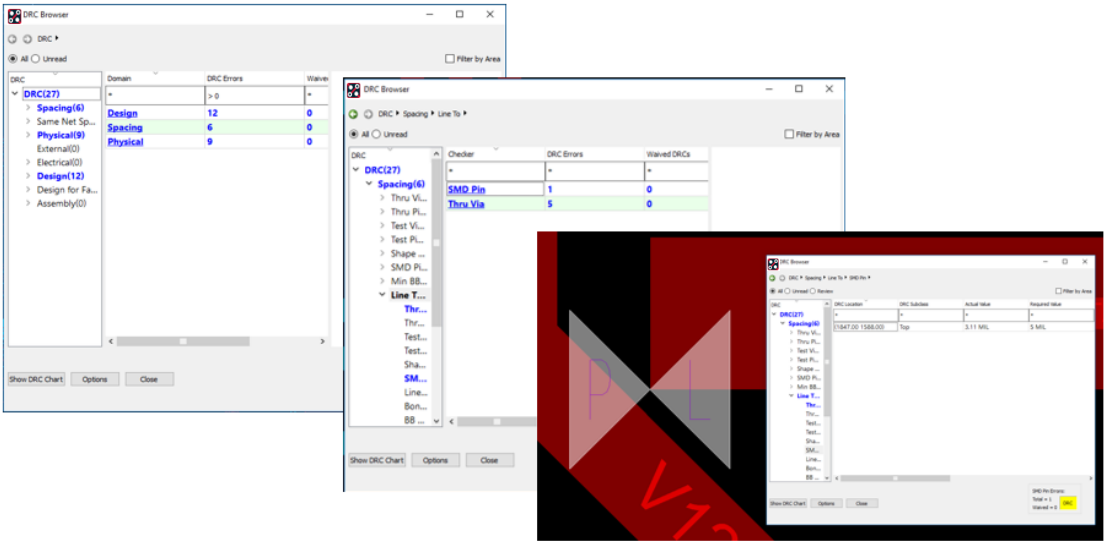
Select ***Check - Design Status*** from the top menu:

- ***Symbol and net*** – This section shows the number of unplaced components and unrouted nets and connections in the design. You can click on the colored boxes to get reports on which components are not placed and which nets and connections are not routed.
- ***Shapes*** – This section shows the number of isolated shapes (islands), unassigned shapes and out of date shapes (shapes not set to Smooth). You can click on the colored boxes to get reports on each of these categories.
- ***DRCs and Backdrills*** – This section shows the number of DRCs present and alerts you if any of those DRCs are causing shorts. You can click on the colored boxes to get reports and locations of DRCs. It shows whether DRC checking is **Up to Date** of **Out of Date**. It also lists any DRCs that have been Waived and if any of those waived DRCs are creating shorts.

Checking for DRCs Using the DRC Browser

Another place to check for DRC errors is the DRC Browser located under ***Tools – DRC Browser*** from the top menu. Here you can list all of the different types of DRCs, click on a DRC type to get a report and even click on a location link in the report that will take you to a DRC on the board.

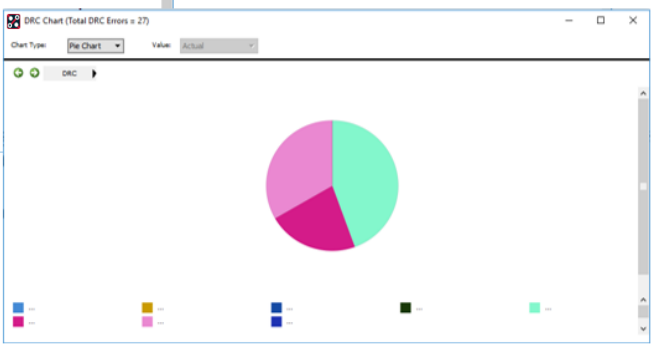
Tools – DRC Browser



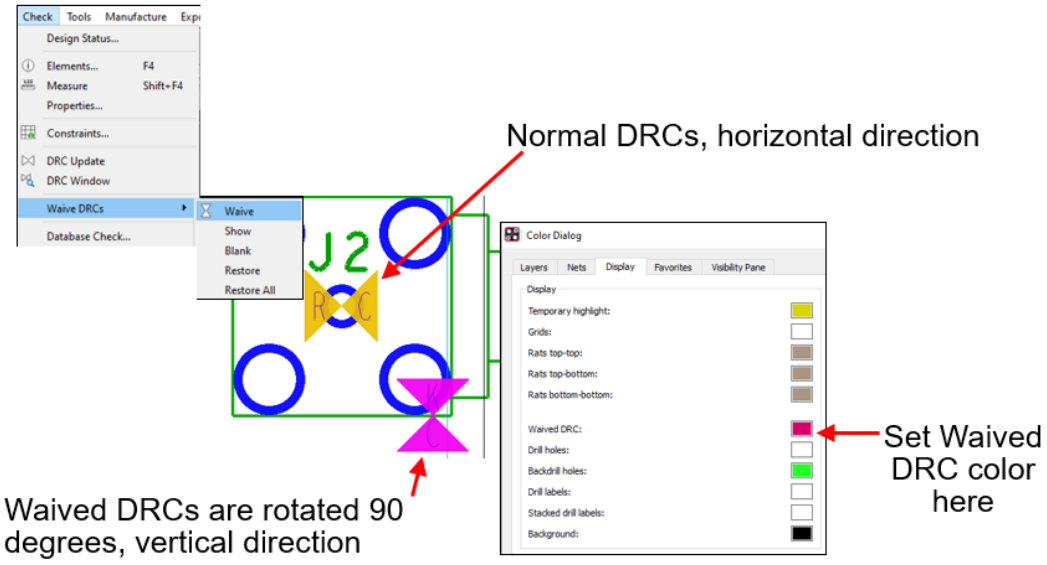
The DRC Browser will also allow you to create Bar and Pie chart reports.

Bar Chart

Pie Chart



Waiving DRCs



Some designs may have design rule error markers that are actually acceptable. You can indicate that such markers are allowable in the design by waiving the DRC with the ***Check - Waive DRCs - Waive*** command.

When you waive a DRC error, the marker is rotated 90 degrees. Once you have waived DRCs, you can show or hide the DRCs as well as restore to their pre-waived state. The color of the Waived DRCs can be controlled in the ***Display*** tab of the ***Color*** dialog. There is also a report that will list all the DRC errors that have been waived.

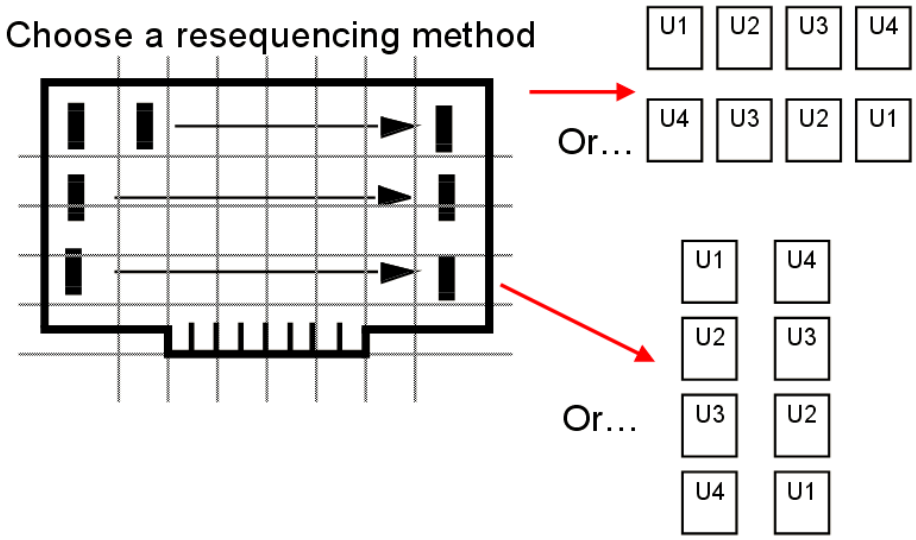
Readying Shapes for Final Artwork

Our design contains a Ground plane, a split Power plane and copper pour areas for AGND and GND_EARTH. All of these shapes were defined as positive dynamic shapes. We now need to make sure that all shapes in the design are updated to smooth to ensure all voids and thermal relief ties have been properly created. This is also necessary for successful artwork generation.

You can use the ***Shape fill*** tab of the ***Global Dynamic Parameters*** form to set all shapes to smooth. This will ensure that your shapes are all artwork quality with all required voids and thermal reliefs.

Then, in the ***Void controls*** tab of the ***Global Dynamic Parameters*** form, you can check that the ***Artwork format*** is set to match your preferred Gerber output format (the default is **RS274X**).

Renaming Reference Designators



It is common to rename (re-sequence) the reference designators on a board and backannotate to the schematic at the end of the layout phase. The process results in a physical layout that is easier to test, debug, rework, assemble, and maintain in the field.

Caution

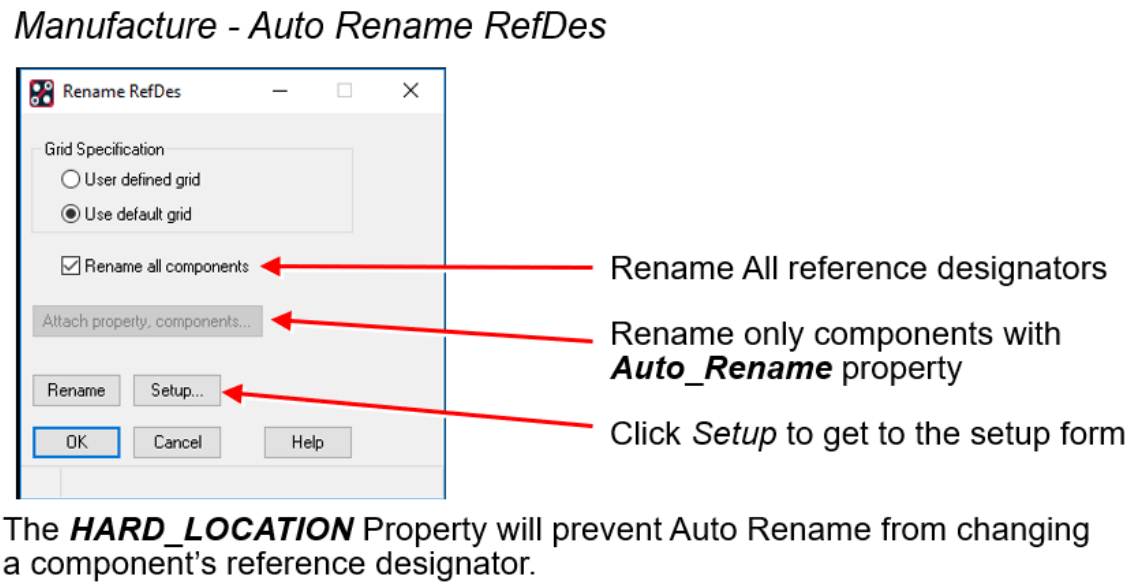
Before attempting to rename components in the PCB Editor, it is advisable to contact the engineer you are working with to get a copy of his most recent schematic. If the engineer has made changes and you change the reference designator names, the two will be out of sync. Therefore, before changing reference designators or swapping functions or pins, be sure to forward annotate the schematic to be certain you are working with the most current information.

The automatic renaming process in PCB Editor lets you rename every component on a design in a single operation. You can also elect to rename individual components by attaching the AUTO_RENAME property to them or rename components on one side of the board only.

Renaming is controlled by placement grid line locations (user-defined or default selection) or by sequential renaming within grid blocks. With grid-based renaming, you can designate the direction (horizontal or vertical) and order (left-right, right-left, upwards-downwards) of the renaming process.

To access automatic renaming in PCB Editor, select ***Logic - Auto Rename RefDes*** from the top menu.

Rename Reference Designators Main Form



The ***HARD_LOCATION*** Property will prevent Auto Rename from changing a component's reference designator.

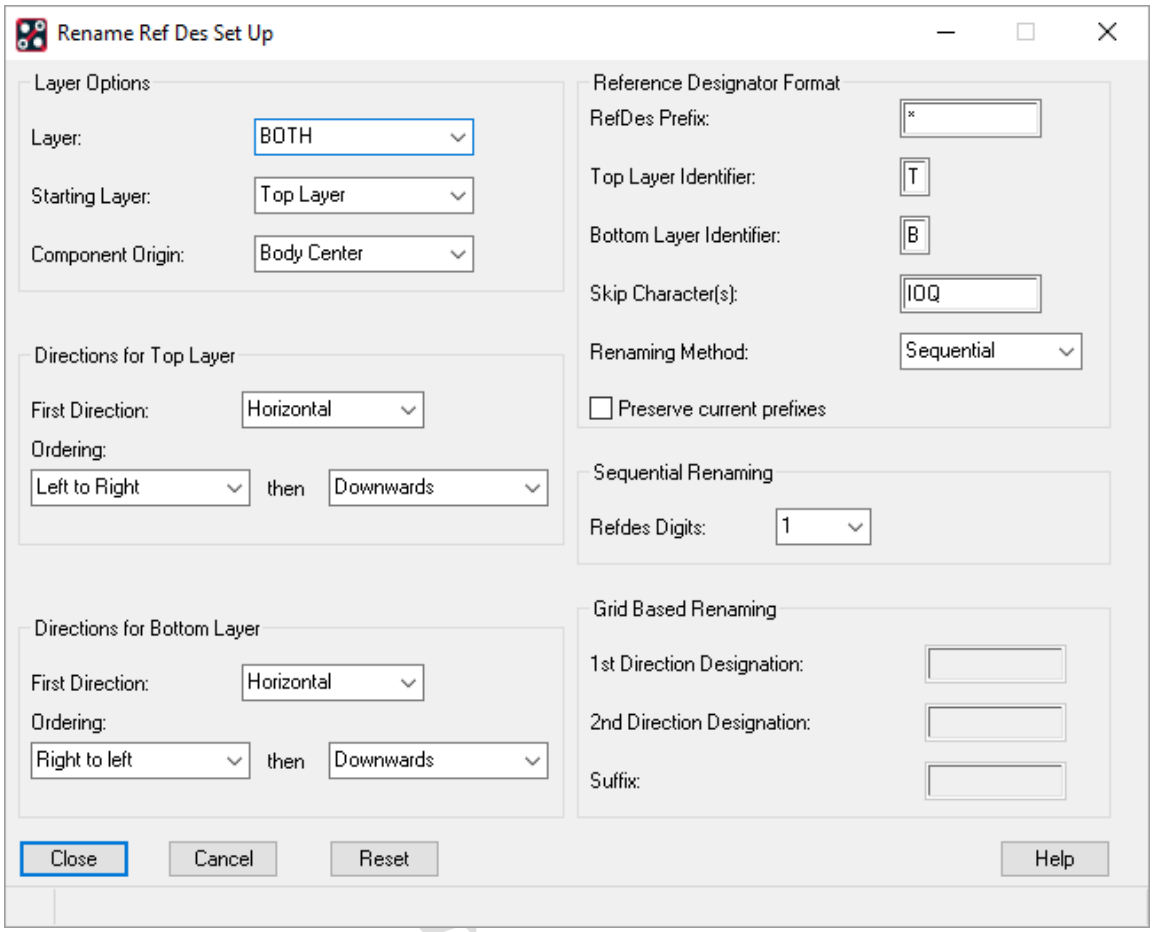
The Auto Rename Refdes command allows you to rename all reference designators, or only those with the ***Auto_Rename*** property attached.

To start the command, select ***Manufacture – Auto Rename Refdes*** from the top menu.

In the Rename RefDes form you will make the following selections:

- Choose the type of placement grid you want to use.
  - **User Defined Grid** - You define a grid on the class BOARD GEOMETRY and subclasses PLACE_GRID_TOP and PLACE_GRID_BOTTOM. The system will use these grids, looking at each grid square based upon the direction specified in the Rename RefDes Setup Form (see next page).
  - **Use Default Grid** - This option basically results in no two parts ever being considered in the same block for renaming purposes.
- Select which components to rename.
  - **Rename All Components** - Renames all components on the side of the board specified in the Rename RefDes Setup Form (see next topic).
  - **Attach Property, Components** - You must attach the ***AUTO_RENAME*** property to all components that are to be renamed in this pass.
- Click '***Setup...***' to check or change sequencing parameters (see next page).
- Click ***Rename*** in the Rename RefDes menu to begin execution.

Rename Reference Designators Setup Form



In the ***Rename Refdes*** form, select the '***Setup…***' button to bring up the ***Rename Ref Des Set Up*** form which is used to set the parameters used when running the rename reference designator command.

Layer Options - Specifies top side, bottom side, or both sides of the design to rename and which layer to rename first. You will also specify the origin point of the part for renaming purposes.

Directions for Top Layer and **Directions for Bottom Layer** - Specifies the rename order for the appropriate layer.

Reference Designator Format - Specifies how the new reference designator names should be created.

- **Ref Des prefix**- Specifies what the starting character or characters of the new name should be. An asterisk in this field specifies that the current reference designator format should be used as the starting character. You can also check the ***Preserve Current Prefixes*** box.
- **Top Layer Identifier** and **Bottom Layer Identifier** - Specifies a character that will be appended to the new reference designator name on the appropriate layer.
- **Skip Characters** - Identifies the characters that should not be included during rename when using the ***Grid Based*** method.
- **Renaming Method** - Can be set to either ***Sequential*** or ***Grid Based***.
    - If you choose the ***Sequential*** method, the ***Sequential Renaming*** section becomes available. Use the field Ref Des Digits to specify the minimum number of digits that should be used when creating a new reference designator name. For example, if 2 is specified, the numbers following the reference designator prefix would be 01, 02, 03, etc.
    - If you choose the ***Grid Based*** method, the ***Grid Based Renaming*** section becomes available. You use the ***First Direction Designation*** and ***Second Direction Designation*** fields to assign the prefixes to be used when creating the new reference designator name. Use the ***Suffix*** field if there is more than one component in the same grid cell. If you are going to use the grid based renaming method, you should set a ***User Defined Grid***.

Once you have specified all the parameters in the ***Rename Ref Des Setup*** form, select ***Close*** in this form. To execute the renaming sequence, select ***Rename*** in the ***Rename Ref Des*** form.

Rename Reference Designators — Key Points

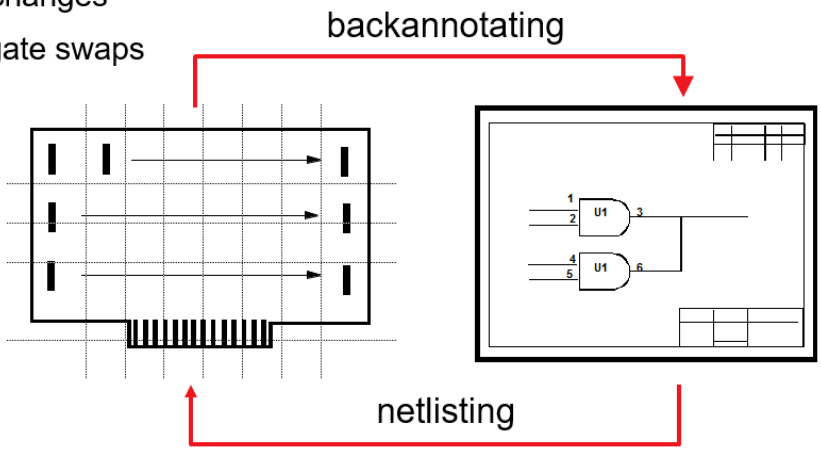
Things to Remember

- Reference designators can only be renamed ***ONCE*** between back annotations
- Before renaming reference designators, you should verify that the schematic and the layout are in sync
- A component can be individually renamed by editing the attached reference designator text (***Edit - Text***)
- An ***AUTO_RENAME*** property can be attached to specific components to sequence them separately
- A ***HARD_LOCATION*** property will prevent components from being renamed
- User-defined grid cells can be used to determine specific row and column boundaries
- Once reference designators are renamed, you ***MUST*** backannotate the changes to your schematic source

Backannotation

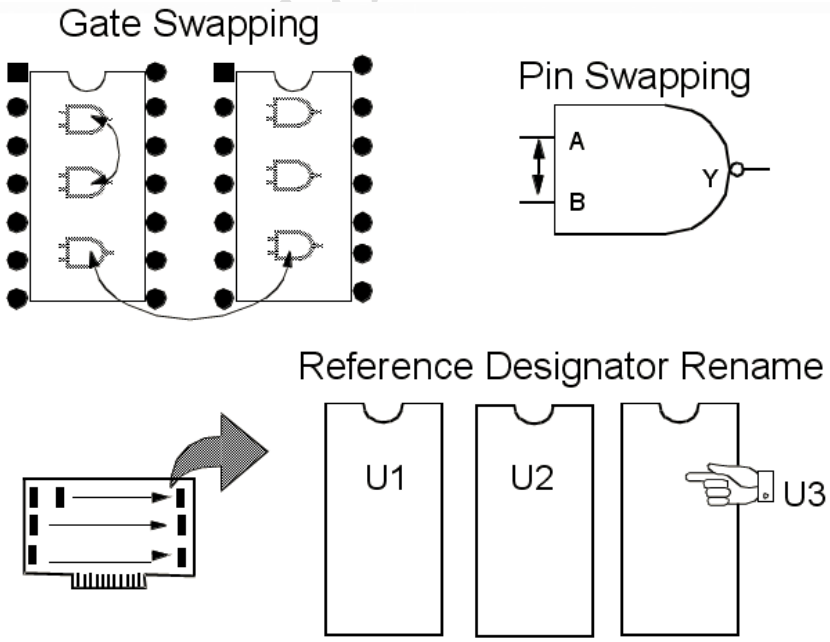
Mapping changes from the physical layout back to the logical schematic world

- Property changes
- Ref-des changes
- Pin and gate swaps



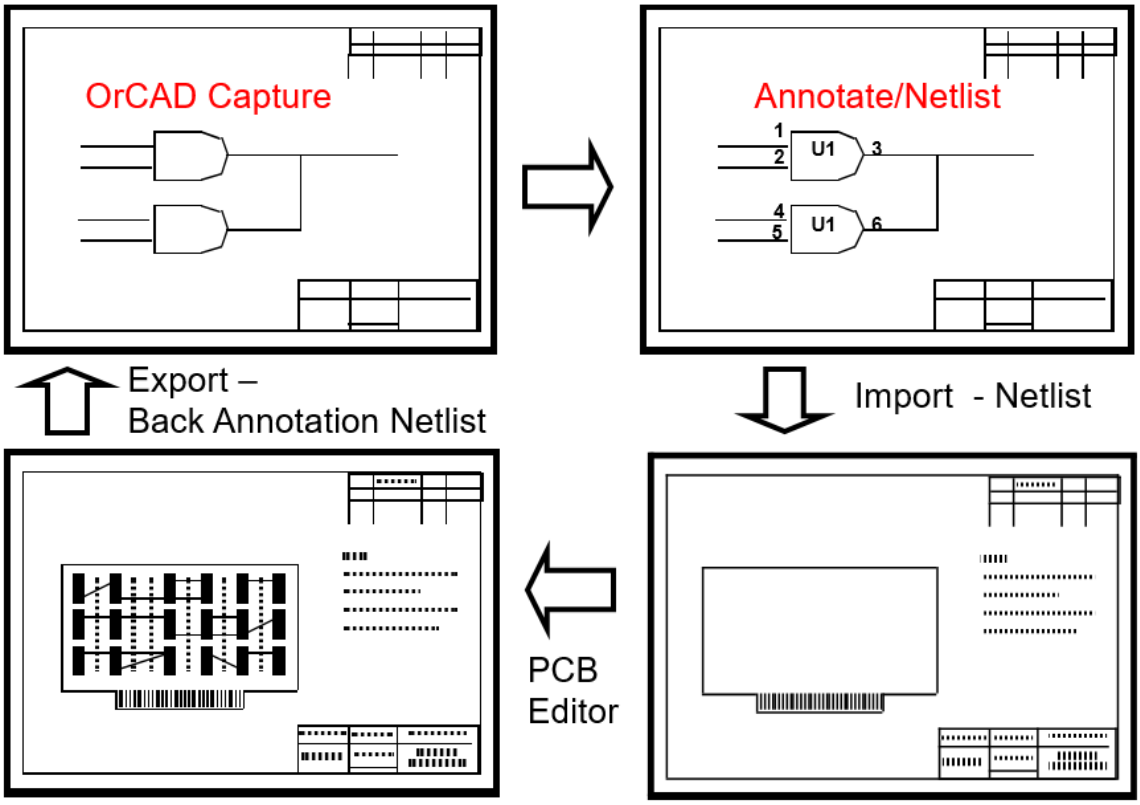
For backannotation to work correctly, the schematic must not have been changed since the last logic import into the PCB Editor board.

Backannotation Examples



The PCB Editor tool can perform gate and pin swapping, which can improve routing. These processes and renaming, represent changes to the PCB Editor database and must be communicated back to the schematic.

Integrating Physical Layout with Logic Design



PCB Editor

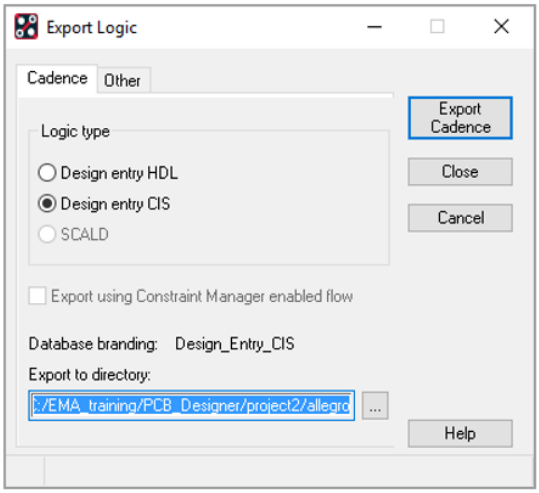
Export Logic - Generates backannotation files that the OrCAD Capture tools use to update the schematic.

OrCAD Capture - Front End

Back Annotate - The Back Annotate program converts the changes made to the physical layout, such as renaming of reference designators and physical pin number changes to the logic devices in each symbol in the schematic.

PCB Editor to OrCAD Capture Backannotation

Export - Back Annotation Netlist



The first step in back-annotating from PCB Editor to OrCAD Capture is to generate the feedback files. These are the same four files (**`compView.dat`**, **`funcView.dat`**, **`pinView.dat`** and **`netView.dat`**) used in the PCB Editor to OrCAD Capture backannotation process. This can be done from within PCB Editor by using the ***Export - Back Annotation Netlist*** command or by using the ***Generate Feedback Files*** option from the ***OrCAD Capture Backannotate*** command.

After the four feedback files have been generated from the PCB Editor design, you must run the backannotation process from within OrCAD Capture. This process will read the PCB Editor generated feedback files, create an output swap file that contains all the required backannotation information required by OrCAD Capture, and update the schematic.

Properties are passed back and forth between these two tools. You define which property names are allowed to pass. They are controlled by listing them in the **`allegro.cfg`** file located at ***<cdsroot> - tools - capture***.

Labs

Lab 12-1: Checking for DRCs and Unconnected Pins

- Confirm whether you have completed all connections

Lab 12-2: Renaming Components

- Use the renaming capability in the PCB Editor to setup resequencing and change reference designators

Lab 12-3: PCB Editor to OrCAD Capture Backannotation (Optional)

- Backannotate changes made in the PCB Editor physical layout for the OrCAD Capture logical schematic

Lab 12-1: Checking for DRCs and Unconnected Pins

Objective: Confirm the number of completed connections on a routed board.

Opening the Routed Design to check DRCs

At this point, you have imported the netlist, set the design's constraints, placed the components, routed the design and created the planes and copper pours. We will now make sure the board is complete and DRC free and your design is ready for post processing.

1. Start the PCB Editor if you don't already have it running.
2. Open the `DRC_design.brd` in the ***solutions*** directory and save it in the ***project2 - allegro*** directory.

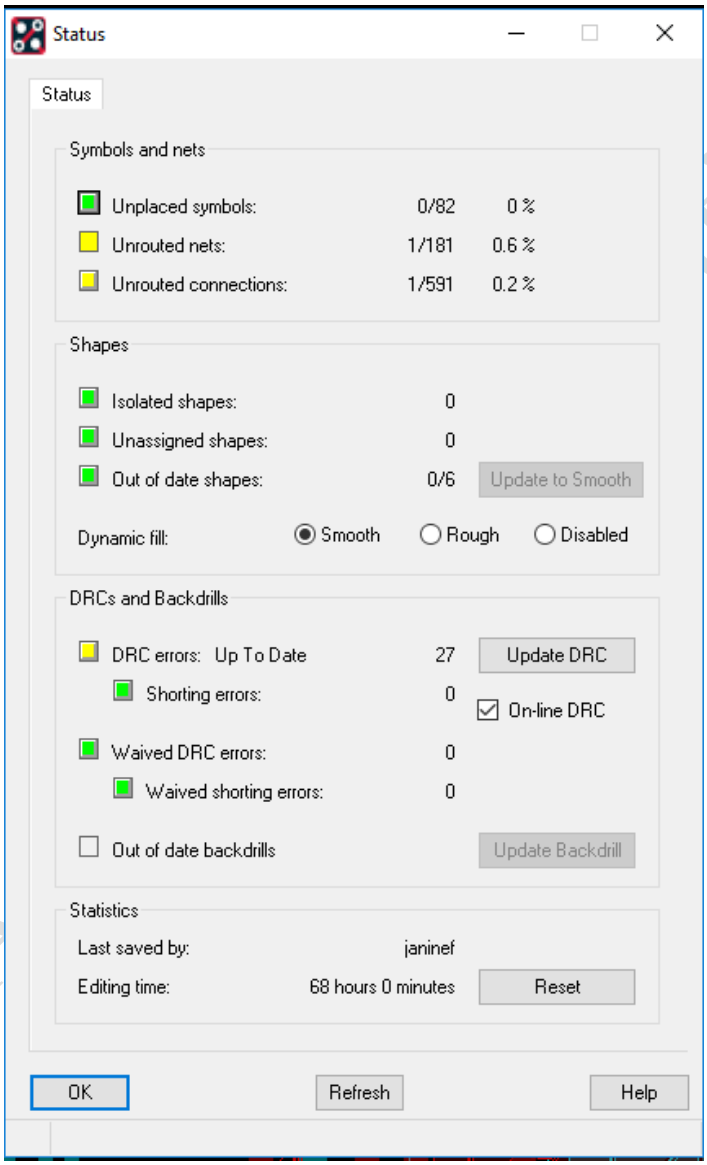
Readying Shapes for Final Artwork

You previously created a Ground plane, a split Power plane and copper pour areas for AGND and GND_EARTH as positive dynamic shapes. You now need to make sure that all shapes in the design are updated to smooth in order to ensure all voids and thermal relief ties have been properly created. This is also necessary to be able to successfully create artwork files.

1. Select ***Shape - Global Dynamic Parameters*** from the top menu.
2. In the ***Shape Fill*** tab's ***Dynamic fill*** section, click the ***Smooth*** button if needed and select ***Update to Smooth***.
   If Update was required, the PCB Editor command line will display messages stating that the shapes are being updated. This will ensure that your shapes are all artwork quality with all required voids and thermal reliefs.
3. Now, select the ***Void Controls*** tab and change the ***Artwork Format*** to ***RS274X*** (the default) if it is not already set.
4. Click ***OK*** to accept the change and dismiss the form.

Using the Design Status Form

1. Select ***Check – Design Status*** to check for the number of DRCs in the design.
   The Status window appears with the number of unplaced symbols, unrouted nets and connections, information regarding shapes and the number of DRCs.

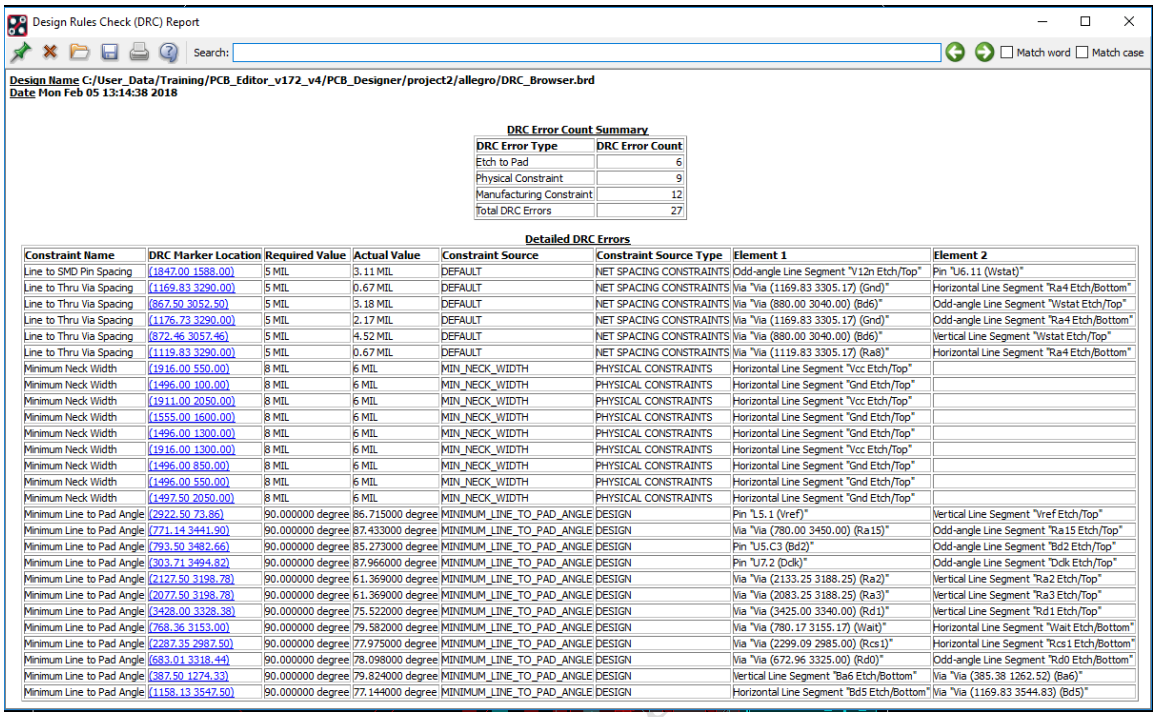


As you can see, there are 27 DRCs in the design.

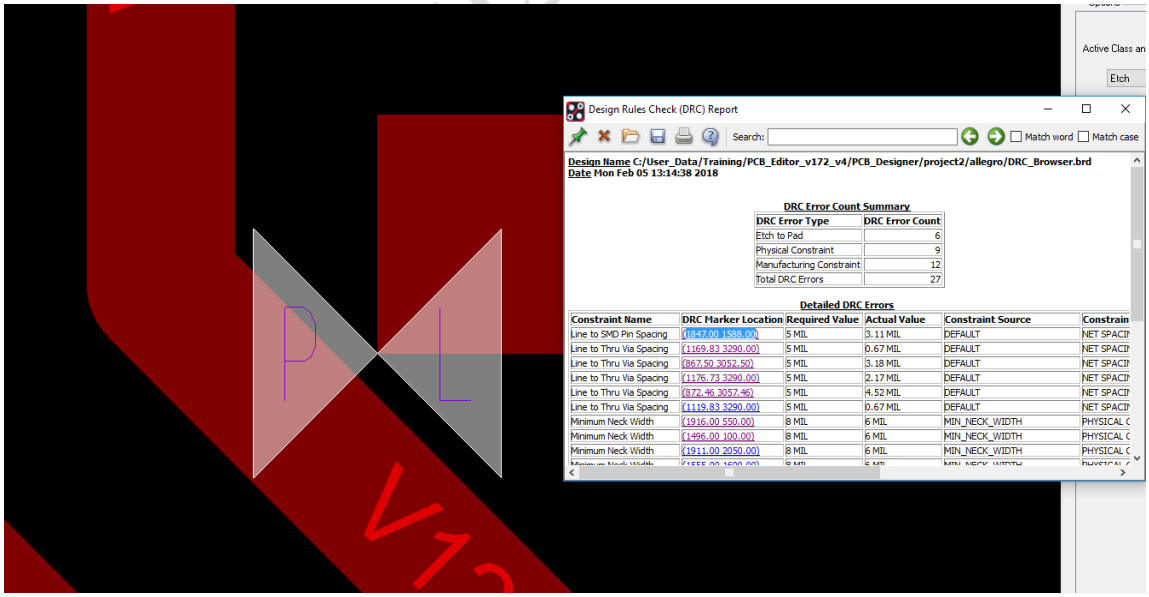
Note In the *Status* form, clicking on the button to the left of the various selection options will open the appropriate report defining the status of that option.

2. Click on the yellow box next to ***DRC errors:***
   This will display the **Design Rules Check (DRC) Report** window.

3. Move the resultant window over and click ***OK*** to dismiss the ***Status*** window.
4. You may resize the ***Report*** window as you like.



5. Using the middle mouse wheel, zoom in to any area of the design.
6. Click on one of the sets of coordinates.



Notice that the window is centered around the DRC that you selected.

7. Click on a couple different sets of coordinates and examin the error.
8. Close the Design Rule Check (DRC) Report window.

Opening the Routed Design to check for unrouted connections

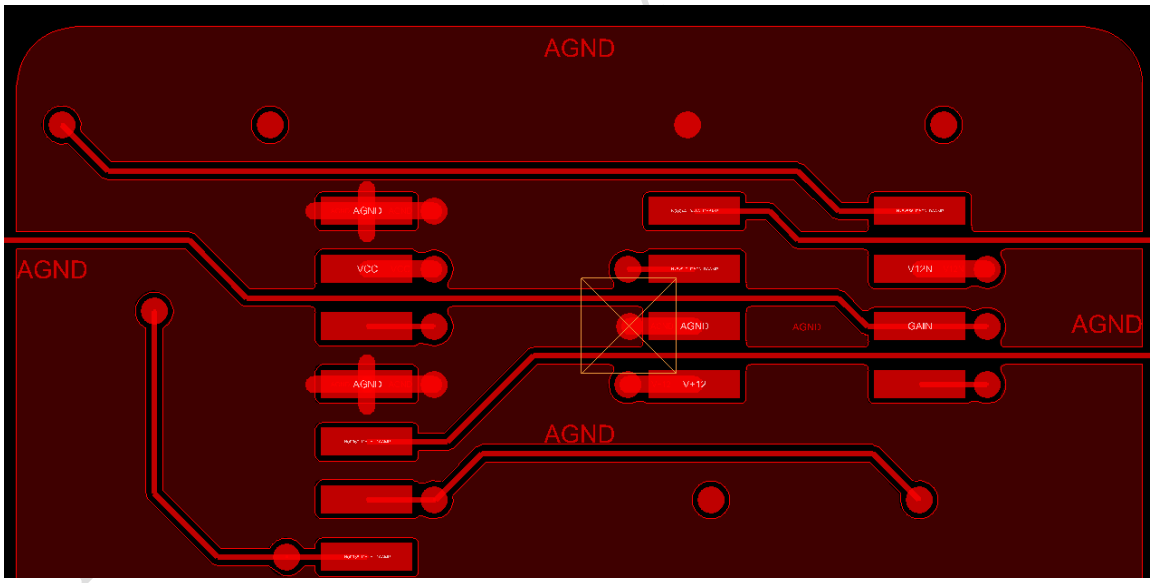
1. Without saving the DRC_design.brd, open the `complete.brd` in the ***solutions*** directory and save it to the ***project2 - allegro*** directory.

Using Rats to look for Disconnects

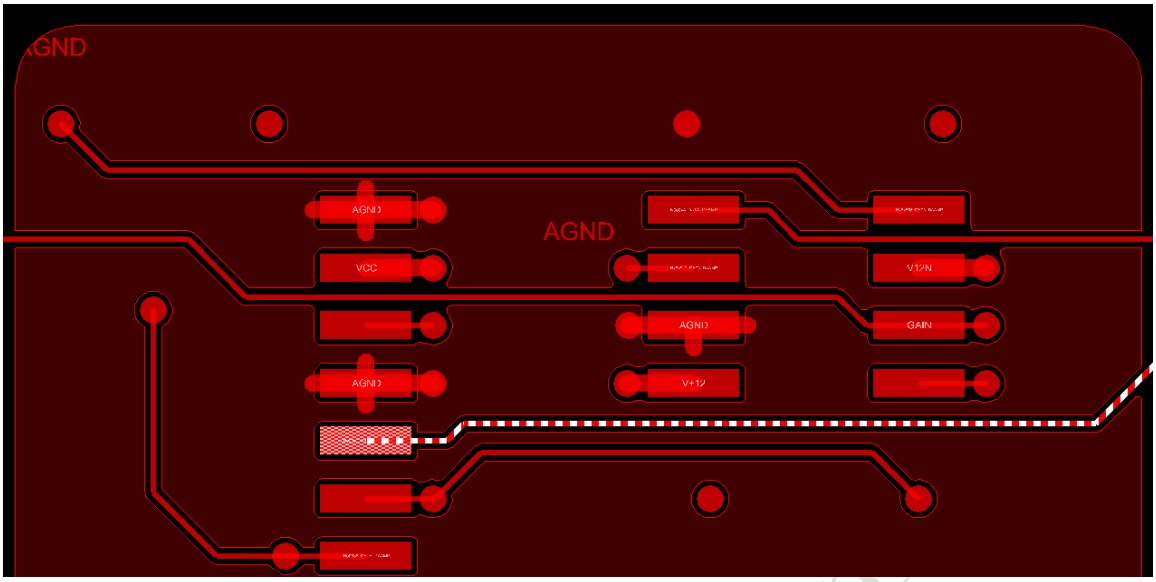
1. Choose ***Display - Show Rats - All*** from the top menu or click on the icon. Any unconnected nets display as ratsnest lines.

Note Although this option is a quick method of finding unconnected pins, it's not always effective with large designs because ratsnest lines may not be easily visible. You can turn the etch layers off in the Visibility tab while looking for ratsnest lines.

2. You will see a special ratsnest for AGND on pin 3 of U18.
   If you look carefully, you'll see that it's actually pin 10 of U18 that is cutoff from the rest of the AGND net because of the way the shape on the top of the board is split by traces running through it.
   You will also notice that there is a small island next to pin 3 of U18. Both of these issues need to be corrected.



3. We could use ***Shape – Delete Unconnected Copper*** to remove the island but, if you look closely, you will see that there is a trace that you can slide (Use ***Route – Slide*** command) down one channel which will solve both problems (see the figure on the next page).



1. Click the Right-Mouse-Button and select Done from the resultant popup.
2. Choose ***File - Save*** from the top menu.
   A window appears and warns you that the **`complete.brd`** file already exists. It asks if you want to overwrite the file.
3. Click ***"Yes"*** to confirm the file overwrite.
   The file `complete.brd` is written to disk.

End of Lab

Lab 12-2: Renaming Components

Objective: Assign new reference designators automatically and interactively, using the renaming qualifications.

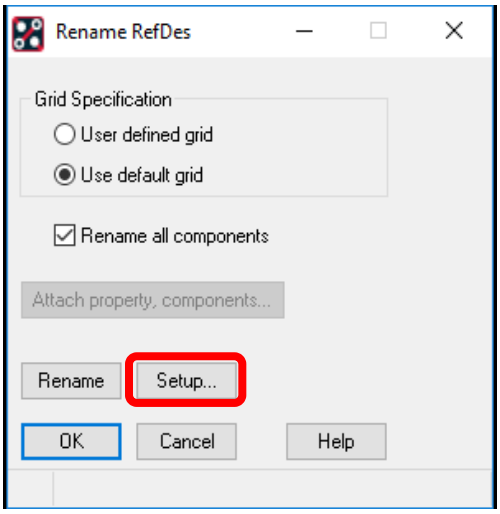
Important

Setting Colors and Visibility

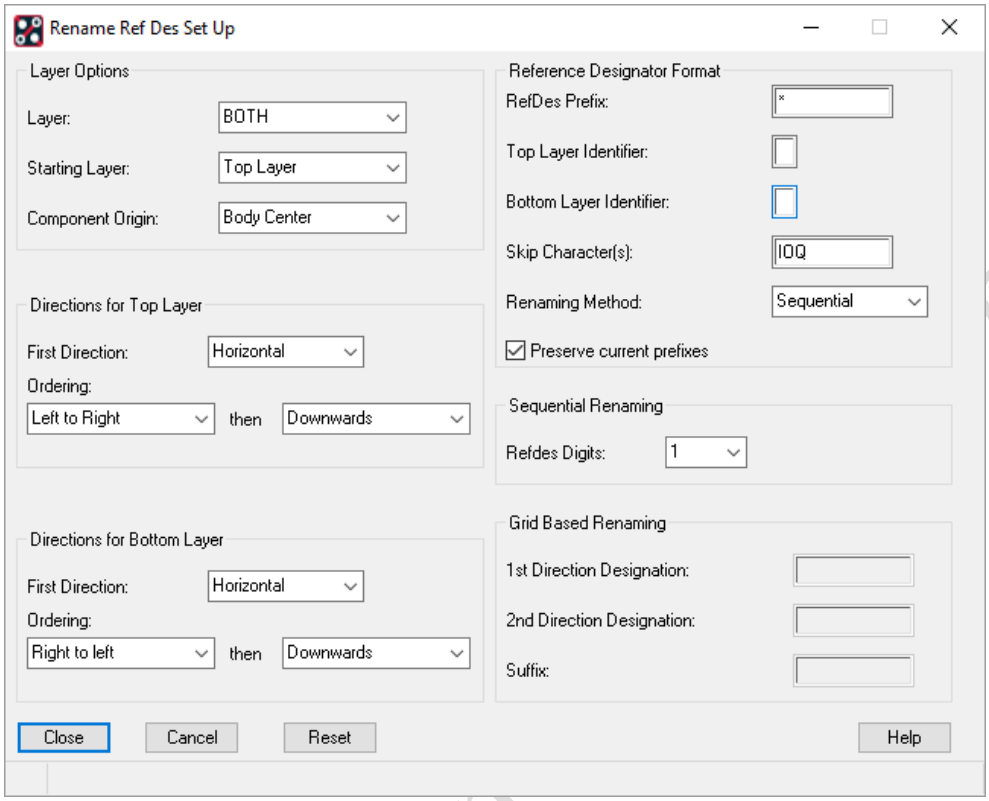
1. If you don't already have PCB Editor running, start PCB Editor.
2. Open the file **`complete.brd`** in the ***propject2/allegro*** directory. If you did not do the last lab, you will find the complete.brd in the ***solutions*** directory.
3. Choose ***Display - Zoom - Fit*** from the top menu.
4. Choose ***Setup - Colors*** from the top menu.
5. Click the ***Global Visibility*** '***Off***' button.
6. Expand the ***Components*** category and select ***Ref Des*** class.
7. Turn '***ON***' the ***ASSEMBLY_TOP*** and ***ASSEMBLY_BOTTOM*** subclasses.
8. Expand the ***Geometry*** category and select the ***Board Geometry*** class.
9. Turn '***ON'*** the ***OUTLINE*** and ***Design_Outline*** subclasses.
10. In the ***Geometry*** category, select the ***PACKAGE GEOMETRY*** class.
11. Turn '***ON***' the ***ASSEMBLY_TOP*** and ***ASSEMBLY_BOTTOM*** subclasses.
12. Select the ***Stack-Up*** category ***Conductor*** group and turn '***ON***' only the following: ***TOP-PINS***, ***BOTTOM-PINS***, ***TOP-VIAS*** and ***BOTTOM-VIAS***.
    It is easier to see the reference designators with the wiring turned off.
13. Click ***OK*** to close the ***Color Dialog*** form.

Renaming Components

1. Choose ***Manufacture - Auto Rename RefDes*** from the top menu.
   The ***Rename RefDes*** form appears.
2. Check to see that ***Use Default Grid*** is selected.
3. Check to see that '***Rename all components***' is selected.
4. Click on the **'*Setup…*'** button.
   The ***Rename RefDes Setup*** form appears.



5. Fill in the Rename Ref Des Set Up for to match the figure below:



Notice that the Top Layer Identifier and the Bottom Layer Identifier fields have been blanked out because we don't want extra characters added to show what side the component is placed on. The Preserve Current Prefixes check box has been enabled to use the current reference designator format.

6. Click ***Close*** to return to the ***Rename RefDes*** form.
7. In the ***Rename Refdes*** form, click ***Rename*** to execute the automatic rename process.
8. Click ***OK*** to close the ***Rename RefDes*** form.
9. Zoom in or pan your view to inspect your results.
10. Choose ***File - Save As*** from the top menu.
    A browser form appears.
11. In the ***File Name*** field, enter **`final`**
12. Click ***Save*** in the file browser.
    The file **`final.brd`** is saved to disk.

    You will overwrite this version of your design while preparing it for final output phases.

Interactively Renaming Parts

1. Zoom in to view a component of your choice.
2. Choose ***Edit - Text*** from the top menu.
   The PCB Editor message area prompts,

   ```
   Pick text to edit
   ```

3. Click on the reference designator of the component you want to rename.
   The selected refdes is highlighted.
4. At the PCB Editor command line, enter ***U99*** (or any name you wish) and press ***Enter***.

Note If the name you choose already exists in your design, you are notified in the PCB Editor's message area that the name is being swapped with another component. This feature prevents the creation of duplicate reference designators.

5. To exit from the ***Edit - Text*** command, right-click and choose "***Done***" from the pop-up menu.
6. Choose ***File - Save*** from the top menu.
   A window appears and warns you that the **`final.brd`** file already exists. It asks if you want to overwrite the file.
7. Click **"*Yes*"** to confirm the file overwrite.
   The file `final.brd` is written to disk.

End of Lab

Lab 12-3: PCB Editor to OrCAD Capture Back Annotation (Optional)

Objective: Create backannotation files to be incorporated into the OrCAD Capture schematic using a revised board database.

You have renamed your reference designators. These database changes must be sent back to the schematic.

Note This lab shows the process used for designs that were created from an OrCAD Capture schematic only!

Note Make sure you are working in the ***project2/allegro*** folder.

1. Choose ***Export – Back Annotation Netlist*** from the top menu in PCB Editor.
2. In the ***Export Logic*** form, select ***Design entry CIS*** (OrCAD Capture) in the ***Logic Type*** section if it is not currently selected.
3. In *the* ***Export to directory*** field, browse to the ***project2/allegro*** directory.
4. Click ***Export Cadence***.
   The feedback files `pinview.dat`, `compview.dat`, `netview.dat`, and `funcview.dat` are created. These files can be used in the OrCAD Capture backannotation process.
5. Select ***Close*** to close the ***Export Logic*** form.

End of Lab

Lesson 13: Preparing the Board Design for Manufacturing

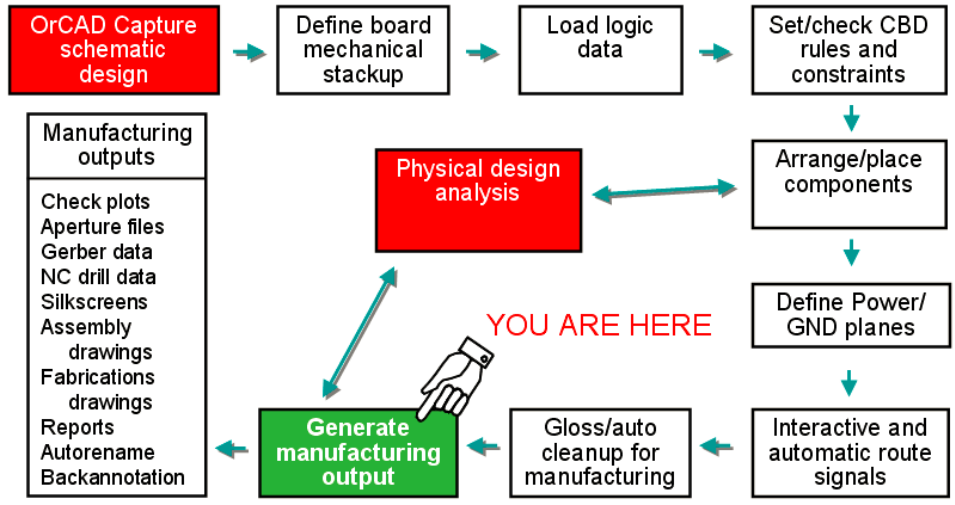
Learning Objectives

In this lesson, you will:

- Generate and edit silkscreen layers, use reports available in the PCB Editor
- Set up design files for artwork, and preview artwork files before plotting
- Generate drill symbols and a drill legend for a fabrication drawing, create check plots, and output a drill file used for drilling the board holes in manufacturing
- Generate an IPC-2581 database for manufacturing your board design

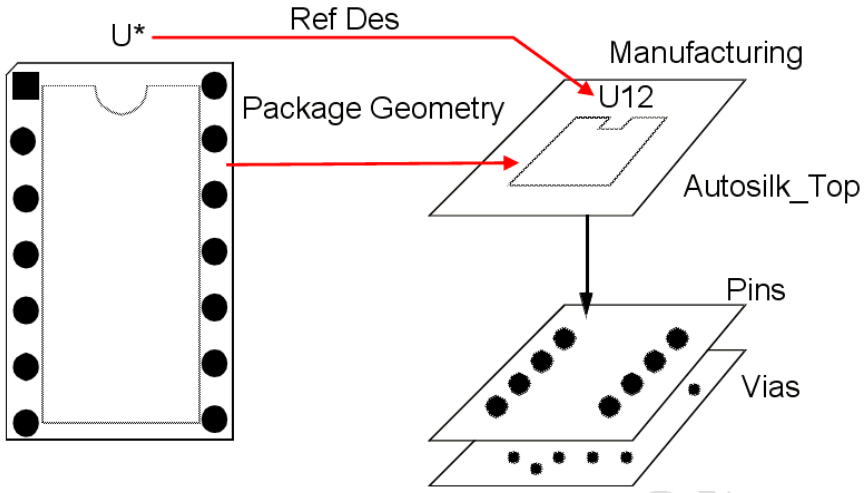
In this section, you will learn more about preparing your design for post processing and will learn how to generate the required outputs. This will include creating silkscreens, generating reports, setting up for artwork, creating artwork files and creating NC files.

Design Layout Process



This design flow is used throughout the entire course. Each box in this flow represents a common step in the design of a printed circuit board. You will now learn the steps and processes required to generate the standard output files to be delivered to manufacturing.

Creating Silkscreens



The PCB Editor has a routine to automatically create silk screens. It will clip lines away from pins and vias when required and attempt to move text out from under parts. This routine is optional and does not have to be run.

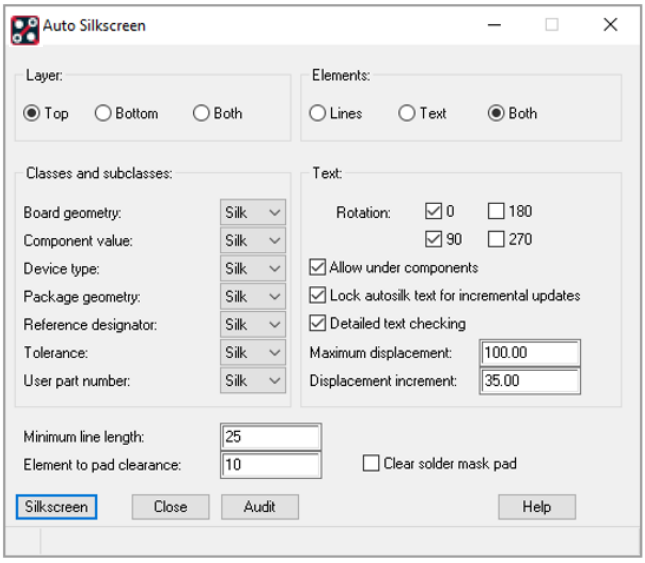
When clipping lines and moving text, the original silk screens subclasses are NOT modified. This means all of the graphics on the Package Geometry class, and text on the Ref Des class, are not touched. The graphics are copied from these original classes, modified as necessary, and placed on the class ***MANUFACTURING***, subclass ***AUTOSILK_TOP*** for the top silk screen, and subclass ***AUTOSILK_BOTTOM*** for the bottom silk screen.

Creating Silkscreens — Menu

Manufacture - Silkscreen

Subclasses available:

- *Silk – only reads silkscreen layers*
- *Any - reads silkscreen layers first, if not available it then reads the Assembly layers*
- *None – nothing is taken from the class*



The options in the Auto Silkscreen form are:

- **Layer -** Specifies the side of the design on which to generate the silkscreen.
- **Elements -** Specifies whether lines, text, or both are processed. Only selected elements are erased from the specified AUTOSILK subclass and regenerated. Any elements that are not selected are untouched.
- **Classes and Subclasses -** Defines the PCB Editor classes where the Auto Silkscreen process looks for silkscreen graphics. For each of the classes listed on the parameter form, you can choose one of the following:
  - **Any**: first uses the SILKSCREEN subclass. If nothing is found in the value you select, the ASSEMBLY subclass is used.
  - **Silk**: only copies graphics from the SILKSCREEN subclass.
  - **None**: specifies that nothing is taken from the class.
- **Text -** Determines how text is (rotated) displayed on the silkscreen.
  - **Allow under Component** - Specifies whether silkscreen text may be positioned under a component that exists on the same side of the design as the one being processed. Text is considered to be under a component if it falls within the extents of the component's graphics on the PACKAGE GEOMETRY class, ASSEMBLY subclass. Enabled by default.
  - **Lock Autosilk Text** – When the user uses the Lock text option during silkscreen generation, it will move the silkscreen to their original locations as they are in the symbol. The Lock actually means that the text is locked against incremental update due to changes with other elements like symbol move or adding a ‘via’, NOT from redoing silkscreen through the silkscreen execution.

For clarity, please refer to the example described below:
If while silkscreen generation using the ***Manufacture – Silkscreen*** command, the option for "Lock Autosilk Text during Incremental Update" and "Clear Soldermask Pad" are selected, the Autosilk will not be placed under soldermask pads of vias or padstacks

But when a 'via' is moved over the silkscreen, this incremental update with the routing will not move the text dynamically.

But if the option for "Lock Autosilk Text during Incremental Update" is not selected then the changes in routing or movement of any symbol will dynamically adjust the text to clear the soldermask pad and the text overlap if it happens by symbol movement.

But the next silkscreen generation will readjust the text and place it at the original location. The reason here is to clear silkscreen of any obstacles.

  - **Detailed Text Checking** - Considers each stroke for each character as a line segment, where the line segment itself is checked for potential obstacles. For instance, if the character 'O' is large enough, a pad may potentially lie in its interior, or it may nestle in the crook of the character 'L'. Otherwise, silkscreen text is checked using the bounding box for the text. The box expands to accommodate the descenders of lowercase characters, whether the string actually has lowercase characters or not. Having this option checked may reduce the performance with larger designs. Enabled by default.
  - **Maximum Displacement** - Specifies in user units the maximum distance in any direction that silkscreen text strings can be moved to avoid intersecting with a pad. The default value is 100 mils.
  - **Displacement Increment** - Specifies in user units the distance increment to use when looking for a location to which a silkscreen text string is moved. This is bounded by the area defined by Maximum Displacement. The default value is 35 mils.
- **Minimum Line Length** - Specifies the minimum length of any line or arc segment allowed on an AUTOSILK subclass. The process of trimming lines and arcs around pads can often produce a number of very small segments. If any of these segments is shorter than the value specified as minimum line length, they are discarded. The default value is 0, which means that no segment is discarded.
- **Element to Pad Clearance** - Specifies in user units the amount of space to be left between silkscreen elements and the edges of pads on that side of the design. The default value is 0, which allows silkscreen elements to touch the pad edge. Using negative values allows silkscreen elements to intersect pads by the specified value.
- **Clear solder mask pad** - Specifies that silkscreen elements do not contact pad areas defined for masking and conductive pad geometries are ignored.
- **Silkscreen** - Runs the process, based on the parameters you set.
- **Audit** - Audits the board based on the parameters you set and generates the autosilk.log file

Incremental Update of Silkscreens

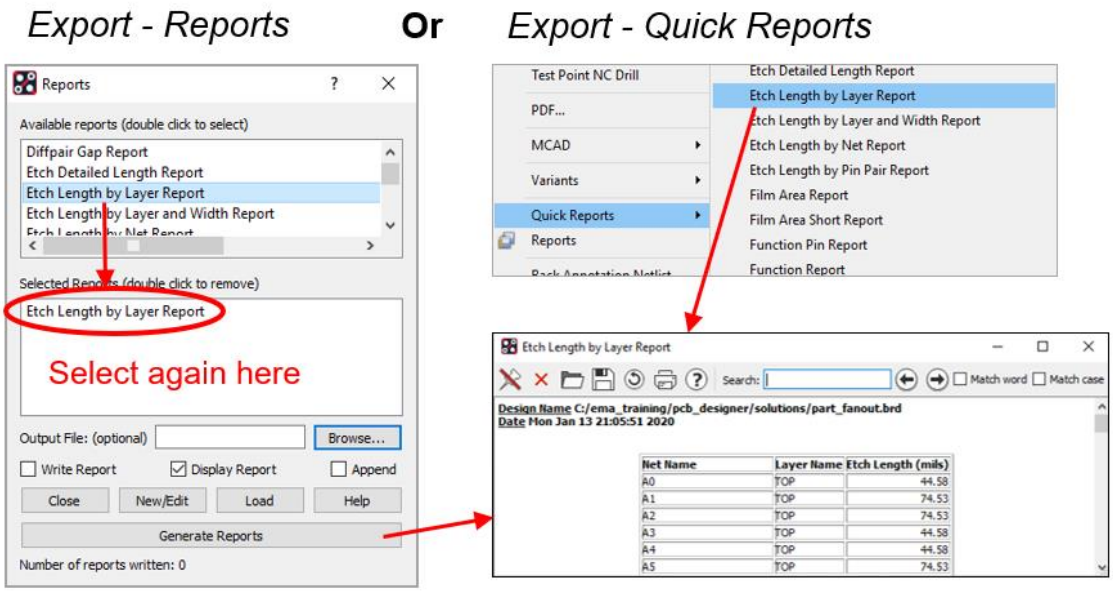
- There must be at least one run of the autosilk process for incremental silkscreen updates to occur
- After incremental silkscreen mode is in effect, the following occurs:
    - If a component is moved, its old silkscreen will be removed, and the new silkscreen will be generated to properly clear around pins and vias
    - If a via is added, any silkscreen that is too close will be updated as required
    - If a via is deleted, any silkscreen that was "clipped" because it was too close will be added back
- When in incremental mode, any operation that results in a silkscreen error will only display a warning in the editor command area that a silkscreen failure occurred. To see the actual error, you must use the silkscreen "Audit" feature.

Note  Running Refresh Symbol may cause both the original silkscreen layers and the Autosilk layers to be regenerated.

The Silkscreen Incremental mode is only enabled after using the ***Manufacture - Silkscreen*** command. When moving or replacing parts in the incremental mode, the autosilk silkscreen is generated based upon the symbol's current silkscreen definition. Therefore, in general, the autosilk layer should not be manually edited. Instead, the original silkscreen subclass should be modified so that whenever any parts are moved, the correct autosilk information will be automatically generated. This includes both line and text information.

When you are either dumping the libraries or creating a clipboard, the autosilk information ***WILL NOT*** be included. Only the symbol's original silkscreen will be used.

Generating Reports



PCB Editor provides many predefined reports that can be run from within the current design. To create a report, you can select either the ***Export - Reports*** option, or the ***Export - Quick Reports*** command.

When you select the ***Export – Reports*** command, the ***Reports*** form is displayed. Use the scroll bar on the right side of the ***Available Reports*** window and then ***double-click*** **on** the desired report. This report name moves to the ***Selected Reports*** window in the lower half of the form. Select the report and click the ***Generate Reports*** button to run the specified report. A report window appears showing your report in an HTML enabled window.

This displayed report window has five buttons: ***Sticky***, ***Cancel***, ***Save***, ***Print***, and ***Help***. It also has a Search feature to find and highlight text within the report. You can save the report to a file from the displayed window by selecting the **Save** icon and specifying a file name in the Reports form that appears.

If you wish to save the report to a file and NOT have the report shown in the PCB Editor, specify a file name in the ***Output File*** field of the ***Reports*** form. The ***Append*** option will append the latest version of the report to the end of a pre-existing file. Select ***Close*** to close the main Reports window.

If you want to create a customized report, you select **New/Edit** to proceed to another form. You can define a new or edit an existing configuration file within the form.

Labs

Labs 13-1: Creating Silkscreens

- Generate and edit silkscreen layers
  - Set visibility
  - Execute the autosilk process
  - Edit the silkscreen

Lab 13-2: Generating Reports

- Use reports available in the PCB Editor

Lab 13-1: Creating Silkscreens

Objective: Generate and edit silkscreen layers to produce a silkscreen layer with no errors.

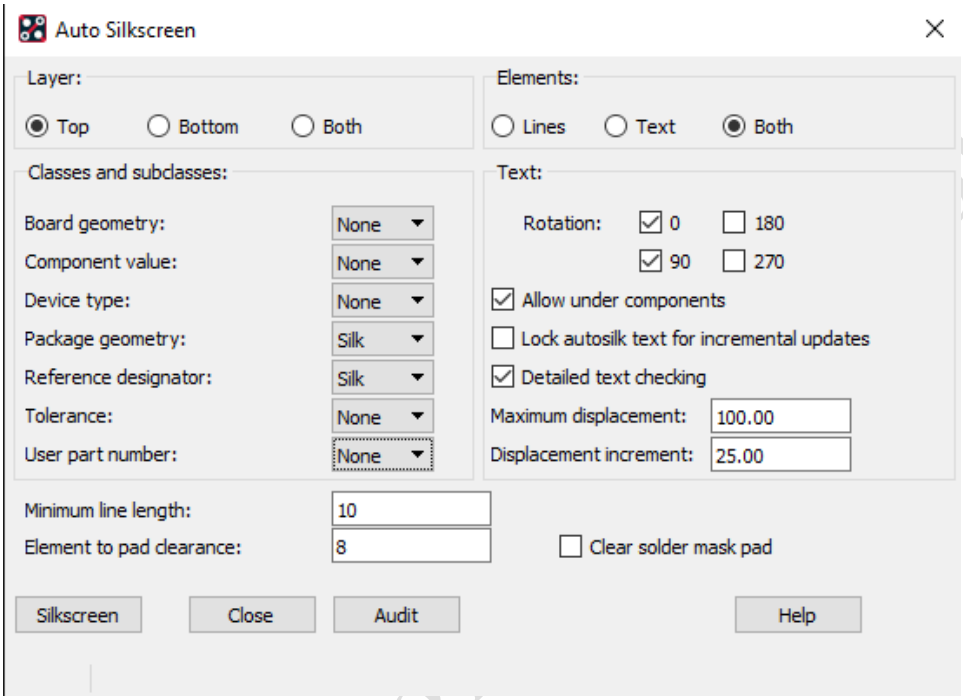
Setting Visibility

Before you proceed, turn ON the drawing layers that display the top silkscreen information.

1. If the **`final.brd`** file is not currently open, open it.
2. Choose ***Setup - Colors*** from the top menu.
3. Turn ***Global Visibility "Off"***
4. Select the ***Manufacturing*** category.
5. Turn '***ON***' the visibility for the ***AUTOSILK_TOP*** subclass.
6. In the ***Available Colors*** section, select the color ***white*** and assign it to the ***AUTOSILK_TOP*** subclass.
7. Expand the ***Stack-up*** category and select the ***Conductor*** group.
8. Turn '***On***' the visibility for the ***PIN*** and ***VIA*** classes on the ***TOP*** subclass.
   We will be working with the objects on the top of the board.
9. Expand the ***Geometry*** category and select the ***Board Geometry*** class.
10. Turn '***On***' the visibility for the ***Design_Outline*** layer.
11. Click ***OK*** to close the ***Color Dialog*** form.
    The display is ready for silkscreen generation.

Executing the Autosilk Program

1. Select ***Manufacture - Silkscreen*** to open the ***Auto Silkscreen*** form.
2. Set the following parameters:



   The Classes and subclasses settings are toggled to determine which subclasses will be copied to the Autosilk subclass.

3. Click ***Silkscreen*** to execute the automatic silkscreen program.

   If the program fails to place any silkscreen reference designators legally (not under components, and away from pads and vias), they will be listed in the ***autosilk.log*** file. The ***autosilk.log*** file also lists the line segments that were removed because they were shorter than the ***Minimum line length***.

4. Choose ***File - Viewlog*** from the top menu.
   The `autosilk.log` file is displayed. Use the scroll bar to review this file.
5. Click ***Close*** to exit the log file.
6. Zoom in to review the resulting silkscreen.

   Notice how the package symbol outlines are broken where they intersect pads and vias. Also note the difference in refdes text sizes. This is controlled by the text block that was used when the refdes labels were added to the package symbols.

Editing the Silkscreen

1. Choose ***Edit - Move*** from the top menu.
2. Set the ***Find*** filter so that only ***Text*** is '***ON***'.
3. Click on a reference designator.
   It is attached to your cursor.
4. Click to place the reference designator in a new location.
   You are still in move mode.
5. If you need to rotate a reference designator, simply click on it, right-click and choose ***Rotate*** from the pop-up menu.
   A handle will appear, which you will use to change the rotation of the text.
6. Left-click to select a new rotation for the text and then left-click again to place the refdes with its new rotation.
7. Play with the locations of the text
   Remember to use the ***Undo*** and ***Redo*** icons if needed.
8. Choose ***File - Save As –*** from the top menu.
9. Rename this drawing by entering the following in the File Name field:
   `final_mfg.brd`
   The file `final_mfg.brd` is written to disk.

End of Lab

Lab 13-2: Generating Reports

Objective: Create reports from the class board to help decide if it is ready to go to manufacturing.

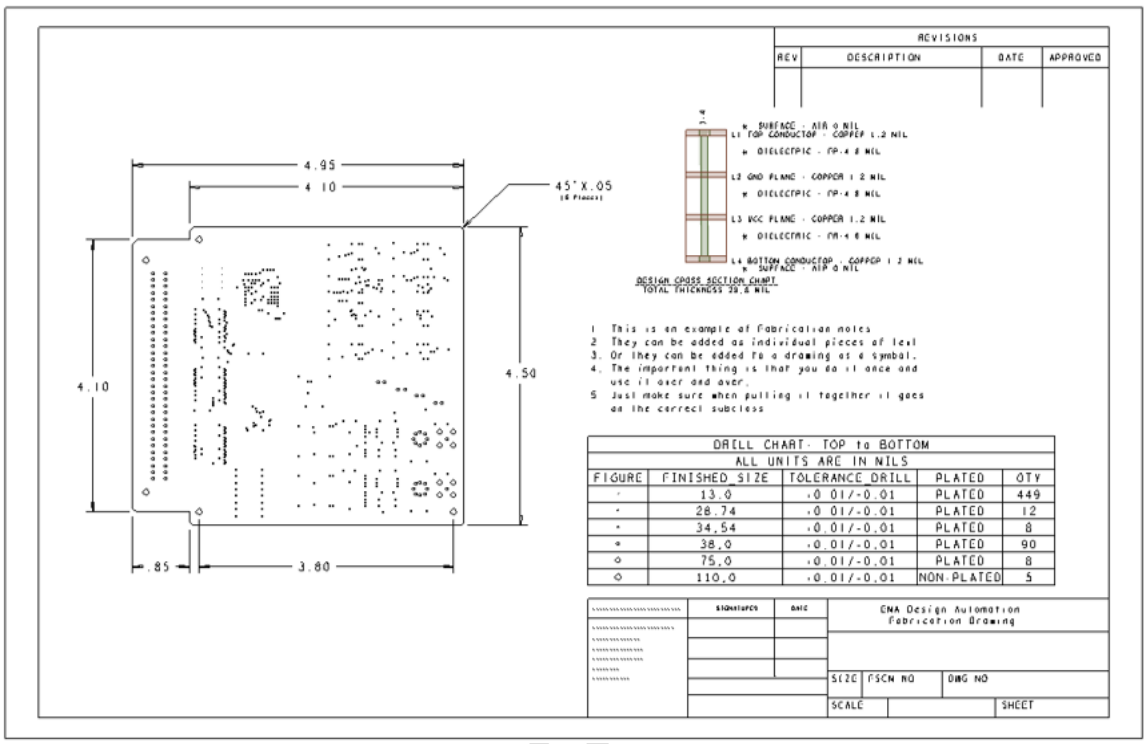
The PCB Editor has several reports that provide information about your design. You can print reports at any time during the processing cycle. A report menu is included.

1. Choose ***Export - Reports*** from the top menu.
   The ***Reports*** dialog box appears.
2. Scroll through the list of ***Available Reports*** and double-click the ***Summary Drawing Report*** from the pull-down list.
3. Once it is in the ***Selected Reports*** window, select it again
4. Click the ***Generate Reports*** button to generate the report.
5. A ***Summary Drawing Report*** appears in a new viewing window.
6. After viewing the report, click the red "***X***" in the displayed ***Summary Drawing Report*** window to close this report window.

7. In the ***Reports*** dialog box, double-click on the ***Summary Drawing Report*** in the ***Selected Reports*** area to remove it from this window.
8. Repeat this process to create an ***Etch Length by Layer Report***, ***Etch Length by Net Report***, ***Design Rules Check Report***, ***Unconnected Pins Report***, ***Unplaced Components Report***, or any other type of report you wish.
9. Click ***Close*** to close the ***Reports*** dialog box.
10. Do ***not*** log out. You will use this file, `final_mfg.brd`, in the next lab.

End of Lab

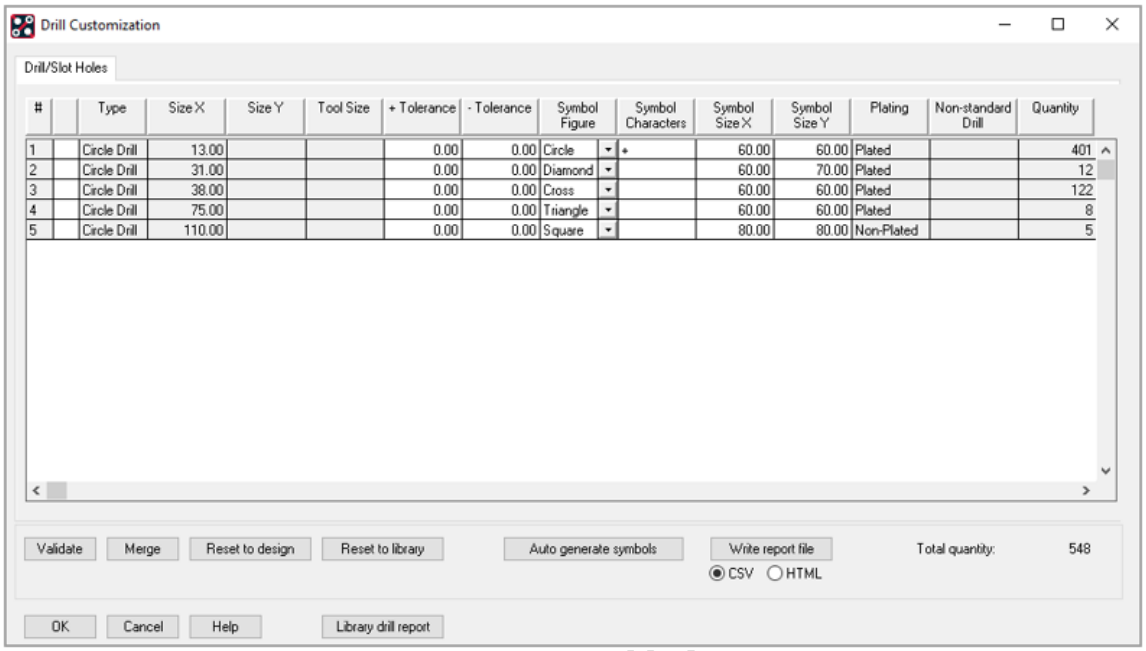
Creating Fabrication Drawings



In order to create a fabrication drawing, you will have to create your own company format and title block symbols. You will also need to dimension your drawing if you have not "Done" so in the board mechanical drawing (covered in Lesson 5). Select the ***Manufacture - Dimension Environment*** option from the top menu and then ***Right-Mouse-Button*** click in the canvas to access all the available drafting and dimensioning commands. For more information on dimensioning, see ***Help - Documentation***.

Drill Customization Spreadsheet

Manufacture – Customize Drill Table



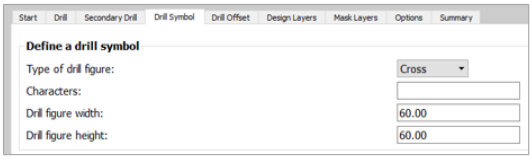
This form allows you to add/customize drill symbols and tolerances. All resulting overrides will appear in blue. The fields in gray are not editable.

The option buttons across the bottom are:

- **Validate** - Flags duplicate drill Symbol Figures or Characters used for different hole sizes. The first error cell it finds will turn red for the first detected hole. Subsequent error cells with duplicate symbols will turn red and display the number of the first hole with the same symbol. Yellow in the error cell flags drills whose entire definition is identical. In that case you can choose ***Merge*** into one.
- **Merge** - Combines drills with common definitions into one entry. The quantity will update for the first duplicate hole.
- **Reset to design** - Ignores any changes and resets the information to the current padstacks.
- **Reset to library** - Ignores any changes and resets the information to the current library padstacks.
- **Auto generate symbols** - Clears existing symbol definitions for drills and slots and automatically generates new ones. These are modifiable.
- **Write report file** - Saves to a file using Comma Separated Value (**`.csv`**) or HTML format. If you save to a **`.csv`** file, the filename is **`drill_customization.rpt`**, which can be opened in Microsoft Excel. If saved to an **`.html`** format, the filename is **`drill_customization.html`** which is in a web-ready report.
- **Library drill report** - Displays a read-only spreadsheet detailing the drill information for all available library padstacks.

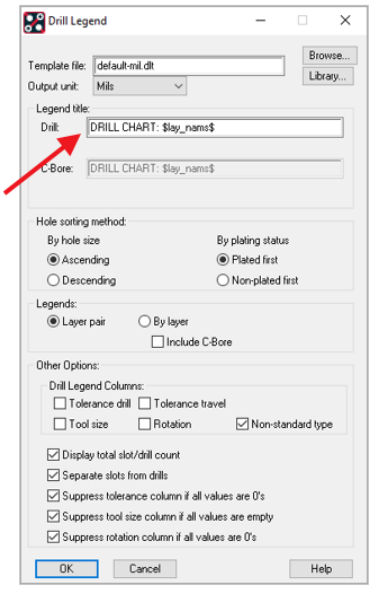
Drill Symbols and Legend Table

Manufacture – Create Drill Table



Drill definitions displayed in table are based on either the padstack definition or the customization in the Drill Customization form

Legend title is based on the layer pair combinations



If fields, such as Tolerance, are all set at 0, the table will suppress that column

DRILL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILS			
FIGURE	SIZE	PLATED	QTY
⊕	13.0	PLATED	401
◇	31.0	PLATED	12
+	38.0	PLATED	122
△	75.0	PLATED	8
□	110.0	NON-PLATED	5

The PCB Editor's ***Drill Legend*** command automatically creates a drill legend containing the drill drawing information. Fill out the ***Drill Legend*** form and select the ***OK*** button.

In the Drill Legend form you can specify a `.dlt` drill legend template file where you can tailor the drill legend to suit your needs.

In addition to a ***Layer Pair*** or ***By Layer*** type of drill legend you can enable the ***C-Bore*** option to create counter bore legends Layer pair and By Layer legends are mutually exclusive, creating one type removes the other if it exists in the design.

- For each ***Layer Pair*** drill legend, for boards with through-hole and blind/buried drill requirements, an **NCLEGEND-<*L1*>-<*L2*>** subclass automatically generates whether the subclasses are visible or not, where <*L1*> and <*L2*> are the layer numbers of the drilled layers. Each subclass includes all holes for that layer pair. Slot hole figures display at the true hole geometry and size, including user-specified characters. Tolerance values display in one column, as +<*value*>/-<*value*>.
- For ***By Layer*** drill legends, an **NCLEGEND-BL-<*L1*>-<*L2*>** subclass generates on the ***MANUFACTURING*** class, where ***-BL*** indicates ***By Layer*** drilling and a groups legend graphics as **DRILL_LEGEND_BL_<*L1*>_<*L2*>**.
- The ***counter bore/counter sink*** are based on which side of the board the pins are on. For counter bore/counter sink legends, **an NCCOUNTERDRILL-<*L1*>** subclass generates on the ***MANUFACTURING*** class and groups legend graphics as **DRILL_LEGEND_CT_<*L1*>** in which <L1> indicates the layer number.

Note The NCLEGEND subclass combines the former NCDRILL_LEGEND and NCDRILL_FIGURE subclasses for multiple layer drills and is automatically visible when generated.

IMPORTANT

Drill Legend data is not updated dynamically. Changes to the database that involve the addition or subtraction of drills require regeneration of the legends.

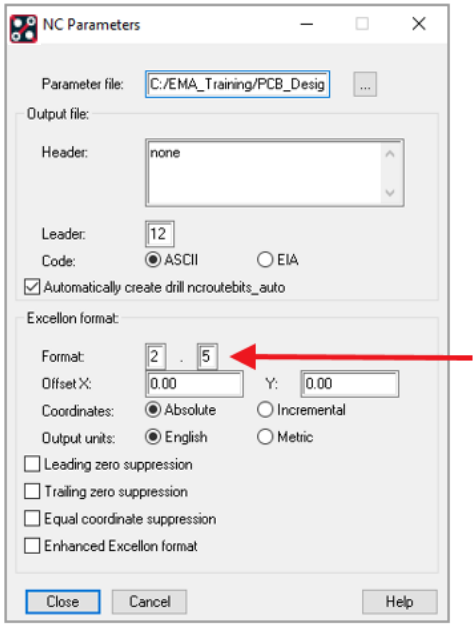
When you create a drill size that references more than one set of tolerances at the padstack level, the drill legend can separately output the drill data for the padstack with the same drill size and plating but different tolerances.

Other options:

- **Drill Legend Columns** – Choose to display drill legend columns based on Tolerance drill, Tolerance travel, Tool size, Rotation, and Non-standard drill type
- **Display total slot/drill count** – Choose to display the total number of slots and drills
- **Separate slots from drills** – Choose to generate legends for drills separately
- **Suppress tolerance column if all values are 0's** – Choose not to display tolerance column if all values are 0's
- **Suppress tool size column if all values are empty** – Choose not to display tool size column if all values are nil
- **Suppress rotation column if all values are 0's** – Choose not to display rotation column if all values are 0's

The NC Parameters File

Export - NC Parameters



NC Parameters form can be accessed as a stand-alone from *Export – NC Parameters* or clicking the *NC Parameters* button in the *NC Drill* form

If accessed from the *NC Drill* form, when closing this form it will return to the *NC Drill* form

Format should match the format settings in the artwork parameters

In order to generate a drill file for manufacturing, you must have a parameter file (`nc_param.txt`) that specifies the format of the drill coordinate data. To set the ***NC Parameters*** for the drill coordinate data, select ***Export - NC Parameters*** from the top menu or select the ***NC Parameters*** button in the ***NC Drill*** form. The ***Parameter File*** field specifies the path and the output text file name. The default is **`nc_param.txt`**.

Note If you had accessed the NC Parameters form from the NC Parameters button in the NC Drill form, it will automatically return you to the NC Drill form.

Output file

- **Header** - Specifies one or more ASCII headers in the output file. The default is none.
- **Leader** - Specifies the leader length.
- **Code** - Specifies the output format. The default is ASCII.

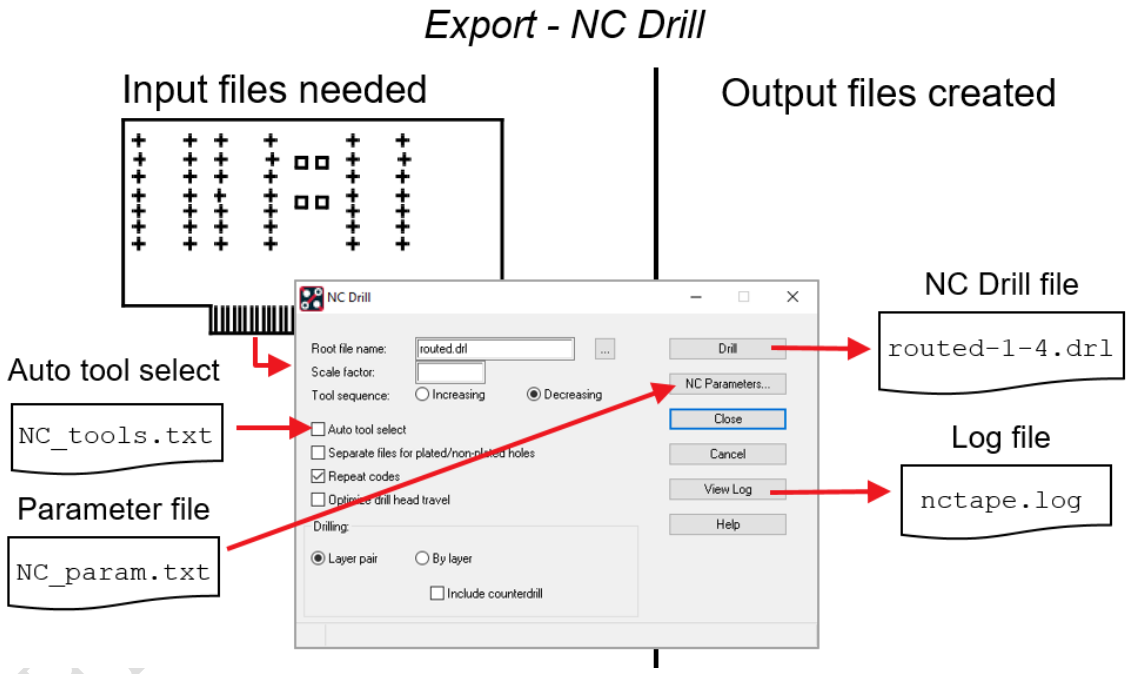
Excellon format

- **Format** - Format for coordinate data in the output NCDRILL file. The default is 2.5.

Note The format settings should match the integers and decimal place format settings in the Artwork Control Form's General Parameter tab.

- **Offset X, Y** - Specifies an offset from the drawing origin for the coordinate data.
- **Coordinates** - Specifies whether the output coordinates are incremental or absolute.
- **Output Units** - Specifies whether the output units are English or Metric. The default is English.
- **Leading Zero Suppression** - Specifies whether the output coordinates are padded with leading zeros.
- **Trailing Zero Suppression** - Specifies whether the output coordinates are padded with trailing zeros.
- **Equal Coordinate Suppression** - Specifies whether equal coordinates are suppressed. The default does not suppress equal coordinates.
- **Enhanced Excellon format** - Chooses to generate a header in NC Drill and NC Route output files that more fully uses Excellon commands.

Generating an NC Drill File



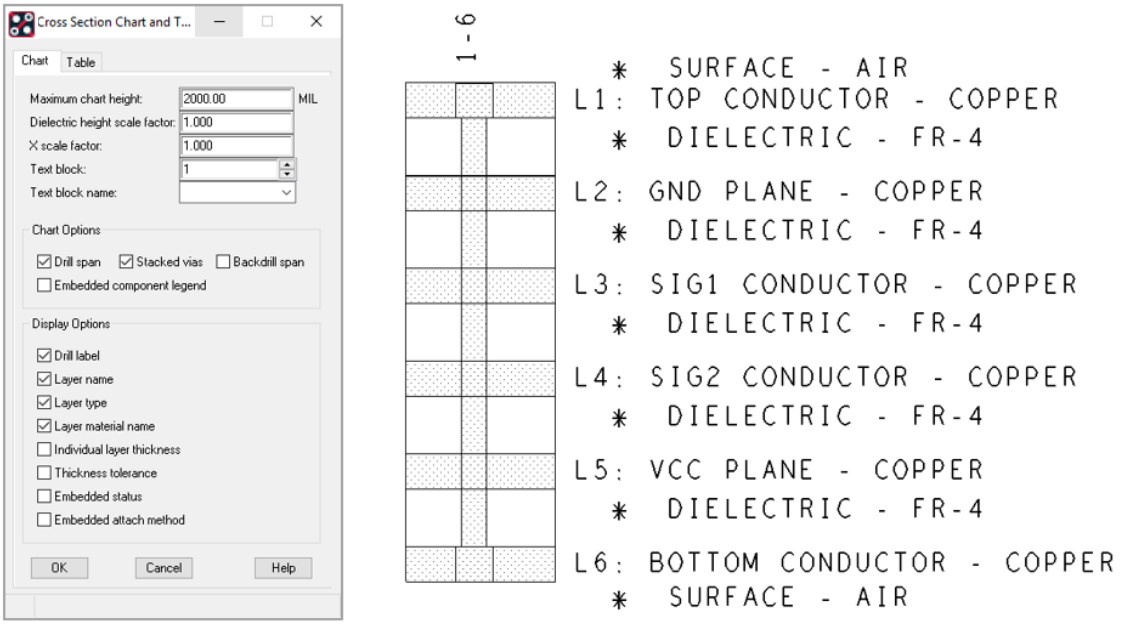
If you are generating drill data for a machine that is able to automatically perform its own drill bit selections, you will also need an `nc_tools.txt` file. PCB Editor searches the NCDPATH you specify the environment file (*env*) to locate these files.

To create a drill file, select ***Export - NC Drill*** from the top menu.

- **Root file name** - You have the option to change the default, which will give the two drilled layers.
- **Scale factor** - This value specifies that all the drill locations are scaled in the output file.
- **Auto tool select** - Specifies whether the drilling machine has an automatic tool changer. If this field is not checked, the drill pauses for manual tool changes (default). If the field is checked, you will need to create an `nc_tools.txt` file.
- **Separate files for plated/non-plated holes** - Will output to two different files if checked.
- **Repeat codes** - Specifies whether your drill supports repeat codes.
- **Optimize drill head travel** - Optimizes drill travel on the NC Drill output files. The log file shows the parameters that were used to create the drill data, a summary of drill sizes and quantities, and any warnings or errors.

Creating the Cross-Section Chart

Manufacture – Cross Section Chart

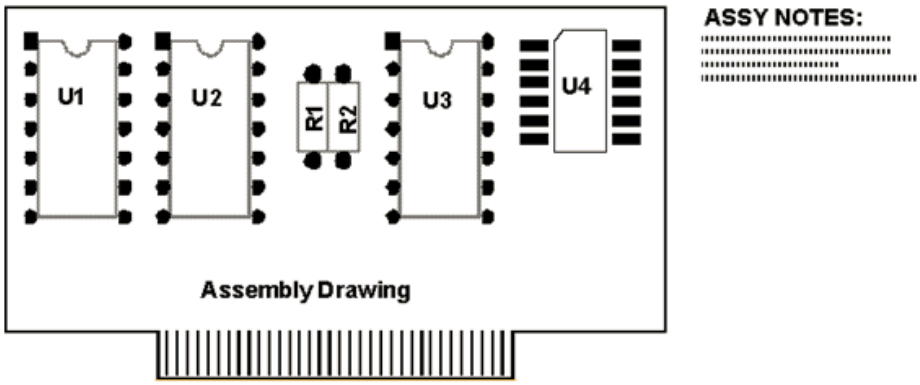


To create a ***Cross Section Chart***, select ***Manufacture – Cross Section Chart*** from the top menu. Use this command to generate a cross section chart displaying the drill span, stacked vias, embedded component legend, and layer information. The chart is generated and placed at a desired location specified by the user. Any regeneration of the chart will use the last saved chart placement.

Settings are:

- **Maximum chart height** - Specify the total height of the cross-section chart in Allegro units
- **Dielectric height scale factor** - Controls the dielectric size as displayed in the cross-section chart. By default, this value is 1.0.
    - If the user wants to make dielectric layer thinner to save space, this value can be set to small decimal number, such as 0.5.
- **X scale factor** - Controls the size of the chart along the x-axis. By default, the value is set to 1. To reduce the width of the chart, you can specify the values less than 1.
- **Text Block** - Use this field to specify the size of the text displayed in the cross-section chart.
- **Chart Options** - Use the options in this section to specify the information to be included in the cross-section chart.
    - **Drill span** - Select this to display the drill span -- includes pin and the 'via' span.
    - **Stacked Vias** - Select this option to display the stacked vias.
    - **Embedded component legend** - Select this to display the embedded components placed on internal PCB layers.
- **Display Options** - Lists the layer information that can be included in the cross-section chart.
    - **Drill label** - Select this option to display the 'via' span labels for single vias. This information is displayed only when the Drill span option is selected.
    - **Layer name** - When selected, displays the layer names, such as TOP, BOTTOM, SIG_1 and so on.
    - **Layer type** - Select this to display the layer type for each layer -- as specified in the Layer Cross Section dialog box.
    - **Layer material name** - When selected displays the material used for each PCB layer. This is same as the information displayed in the Material column of the Layer Cross Section dialog box.
    - **Individual layer thickness** - Select this to display the layer thickness in Allegro units.
    - **Embedded Status** - Displays the Embedded status of the layer as specified in the Embedded Layer Setup dialog box.
        - Supported values are:
          NOT_EMBEDDED
          BODY_UP
          BODY_DOWN
          PROTRUDING_ALLOWED
    - **Embedded attach method** - Displays the method used to attach embedded components to the internal layer. This information is available only for layer with embedded status set to BODY_UP or BODY_DOWN.
        - Supported values are:
          INDIRECT_ATTACH
          DIRECT_ATTACH

Creating Assembly Drawings



If you started your layout from a template design file, you already have a drawing border (A-D size format symbol), as well as format symbols for assembly notes.

You are now ready to create a plot file for the assembly drawing. Like the photoplot process, what you see in the work area is what is included in any plot file. The various format symbols (like assembly notes) need to be created with this in mind. For example, when you create an ASSY_NOTES format symbol (with the Symbol Editor), use a layer for the graphics such as Board Geometry/Assembly_Notes.

When you need to create a plot file for the assembly drawing, toggle the appropriate layers in the layout drawing to make only the assembly-related data visible. To set visibility, select ***Setup – Colors*** from the top menu.

For assembly drawings, you will need to toggle the appropriate layers to display package outlines, reference designators, pins, and so forth. You can also include mechanical symbols for extractors and other mounting hardware.

To create a plot, select ***File - Print***.

Labs

Lab 13-3: Creating Fab and Assembly Drawings

- Generate drill symbols and a drill legend for the fabrication drawing
  - Define drill symbols and legend
  - Create fabrication drawing
  - Create assembly drawing

Lab 13-4: Creating an NC Drill File

- Output a drill file used to drill the board holes during manufacturing

Lab 13-3: Creating Fab and Assembly Drawings

Objective: Generate drill symbols and a drill legend for a fabrication drawing.

Objective: Create fabrication and assembly drawings to provide documentation.

Opening the Final Design File

1. You will be using **`final_mfg.brd`** from the previous lab.

Setting Visibility

In order to generate drill symbol and legend information, you must make all pins visible. Drill symbols and legend information for routing vias are also generated, but they do not need to be visible. In this section, you will turn on the visibility for all pins and vias.

2. Choose ***Setup - Colors*** from the top menu to open the ***Color Dialo****g* form.
3. Select the ***Global Visibility 'Off***' button field to make invisible all classes and subclasses.
4. Expand the ***Geometry*** category and select the ***Board Geometry*** class.
5. Turn '***ON***' the ***Design_Outline***, and ***Dimension*** subclasses.
6. Select the ***Drawing format*** category and turn '***ON***' all items in that class by selecting the '***All***' box.
7. Click ***OK*** to close the ***Color Dialog*** form.
8. Select ***Display - Zoom - World*** from the top menu.
9. You can zoom in around the drawing format if you wish.

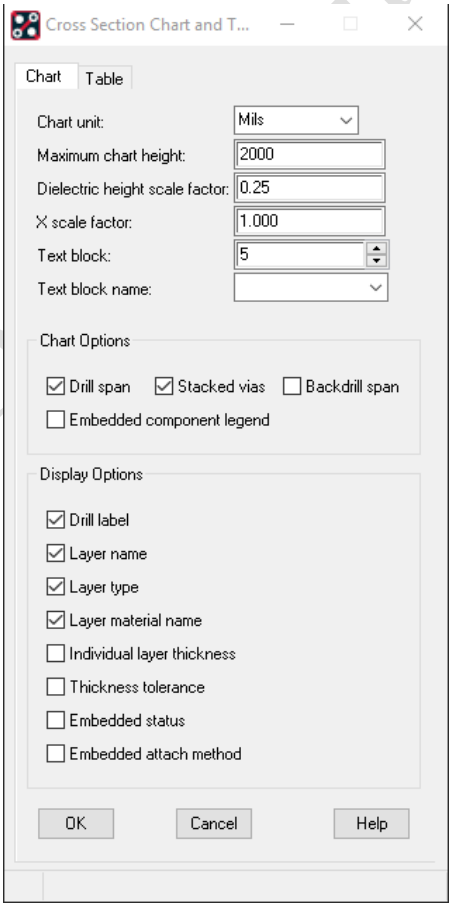
Creating Drill Symbols and Legend

1. Select ***Manufacture – Customize Drill Table*** from the top menu.
   The ***Drill Customization*** form appears.
2. Click on the ***Validate*** button in the lower left of the form.
   The message ***No validation errors detected*** appears in the command window.
3. Click ***OK*** to dismiss the form.
4. Select ***Manufacture – Create Drill Table*** from the top menu.
   The ***Drill Legend*** form appears.
5. Accept the defaults and click OK.
   When processing is complete, a rectangle appears attached to your cursor, and the PCB Editor's message area prompts you to pick a location for the legend.

6. Place the legend to the right of the board, within the format drawing.
7. Take a look at the Drill Legend you placed. It is a drill chart for the pins that traverse from the Top layer of the board to the Bottom.
   If you were working with blind or buried vias, a different drill chart would appear for each legal layer combination. Also note the drill symbols in your design representing the through holes.
8. Choose ***File - Save*** from the top menu.
   A window appears and warns you that the **`final_mfg.brd`** file already exists. It asks if you want to overwrite the file.
9. Click '***Yes***' to confirm the file overwrite.
   The file **`final_mfg.brd`** is written to disk.

Creating the Cross-Section Chart for the Fab Drawing

1. Select ***Manufacture - Cross Section Chart*** from the top menu.
2. Set the ***Cross Section Chart*** form to the following settings.



3. Click ***OK***.

A box will appear on your cursor.

4. Place the box to the right of the board outline, above the Drill Legend.
5. In the ***Options*** tab, set the ***Active Class*** to ***Drawing Format*** and ***Active Subclass*** to ***Title_Data***.
6. Choose ***Edit - Text*** from the top menu.
7. In the PCB Editor's work area, click on the ***COMPANY NAME*** text in the title block (lower right corner of the drawing format), and type in your own company name to replace the current text.
   When editing text in PCB Editor you are always in ***Overstrike mode***.
   If your company name is not long enough to replace the current text, you may use the ***Space Bar*** to remove the rest of the previous text.
8. Right-click and choose "***Done***".

Creating an Assembly Drawing

1. Choose ***Setup - Colors*** from the top menu to open the ***Color Dialo****g* form.
2. Turn ***'Off' Global Visibility***
3. Expand the ***Geometry*** category and select the ***Board Geometry*** class.
4. Select the ***Geometry*** category and turn '***On***' the ***Assembly_Notes*** and ***Design_Outline*** subclasses in the ***Board Geometry*** Class
5. Then, in the **Package Geometry** class, turn '***On***' the ***Assembly_Top*** subclass.
6. Expand the ***Stack-Up*** category and select the ***Conductor*** group, turn '***On***' the ***Pin/Top*** class/subclass.
7. Select the ***Components*** category, turn '***On***' the ***Ref Des/Assembly_Top*** class/subclass.
8. Select the ***Drawing format*** category and turn '***ON***' all items in that class by selecting the '***All***' box.
9. Click ***OK*** to close the ***Color Dialog*** form.
   The assembly drawing information is now visible.
10. Select ***Display - Zoom - World*** to display the entire drawing format.

End of Lab

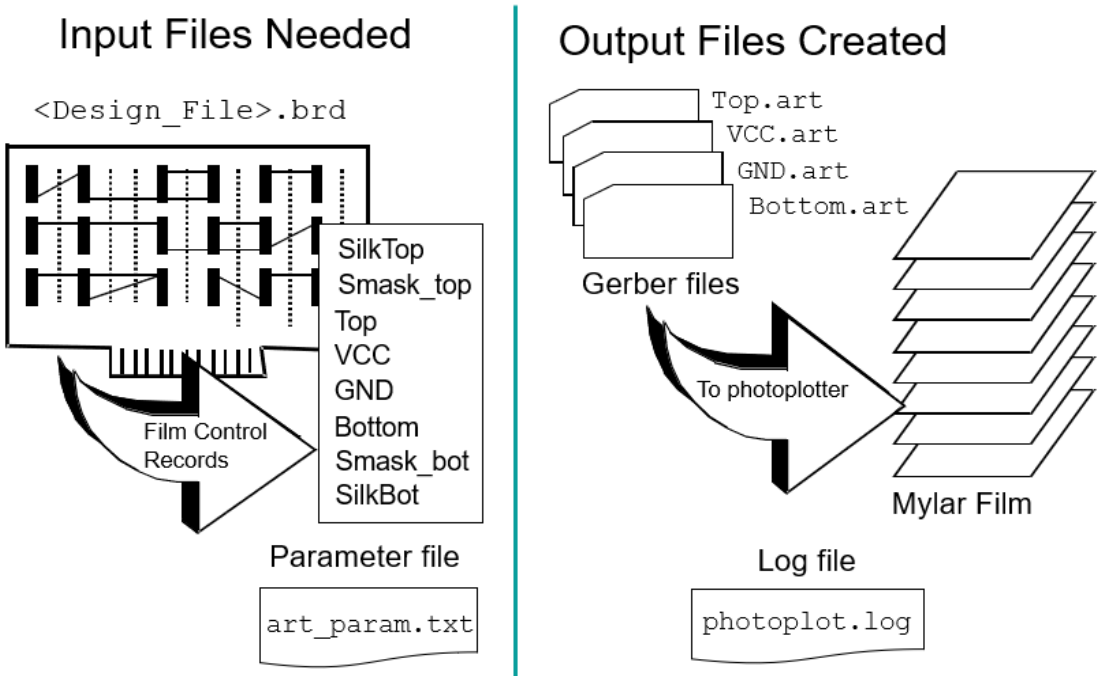
Lab 13-4: Creating an NCDRILL File

Objective: Create a drill file used to drill the holes during manufacturing.

1. Select ***Export - NC Parameters*** from the top menu.
   An ***NC Parameters*** form appears.
2. In the ***Excellon format*** section, verify that the ***Format*** is set to ***2.5***.
3. Click ***Close***.
   The parameters are written to a file called **`nc_param.txt`**.
4. Select ***Export - NC Drill*** from the top menu.
5. An ***NC Drill*** form appears.
6. Click ***Drill*** to start the file creation process.
7. Click ***Close***.
   Since the drill data is extracted from the `final_mfg.brd` board file, the drill file will be named **`final_mfg-1-4.drl`** and written to disk.
8. If you have time, use the File Manager or a viewer of your choice to view the `release-1-4.drl` file.
9. Choose ***File - Viewlog*** to view the **`ncdrill.log`** file that was created.
   The log file displays format information, as well as hole size and quantity data.
10. Click the ***Close*** button in the log file window to close the window.
11. Choose ***File - Save*** from the top menu.
    A window appears and warns you that the **`final_mfg.brd.`** It asks if you want to overwrite the file.
12. Click ***"Yes"*** to confirm the file overwrite.
    The file **`final_mfg.brd`** is written to disk.

End of Lab

Generating Artwork



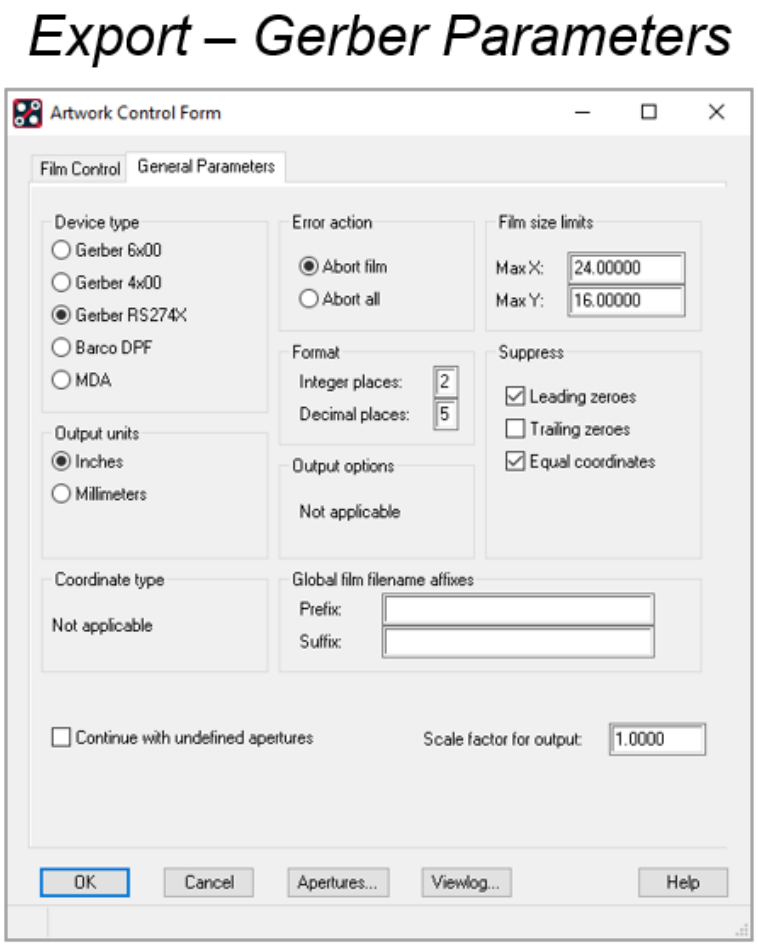
Artwork files, or Gerber files, are some of the most important items required to manufacture a printed circuit board. The following items and files must be created in order for PCB Editor to generate the artwork files.

First, **Film Control** records must exist within the PCB Editor design. The records identify the artwork routine where all of the data resides for each artwork file. Note that these records are stored internally in the data base and not in a file on disk.

Second, the file *art_param.txt* must exist. This file contains the parameters used when creating artwork and must be sent to the board fabrication vendor along with the artwork files themselves.

With the preceding items defined, PCB Editor can create artwork files for the design. The artwork file names created by default will be the film control record name appended with `.art`. Along with the artwork files, a log file titled `photoplot.log` will be created. It is very important to check this log file to ensure all artwork files have been created successfully.

Artwork Control Form - General Parameters Tab



You can directly access the ***General Parameters*** tab of the ***Artwork Control Form*** by selecting ***Export – Gerber Parameters*** from the top menu. The ***General Parameters*** form displays the default settings if no **`art_param.txt`** file exists in your ***ARTPATH*** variable (in the *env* file). To control artwork parameters for all users, set the ARTPATH variable to the location of an existing **`art_param.txt`** file.

The options available will change based upon which format you have selected.

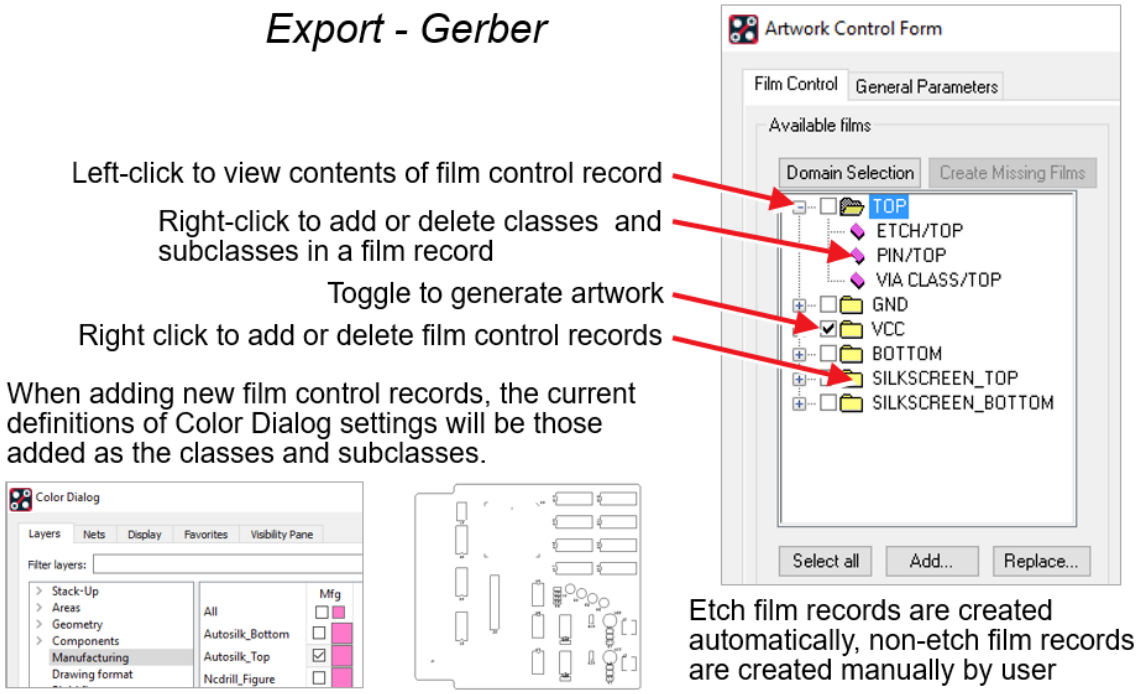
- **Device Type -** Specifies the Gerber format to be used (default is Gerber RS274X).
- **Error Action -** Specifies the action taken when an error is found during processing (such as an undefined aperture). All errors are written to the log file.
- **Film Size Limits** - Specifies the dimensions of the film used by the photoplotter. This is not really an issue anymore.
- **Format** - Specifies the number of integer places and decimal places in the output coordinates (range is from 0 to 5). Gerber format should reflect your design accuracy settings. For example, if design units are mils, and accuracy is set to 1 (sub-mil values), then make your Gerber format accurate to a minimum of four decimal places (output is in inches).

Caution

When outputting to a raster format, be sure the **Format** is set one place greater than the **Drawing Accuracy**. Example: Database Units = Mils, Accuracy = 1; Artwork Format = 2.5. If the format is not set properly, it could cause problems with inaccurate arc coordinates in the artwork files and possible shape/void plotting failures.

- **Suppress** - Controls whether the PCB Editor tool writes leading or trailing zeroes, or equal coordinates in the Gerber data file. You cannot suppress both leading and trailing zeroes. Selecting Equal Coordinates reduces the size of the final Gerber data file.
- **Output Units** - Specify the output units as either inches or millimeters. Inches should be used for English unit boards, and Millimeters should be used for metric unit boards. You should always output the Gerber files in the same format as your design.
- **Global film filename affixes** - Allows you to change the name of the Gerber files.
    - **Prefix** field - Adds a user-defined, case-sensitive string before generated film filenames on a board-level basis. For example, if you entered a string of ABC_, the output Gerber file names would be ABC_TOP.art, ABC_BOTTOM.art, etc.
    - **Suffix** field - Appends a user-defined, case-sensitive string after generated film filenames on a board-level basis. For example, if you entered a string of _DEF, the output file names would be TOP_DEF.art, BOTTOM_DEF.art, etc. If you wish to change the extension from .art, you can use the ***ext_artwork*** environmental variable available in the ***User Preferences Editor***, under the ***File Management/Versioning*** category.
- **Continue with undefined apertures** - Tells the PCB Editor program what to do when it cannot find a definition for a flash aperture in the padstack.
- **Scale Factor for Output** - Scales all entries in the Gerber file.

Artwork Control Form - Film Control Tab



The film control records define the artwork files that will be created, as well as the contents of those artwork files. The film control records are stored internally in the PCB Editor design. The Film Control folder tab is where you specify the film control records. The first time you access this form, the system will have automatically created one film control record for each ***etch*** subclass of the design.

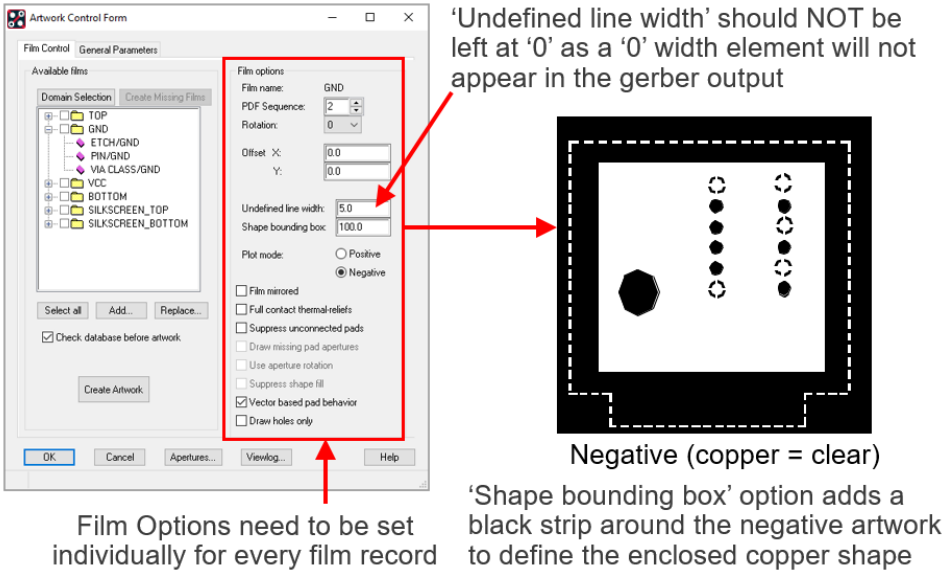
Each etch film control record will contain the classes Etch, Pin and Via for that subclass. To see the class and subclass pairs that are defined for a film control record, select the plus sign to the left of the film control record name.

To add a subclass to a film control record, select any current class/subclass pair within the film control record with the ***Right-Mouse-Button*** and select ***Add*** from the pop-up menu. You will be prompted to enter the name of the new class/subclass to the film control record. After you choose the new subclass, select ***OK***. The new subclass is added.

To create a new film control record, open the ***Color Dialog*** form and make visible all of the class/subclass pairs required for the artwork. Right-click on an existing film control record and select ***Add***. The class and subclass pairs that are currently visible will be the contents of the new film control record.

To delete a film control record, select the name of the film control record with the ***Right-Mouse-Button*** and select ***Cut*** from the context-sensitive menu.

Artwork Control Form - Film Options

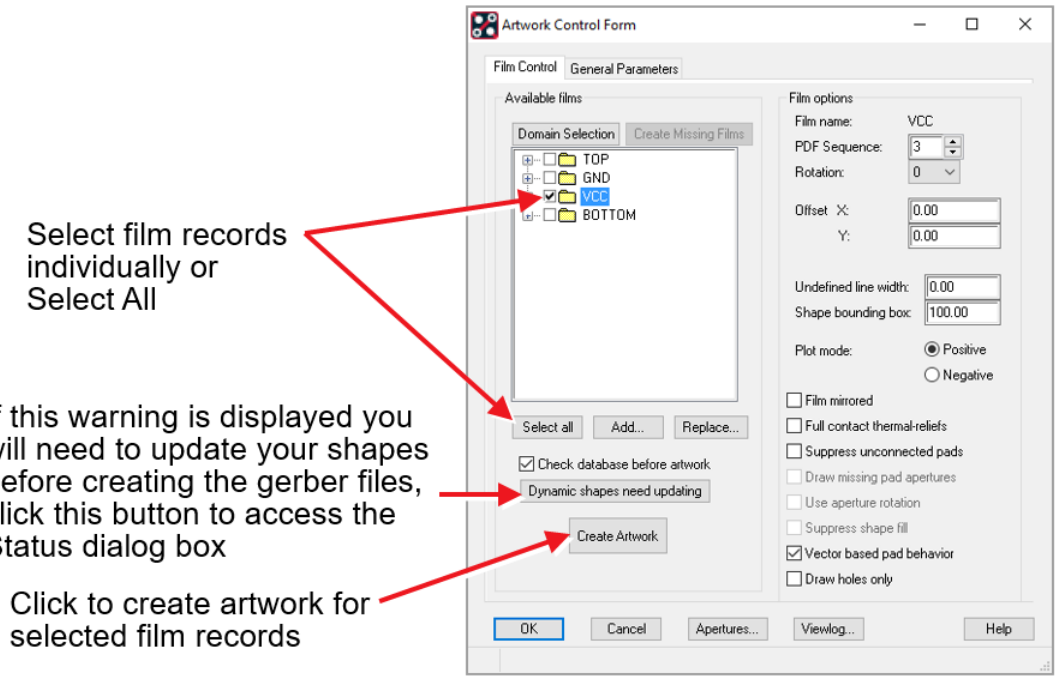


The Film Options form further describes each film control record. View film options for a film control record by selecting the film control record name with the Left-Mouse-Button.

- **Film name** - Displays the artwork data file name.
- **PDF Sequence** – Allows you to control the order of films in a PDF output. The PCB Editor auto-numbers the films but you can override the order.
- **Rotation** - Specifies in degrees the rotation of the plotted film image.
- **Offset X Y** - Shifts the positions of the photoplot coordinates. You can enter positive or negative values in these fields.
- **Undefined line width** -Specifies the photoplotted width of any line that has a zero width in the PCB Editor layout (for example, text, assembly, and silkscreen lines).
- **Shape bounding box** - Applies to negative planes only. Adds a 100-mil (default) outline around the negative shape edge to define a wide border.
- **Plot mode** - Specifies positive or negative artwork. This should always be set to positive except for negative planes.
- **Film mirrored** - Mirrors the artwork about the Y axis.
- **Full contact thermal-reliefs** - Specifies no thermal relief flash for pins and vias with negative planes.
- **Suppress unconnected pads** – Prevents the plotting the pads of pins and vias that have no connections (for flashing "used pads only" on inner layers).
- **Draw missing pad apertures** - Substitutes another aperture in the aperture list and uses it to draw the pad. This feature will not resolve missing flash names. This button does not appear in raster-based parameter forms. Available for Gerber 6x00 and 4x00 only.

- **Use Aperture Rotation** - Means that the Gerber data can use apertures in the aperture list that have rotation information defined for them (for example, flash names). This button does not appear in raster-based parameter forms. Available for Gerber 6x00 and 4x00 only.
- **Suppress shape fill** - Specifies that areas outside the shapes and all voids are not to be filled on a negative film. You must replace the filled areas with separation lines. Used for negative nested shapes. Available for Gerber 6x00 and 4x00 only.
- **Vector based pad behavior** - Specifies that raster artwork use vector-based decisions to determine which type of pad to flash.

Artwork Control Form - Generating Gerber Files



After you have specified the artwork parameters, generated an aperture list (if required), and created all artwork film control records, you should be ready to create your artwork files. However, if the ***Dynamic shapes need updating*** button is displayed then your dynamic shapes need to be updated prior to creating the artwork file. Clicking on this button will take you to the ***Status*** dialog box (discussed earlier in the lesson) where you can run the ***Update to Smooth*** function to bring your shapes up-to-date.

To identify which artwork files should be generated, either select the ***blank box immediately to the left of the film control record name*** for each artwork file to be created or choose the ***Select All*** button to have all artwork files generated. Select the ***Create Artwork*** button to create the artwork files.

Note Remember, all artwork files will be created on disk with a file name of the film control record name, appended with the string `.art`. Also, remember to check the log file `photoplot.log`.

Labs

Lab 13-5: Creating Artwork Files

- Set up the design file for artwork
  - Set up artwork general parameters
  - Import FILM_SETUP.txt file
  - Create new film control records for Pastemask_Top and Pastemask_Bottom
  - Generate the manufacturing Gerber files

Lab 13-5: Creating Artwork Files

Objective: Using a completed board that has passed all the tests and is ready for manufacturing, you will set up the design file to produce artwork.

In this lab, you will learn how to define the artwork layers required for photoplotting a design. You will learn about parameter and film record files that are used to create the photoplot files.

Setting Up the Artwork General Parameters

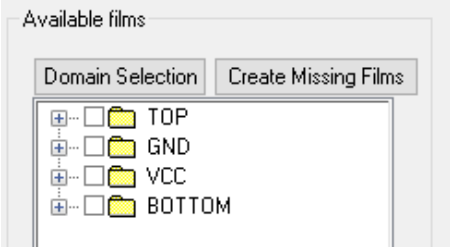
1. You will be using **`final_mfg.brd`** from the previous lab.
2. Choose ***Export – Gerber Parameters*** from the top menu.
3. You might get a message about the artwork output type set while creating your dynamic shapes. We will take care of that. Click ***OK***.
4. You might get a message about the resolution of the database vs. artwork output. We will take care of that as well. Click ***OK***.
5. The ***Artwork Control Form*** opens to the **General Parameters** tab.
   This tab specifies the plotter type, film size, and format of the manufacturing data.
6. You will create Gerber files in the ***RS274X*** format (the Default).
   This should take care of the output type message.
7. The default ***Format*** option is set to:
   Integer Places: 2
   Decimal Places: 5

   This should take care of the resolution message.
8. Click ***OK*** to close the form.
   When you close the ***Artwork Control Form***, the parameter settings will be written to a file called **`art_param.txt`** in the working directory.

Checking existing Film Control records

By default, the PCB Editor software will create a film control record for each of the ***etch*** subclasses in the design as long as you set up the etch layer in the ***Layout Cross-Section*** form before opening the ***Artwork Control Form***.

Note If you add new etch layers after you have opened the Artwork Control form, open the Artwork Control form and click on the '***Create Missing Films***' button above the existing film records. This will automatically add the new ***etch*** film records.



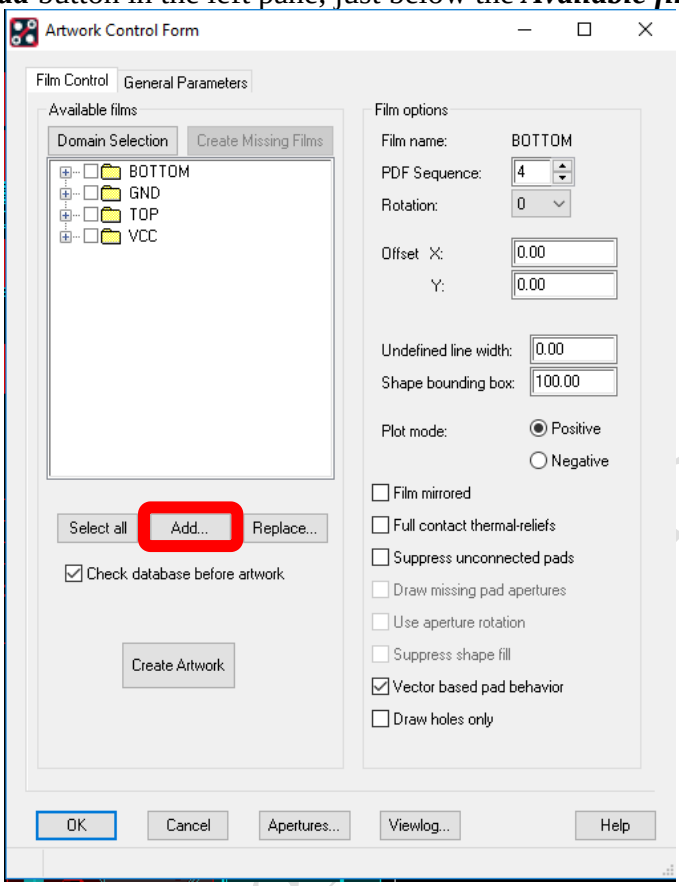
1. Select ***Export - Gerber*** from the top menu.
2. The ***Artwork Control Form*** opens to the ***Film Control*** tab.
   This tab specifies which artwork files are to be created and which objects in the PCB Editor database constitute each artwork file. Notice that, by default, for this design there are four entries in the ***Available Films*** window of the ***Film Control*** tab. There is one entry for each of the ***etch subclasses*** of your design.
3. Select the ***plus + sign*** to the left of the ***BOTTOM*** entry in the ***Available Films*** window of the Artwork Control form.
   The BOTTOM film record expands to display the class/subclass entries that will be included in the manufacturing file for this artwork film. By default, the PCB Editor software includes the ETCH, PIN, and VIA class for each of the etch layers.
4. Select the ***BOTTOM*** film record in the ***Available Films*** window (select on the word BOTTOM).
   The ***Film Options*** section on the right side of the form displays the current options set for the selected film control record.
5. In the ***Film Options*** section for the ***BOTTOM*** film record set the ***Undefined Line Width*** field to ***5***.
6. Select the rest of the film records (***GND, TOP and VCC)***, one at a time in the ***Available Films*** window and set the ***Undefined Line Width*** field to ***5*** in the ***Film Options*** section.
7. Click ***OK*** to save your settings and dismiss the ***Artwork Control Form***.

Importing a FILM_SETUP.txt file

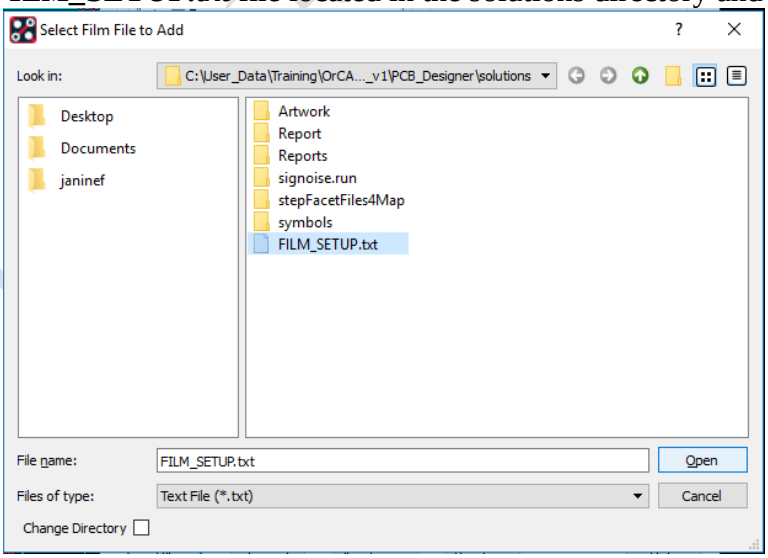
If you have a consistent layer scheme for things like your Silkscreen, Fabrication and Assembly drawings, it is possible to save those film records in a ***FILM_SETUP.txt*** file for reuse in future designs.

1. Select ***Export - Gerber*** from the top menu.
2. The ***Artwork Control Form*** opens to the ***Film Control*** tab.

3. Click on the ***Add*** button in the left pane, just below the ***Available films*** window.



4. Select the ***FILM_SETUP.txt*** file located in the solutions directory and click ***Open***.



5. Notice that the Available films window has been populated with Assembly, Fabrication, Silkscreen and Soldermask film records.
6. Click on one of the new film records and see the ***Undefined line width*** is set to 5 mil.
7. Right click on the ***FAB*** film record and select ***Display for Visibility*** from the popup.
8. Click OK to dismiss the form and see that the Fab drawing is displayed.

Creating New Film Control Records

You will also need to create artwork files for your Pastemask layers. You need to create a film control record for each of these. By default, when you create a new film control record, all currently visible classes and subclasses displayed in the PCB Editor's work area are added to the film control record.

1. Choose ***Setup - Colors*** from the top menu.
2. At the top of the form select the ***Global Visibility 'Off'*** button to make all class and subclasses invisible.
3. Select the **Geometry** category and turn '***ON***' the ***Design_Outline*** and ***Pastemask_Top*** subclasses
4. Select the Stack-Up category and turn ***'ON'*** the ***Pastemask_Top*** subclass for both the ***Pin*** and ***Via*** Classes.
5. Click ***OK*** to save your settings and dismiss the Color Dialog form.
6. Select ***Export - Gerber*** from the top menu.
7. The ***Artwork Control Form*** opens to the ***Film Control*** tab.
8. Using the ***Right-Mouse-Button*** on any of the existing film records and select ***Add*** from the pop-up menu.
   A text form opens, asking for the name of the new film.
9. Enter a name of **`PASTEMASK_TOP`** and select the ***OK*** button.
   A new film record is added. If you expand this selection you will find the class/subclass elements you made visible in the ***Color Dialog*** form have been added to the film record.
10. Follow the process we just used (Steps 1 – 9) to create the PASTEMASK_BOTTOM film record.
11. Make sure to set the ***Undefined Line Width*** field to ***5*** in the ***Film Options*** section for each of these new film records.

Saving the Design File

1. Choose ***File - Save As*** from the top menu.
2. Rename this drawing by entering the following in the File Name field:
   `final_mfg_done.brd`
   The file `final_mfg_done.brd` is written to disk.

Creating the Manufacturing Gerber Files

1. Choose ***Export - Gerber*** from the top menu.
2. The ***Artwork Control Form*** opens to the ***Film Control*** tab.
3. The check box to the left of each film control record controls whether a manufacturing file will be created for that record. Since you want to generate all artwork files, select the ***Select All*** button below the ***Available Films*** window.
4. Select the ***Create Artwork*** button.
   At the bottom of the ***Artwork Control Form*** a message will be displayed:

   ```
   Plot generated
   ```

   The Gerber format artwork files are written to your current working directory.

   If you wish, you can use the Windows Explorer command to check for these files. Each artwork file has the same extension (`top.art`, `gnd.art`, `vcc.art`, `bottom.art, etc.`). These are the plot files that are used to create the film required for manufacturing the board.
5. Select the ***Viewlog*** button at the bottom of the form to see the **`photoplot.log`** file.
   Check to make sure all artwork files have been created successfully. This is a great file to send to your vendor along with the set of artwork files.
6. Click the ***Close icon*** to exit the log file.
7. Click ***OK*** in the ***Artwork Control Form*** to close the form.

End of Lab

Creating an IPC-2581 Database

An IPC-2581 database is a neutral CAM database that can be used by fabricators and assembly vendors to manufacture your design.

It offers many advantages over traditional Gerber, NC-Drill, and IPC-356 Netlist exports.

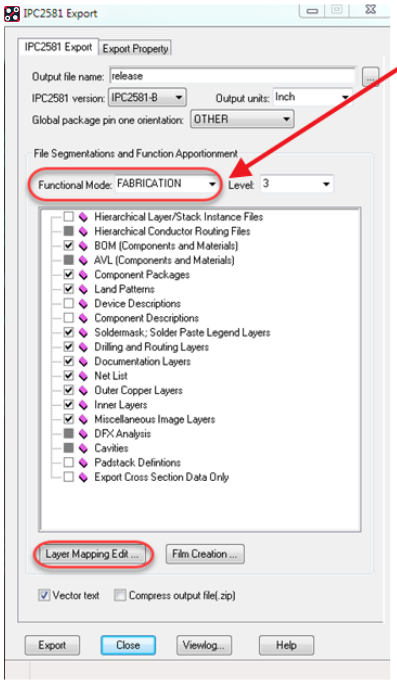
The database contains all the necessary elements consolidated into a single file.

These include:

- All CAD database artwork films
- Design Stackup
- NC-Drill Data
- CAD netlist
- Component and Net Properties

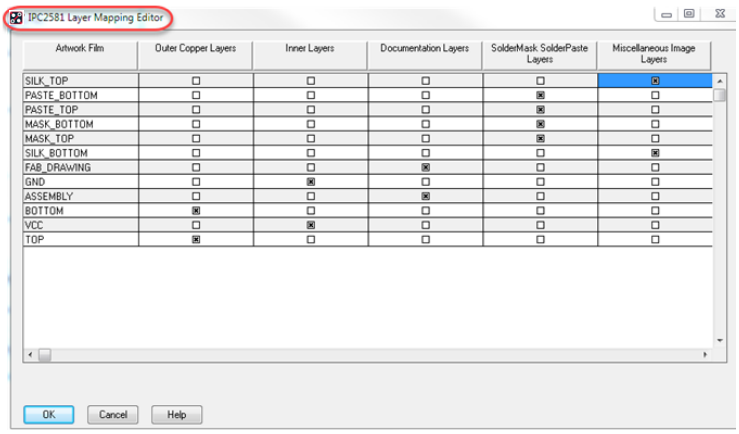
- Additional benefits include reduced or waived NRE tooling costs
- Information about the IPC-2581 consortium can be found at: http://www.ipc2581.com

Export - IPC-2581



Various functional modes allows the user to tailor the output database for fabrication, assembly, test, etc.

IPC-2581 Layer Mapping Editor allows for definition of copper layers, mask and paste layers, and documentation layers



Note Film records need to be setup prior to exporting any manufacturing data (ie; IPC-2581 data, Gerber files, ODB++, etc.)

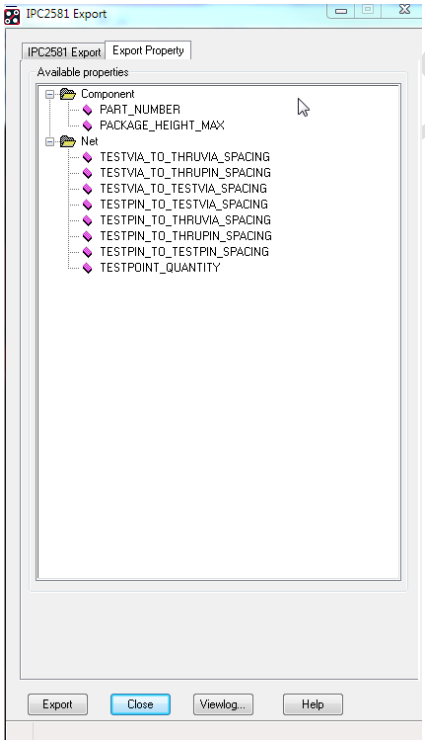
The options for IPC-2581export are:

- IPC2581 Version – Supported versions are IPC2581-B, IPC2581-A, IPC2581-1
- Output Units – Inch, Millimeter, Micron
- Global package pin one orientation – Other, Lower_Left, Upper_Left, Left, Upper_Center, Left_Center
- Functional mode – User defined, Design, Fabrication, Assembly, Test
- Level – Specifies the data complexity of the IPC2581 file needed for each functional mode. Supported levels 1, 2, 3
- Layer Mapping Edit – Allows user to map copper layers, document layers, mask and paste layers
- Film Creation – gives you access to film record setup to define film artworks
- Vector Text – Select to export the text characters as line segments
- Compressed output – Allows the option of creating a compressed zip file of the IPC2581 database

Optional IPC-2581 Export Properties:

- Component properties
- Net properties

Here is an example of some sample component and net properties that were added:



Labs

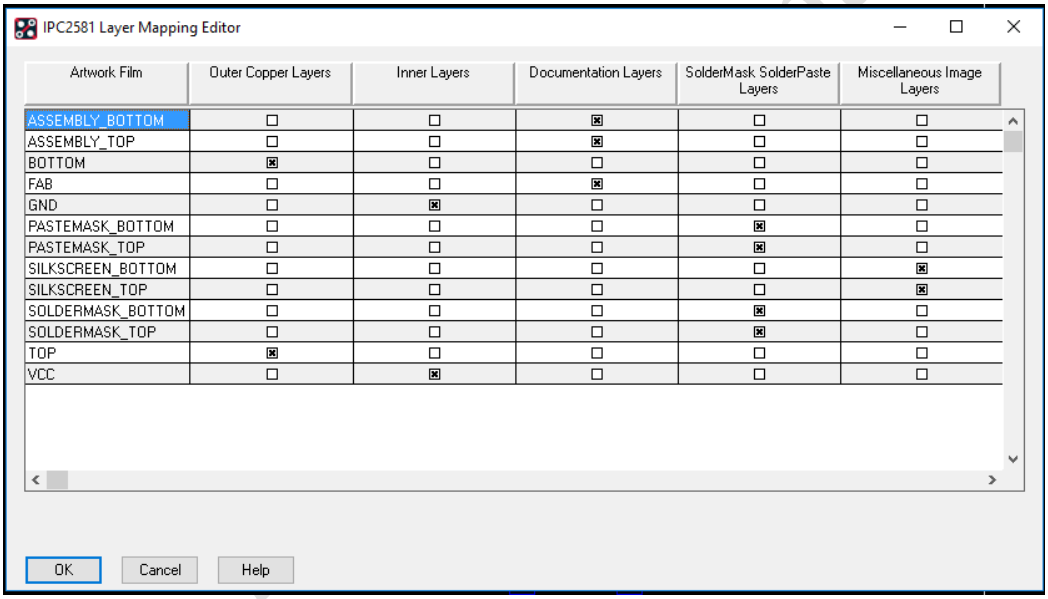
Lab 13-6: Creating an IPC-2581 Manufacturing Database

- Generate an IPC-2581 database for manufacturing your board design
  - Setup of functional modes
  - Setup layer mapping for layer types

Lab 13-6: Creating an IPC-2581 File

Objective: Create an IPC-2581 database used in manufacturing the PCB.

1. You will be using the **`final_mfg_done.brd`** from the previous labs.
   If you did not finish the previous labs, a copy of **`final_mfg_done.brd`** may be found in the **solutions** folder.
2. Select ***Export – IPC-2581*** from the top menu.
3. Set IPC2581 version to "IPC2581-B", output units to "Inch".
4. Global package pin one orientation should be set to "Other".
5. Set ***Functional Mode*** to "Fabrication" Level "3".
6. Select Vector text
7. Next select ***Layer Mapping Edit*** and map the layers to the following:



8. Next select export to create the IPC-2581 database, the resulting file will be ***release.xml***.
9. Select ***Close*** to dismiss the form.

End of Lab

Note This database can be imported into the PCB Editor for comparison review

Here are several free viewers for IPC-2581 data:

- Wise Software Solutions - Wise 2581 Viewer
- Downstream Technologies - VU2581Viewer
- PCB – Investigator V8 - IPC2581 PCB Investigator Viewer

Links for the viewers are available on the IPC-2581 Consortium website
http://www.ipc2581.com/index.php/ipc-2581-free-viewers

Appendix A: Preselection Mode

Creating a Selection Set

Mouse Action	Result
LMB pick (single select)	Clears previous selection set and adds highlighted element at the mouse location to the selection set.
Shift + LMB pick (extend select)	Adds highlighted element at the mouse location to the selection set.
Ctrl + LMB pick (toggle select)	Adds the highlighted element at the mouse location if not already in the selection set. Removes the highlighted element from the selection set if the selection set already contains it.
Selection by window	Clears previous selection set. Adds elements enabled in the Find Filter and that overlap the window to the selection set.
Shift + Select by window	Adds elements enabled in the Find Filter and that overlap the window to the selection set.
Ctrl + Select by window	Removes elements enabled in the Find Filter, overlapping the window or already in the selection set.

While in an application mode, the tool highlights design elements you have chosen in the design window as a selection set. Commands applicable to an application mode operate on this selection set. You modify the elements in the selection set by using any of the mouse operations described above.

Context-Sensitive Right-Mouse-Button Pop-Up Menu

The commands that populate the context-sensitive, RMB pop-up menu depend on:

- Current application mode
- Design elements already in the selection set
- Design elements selectable at the current mouse position

Hovering your cursor over...	...populates the pop-up menu with
an element already in the selection set	commands applicable to the selection set
an area where nothing is selectable, such as black space in the design	commands that don't use design elements as input such as the Design Parameter, Change Active Layer, Customization, SuperFilter, and Options.
the cursor is not over an already selected element and the element underneath the cursor could potentially be selected	commands applicable to that element

Application-mode commands are accessible from a Right-Mouse-Button pop-up menu based on the current selection set. The commands that populate the context-sensitive, Right-Mouse-Button pop-up menu depend on the location of your cursor and whether you have already created a selection set.

Etch Edit Default LMB Drag Command Execution

Element	Drag	Shift drag	Ctrl Drag	Double-Click
Group	Move	Move	Copy	None
Symbol	Move	Spin	Copy	None
Pin	None	None	None	Add Connect
Via	Slide	Move	Copy	Add Connect
Cline *	Move	Move	Copy	None
Line	Move	Move	Copy	None
Shape	Move	Move	Copy	None
Frect	Move	Move	Copy	None
Rect	Move	Move	Copy	None
Line Seg *	Slide	None	Delay Tune	Slide
Arc Seg	Slide	None	None	Slide
Figure	Move	Move	Copy	None
Text	Move	Move	Copy	None
Ratsnest	None	None	None	Add Connect
Rat T	Slide	Move	None	None

In the pre-selection use model, you can automatically execute a default command with a Left-Mouse-Button click, drag, shift-drag or Ctrl-drag on an element. In the Etch Edit application mode, the default commands are as documented above.

You can set an option so that the double click column commands can be executed using a single click. In order to accomplish this, in the pre-select mode, select Right-Mouse-Button in an open area and select ***Customize - Enable Single Click Selection***.

Note When you execute a command by dragging in any application mode, use the **Esc** key to allow the Left-Mouse-Button to be released, yet continue dragging.

If you decide that you prefer not to use the dray command executions, you can disable these drag executions by selecting the ***Disable Automatic Drag Operations*** in the ***Customize*** selection of the Right-Mouse-Button Common Areas.

* Choosing the midpoint of a cline or line seg invokes the slide command; to invoke the add connect command from the midpoint of a cline or line seg, right-click and choose ***add connect*** from the pop-up menu.

General Edit Default LMB Drag Command Execution

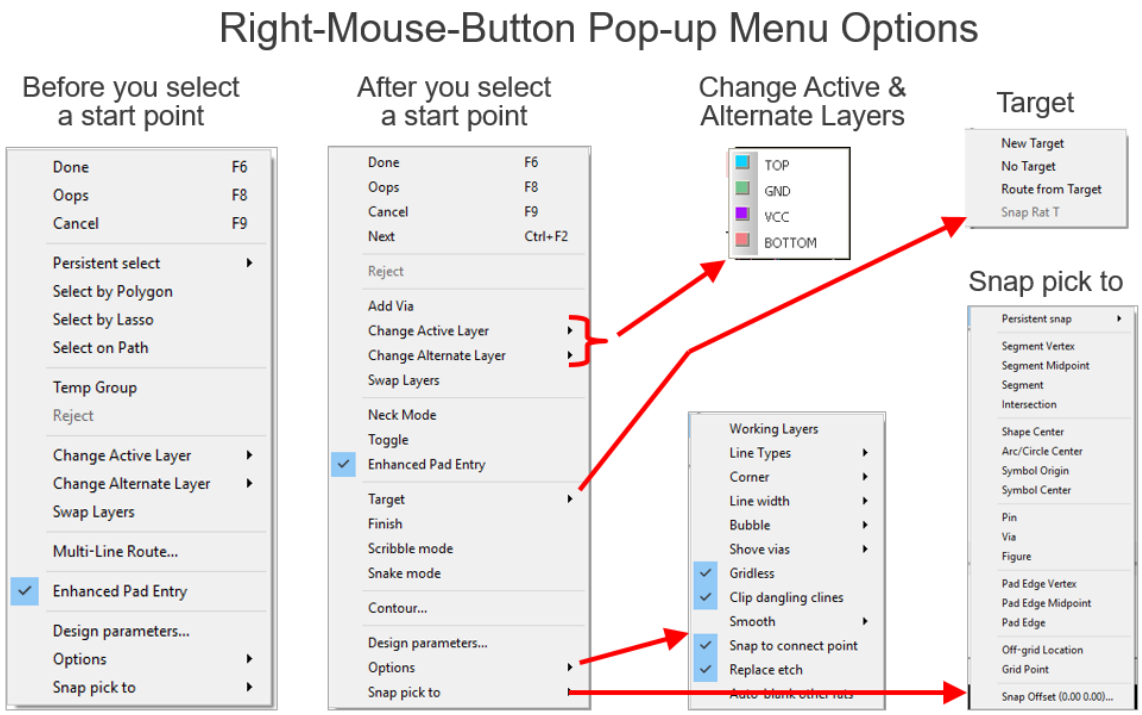
Element	Drag	Shift Drag	Ctrl Drag
Cline	Move	Move	Copy
Cline_Seg	Slide	None	None
Figure	Move	Move	Copy
Group	Move	Move	Copy
Line	Move	Move	Copy
Rat_T	Slide	Move	None
Symbol	Move	Spin	Copy
Shape	Move	Move	Copy
Text	Move	Move	Copy
Via	Slide	Move	Copy

In the pre-selection use model, you can automatically execute a default command with a Left-Mouse-Button click, drag, shift-drag or Ctrl-drag on an element. In the General Edit application mode, the default commands are as documented above.

Note When you execute a command by dragging in any application mode, use the **Esc** key to allow the Left-Mouse-Button to be released, yet continue dragging.

If you decide that you prefer to not use the drag command executions, you can disable these drag executions by selecting the ***Disable Automatic Drag Operations*** in the ***Customize*** selection of the Right-Mouse-Button Common Areas.

Routing Pop-Up Menu Options



Immediately after selecting ***Route - Connect***, you view a pop-up menu (you cannot access this RMB popup in the Pre-Select mode). During the process of adding segments, different options are available:

- **Done** - Exits the Add Connect command.
- **Oops** - lets you undo or take back the last added point in the wire path (can be used to repetitively remove all wire segments and vias for the current connection).
- **Cancel** - Cancels all selections and exits from the command.
- **Next** - Lets you start on a new connection without exiting from connect mode (this is not available in the Pre-Select mode).
- **Reject** - Applies if multiple objects are stacked on top of each other. It lets you reject a currently selected object and select another object from a window (this is not available in the Pre-Select mode).
- **Add Via** - Used to add through-hole, blind, or buried routing vias.
- **Change Active Layer** - Allows you to change the current Active Layer.
- **Change Alternate Layer** - Allows you to change the current Alternate Layer.
- **Swap Layers** - Interchanges the Active and Alternate layers in the Options form.
- **Neck Mode** - Changes the line width for the next segment to the Neck Width specified in the Physical Rule Set for the Minimum Neck Width.
- **Toggle** - Lets you switch the initial direction of the projected wire path.

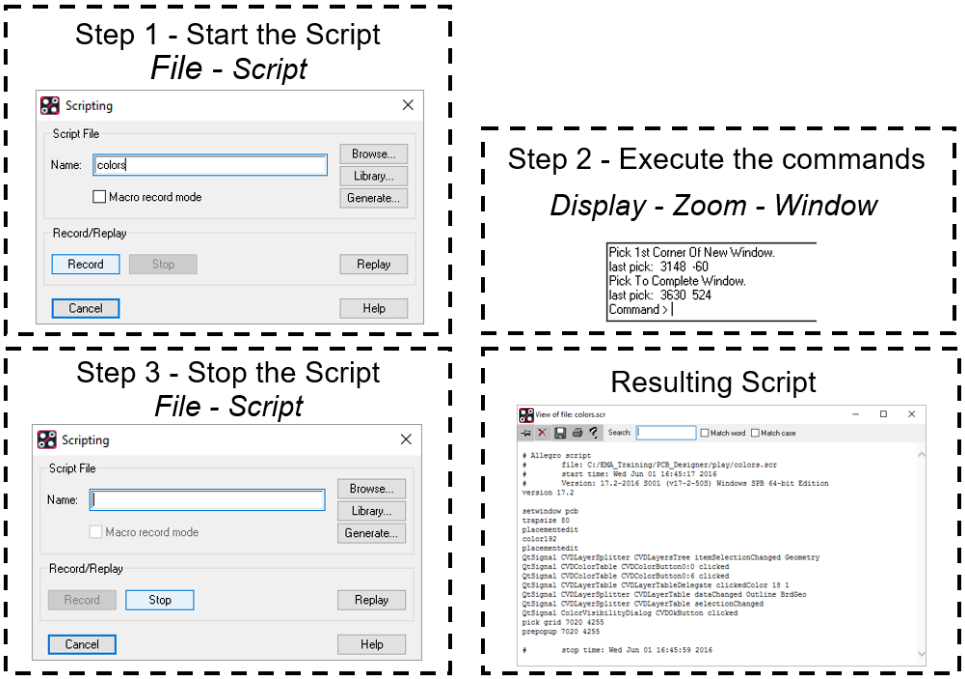
- **Enhanced Pad Entry** - Improves the transition of clines that exit or enter a padstack. It also contributes in the reduction of acute angles that form acid traps.
- **Target** – Defines the projected routing between two nodes (defaults to closest pin).
    - **New Target** - Lets you select a new rubber band target pin.
    - **No Target** - Eliminates the rubber band line from the cursor to the target pin.
    - **Route from Target** - Starts routing from the target pin instead of the pin selected.
- **Finish** - Completes the connection using an automatic router. This routing is performed on the active layer only. No autorouting licensing is needed for this feature.
- **Scribble mode** – Lets you scribble a route path between two points using smart shove and push techniques. Once the routing is completed the etch solution is generated by the application for the scribbled path.
- **Snake mode** – Allows you to route through a pin array
- **Design Parameters** - Displays the standard Design Parameters form.
- **Options** - Allows you to set the different interactive routing parameters in the Options tab. These parameters will be discussed in the following Options Forms topics.
- **Snap pick to** - Allows you to snap the starting point to an object that is near your cursor.
    - **Persistent snap** – Lets you select any of the Snap pick to options which will retain the selected snapping for all further selections. Each pick of an operation will snap to the persistent option. The active snap mode applies to all commands and application modes that performs snapping. By default, this option is set to off.
    - **Segment Vertex** - The pick point snaps to the nearest vertex of any of the supported object types.
    - **Segment Midpoint** - The pick point snaps to the nearest mid-point of the supported segment type.
    - **Segment** - The pick point snaps to the nearest point on the segment.
    - **Intersection** - The pick point snaps to the intersection of the segments.
    - **Shape Center** - The pick point snaps to the center of the shape.
    - **Arc/Circle Center** - The pick point snaps to the center of an arc segment or a circle.
    - **Symbol Origin** - The pick point snaps to the origin of the symbol.
    - **Symbol Center** - The pick point snaps to the center of the symbol.
    - **Pin** - The pick point snaps to the nearest pin.
    - **Via** - The pick point snaps to the nearest via.
    - **Figure** - The pick point snaps to the nearest figure.
    - **Pad Edge Vertex** - The pick point snaps to the nearest vertex of pad edge.
    - **Rectangle Edge Midpoint** - The pick point snaps to the nearest mid-point of the pad edge.
    - **Rectangle Edge** - The pick point snaps to the nearest point on the pad edge.
    - **Off-grid Location** - The pick point directly returns without snapping.
    - **Grid Point** - The pick point snaps to the nearest grid point.

- **Snap Offset** - The pick point snaps at a given offset to one of the selected snap definitions. You can define the offset from a snapping destination in two ways by either setting:
  - X and Y coordinates
  - Or distance and angle

  If persistent snap is enabled, the Snap Offset values are remembered throughout the editing session and for all commands that use snapping.

Appendix B: Scripts and Macros

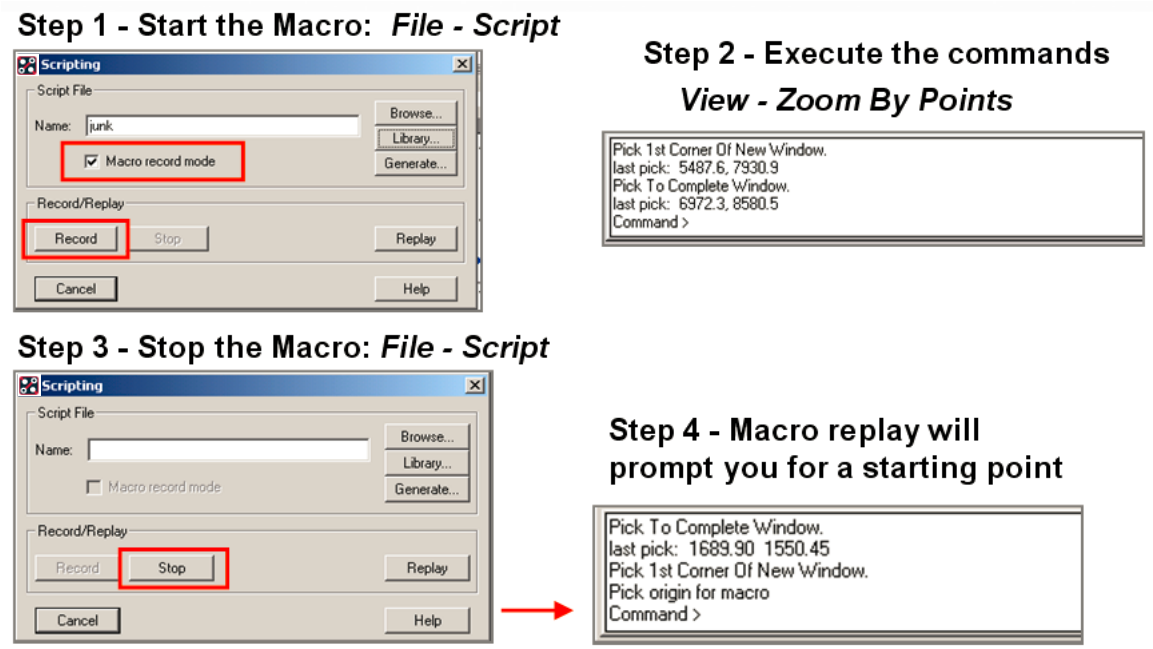
Scripts



With scripts, you can have the PCB Editor record and save all your menu selections and mouse picks in a text file. You initiate such script recording by clicking **Record**. While a script is recording, the script file name appears in the Status window. All your executed commands will be recorded in a text file, until you stop the recording. You can then replay the file in the same design or a different design to quickly execute repetitive operations.

- **Browse** - Displays a script file browser that lets you choose a script file to replay.
- **Library** - Displays a script file browser that opens your script path location (*env* file) and lets you choose a script file to replay.
- **Generate** - Displays a file browser from which you can choose a `.jrl` file to convert into a script file.

Macros



We created a script earlier in the course. Macros vary slightly from scripts. Scripts, when replayed, use absolute coordinates for any X and Y input. Macros on the other hand use relative X and Y coordinates for input. When replaying a macro, you must identify in the PCB Editor, the origin of the macro. All X and Y coordinates contained in the macro will then be relative to the point you chose.

To create a macro, use the following procedures:

6. Choose File - Script.
7. In the Name field, enter the name you want to give to the script.
8. Toggle the Macro Record mode on.
9. Click **Record**.
10. Perform the tasks that you want the script to run.
11. Choose ***File - Script*** and click **Stop** in the Scripting dialog box.

To replay a script or macro:

12. Choose File - Script.

13. In the File field, enter the name of the script you want to replay.

14. Click **Replay**.

15. Select the starting point for the macro.

Macro and Script Results

The same command recorded is: *View > Zoom By Points*

Macro File - recordmacro

```
setwindow pcb
# Allegro script
#     file: D:\user1.spare\allegro\advanced\1Customizing\
#     start time: Thu Jun 03 19:00:15 2004
#     Version: 15.2 b004 (v15-2-47A) i86
version 15.2

trapsize 1628
# Macro file: coordinates are relative to pick on replay.
zoom points
pick_origin
pick rel 0.00 0.00
pick rel 892.37 221.46
trapsize 1258
#     stop time: Thu Jun 03 19:01:
```

Prompts for user input

Script File - record

```
setwindow pcb
# Allegro script
#     file: D:\user1.spare\allegro\advanced\1Customizing\
#     start time: Thu Jun 03 19:16:04 2004
#     Version: 15.2 b004 (v15-2-47A) i86
version 15.2

trapsize 1001
pick 1501.37 1376.64
pick 1771.62 1498.75
#     stop time: Thu Jun 03 19:16:17 2004
```

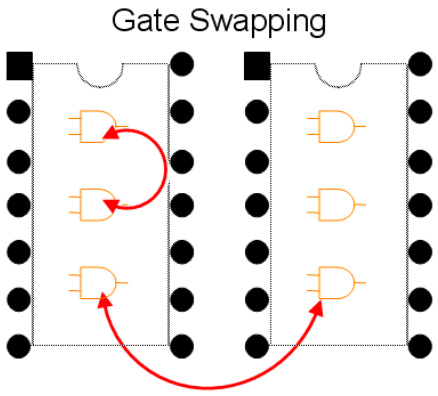
The same command was recorded here using the macro mode and the script mode. The resulting files are different because the macro is looking for input from the user when it gets replayed.

Every action included in the macro takes place relative to the coordinates that are chosen as a starting point. Macros can be used for placing multiple clipboard files or modules in a step-and-repeat pattern, starting from different starting points, and defining a fabrication drawing that has various starting points from where to place the format symbols.

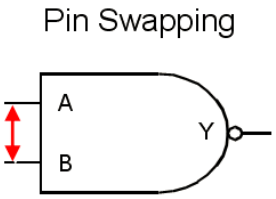
To start recording a macro, first you enable the **Macro Record Mode** check box.

Appendix C: Pin and Gate Swapping

Swapping of Functions (Gates) and Pins



Gate swapping is available for any homogeneous schematic capture library symbol without having to be defined



Pin swapping is available only if the swappable pins are defined in the schematic capture library symbol

After component packages are placed on your board, you can use PCB Editor's interactive pin and gate swapping features to further reduce signal lengths and crossovers.

As shown, swapping features include the following possibilities:

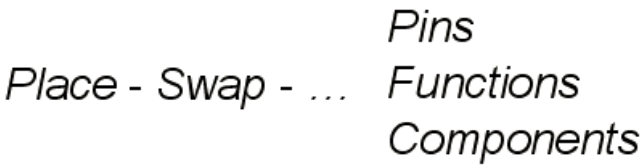
- Functions (gates) can be swapped within a package.
- Functions (gates) can be swapped between packages of like types.
- Swappable pins within a function (gate) can be swapped but only if defined as swappable in the schematic capture library symbol.

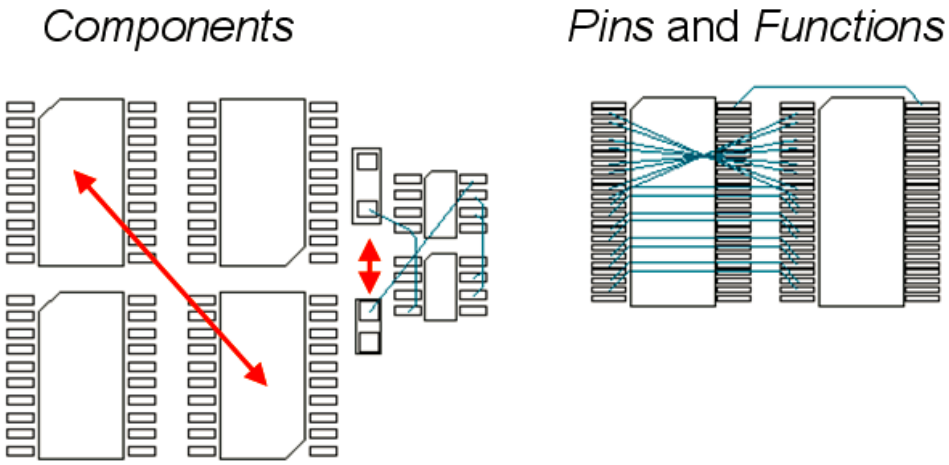
You can perform pin and gate swapping on devices that meet one of these requirements:

- The device is described in OrCAD Capture and contains pin and/or gate information.
- An associated device file with a third-party schematic has been used that contains pin and/or gate information.

Note Devices that have been loaded into your design through a third-party netlist must use device files that contain pin and/or gate information, or else swapping will not be available for these devices. You can find more information in CDSDoc, the online documentation.

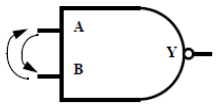
Interactive Swap



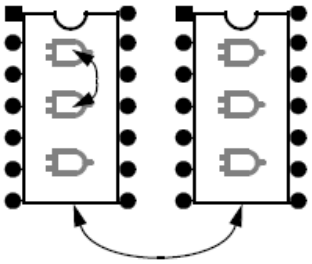


When displaying ratsnests, you may discover gate-to-slot or pin-to-net assignments that create unnecessary congestion. Manual gate and pin swapping can reduce congestion and allow the ratsnests to flow in a more organized manner, which helps routing. See Lesson 6 titled *Importing Logic Information into PCB Editor* for more details on which part definition statements are required in order to support gate and pin swapping.

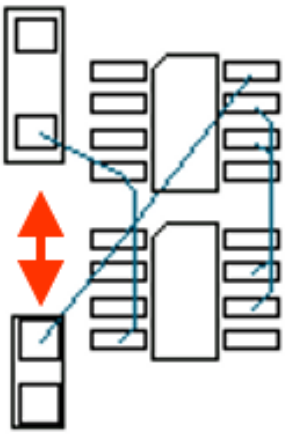
- **Pins** - Lets you select two equivalent pins for swapping (for example, inputs on a nand2, or inputs on a resistor pack).



- **Functions** - Lets you select two equivalent gates for swapping.



- **Components** - Trades the locations of two entire packages.



Objective: Use manual component, pin, and gate swapping to improve routing.

When placing components, you can achieve better routing results by minimizing signal crossings, roughly indicated by the ratsnest lines between pins. You can always swap placed components, which is especially effective when the components are of similar size and shape. By swapping pins and gates, you can have a cleaner arrangement of conductors.

Lab C-1: Component and Gate Swapping

Swapping Components

At this point, you can turn on the ratsnests to see how the pins for each net are arranged.

1. Turn all the ratsnests on by choosing ***Display - Show Rats - All*** from the top menu.
2. **Zoom In** to the ***MEM*** room area.
3. Choose ***Place - Swap - Components*** from the top menu.
4. Click two parts for swapping, such as adjacent ICs in the MEM room at the upper right of the board.
   The two parts are swapped.
5. Try swapping several other pairs of components and see whether you can reduce the complexity of the ratsnest.
   The PCB Router will do a better job if the ratsnests are more horizontal and vertical rather than diagonal because it will not have to add as many vias.
6. When you are through swapping, right-click and choose **"*Done*"** from the pop-up menu.

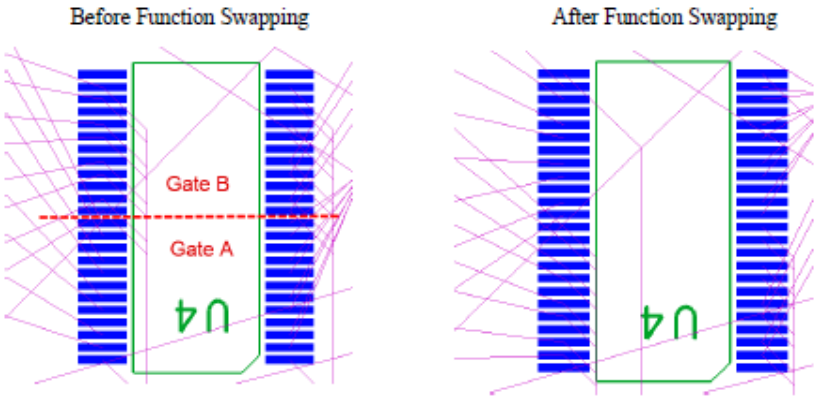
Note ICs U10 through U17 have a ROOM property of MEM and should therefore be placed in the MEM room. Check the room properties of the ICs you place to verify they are in their proper rooms.

Swapping Functions (Gates)

After swapping physical package locations, you can further optimize your placement through gate and pin swapping. To demonstrate this, you will work with U4, an SOIC48 designated with an FCT16245 function. Not all components are defined for pin or gate swapping, but U4 - a component you have already placed — does have definitions for function (gate) swapping.

1. Zoom in to the area of your design where U4 has been placed.
2. Click the ***Rats All*** icon to display all ratsnest lines.
3. Choose ***Place - Swap - Functions*** from the top menu.
4. Select a pin on ***U4*** that has a ratsnest line.
   If the pin you selected belongs to a function (gate) that can be swapped, the pins of other similar functions that can also be swapped are highlighted. If the pin you selected is a power or ground pin, the command line will report this, and you will need to pick another pin in order to find a function pin.

5. Select a second pin from the highlighted choices.
   This part has two functions. One function consists of the pins in the top half of the part, and the other function consists of pins in the bottom half of the part.



6. Right-click and choose ***Next*** from the pop-up menu.
   The ratsnest lines from the two gates are swapped. The changes are subtle, so you need to watch carefully.
7. Select another pin on ***U4*** that has a ratsnest line.
8. Select a second pin from the highlighted choices.
9. Right-click and choose **"*Done*"** from the pop-up menu.
10. If you are interested, you can select ***Check - Elements***, be sure *Functions* is toggled on in the Find Filter and select a pin on U4.
    This describes the functionality of the gates that reside in this component. Notice that there are only two gates (latch) in this part, G1 and G2.
11. Choose ***File - Save As*** from the top menu.
12. Rename this drawing by entering the following in the File Name field:
    `swap_placed`.
13. Select ***Save*** to save the **`swap_placed.brd`** file.

End of Lab