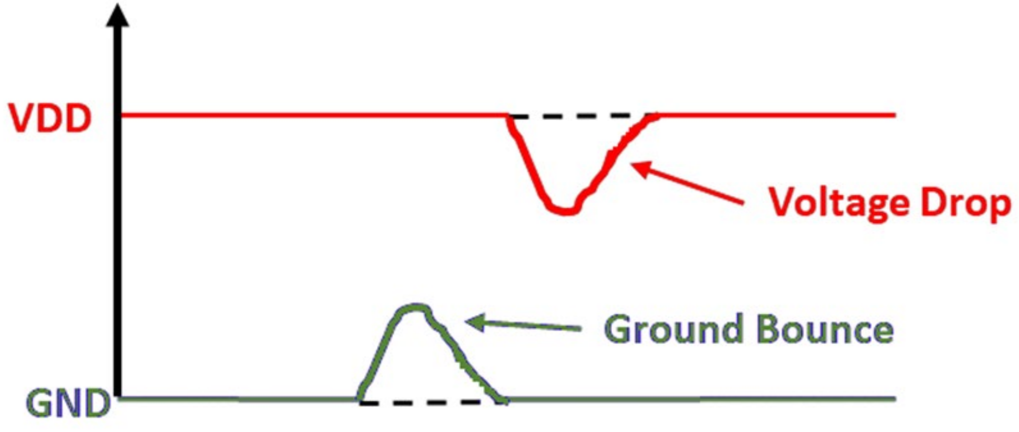
Design Challenges

Whack-a-Mole

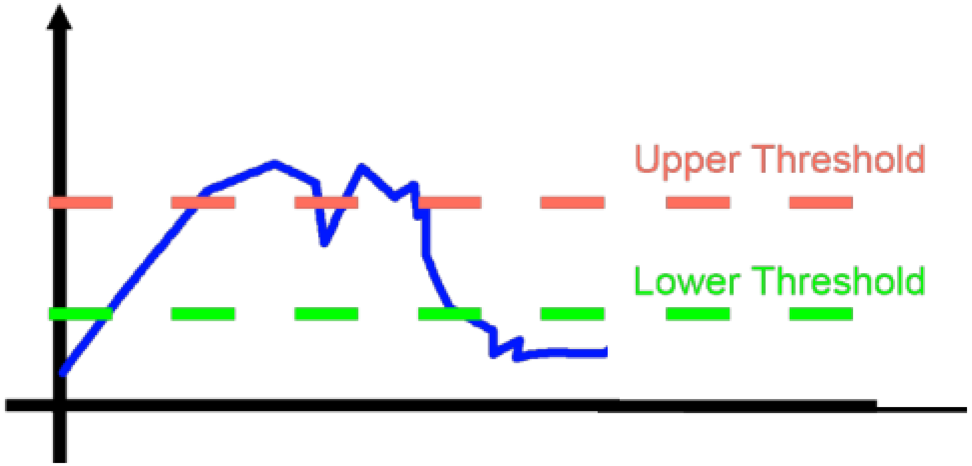
At current speeds and complexity, design issues are:

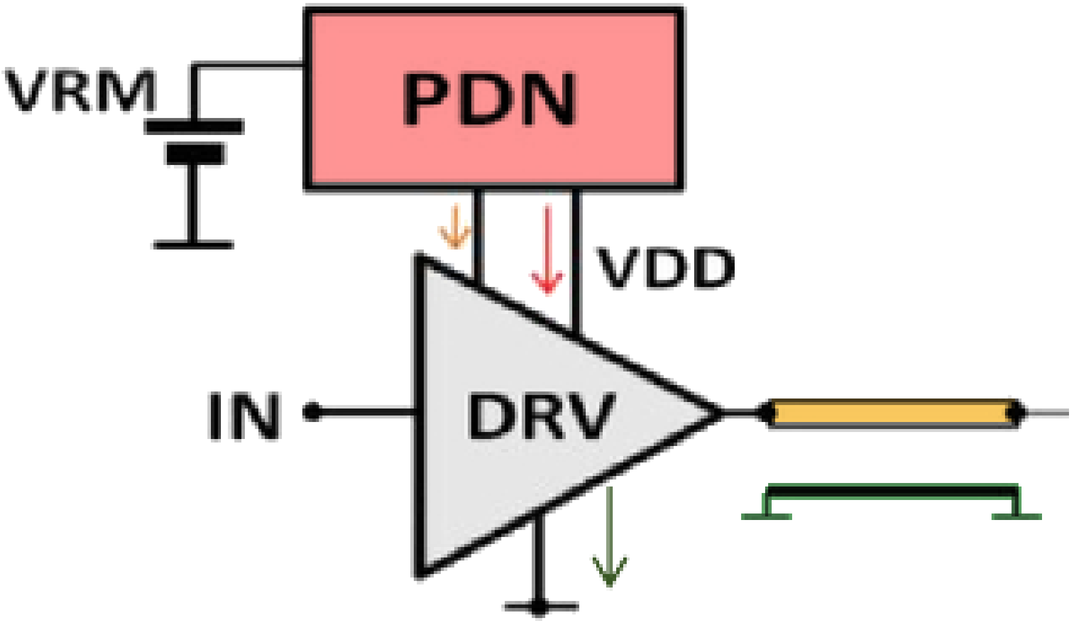
- Multi-domain
- Interrelated
- Hard to pinpoint and debug in the lab

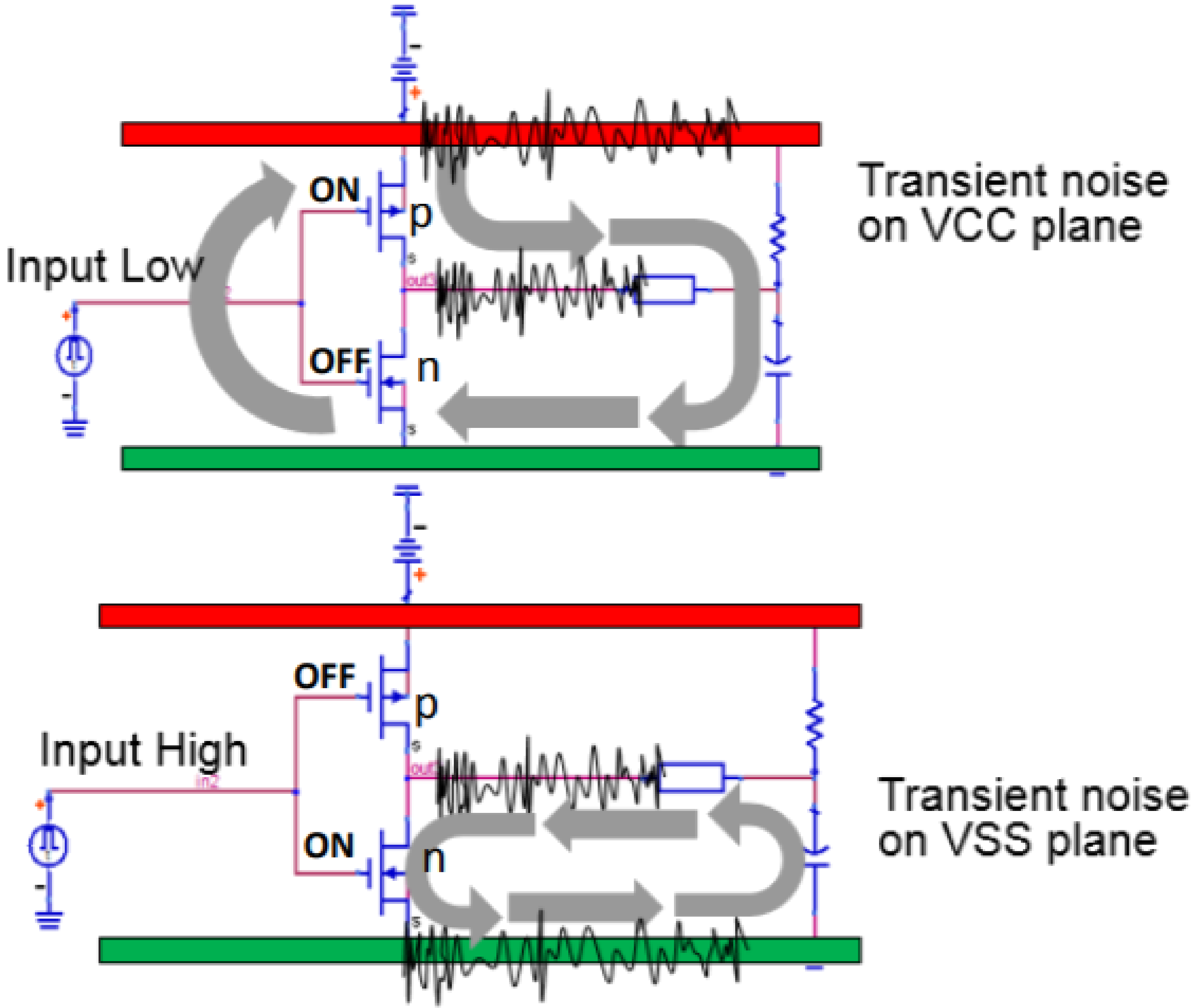
Power Integrity

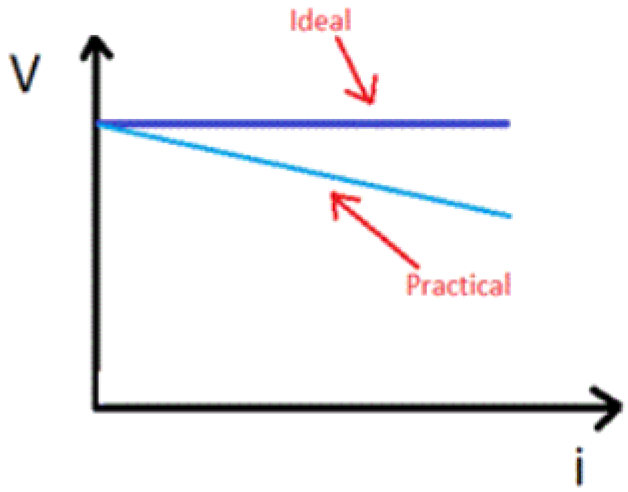


Signal Integrity

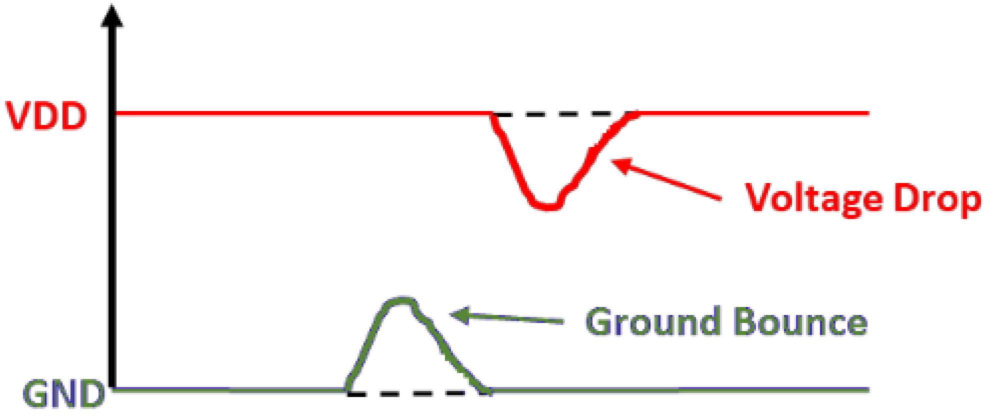




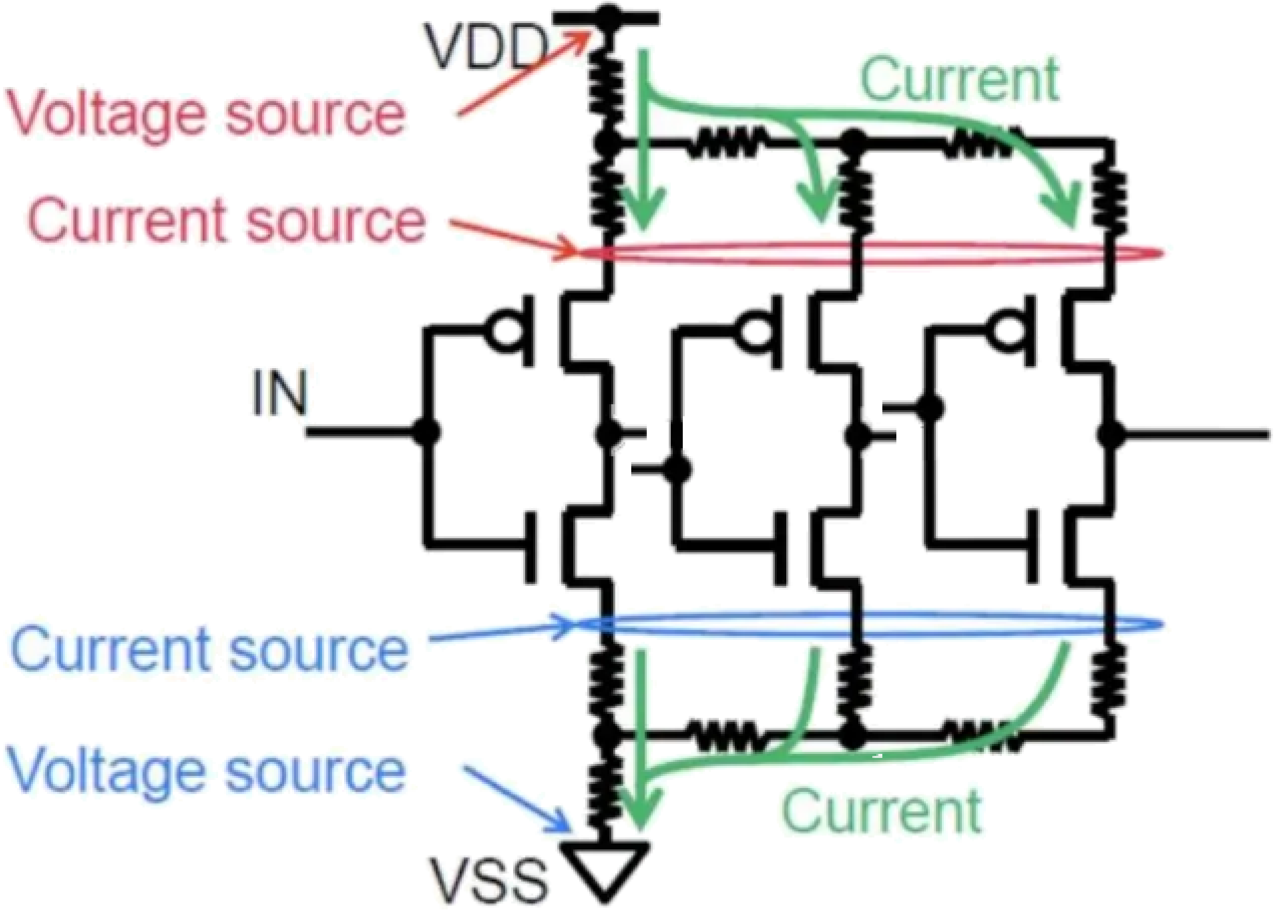

Transient noise
on VCC plane
ON
p
Input Low
OFF
n
OFF
p
Input High
ON
n
Transient noise
on VSS plane



Ideal
V
Practical
i

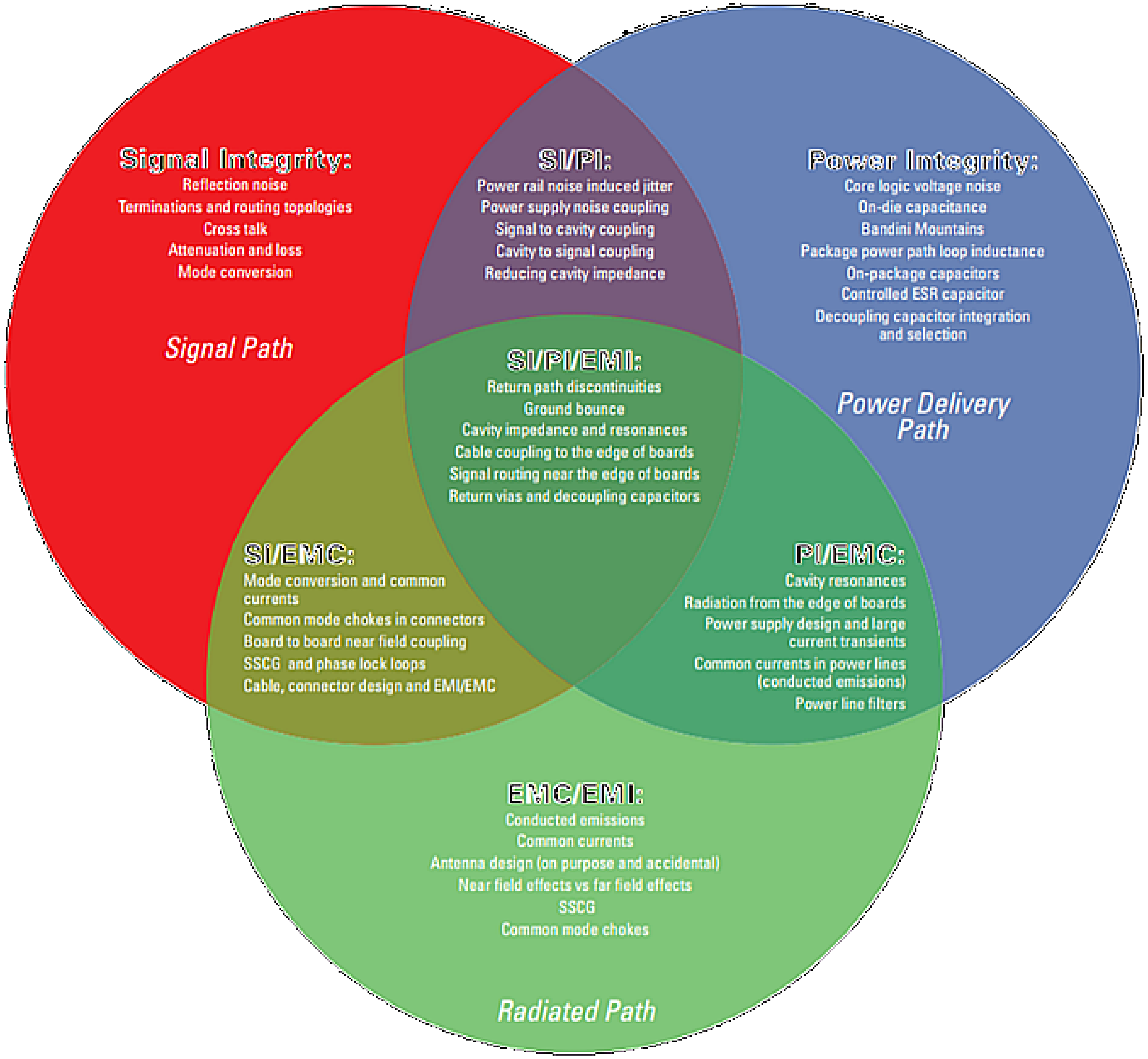


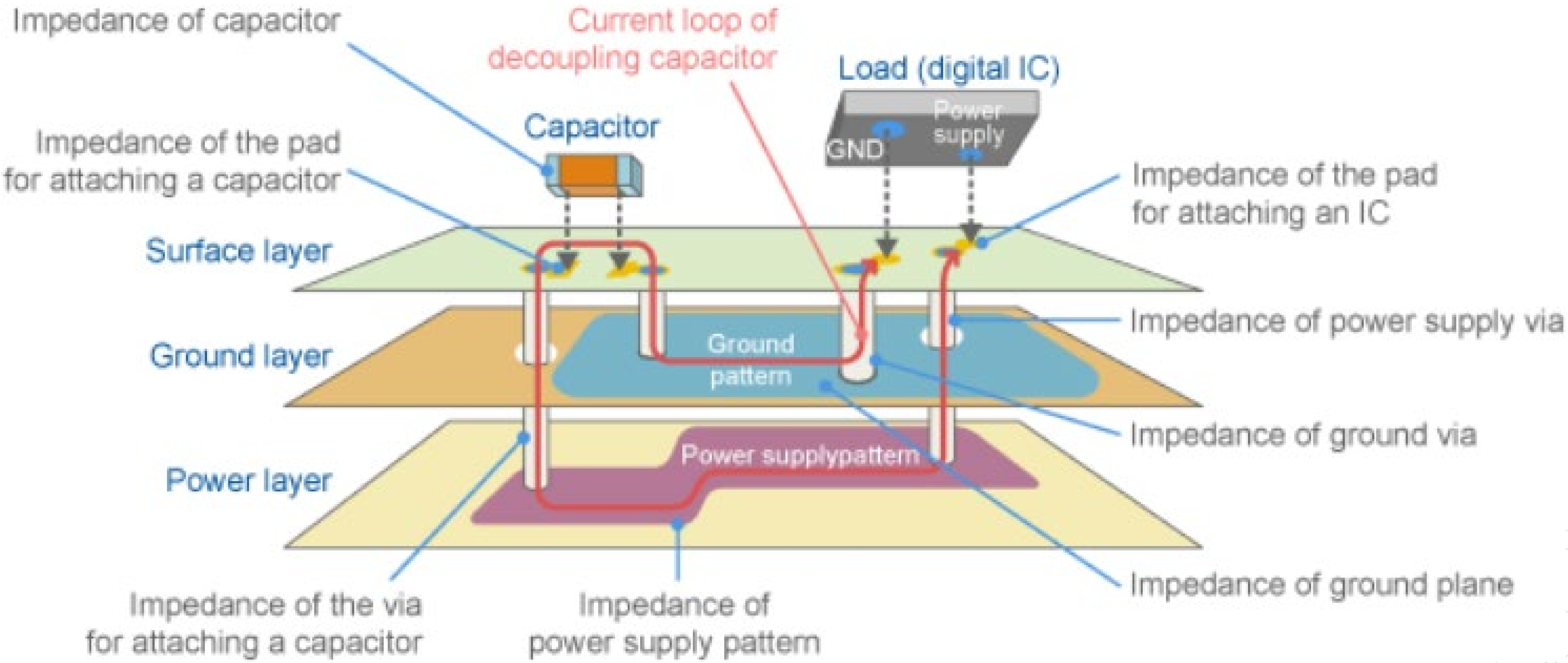
VDD
Voltage Drop
Ground Bounce
GND



VDD
Voltage source
Current
Current source
IN
Current source
Voltage source
Current
VSS

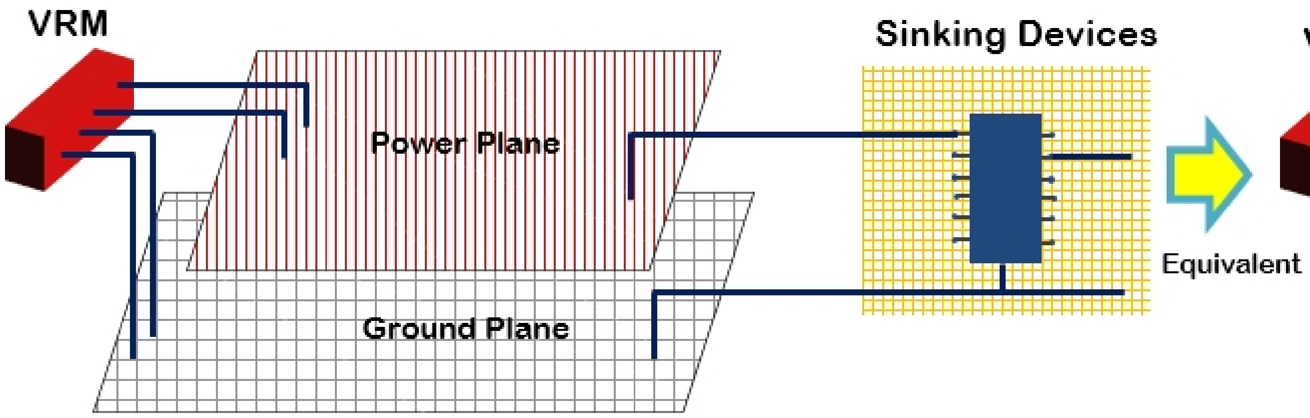
cādence

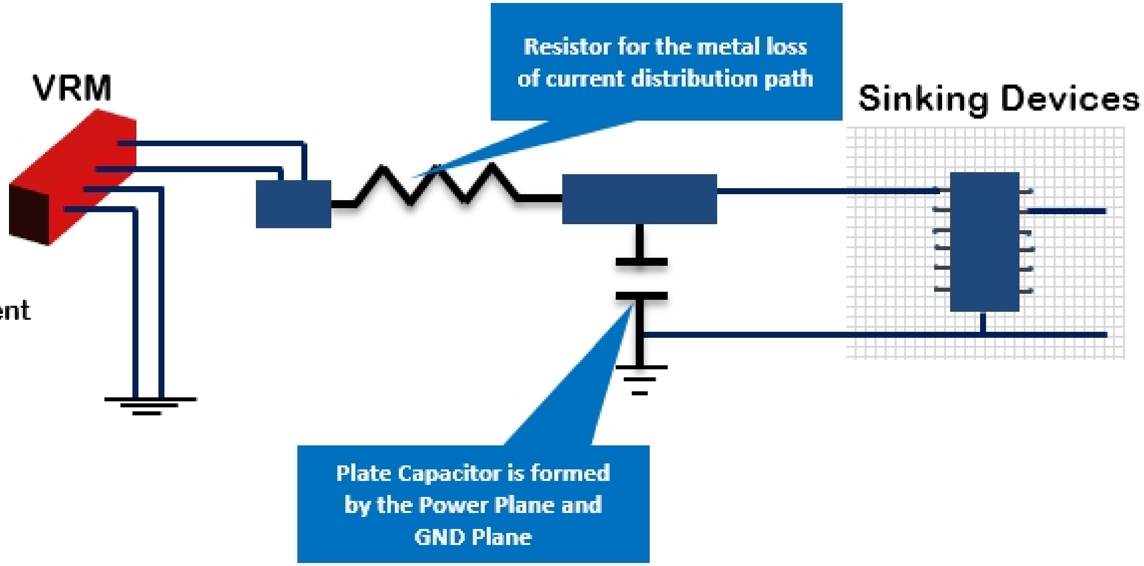

Signal Integrity:
Reflection noise
Terminations and routing topologies
Cross talk
Attenuation and loss
Mode conversion
Signal Path
SI/PI:
Power rail noise induced jitter
Power supply noise coupling
Signal to cavity coupling
Cavity to signal coupling
Reducing cavity impedance
Power Integrity:
Core logic voltage noise
On-die capacitance
Bandini Mountains
Package power path loop inductance
On-package capacitors
Controlled ESR capacitor
Decoupling capacitor integration and selection
Power Delivery Path
SI/PI/EMI:
Return path discontinuities
Ground bounce
Cavity impedance and resonances
Cable coupling to the edge of boards
Signal routing near the edge of boards
Return vias and decoupling capacitors
SI/EMC:
Mode conversion and common currents
Common mode chokes in connectors
Board to board near field coupling
SSCG and phase lock loops
Cable, connector design and EMI/EMC
PI/EMC:
Cavity resonances
Radiation from the edge of boards
Power supply design and large current transients
Common currents in power lines (conducted emissions)
Power line filters
EMC/EMI:
Conducted emissions
Common currents
Antenna design (on purpose and accidental)
Near field effects vs far field effects
SSCG
Common mode chokes
Radiated Path



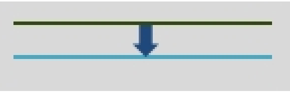
Impedance of capacitor
Current loop of decoupling capacitor
Load (digital IC)
Capacitor
Power supply
GND
Impedance of the pad for attaching a capacitor
Impedance of the pad for attaching an IC
Surface layer
Ground layer
Ground pattern
Impedance of power supply via
Impedance of ground via
Power supplypattern
Power layer
Impedance of ground plane
Impedance of the via for attaching a capacitor
Impedance of power supply pattern

cadence





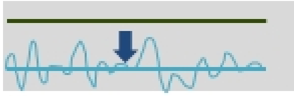
Cause the Voltage level shifted from the ideal level



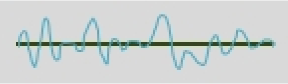
We Need DC Analysis (Static IR Drop)

- Voltage Drop
- Current Densities

Total Effect



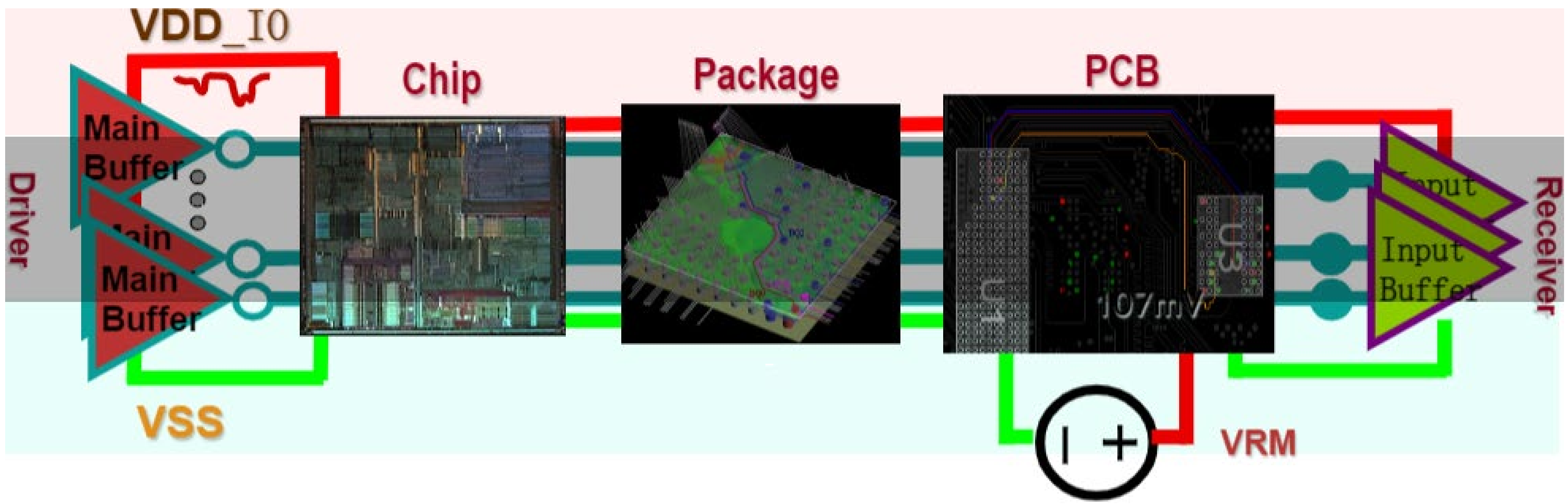
Cause the Voltage level variation from the ideal level during current transition

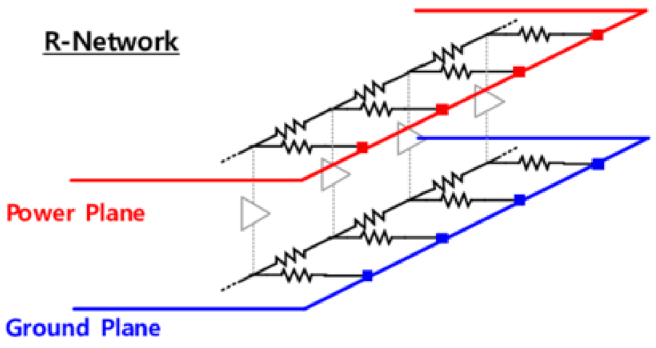


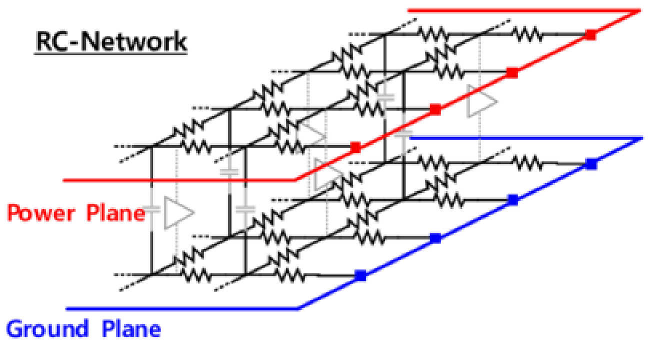
We Need AC Analysis (Dynamic IR Drop)

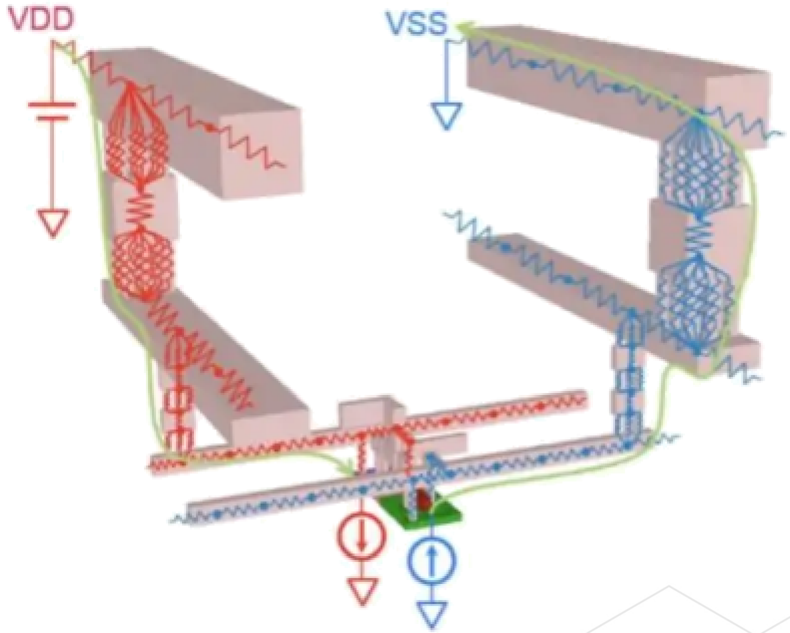
- Decoupling / Target Impedance
- Plane Noise

From the electrical point of view, the goal in designing a PDN is simple to describe: minimize the impedance between power and ground for the appropriate frequency range


VDD_IO
Chip
Package
PCB
Driver
Main Buffer
Main Buffer
Input Buffer
Receiver
107mV
VSS
VRM

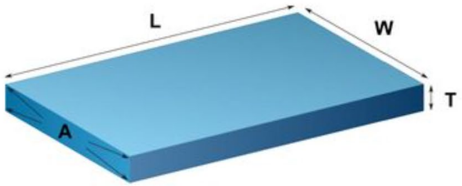

R-Network
Power Plane
Ground Plane


RC-Network
Power Plane
Ground Plane


VDD
VSS

cādence

Power Plane Resistance – Squares method



$$R = \frac{\rho L}{A} = \frac{\rho L}{WT}$$

$$R_{SQUARE} = \frac{\rho \cancel{L}}{\cancel{L} T} = \frac{\rho}{T}$$

For a square of Copper W = L
Resistance is independent of size

- **R** = Total resistance
- **A** = Cross-sectional area of plane
- **W** = Width
- **T** = Thickness, defined by copper weight
- **P** = Resistivity of Copper, typically 1.7μΩ-cm (0.67μΩ-in) at 25°C

Copper Weight oz	Thickness mm [mils]	mΩ/square at 25°C
0.5	0.02 [0.7]	1.0
1	0.04 [1.4]	0.5
2	0.07 [2.8]	0.25

Via Resistance

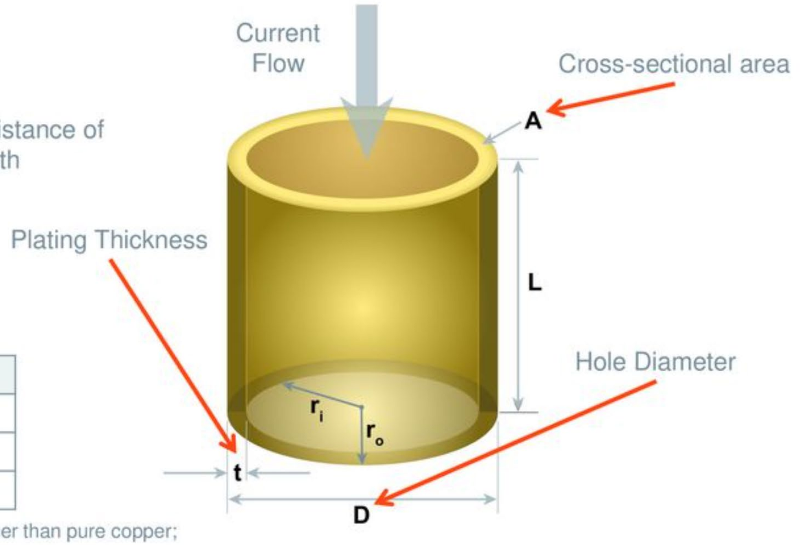
Resistance of Via equivalent to resistance of trace with equivalent CSA and length

$$R = \frac{\rho L}{A}$$

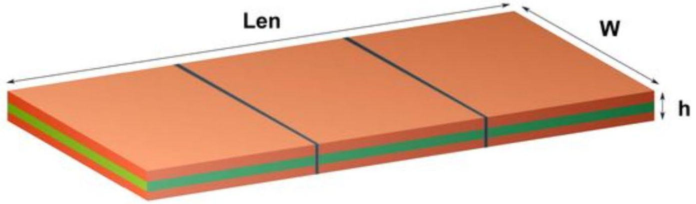
$$R = \frac{\rho L}{\pi(ro^2 - ri^2)}$$

Material	μΩ-cm	μΩ-in
Copper	1.70	0.67
Copper (plated)	6.0	2.36
Gold	2.2	0.87

*Note: resistivity of plated copper can be higher than pure copper; consult with PCB vendor



Power Plane Inductance – Rule of Thumb

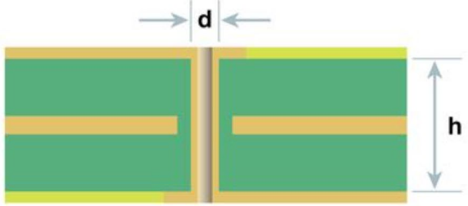


$$L_{LOOP} = \mu_0 * h * \frac{Len}{W} = 32\text{pH/mil} * h * \frac{Len}{W}$$

$$L_{LOOP} = \mu_0 * h * \frac{Len}{W}$$

Inductance per square of two adjacent parallel power planes approximately 32pH per mil of dielectric
Example: 3.1mil dielectric approximately 100pH per square*

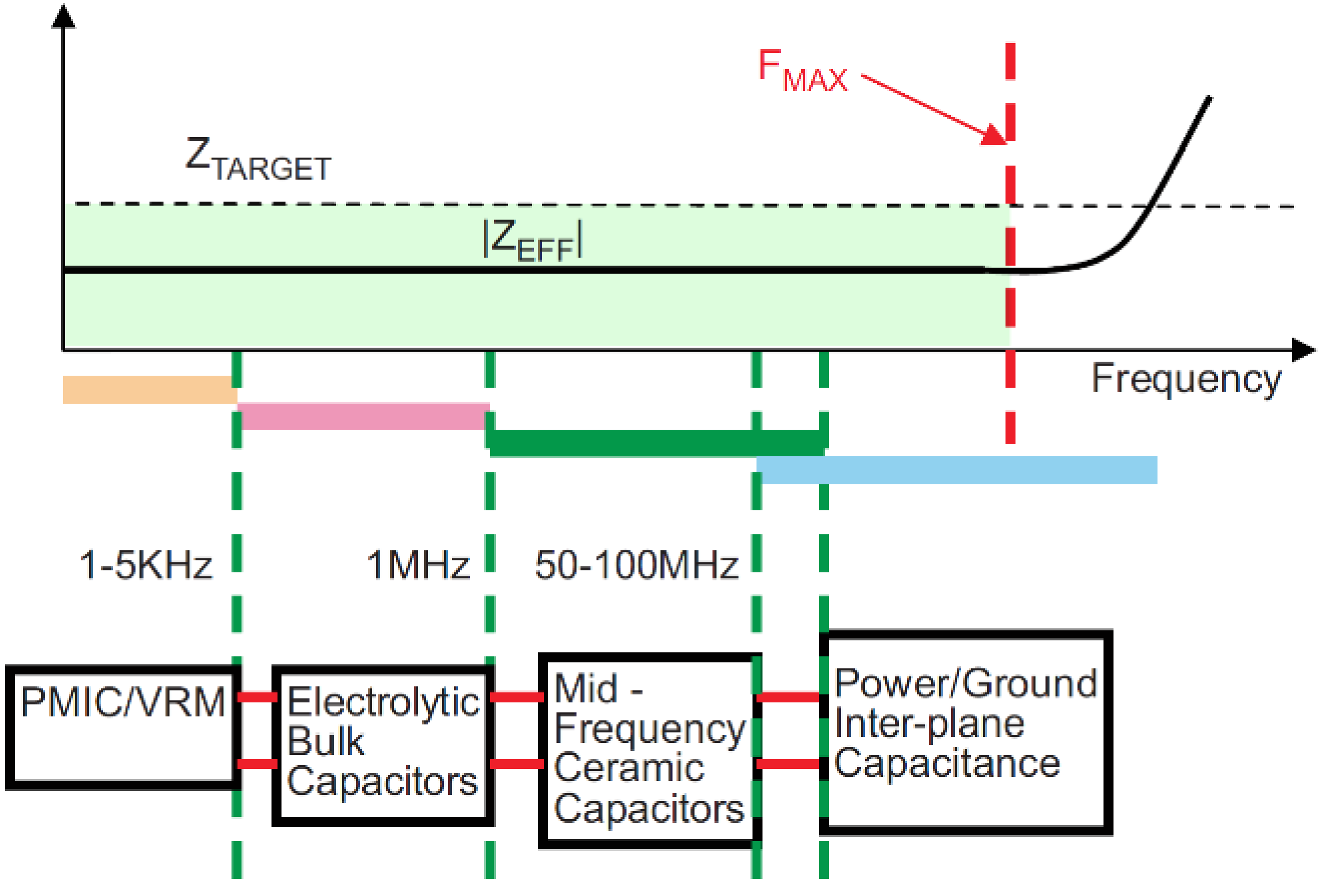
Via Inductance



$$L_{via} = 5.08\,h\left[ln\left(\frac{4h}{d}\right) + 1\right]$$

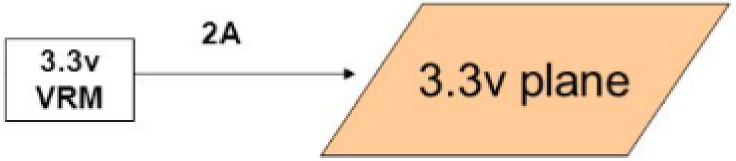
Where:
- L_{via} = inductance of via, nH
- D = via diameter, in.
- H = length of via, in.

Target Impedance Calculation



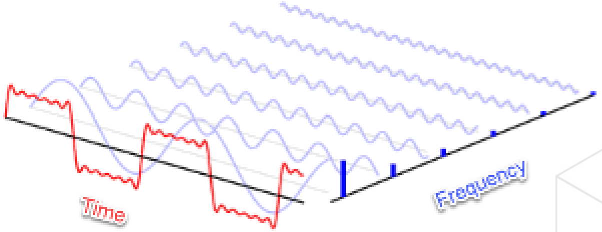
$$Z_{Target} = \frac{(Power\_Supply\_Voltage) \times (Allowed\_Ripple)}{Current}$$

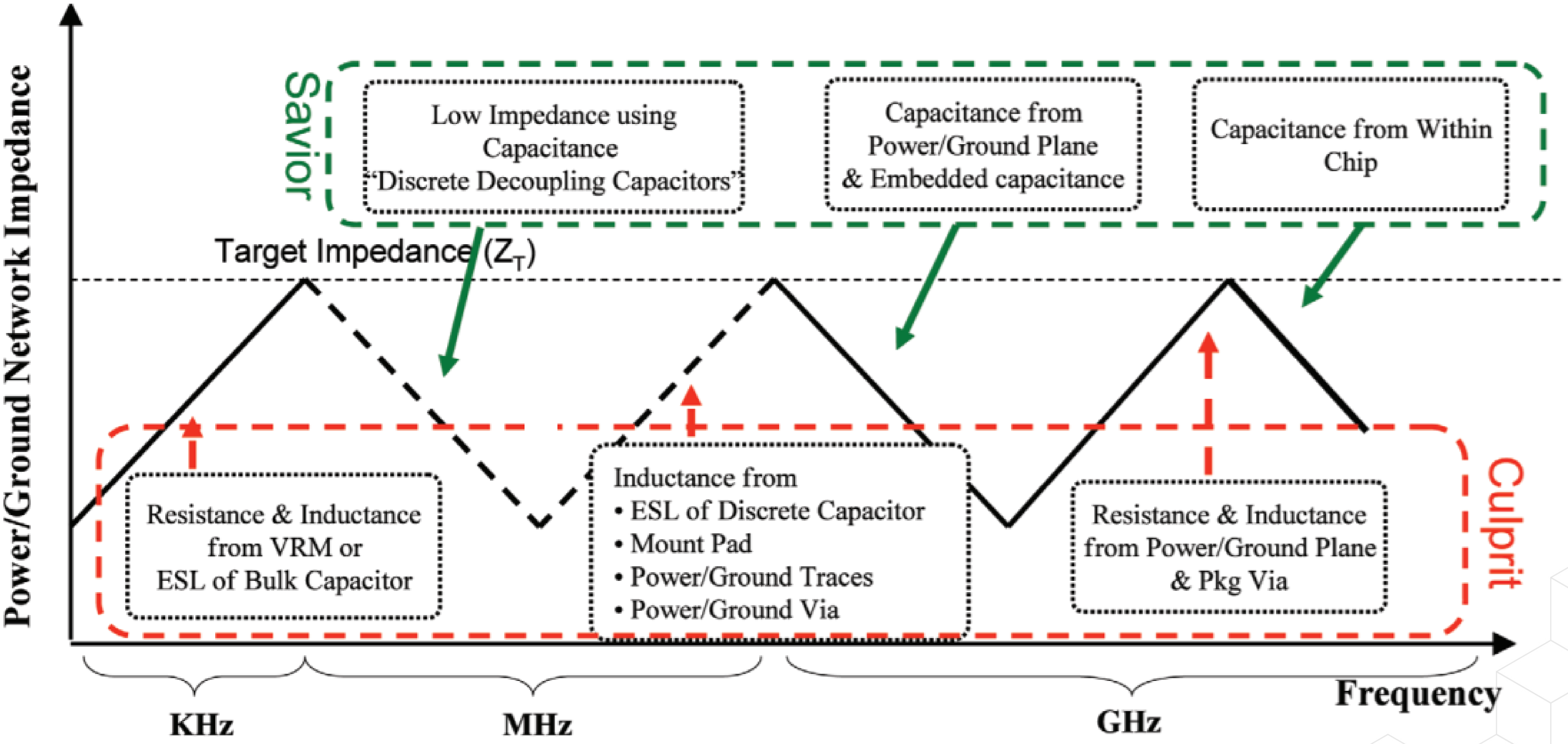
Example:



$$Z_{Target(3.3v)} = \frac{(3.3v) \times (5\%)}{2A} = 82.5m\Omega$$

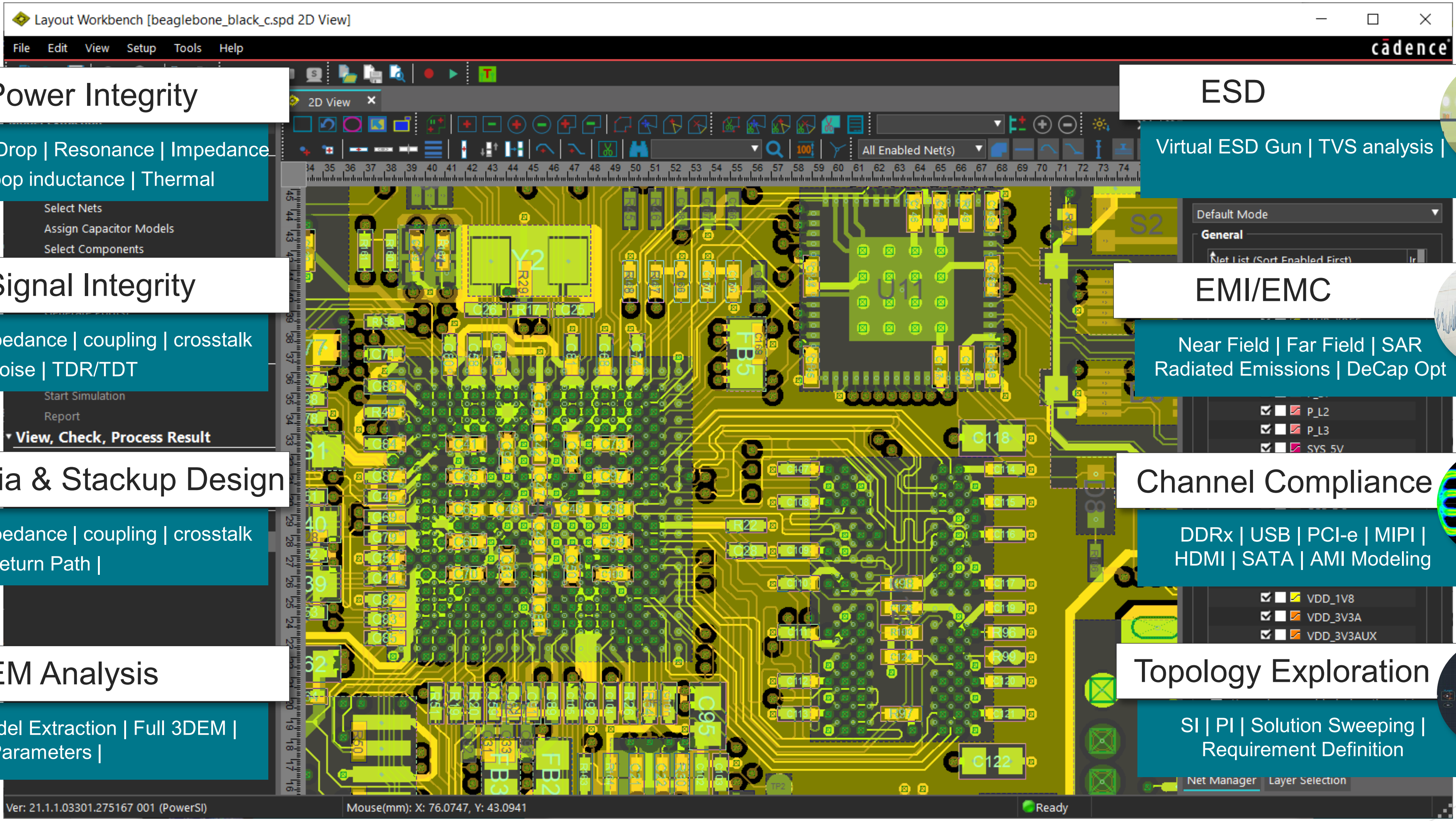
Target Impendence is the goal!!!




Power/Ground Network Impedance
Savior
Low Impedance using Capacitance "Discrete Decoupling Capacitors"
Capacitance from Power/Ground Plane & Embedded capacitance
Capacitance from Within Chip
Target Impedance (Z_T)
Resistance & Inductance from VRM or ESL of Bulk Capacitor
Inductance from
• ESL of Discrete Capacitor
• Mount Pad
• Power/Ground Traces
• Power/Ground Via
Resistance & Inductance from Power/Ground Plane & Pkg Via
Culprit
KHz
MHz
GHz
Frequency

cadence

Sigrity Unified Analysis WorkBench



Power Integrity

IR Drop | Resonance | Impedance
Loop inductance | Thermal

Signal Integrity

Impedance | coupling | crosstalk
Noise | TDR/TDT

Via & Stackup Design

Impedance | coupling | crosstalk
Return Path |

EM Analysis

Model Extraction | Full 3DEM |
S-Parameters |

ESD

Virtual ESD Gun | TVS analysis |

EMI/EMC

Near Field | Far Field | SAR
Radiated Emissions | DeCap Opt

Channel Compliance

DDRx | USB | PCI-e | MIPI |
HDMI | SATA | AMI Modeling

Topology Exploration

SI | PI | Solution Sweeping |
Requirement Definition