A Dive into DDR5:
An Engineer's Guide to Simulating and Validating the Latest Generation of DDR

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Sept. 22, 2021

Meet the Presenter

- Stephen Newberry:
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  - B.S. in ECE from Rutgers
  - Former U.S. Coast Guard Electrician's Mate
  - Husband and father of 4

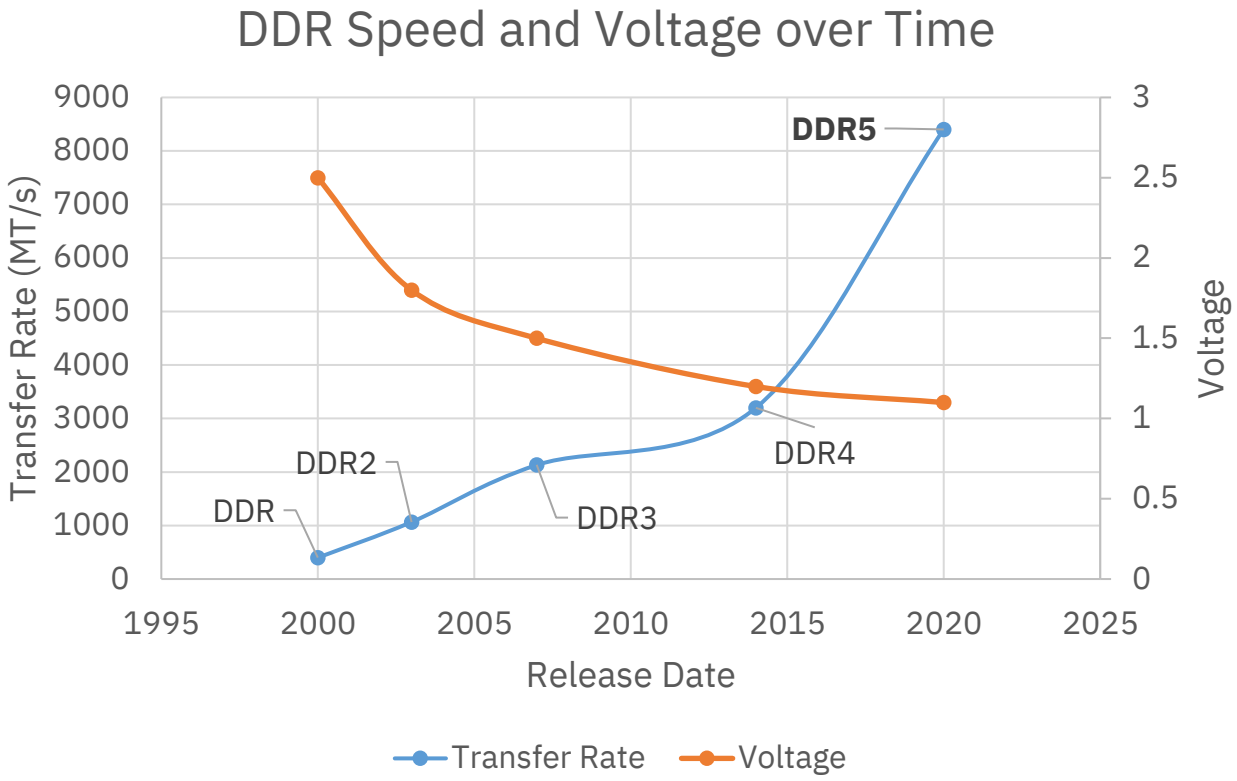
Introduction

- This overview has **two goals**:
  - Provide **basic info** about DDR5 changes
  - Introduce simulation with **IBIS-AMI** and **DFE**

- Intended audience:
  - **Familiar** with prior DDR specifications
  - Want to see the **major updates** in DDR5
  - Jump into **simulation**

- DDR4 is fast
  - DDR5 is ***blazing***
  - Tables in JESD79-5 have placeholder text to **8400 MT/s!**

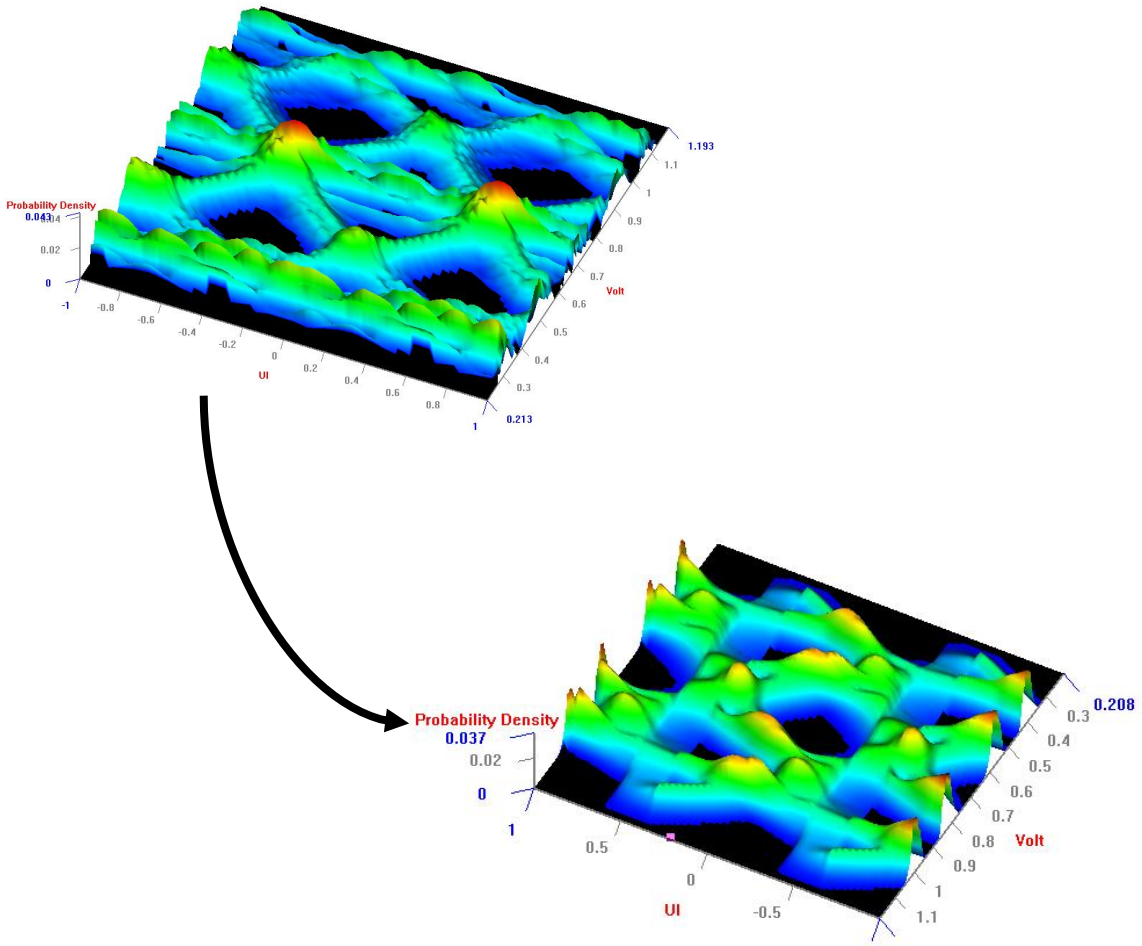
- Many clever features are employed to gain functionality
  - **Better** but not significantly **different** – basic architecture unchanged
  - **Not** (yet) using **differential** signaling for data
  - Package sizes and **pinouts** are similar
  - Advances require **alternate approach** to simulation and analysis



Data from Wikipedia: https://en.wikipedia.org/wiki/DDR_SDRAM

Outline

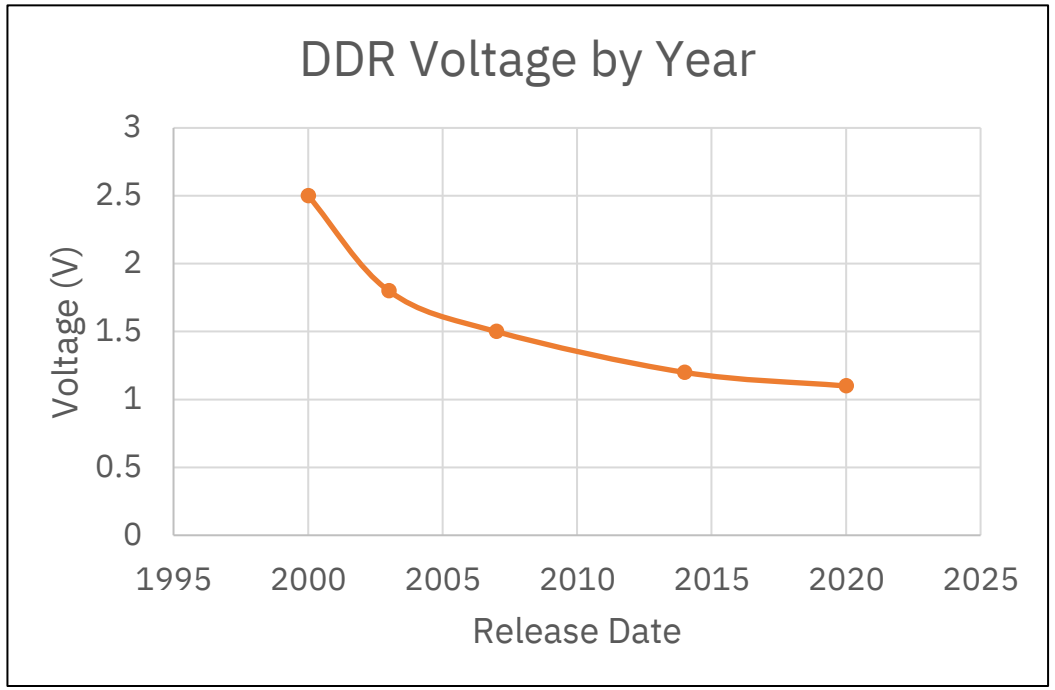
1. Major Changes from DDR4
    1. Reduced VDD/VDDQ
    2. CA Bus: Non-Specific Signal Names
    3. CA Bus: Internal Vref
    4. On-Die Termination Changes
2. New Features in DDR5
    1. VRM on DIMM
    2. Duty Cycle Adjuster
    3. On-Die ECC
    4. Decision Feedback Equalization
3. Simulation Example
    1. Full byte lane with DFE



1. Major Changes from DDR4

VDD/VDDQ to 1.1V

- DDR4 was 1.2V
- Sequence: VPP then VDD/VDDQ
  - Then RESET_n
- DC Operating Range: +6%/-3%
  - On all VDD/VDDQ/VPP
- PDN Impedance preliminary specification:
  - 10 mΩ from 2-10 MHz
  - 20 mΩ at 20 MHz



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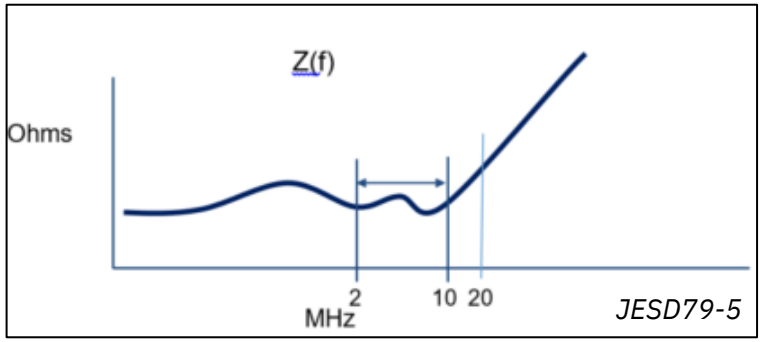


CA Bus: Non-Specific Signal Names

- DDR4 used specific pins: ACT_n, RAS_n, CAS_n, etc.
- DDR5 uses generic bus: CA[0..13]
- No pin-swapping allowed
  - Commands may be multi-cycle
  - But be aware of MIR pin (mirror) for clamshell configuration
    - Internally swaps even CA pin with next highest odd CA
- Biggest impact to the designer?
  - Easier schematic capture: simple bus connection
- Fewer CA pins mean more GND pins
  - Improved return path = better signal integrity

DDR5 command encoding[22][*final standard verification needed*]

Command	$\overline{CS}$	Command/address (CA) bits												
		0	1	2	3	4	5	6	7	8	9	10	11	12	13
Active (activate) Open a row	L	L	L	Row R0–3				Bank		Bank group			Chip CID0–2		
	H	Row R4–16													R17/ CID3
Unassigned, reserved	L	L	H	V											
	H	V													
Unassigned, reserved	L	H	L	L	L	V									
	H	V													
Write pattern	L	H	L	L	H	L	H	Bank		Bank group			Chip CID0–2		
	H	V	Column C3–10						V	$\overline{AP}$	H	V	CID3		
Unassigned, reserved	L	H	L	L	H	H	V								
	H	V													
Mode register write	L	H	L	H	L	L	Address MRA0–7								V
	H	Data MRD0–7							V	CW	V				
Mode register read	L	H	L	H	L	H	Address MRA0–7								V
	H	V								CW	V				
Write	L	H	L	H	H	L	$\overline{BL}$	Bank		Bank group			Chip CID0–2		
	H	V	Column C3–10						V	$\overline{AP}$	$\overline{WRP}$	V	CID3		
Read	L	H	L	H	H	H	$\overline{BL}$	Bank		Bank group			Chip CID0–2		
	H	V	Column C3–10						V	$\overline{AP}$	V		CID3		
Vref CA	L	H	H	L	L	L	Data								V

Data table from Wikipedia: https://en.wikipedia.org/wiki/DDR5_SDRAM

CA Bus Internal VREF

- DDR4 used external VREFCA
- DDR5 has internally generated VREFCA
  - Identical to VREFDQ
- Internally adjustable via register commands
  - From 45% to 97.5% of VDDQ
  - 0.5% increments
- Reduced PCB design requirements
  - No VTT/VREF regulator needed

Table 1 — DDR4 SDRAM X4/8 Ballout using MO-207

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c[3]				DM_n, DBI_n TDQS_t[2], (NC)[1]	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4 (NC)[1]	DQ2				DQ3	DQ5 (NC)[1]	VSSQ	D
E	VSS	VDDQ	DQ6 (NC)[1]				DQ7 (NC)[1]	VDDQ	VSS	E
F	VDD	(C2)[5] ODT1[6]	ODT				CK_t	CK_c	VDD	F
G	VSS	(C0)[5] CKE1[6]	CKE				CS_n	(C1)[5] (CS1_n)[6]	TEN (NC)[7]	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				A17 (NC)[4]	A13	VDD	N

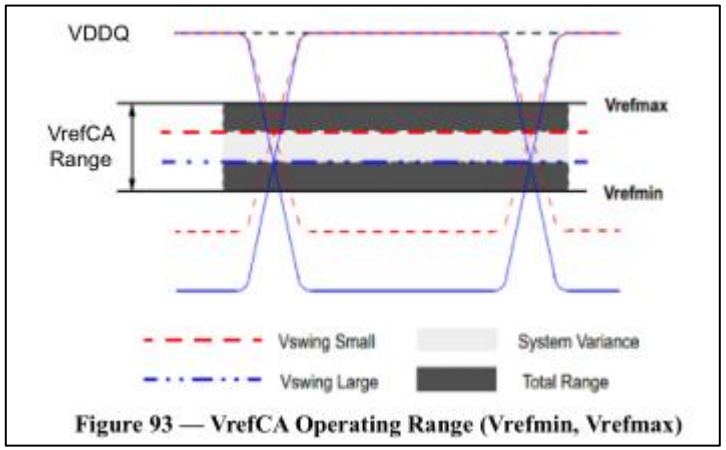
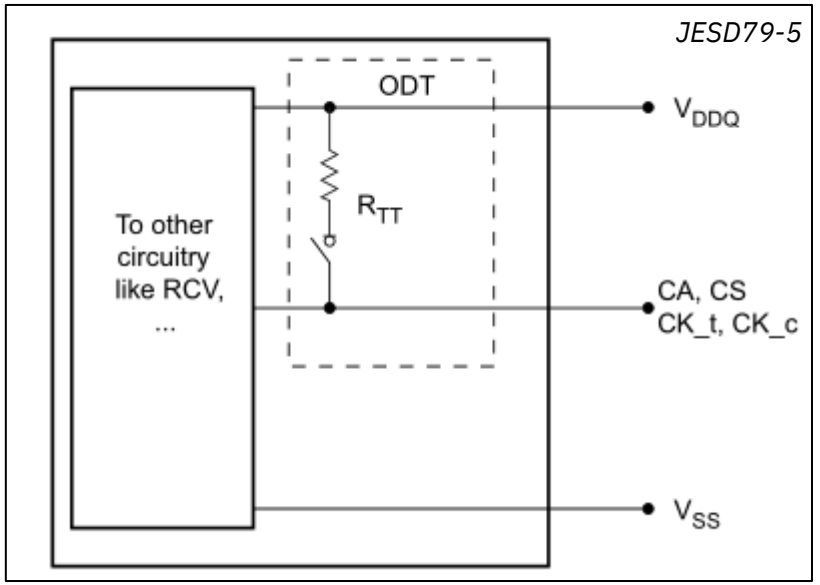


Figure 93 — VrefCA Operating Range (Vrefmin, Vrefmax)

JESD79-5

On-Die Termination Changes

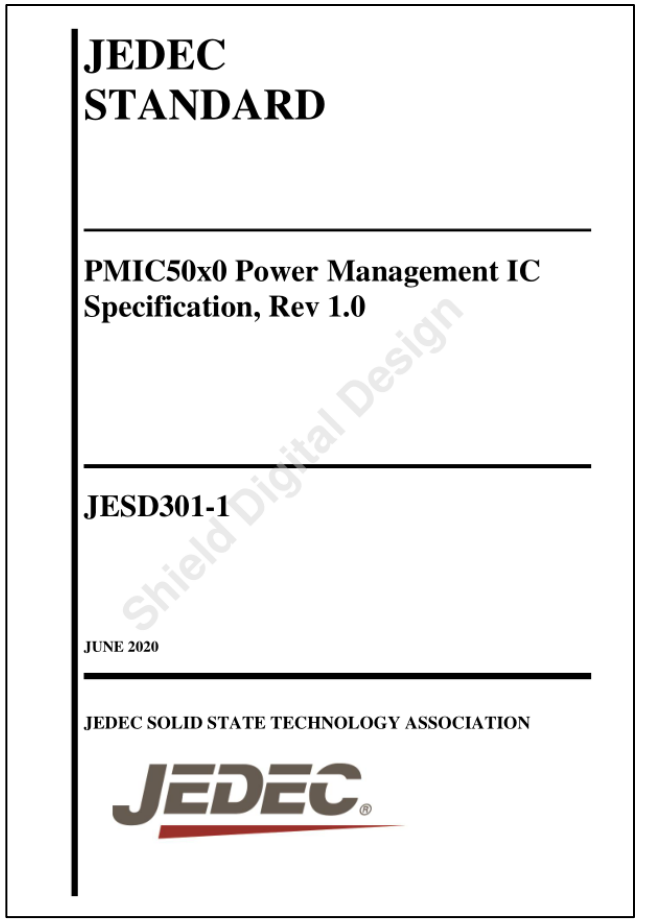
- All ODT is now fully command/register based
  - No dedicated ODT pin
- ODT is now available for CA bus
  - DQ/DQS still use direct routing from controller to DRAM
  - CA bus uses fly-by routing
- Pin CA_ODT allows different settings for end-of-group
  - Could use 40Ω for end device but ODT disabled for other devices



2. New Features in DDR5

VRM on DIMM

- Excellent for **power integrity**
  - DC (IR drop) and AC (PDN impedance)
- **Four SMPS, three LDO**
  - 15W of power
  - 4.25 – 15V input for SMPS, 3 – 3.6V input for LDO
  - OV protection for SMPS input
  - OV/UV/OC protection for SMPS output
  - ADC for voltage, current, temp measurement
- **Two management** interfaces
  - I2C or “I3C Basic”
    - I3C is a MIPI modification of I2C (open-drain or push-pull, faster data rates)
    - Same pins for both


JEDEC
STANDARD

PMIC50x0 Power Management IC
Specification, Rev 1.0

JESD301-1

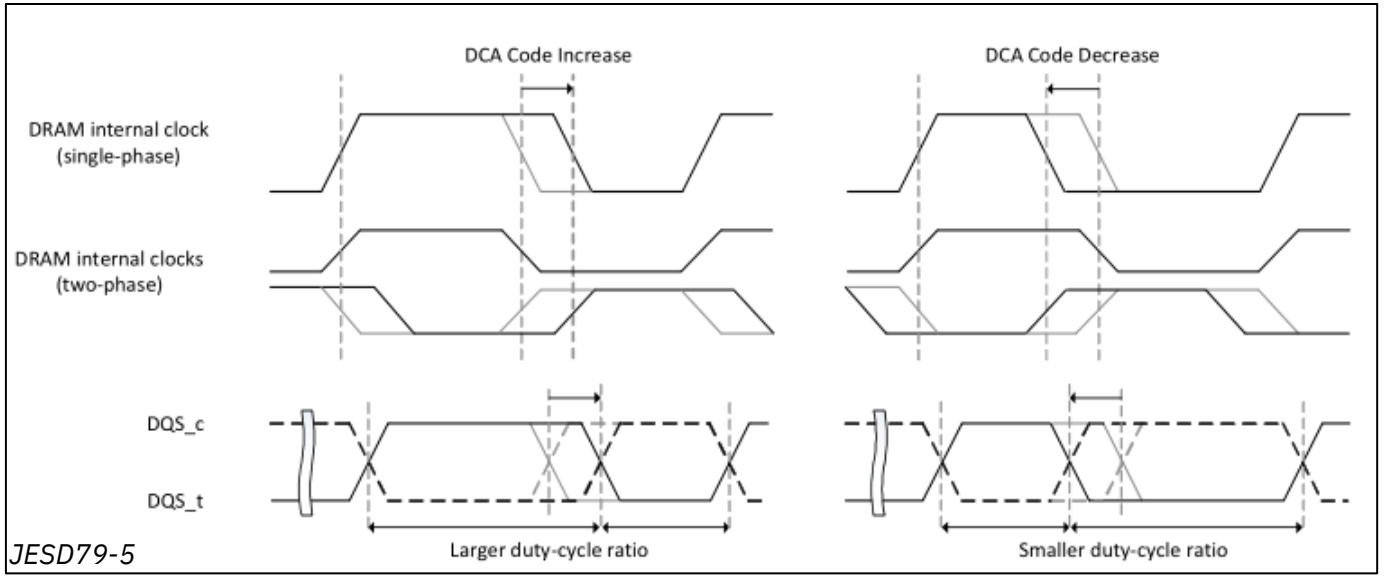
JUNE 2020

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

JEDEC

Duty Cycle Adjuster

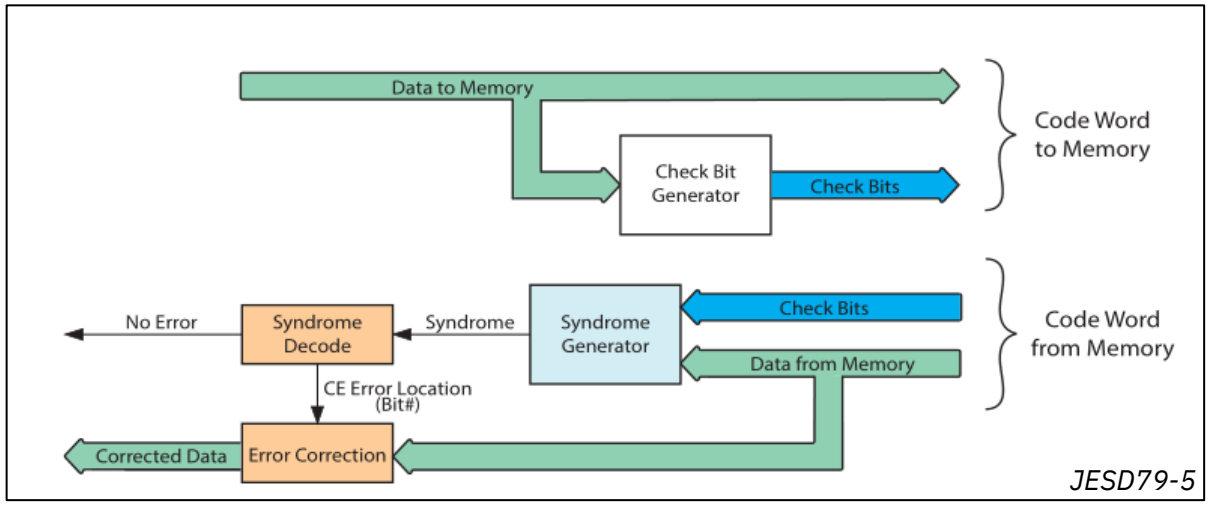
- Memory controller can **adjust** DRAM internal DQS/DQ duty cycle
  - Compensate for duty cycle error of all DQS/DQ
- Register-adjustable in **8-steps each**, positive and negative
- 28 to 56 ps adjustment **range**
- **Global or per-pin** adjustment

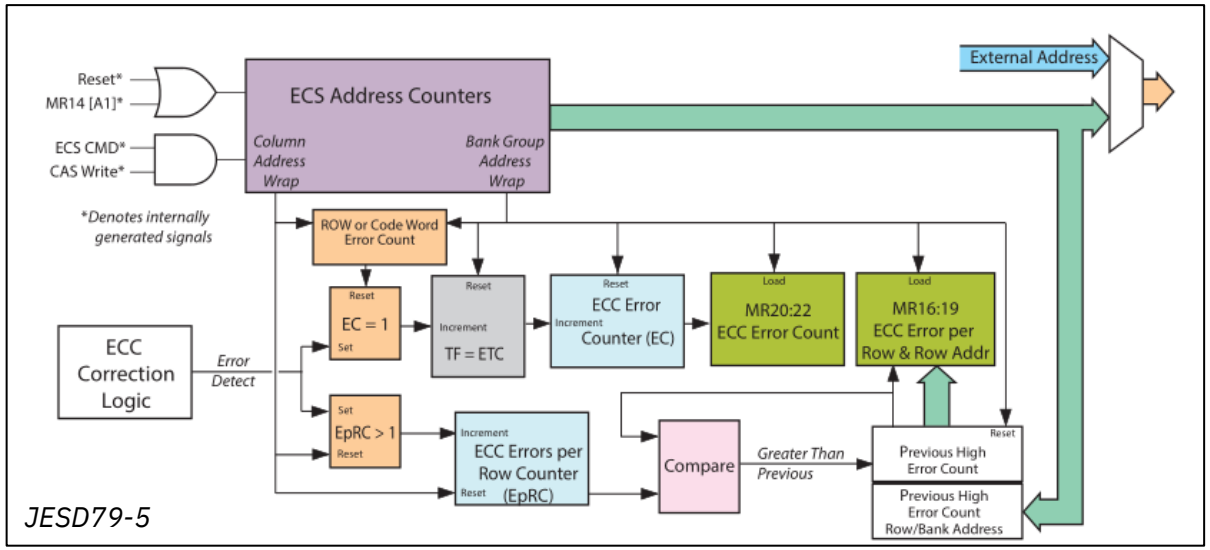


On-Die ECC

- Single Error **Correction**
- 128 data bits, 8 ECC check bits
- DRAM **dynamically corrects** single-bit errors
- Error **counting**/tracking

On-Die ECC Block Diagram

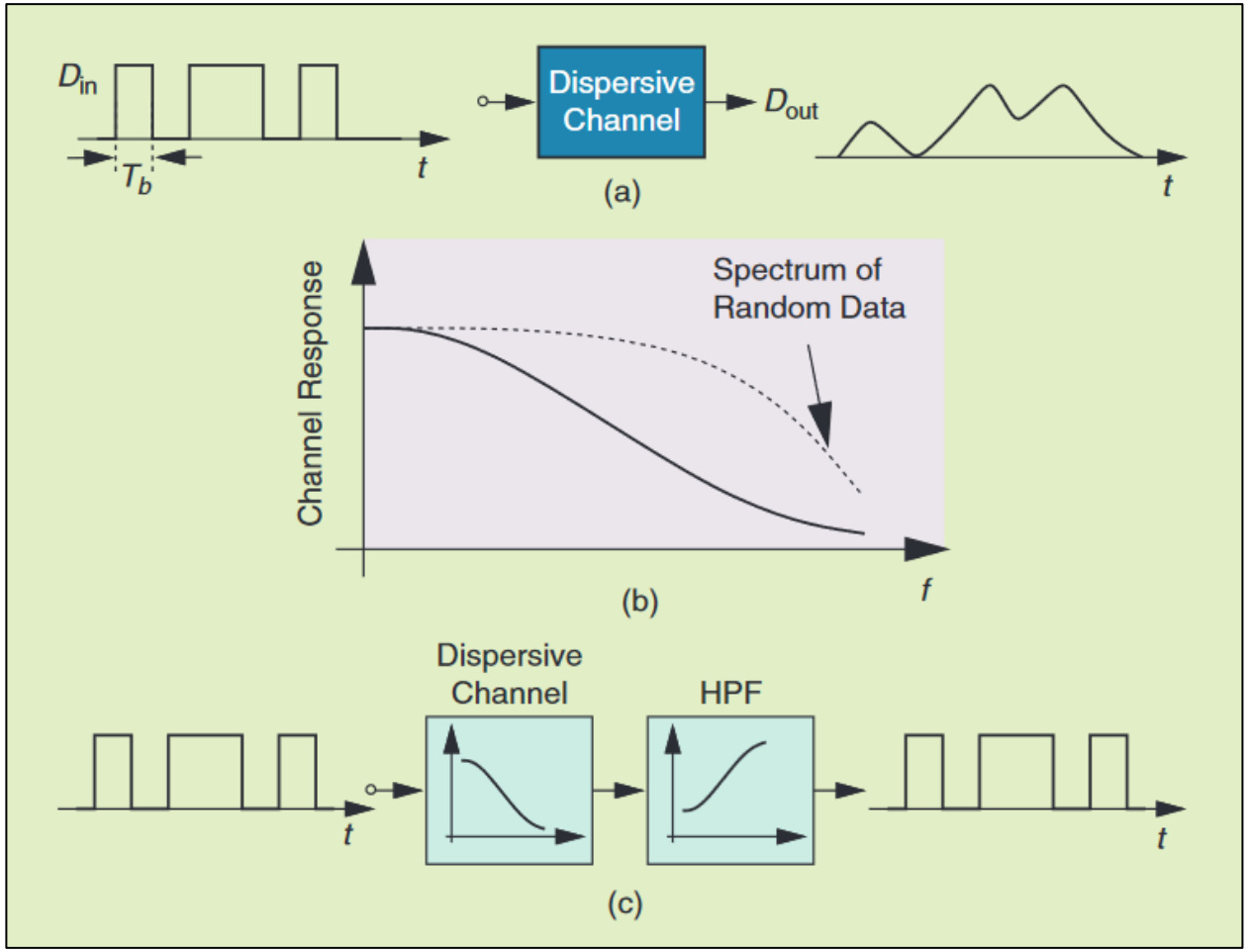




ECC Transparency and Error Scrub Block Diagram

Decision Feedback Equalization

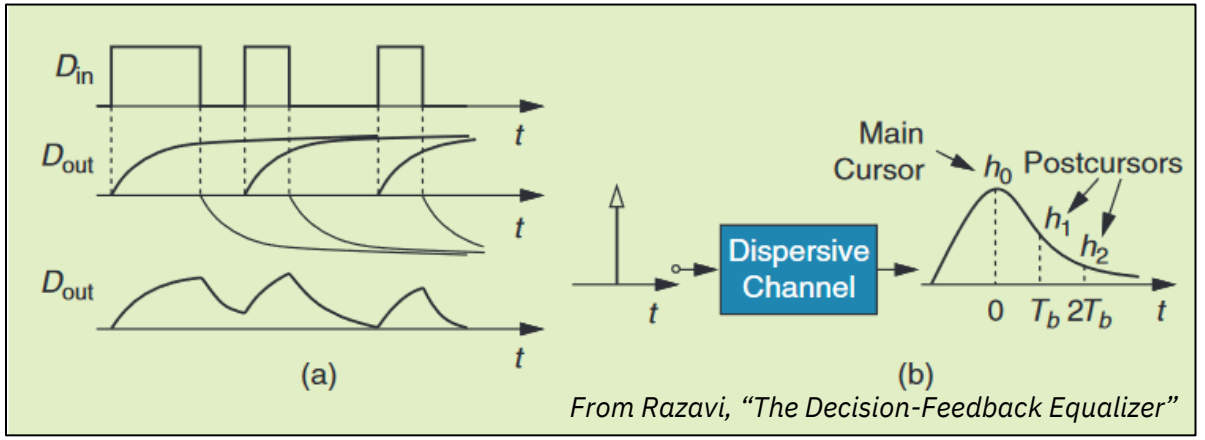
- **ISI** increases and eye closes
  - Due to higher data rates (at or above 3200 MT/s)
- Memory channels are **reflective**
  - Due to many impedance discontinuities
- Provides a high frequency **boost**
  - Compensates for channel loss



From Razavi, "The Decision-Feedback Equalizer"

Decision Feedback Equalization

- Approximate **linear equalization** with FIR filter
  - Only **linear** stages (delay and scaling)
- Typical pros/cons of DFE
  - No amplification of **noise** (such as CTLE)
  - **No pre-cursor** equalization
- Remove **scaled interference** from four previous bits
  - Based on the channel impulse response
  - Four bits in a 4-tap DFE



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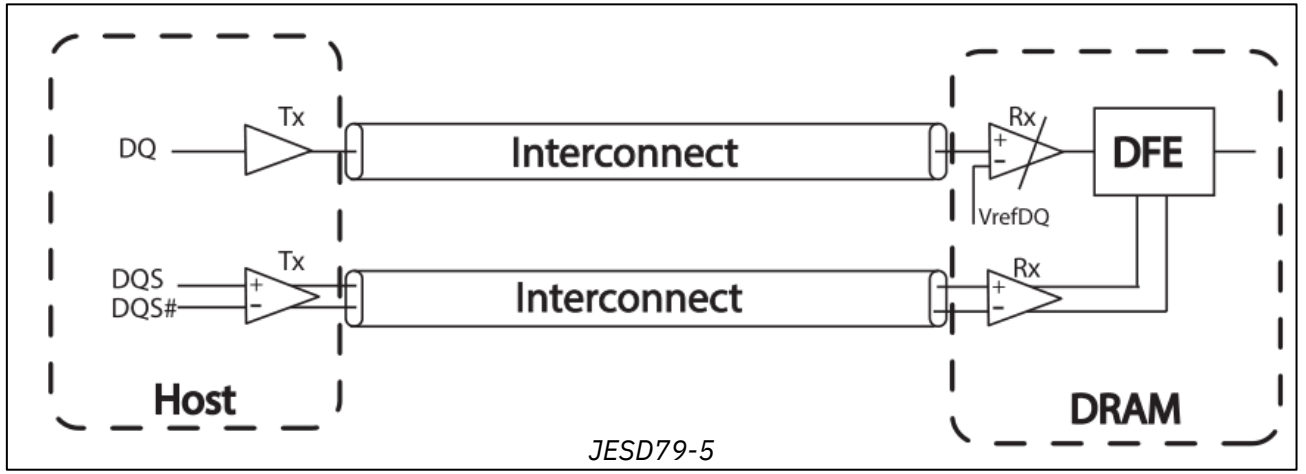
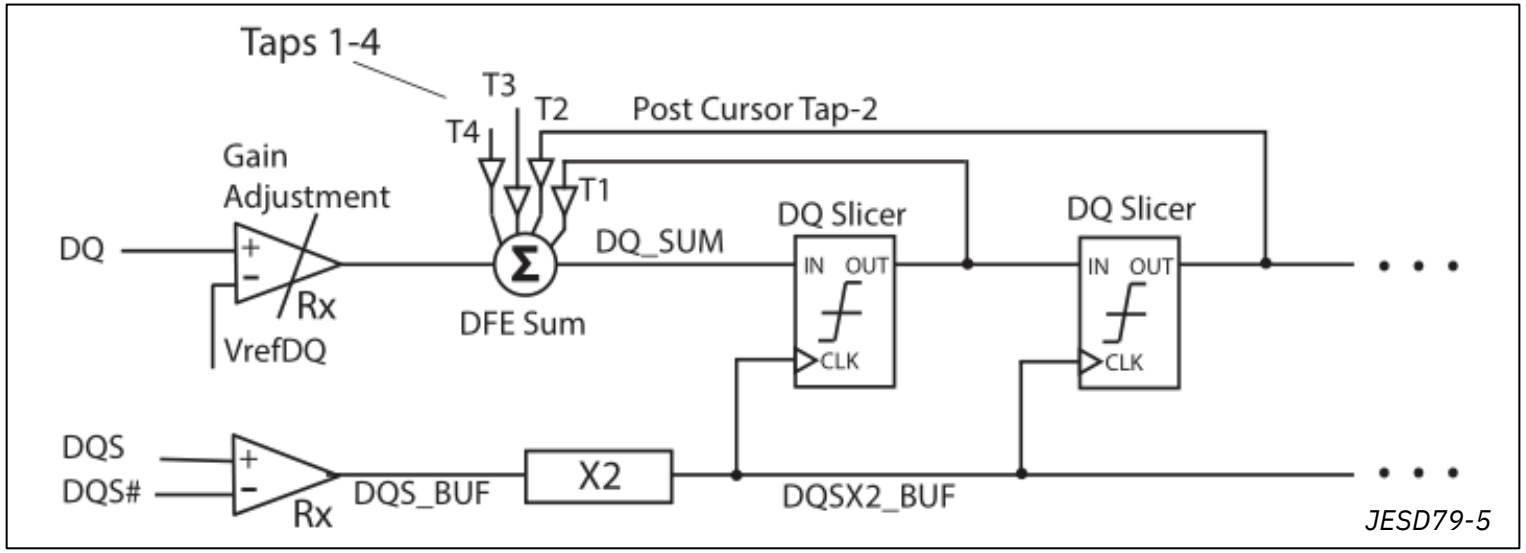


JESD79-5

Decision Feedback Equalization

- **4-Tap DFE** equalizes DQ signals
- May implement 1-way, 2-way or 4-way **interleaved** DFE
  - 1-way shown below
  - Interleaving reduces slicer clock rate (and power)
- Gain Bias:
  - **-6 dB to +6 dB**



Bringing It All Together: Simulation

- DDR5 made things better with DFE
  - But with increased data rate, **simulation is a must** to ensure successful system design

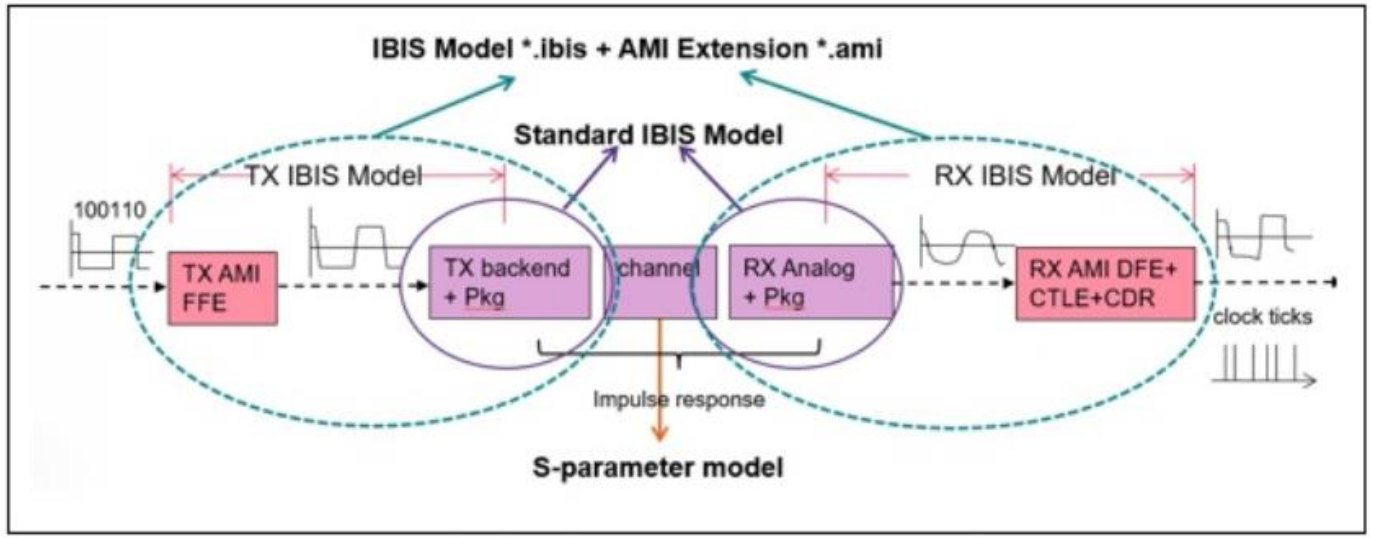
- Questions arise:
  - Advanced processing is on-chip with DFE, how do we simulate this?
  - Is a vendor AMI model required?
  - Will my power distribution network design withstand the faster switching speed?

- In order to answer the question: **“How do you know it will work?”**
  - We will incorporate both IBIS-AMI and power-aware simulation

3. DDR5 Simulation

What is IBIS-AMI?

- Algorithmic Modeling Interface
- Extends traditional IBIS (behavioral models)
  - Equalization and other non-LTI effects
  - Ultra-low BER (statistical simulation)
  - Package sNp models
- Statistical simulation based on channel pulse response, or
- Time-domain simulation



https://www.signalintegrityjournal.com/articles/2020-back-to-basics-ibisibis-ami-and-the-path-to-lpddr5

Demo: Plan

- Simulate one byte lane (DQ + DQS)
  - 6400 MT/s
  - 10” PCB trace model
  - DFE on the receiver
  - Verify minimum eye height/width meets spec (70mV/0.25UI at BER > 1E-16)

Demo: Setup and PCB

- Prep: Have IBIS model in a clean directory ready to use
- Open TopXplorer, start a new topology
  - Menu: Topology->New
- Create a SystemSI/Parallel Bus Analysis/Blank
- Add CTRL IBIS, MEM IBIS
- Add Trace Model
  - Edit Trace, Microstrip:
    - 10x, 4mil width, 4mil space, 0.7mil thickness, 4mil substrate
      - System has extremely tight density requirements and cannot use up more area
    - Length: 10000mil
    - Include Power
  - Edit VRM: Voltage range: 1.1 V Typical; 1.067 to 1.166 V

Demo: Controller IBIS

- Load IBIS
  - Select component “DDR5_Controller”
  - Check “Explicit IO Power/Ground Terminals”
  - Verify the Bus Definitions
- Select CTRL IBIS
  - Uncheck “Ideal Power”
  - Check “Package Parasitics”
- Redo same steps for receiver (Don’t forget to select receiver component)

Demo: Connections

- Controller side:
  - Verify power and grounds connected
  - Select DQ0 to DQ7 and A-H, right click and “Connect by pin pair”
  - Same with DQS0 P/N and I/J
- Follow same steps between trace and receiver

Demo: Simulation Setup

- Check “Use Channel Simulator”
- Check Connectivity, verify magnitude is ~0.8
- Set timing budget
  - Set data rate to 6.4 Gbps
- Set Analysis Options
  - Corner – Keep only Typ selected
  - Bus Simulation – select write only
  - Channel Sim – No change
  - IO Models:
    - Change stimulus to PRBS32
    - Verify DQS still 01/10
  - Change bits to display: Last 1000
  - Change jitter to include both RJ and DJ
  - Check only DQ0 and DQS P/N (Too long to run simulate all)

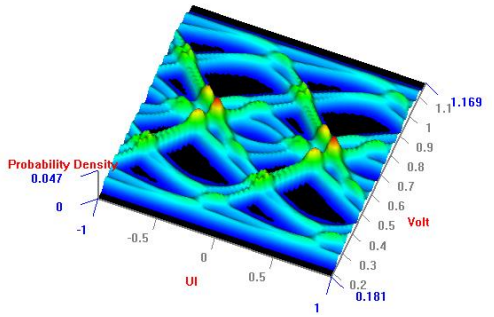
Demo: Simulate

- Save Topology
- Enable Distributed and Set up Resources (Default)
- Run (Note: takes 2.5min on my machine)

- **Poll Question**

Demo: Simulate

- Save Topology
- Enable Distributed and Set up Resources (Default)
- Run (Note: takes 2.5min on my machine)
- Eye is closed
- NOTE: Mention that this configuration wouldn’t have worked with DDR4, but with the new addition of DFE to DDR5 we can make it work at even higher data rates



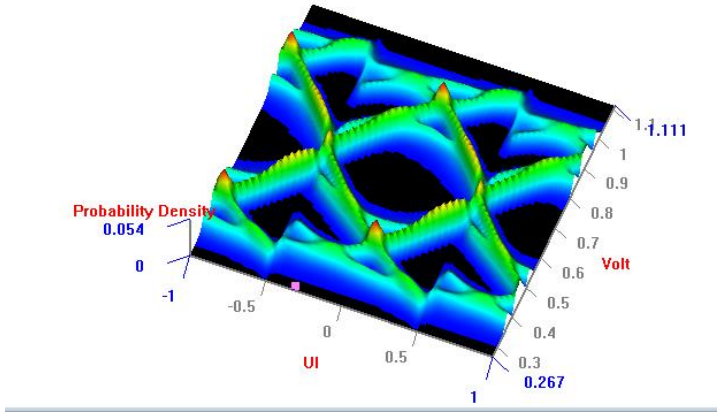
Demo: Add DFE

- Right-click the MEM IBIS and choose “Add AMI”
- Select the included “Memory Licensed” AMI/DLL files
- Review the DFE tap settings (4-tap for DDR5)
- Re-run

- **Poll Question:**

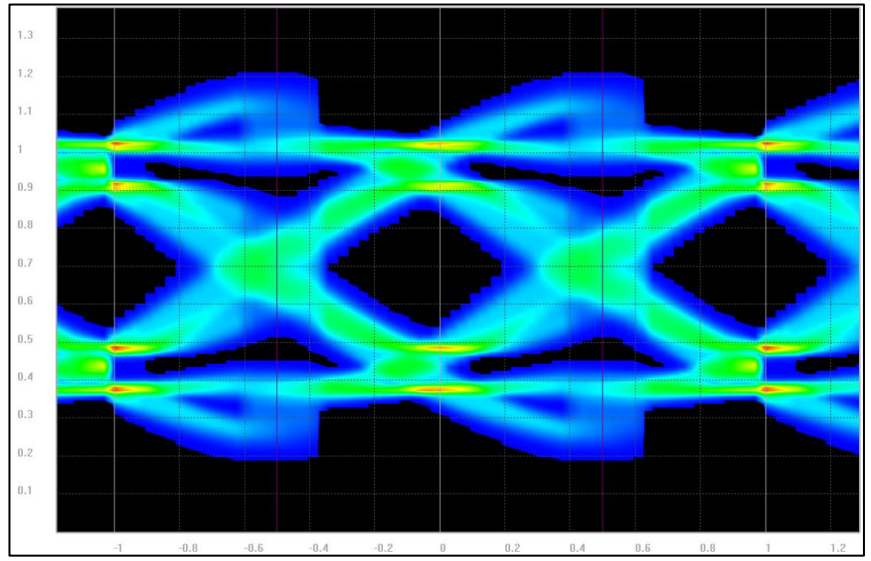
Demo: Add DFE

- Right-click the MEM IBIS and choose “Add AMI”
- Select the included “Memory Licensed” AMI/DLL files
- Review the DFE tap settings (4-tap for DDR5)
- Re-run
- Results in a wide-open eye (0.54UI/140mV at BER of 1E-16)
  - Meets our requirements



Conclusion

- DDR5 is a **major** performance improvement
  - Speeds from 3200 MT/s up to 8400 MT/s
- More **complex** simulation than DDR4
- Tools exist which can ensure **successful** design of your DDR5 system



References

1. JEDEC JESD 79-5, DDR5 Specification
    1. https://www.jedec.org/system/files/docs/JESD79-5.pdf
2. JEDEC JESD 79-4, DDR4 Specification
    1. https://www.jedec.org/system/files/docs/JESD79-4.pdf
3. JEDEC JESD 301-1 PMIC Specification
    1. https://www.jedec.org/system/files/docs/JESD301-1.pdf
4. Micron DDR5: Key Module Features
    1. https://media-www.micron.com/-/media/client/global/documents/products/technical-marketing-brief/ddr5_key_module_features_tech_brief.pdf
5. Razavi, *The Decision-Feedback Equalizer*
    1. https://www.seas.ucla.edu/brweb/papers/Journals/BRFall17DFE.pdf

Thank you!