

Differential Pin Pair Visibility for Logic Assignment and Routing

Product Version 16.6
December 21, 2015

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Purpose

Designs very often use hundreds or thousands of differential pairs. This document describes a new OpenGL feature that addresses the challenges in visualizing differential pair information and differential “mates” once there are many of them close together in the design. This feature is available in Allegro® PCB Editor, Cadence® SiP Layout, and Allegro® Package Designer (APD). This method enables differential pin-pair markers.

Audience

This document is intended for IC and board designers and engineers using any or all of Allegro PCB Editor, SiP Layout, and APD.

Overview

Differential signaling has become the norm supporting all sorts of digital interface protocols across IC packages and boards. Designers have to manage hundreds and thousands of differential pairs that need to be properly assigned and then constrained for routing.

One of the main challenges when dealing with differential signals in the layout part of the differential interface is visualizing the differential pair information and the differential “mates” once there are many of them close together in the design. Categorizing the differential pair signals themselves as also the differential pin pair mates is a challenging task.

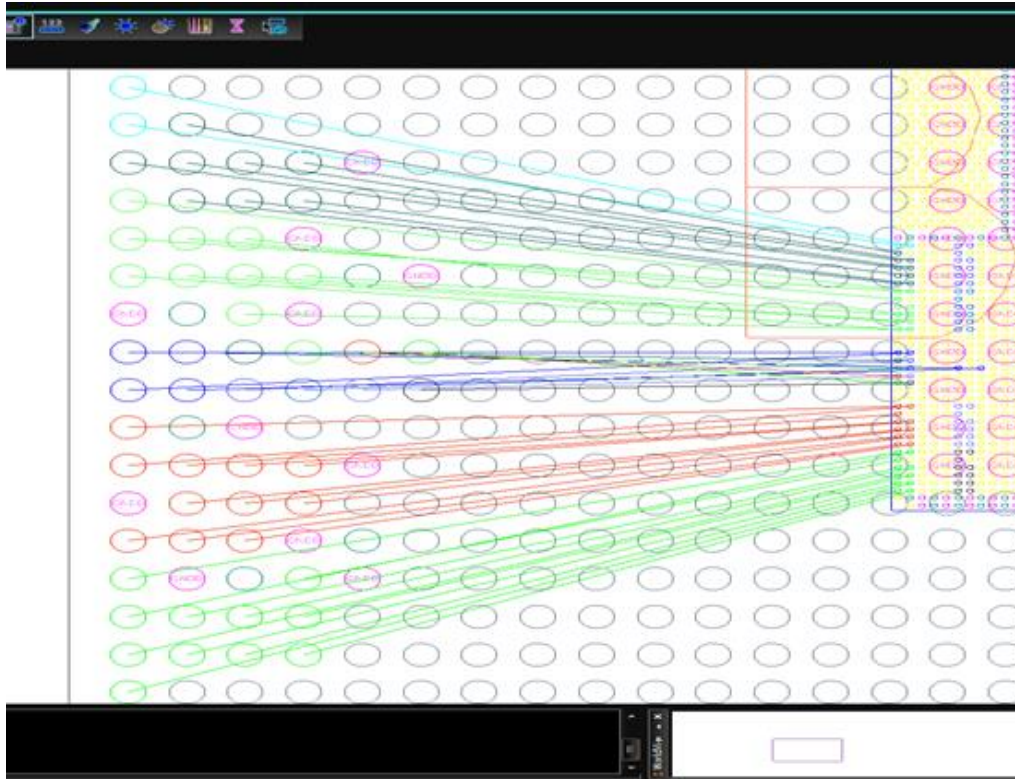
One way of visualizing differential signals and their pin pair mates is to use color-coding schemes. However, this method fails when dealing with hundreds of differential pairs in your design.

The following example uses DDR3 on a package substrate and byte lane. The example shows an early signal assignment planning from bump to ball mapping.

Using the color-coding method, a typical approach would be to assign a unique color to the byte lane of interest, address, command/control, and so on.

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The following image shows color-coded byte lanes:



The main issue with the color-coded approach is identifying the differential strobe on each of the byte lanes without having to add another special color.

A very simple way is to use the new OpenGL-based feature available in Allegro® PCB Editor, SiP Layout, and Allegro® Package Designer (APD).

Enabling the differential pin-pair marker

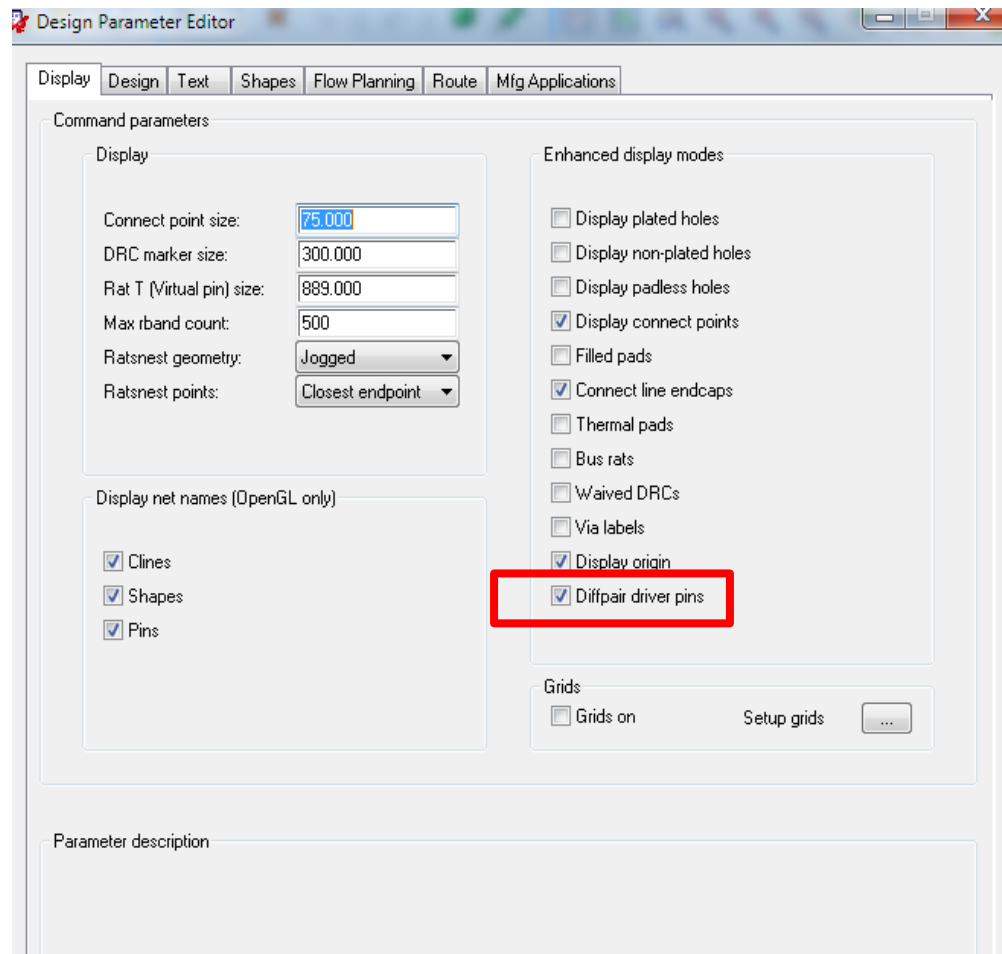
Using the new OpenGL-based feature, you can visually display the diff pair pin pairs by adding a differential *marker* between the pin pairs. This feature lets you quickly isolate the differential pin pairs of interest whether you are assigning or optimizing a byte lane or hundreds of differential signals.

To enable the differential pin-pair marker setup, do the following steps:

1. Create your differential pairs. Choose *Logic -- Assign Differential Pair* or use Constraint Manager.
2. Choose *Setup -- Design Parameters*.

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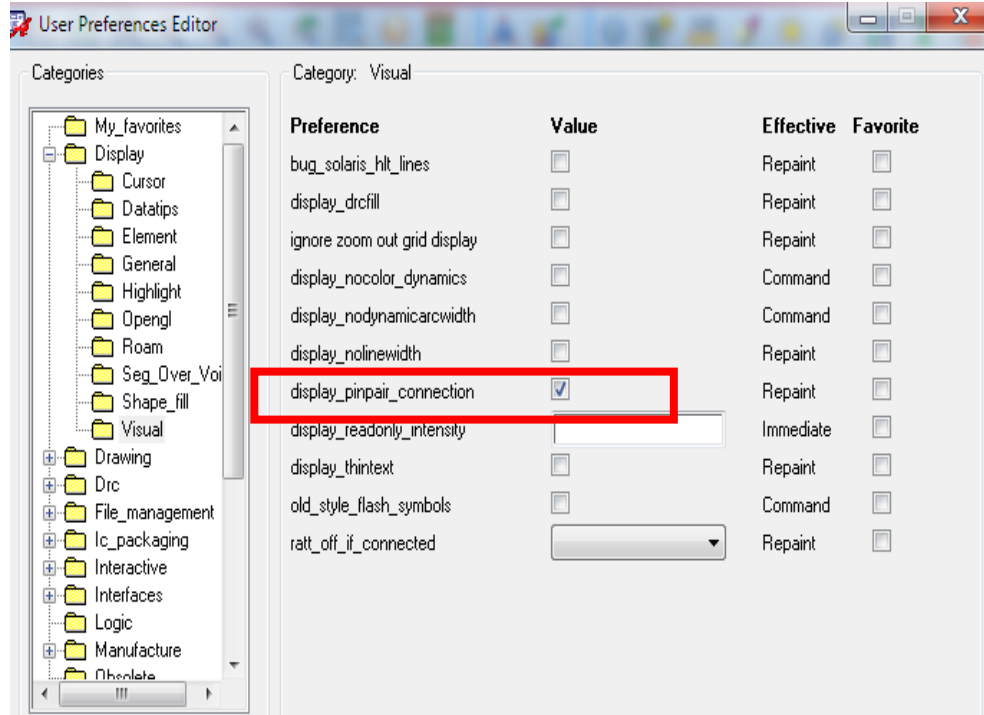
3. Select *Diffpair driver pins*.



4. Choose Setup -- User Preferences

Differential Pin Pair Visibility for Logic Assignment and Routing

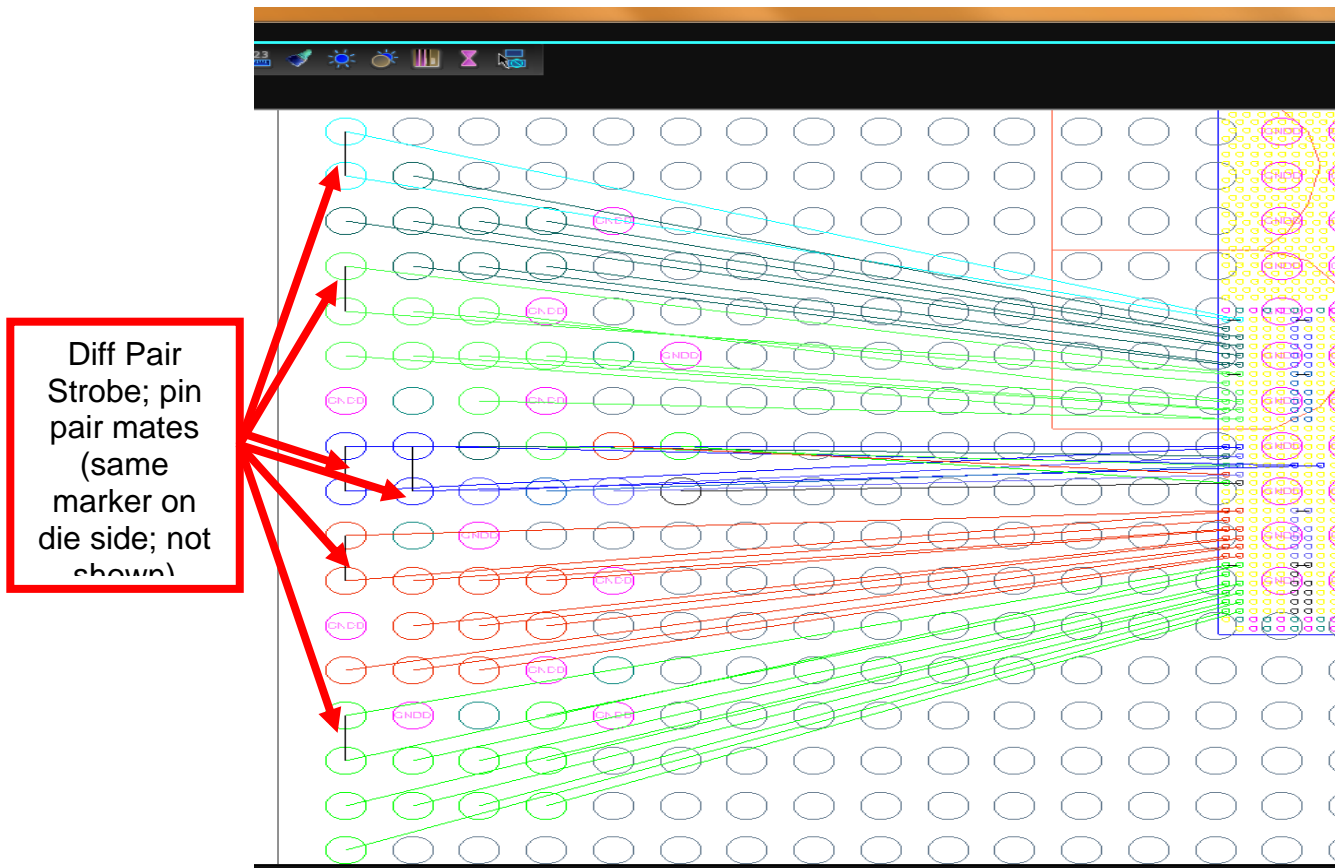
5. Select *display_pinpair_connection* under *Display – Visual* category.



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6. Close User Preferences Editor.

The differential pin pair markers will be visible as shown below.



Support

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