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How to create a symbol from SiP and import into Virtuoso

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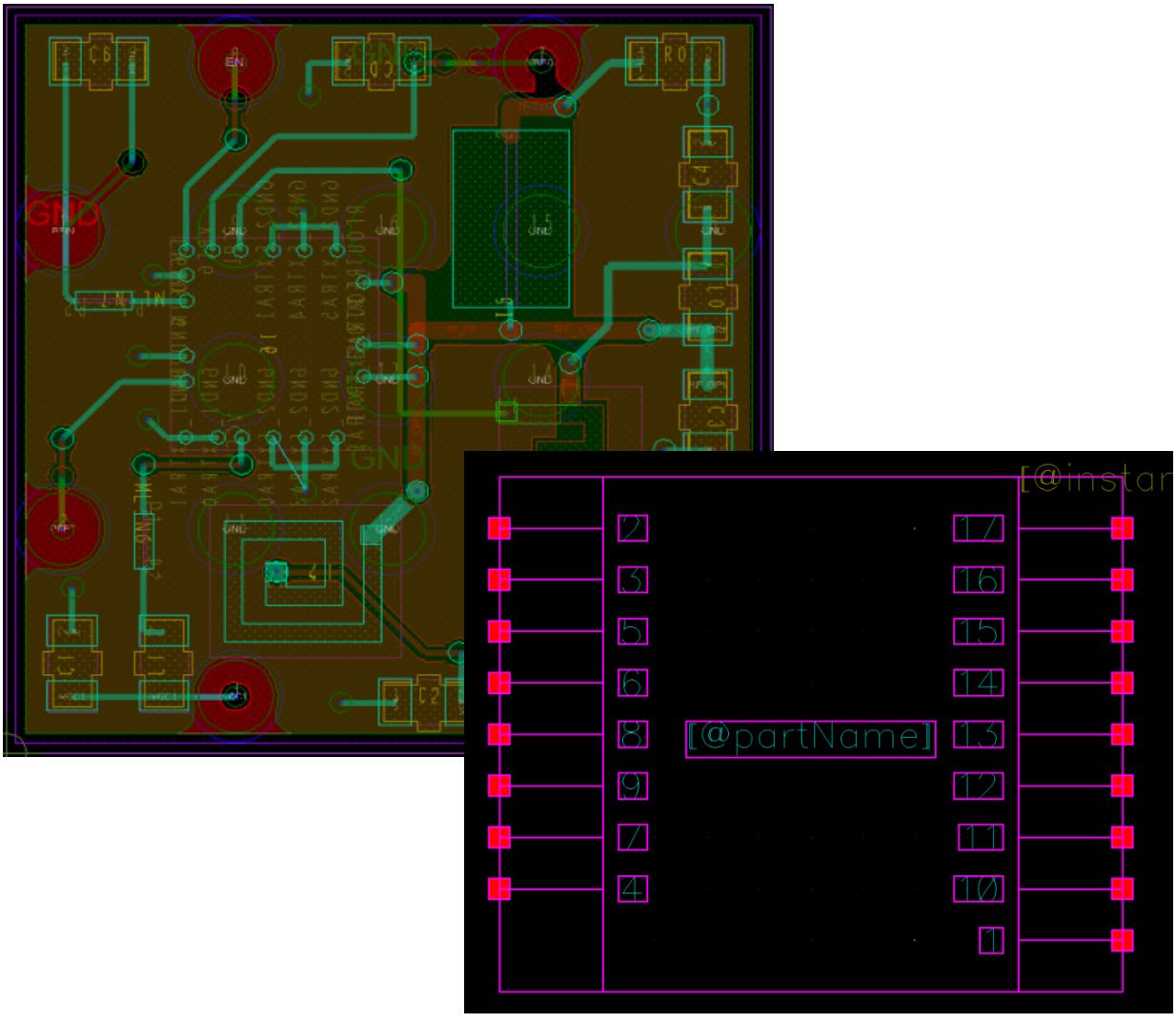

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Purpose

This Application Note will help you to create a BGA, LGA, or another package symbol in the Linux environment, and import them into Virtuoso to use in Virtuoso® Schematic Editor. This needs to be used with VSDP/VMT or VRF.

This document will help designers use chips and connectivity from SiP Layout to create a symbol it Virtuoso. This will save time and let users create a library of the part needed in the design.

Audience

This document is intended for layout designers who are experience with VSDP, Virtuoso and need to import the schematic symbols from SiP Layout such as BGA, LGA or any other non-logic symbol.

Terms

VSDP	Virtuoso System Design Platform
VSE	Virtuoso Schematic Editor
VMT	Virtuoso Multi-Technology
VRF	Virtuoso Radio Frequency

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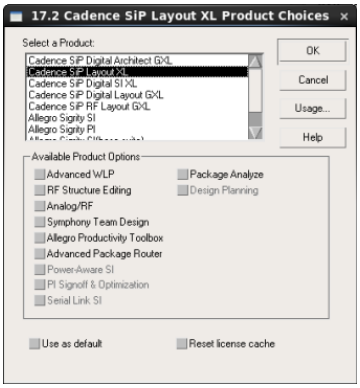
Creating chips and connectivity files

1. Start SiP Layout in Linux by typing `cdnsip &` at the terminal command prompt.

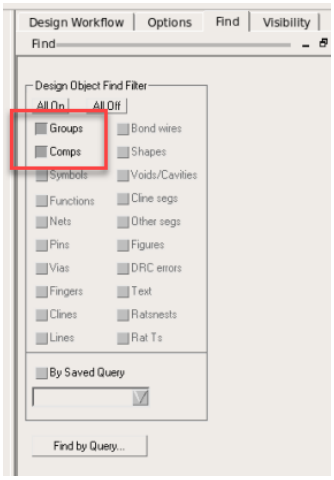
2. When SiP Layout is opening, you will see the following dialog. Select the **Cadence SiP Layout XL** license and select **OK**.

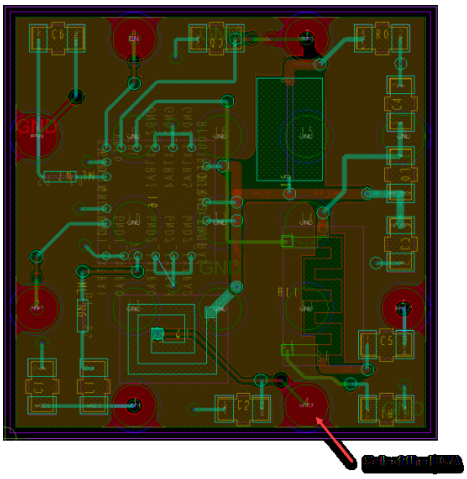


3. Open the design by going to **File > Open** and browse to **PA_VRF_Layout_routed.sip**.

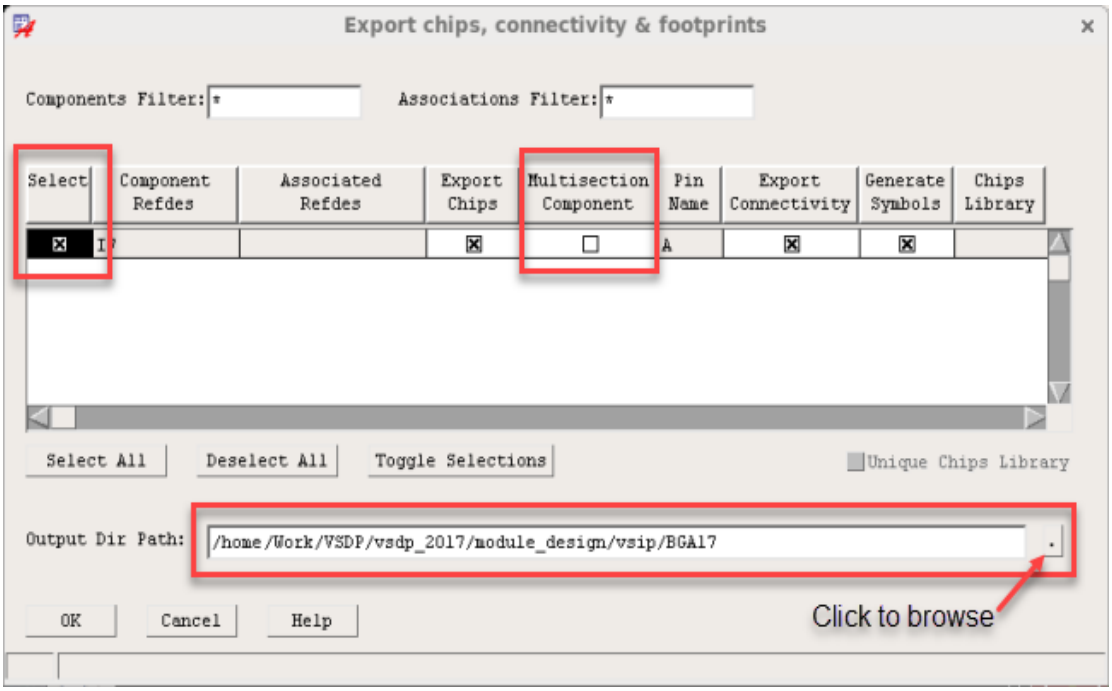
4. Once the file is loaded, go to **File > Export > Chips and Connectivity**.

5. In the **Design Object Find Filter**, make sure only **Groups** and **Comps** are selected. Select the BGA in the design canvas. A dialog will appear.





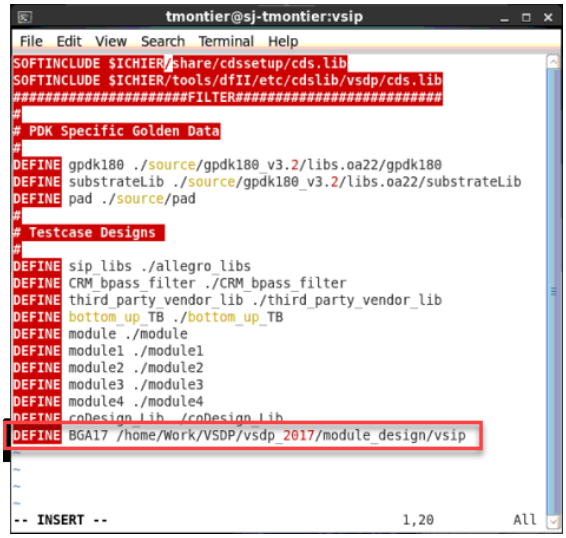
6. Make sure to check the **Select** box and to uncheck the **Multisection Component** checkbox. Next, you will add **Output Dir Path** by browsing to the directory to which you want the files to go. Make sure you create a **BGA17** directory at the root of the design.



7. Select **OK** and the files will be created.

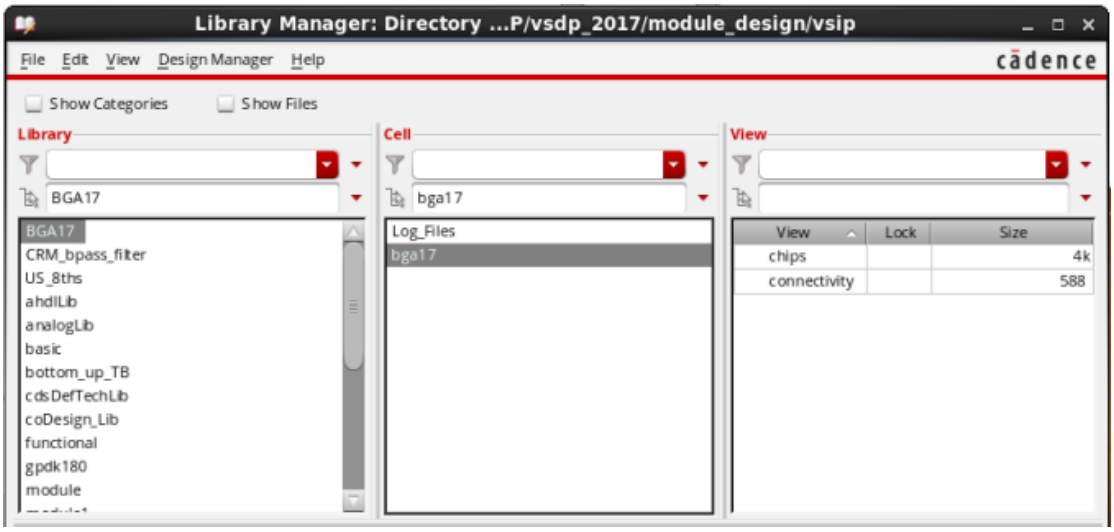
Importing chips and connectivity files

1. First, you will need to add the library location to the **cds.lib** file. It is done by editing the **cds.lib** file.



2. Next, make sure you are in the startup directory (for example, /home/Work/VSDP/vsdp_2017/module_design/vsip/). In the terminal command prompt, type `Virtuoso -sdp &` to start the program (if you are using VSDP).

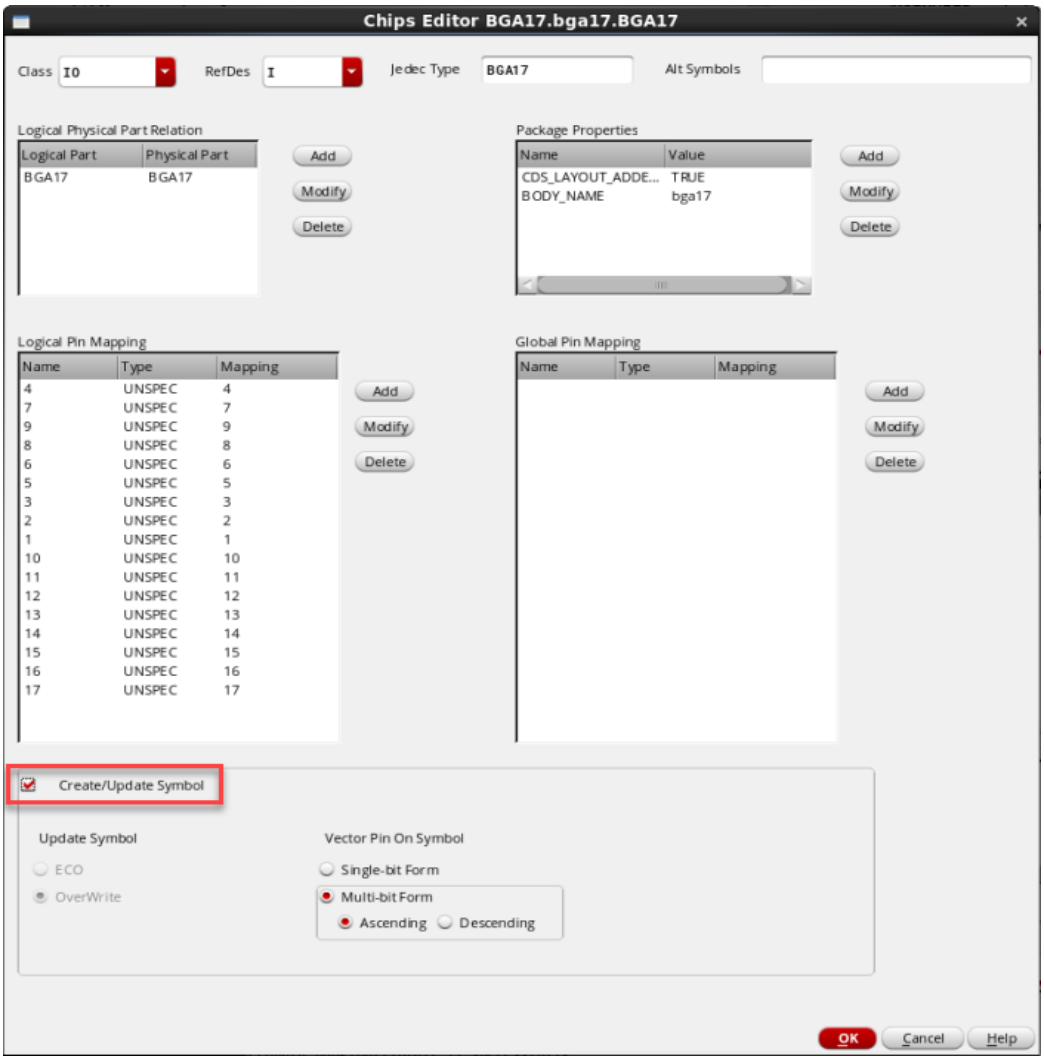
3. Once the Virtuoso is open, go to the menu and select **Tools > Library Manager**. The Library Manager will be open.



4. Double-click on the **BGA17** library and then the **bga17** cell. You will notice the **chips** and the **connectivity** views.

5. Double-click on the **chips** view. Click **OK**.

6. The Chips Editor dialog box will come up. Then, select the **Create/Update Symbol** checkbox.



7. Select **OK**. Then, select **Yes** and **OK** in the BIDIR pin dialog. Select **Yes** and **OK** in the second dialog to create the symbol.

8. In the **Library Manager**, you will notice that the symbol and other supporting views have been created. Double-click on the **symbol** view. The symbol will open.

9. Close the view by selecting **File > Close**.

Summary

In this document, you learned to create the chips and connectivity files from SiP Layout and import the chips file into Virtuoso to create the symbol file.

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