cādence[®]

How to create a symbol from SiP and import into Virtuoso

Product Version SPB17.2 and IC6.1.7 May 2019



Copyright Statement

© 2019 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence and the Cadence logo are registered trademarks of Cadence Design Systems, Inc. All others are the property of their respective holders.

Contents

Purpose	4
Audience	4
Terms	4
Creating chips and connectivity files	5
Importing chips and connectivity files	7
Summary	9
Support	9
Feedback	9
Importing chips and connectivity files Summary Support Feedback	7 9 9 9

Purpose

This Application Note will help you to create a BGA, LGA, or another package symbol in the Linux environment, and import them into Virtuoso to use in Virtuoso® Schematic Editor. This needs to be used with VSDP/VMT or VRF.

This document will help designers use chips and connectivity from SiP Layout to create a symbol it Virtuoso. This will save time and let users create a library of the part needed in the design.

Audience

This document is intended for layout designers who are experience with VSDP, Virtuoso and need to import the schematic symbols from SiP Layout such as BGA, LGA or any other non-logic symbol.

Terms

VSDP	Virtuoso System Design Platform
VSE	Virtuoso Schematic Editor
VMT	Virtuoso Multi-Technology
VRF	Virtuoso Radio Frequency

Download

Testcase database and references can be found at 'Attachments' and 'Related Solutions' sections below the PDF. This pdf can be searched with the document title on <u>https://support.cadence.com</u>

Creating chips and connectivity files

- 1. Start SiP Layout in Linux by typing cdnsip & at the terminal command prompt.
- 2. When SiP Layout is opening, you will see the following dialog. Select the **Cadence SiP Layout XL** license and select **OK**.



- Open the design by going to File > Open and browse to PA_VRF_Layout_routed.sip.
- 4. Once the file is loaded, go to File > Export > Chips and Connectivity.
- 5. In the **Design Object Find Filter**, make sure only **Groups** and **Comps** are selected. Select the BGA in the design canvas. A dialog will appear.



 Make sure to check the Select box and to uncheck the Multisection Component checkbox. Next, you will add Output Dir Path by browsing to the directory to which you want the files to go. Make sure you create a BGA17 directory at the root of the design.

Learn more at Cadence Support Portal - https://support.cadence.com © 2019 Cadence Design Systems, Inc. All rights reserved worldwide.



7. Select **OK** and the files will be created.

Importing chips and connectivity files

1. First, you will need to add the library location to the **cds.lib** file. It is done by editing the **cds.lib** file.

R		tmo	ntier@sj	tmonti	er:vsip		_ 0	×
File	Edit Viev	v Search	Terminal	Help				
SOFTIN	ICLUDE \$1	CHIER <mark>/</mark> sha	re/cdsse	tup/cds	.lib			6
SOFTIN	ICLUDE \$1	CHIER/too	ls/dfII/	etc/cds	lib/vsd	o/cds.lib		
#	*****	, <i></i>	'ILIEK###	*******	******	*****		
# PDK	Specific	: Golden D	ata					
#								
DEFINE	gpdK180) ./SOUFCE	/gpdk180	V3.2/L	1DS.0a22	2/gpdk180	tratel ib	
DEFINE	pad ./	source/pad	l l	0K100_0	5.2/ (10:	5.0022/5005	CIGCELLD	
#								
# Test	case Des	signs						
# DEETNE	sin li	os /alleo	ro libs					
DEFINE	CRM bpa	ass filter	./CRM b	pass fi	lter			
DEFINE	third_p	party_vend	lor_lib ⁻ .	/third_	party_ve	endor_lib		1
DEFINE	bottom	_up_TB ./t	ottom_up	TB				
DEFINE	module	./module	1					
DEFINE	module2	2 ./module	2					
DEFINE	module:	3 ./module	3					
DEFINE	coDesid	+./module	aDesian	Lib				
DEFINE	BGA17	/home/Work	/VSDP/vs	dp_2017	/module	design/vsi	р	
~								
~								
~								
INS	ERT					1,20	Al	ι 🧧

- 2. Next, make sure you are in the startup directory (for example, /home/Work/VSDP/vsdp_2017/module_design/vsip/). In the terminal command prompt, type <code>Virtuoso -sdp &</code> to start the program (if you are using VSDP).
- 3. Once the Virtuoso is open, go to the menu and select **Tools > Library Manager**. The Library Manager will be open.



4. Double-click on the **BGA17** library and then the **bga17** cell. You will notice the **chips** and the **connectivity** views.

Learn more at Cadence Support Portal - https://support.cadence.com © 2019 Cadence Design Systems, Inc. All rights reserved worldwide. 5. Double-click on the **chips** view. Click **OK**.



6. The Chips Editor dialog box will come up. Then, select the **Create/Update Symbol** checkbox.

Image: Construction of the symbol Index (Type) BGA17 At Symbols Image: Construction of the symbol Index (Type) Index (Type) Index (Type) Image: Construction of the symbol Index (Type) Index (Type) Index (Type) Image: Construction of the symbol Index (Type) Index (Type) Index (Type) Image: Construction of the symbol Index (Type) Index (Type) Index (Type) Image: Construction of the symbol Index (Type) Index (Type) Index (Type) Image: Construction of the symbol Index (Type) Index (Type) Index (Type) Image: Construction of the symbol Index (Type) Index (Type) Index (Type) Image: Construction of the symbol Index (Type) Index (Type) Index (Type) Image: Construction of the symbol Index (Type) Index (Type) Index (Type) Image: Construction of the symbol Index (Type) Index (Type) Index (Type) Image: Construction of the symbol Index (Type) Index (Type) Index (Type) Image: Construction of the symbol Index (Type) Index (Type) Index (Type) Image: Construction of the symbol <td< th=""><th>-</th><th>Chips Edit</th><th>tor BGA17.bga17.BGA17</th><th>×</th></td<>	-	Chips Edit	tor BGA17.bga17.BGA17	×
Logical Part Relation Image Parkage Properties Image Image BGA17 BGA17 Image	Class 10 Re	efDes I Jedec Type	e BGA17 Alt Symbols	
regical Fin Mapping Image: Construction of the symbol	Logical Physical Part Relation Logical Part Physical Par B GA 17 B GA 17	rt Add Modify Delete	Package Properties Name Value CDS_LAYOUT_ADDE TRJE B ODY_NAME bga17	Add Modify Delete
Name Type Mapping 4 UNSPEC 7 9 UNSPEC 9 8 UNSPEC 8 6 UNSPEC 9 10 UNSPEC 1 11 UNSPEC 10 11 UNSPEC 11 12 UNSPEC 15 16 UNSPEC 15 16 UNSPEC 17 Vpdate Symbol Vector Pin On Symbol © Creater/Update Symbol Single-bit Form © Ascending Descending	Logical Pin Manning		Global Pin Manning	3
4 UNSPEC 4 Add Add 7 UNSPEC 7 Modify Add Modify 8 UNSPEC 9 Modify Delete	Name Type	Manning	Name Type Marping	
Create/Update Symbol Update Symbol ECO Single-bit Form OverWrite Multi-bit Form Ascending Descending	4 UNSPEC 7 UNSPEC 9 UNSPEC 8 UNSPEC 6 UNSPEC 3 UNSPEC 2 UNSPEC 1 UNSPEC 10 UNSPEC 11 UNSPEC 12 UNSPEC 13 UNSPEC 14 UNSPEC 15 UNSPEC 16 UNSPEC 17 UNSPEC	A Add 7 9 Modify 8 6 5 3 2 1 10 11 12 13 14 15 16 17 1 1 1 1 1 1 1 1 1 1 1 1 1		Add Mcdify Delete
	Create/Update Symbol Update Symbol ECO OverWrite	Vector Pin On Symbo Single-bit Form Multi-bit Form Ascending	ol Descending	

Learn more at Cadence Support Portal - https://support.cadence.com © 2019 Cadence Design Systems, Inc. All rights reserved worldwide.

7. Select **OK**. Then, select **Yes** and **OK** in the BIDIR pin dialog. Select **Yes** and **OK** in the second dialog to create the symbol.



- 8. In the **Library Manager**, you will notice that the symbol and other supporting views have been created. Double-click on the **symbol** view. The symbol will open.
- 9. Close the view by selecting **File > Close**.

Summary

In this document, you learned to create the chips and connectivity files from SiP Layout and import the chips file into Virtuoso to create the symbol file.

Support

Cadence Support Portal provides access to support resources, including an extensive knowledge base, access to software updates for Cadence products, and the ability to interact with Cadence Customer Support. Visit <u>https://support.cadence.com</u>.

Feedback

Email comments, questions, and suggestions to <u>content_feedback@cadence.com</u>.