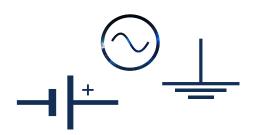
RULES FOR Schematic symbols







Rules for Schematic Symbols

Written By Theodor Iacob

A s the adage goes, *the only thing that is constant is change*. I could not agree more. Therefore, to succeed we must be able to adapt to changes. This can apply to schematic design. I believe we need to reconsider (and perhaps change) some of the rules for schematic symbols most of us have been following for approximately the last 40 years. By doing so, we will start to create a more readable and effective schematic layout.

Why Do We Need Better Schematics?

- To make a better layout
- Huge impact on readability and quality of the design
- Less design errors, support, and service calls
- Better IC definition (pinout helps layout) provide IC designers
- Increase designers' productivity
- Better products

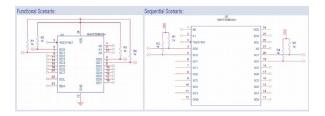
Do Not Blindly Apply Schematic Rules

There is an unspoken "rule" in the industry which states power pins need to be placed at the top edge and ground pins at the bottom edge. This is an archaic rule. This rule also requires input pins are placed on the left side and the output pins on the right side.

24		U7 MAX73588	UG+
U? N	MAX7358EUG+	A0	VDD 24
		2 A1	SDA 23
5 SC0	A0 2		SCL 22
G SC1	A1 21 0	0-4 SD0	A2 21
11 SC2	4	5 SC0	SC7 20
SC4	SD0 6 SD1 8 SD2 10	- 6 SD1	SD7 19
	SD2 10 SD3 13	0 7 SC1	SC6 18
20 SC6 SC7	SD3 13 SD4 15 SD5 17	B SD2	SD6 17
22 SCL		9 SC2	SC5 16
23	SD6 19 0	10 SD3	SD5 15
SDA	3ND	- 11 SC3	SC4 14
2		12 GND	SD4 13

What's the big deal you might ask? Well first, it is important to remember these rules were put into place when TLLs were ruling the world and they had only one power and one ground pin. Nowadays, newer chips have multiple supplies and their locations on the package are strongly related to their function—making them critical. Based on this information and the evolution of technology, a better way to make a symbol is to create the schematic symbol with the pins in the same order as the physical part.

To help me illustrate why, let's look at an example: say an IC needs two pins to be connected with a resistor — one is an input and one is an output. This is an analog IC and therefore needs a signal to pass through that external resistor. Ac-cording to the current rule, you would place the input on the left and the output on the right. Since this part has 24-pins, by following the above stated rule, placing those two pins on left and right respectively, will force a designer to place the resistor above the part and have a wire straddle and jump all over many other wires (or they would have to use "air" wires) which would make the schematic difficult to follow.



Remember, the designer of this IC intentionally placed those two pins next to each other to make the layout clean and get the best signal integrity. So why would one want to make the schematic a mess?

Instead of blindly following these archaic rules, which would lead to an extremely confusing schematic, I recommend matching the pin-ordering with the physical part. The primary goal for doing so is to create an intuitive layout (top view) that is easy to follow, debug, and test.





Most parts we use today are analog-intensive and their pin-order is dictated by the functions they need to do. Those pins are grouped and ordered to make those functions work their best. Therefore, for analog parts, the default should be to follow the part's physical pin-ordering.

Many times, layouts are ruined because it is difficult to understand the intent of the schematics. Remember: A good schematic should help the layout. I find many schematics are difficult to read and follow signals and the major contributor to this problem is the above-mentioned rule, which forces pins to be placed in this way.

In my opinion, rules need to be changed. We need to consider what a part's primary use is first and foremost. Rules, like the one previously mentioned, should only be applied to large digital parts where the functionality is primarily logical (like processors, memories, multibit bus drivers, etc.) and smaller parts that are primarily analog [like power supply ICs (buck, boost, chargers, LDOs, etc.), level translators, buffers, drivers, amplifiers, temp sensors, filters, protection devices, FETs, and many others] should be defined with their pin-order matching the physical part.

How does changing these rules help?

- The electrical engineer will better understand where passive components need to be placed around this IC. It will be much clearer which pins are carrying sensitive signals and which are high current ones. It will help in assigning pins in devices that have multiple similar functions, such that the layout is simpler, without the need to jump wires.
- 2. Layout designers will benefit by better understanding the circuit function and how it translates to layout through a logical placement and better routing.

- 3. Test people will better understand the circuit and how to test it.
- 4. Service people will be able to learn a new diagram faster and repair the system quicker.

By changing our mindset and refusing to follow certain rules blindly without fully understanding their origins, we can create better more readable schematics. When we treat schematics with more care and respect we all benefit including: colleagues, suppliers, and customers who need to use them. Schematics should not be just a means to generate a BOM and a netlist—they are much more than that.

About the Author

Theodor lacob is an expert in electrical schematics and board layout with over 26 years' experience within the electronics industry. He is extremely knowledgeable in a wide range of systems and applications including: consumer electronics, high-speed analog, industrial, solar, and medical. He has experience in power design from mA to hundred amps, single-phase, multi-phase, buck, boost, and more.

He is an ambassador of schematic readability and believes while tools affect productivity, it is up to the designer to determine the quality of their schematics and layout. Currently, he is working as a Power Systems Engineer for one of the top technology companies in Silicon Valley.