SIERRA CIRCUITS

EMA Design Automation

Design Documentation and How to Communicate

Design Intent with your Manufacturing Partner

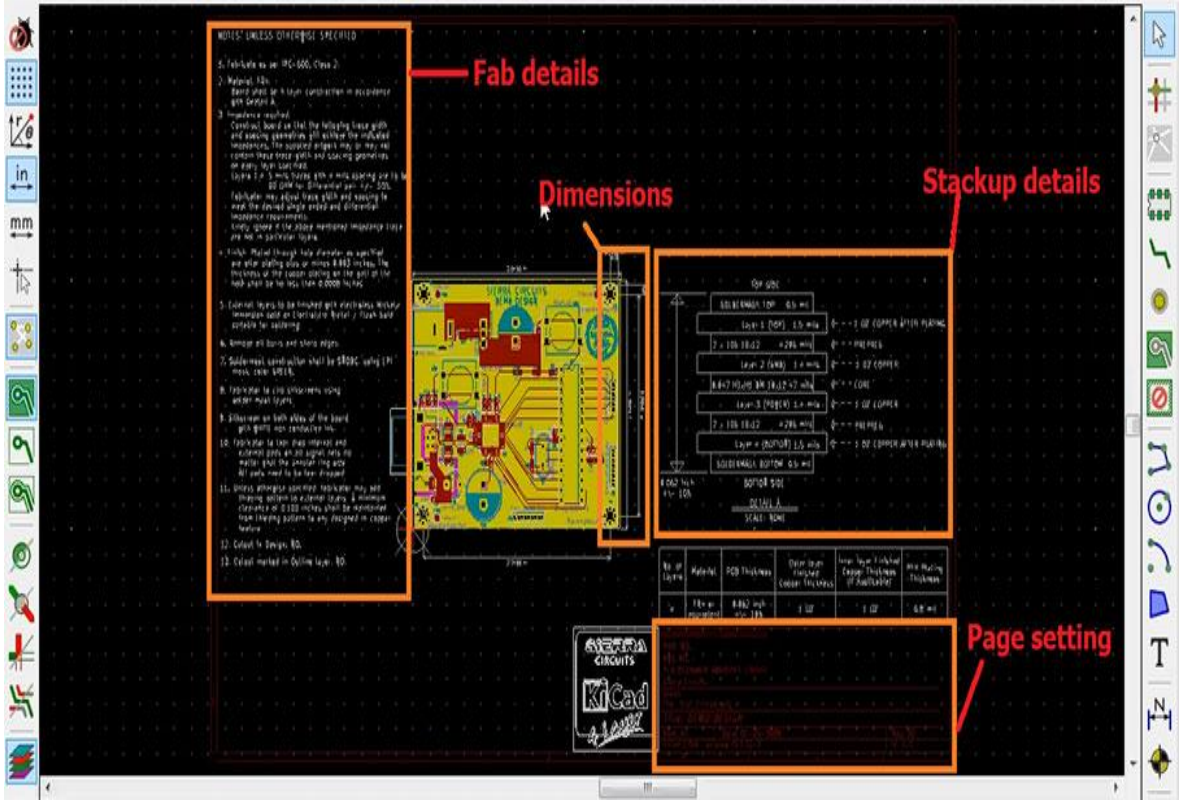

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Table of Contents

Sierra Circuits' PCB Fab and Assembly Capabilities

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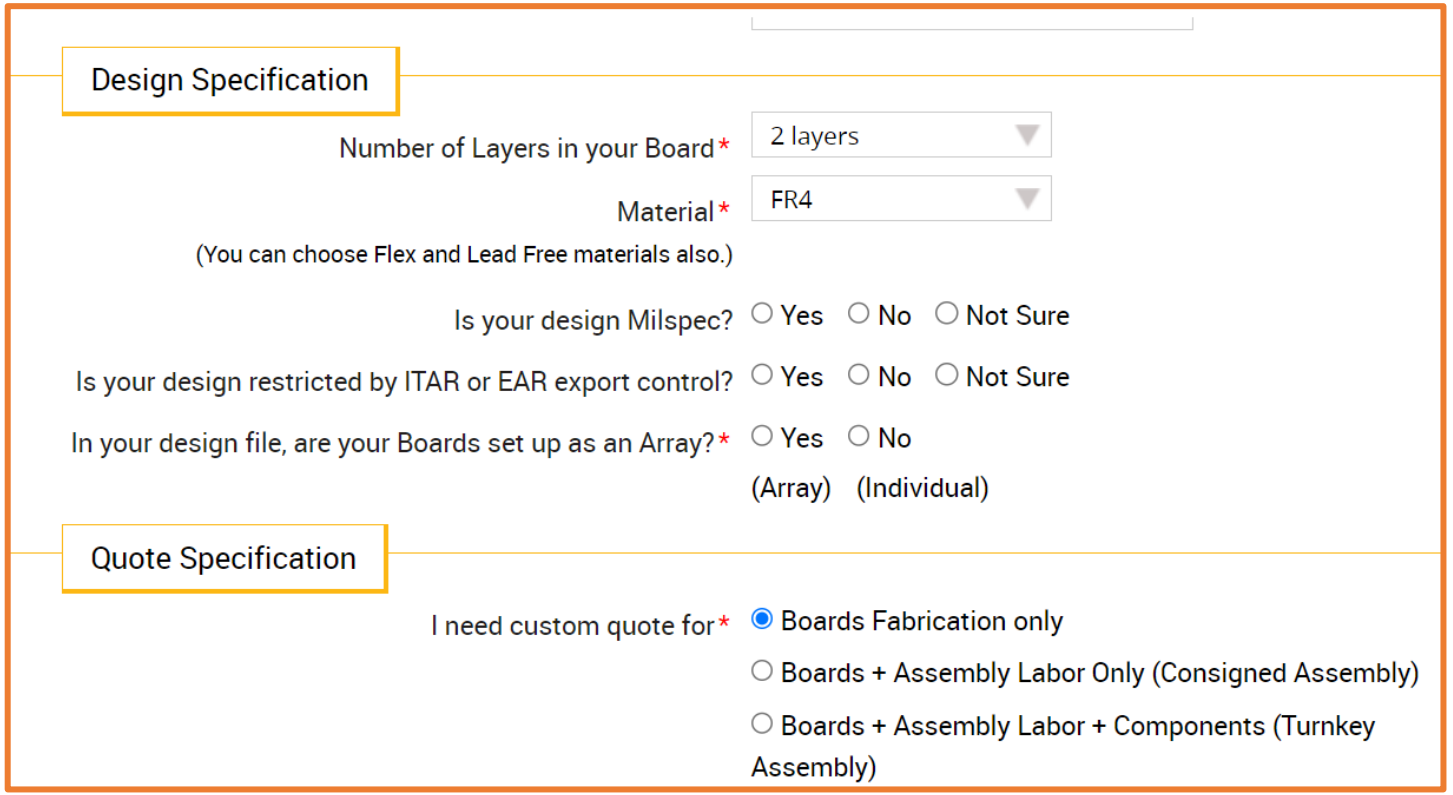
Required design data for PCB fab and assembly

- Documenting your manufacturing requirements ensures a successful production without any shadow of faults

- PCB design document integrates the details such as:
  - Hardware dimensional drawings
  - Schematic representation
  - BOM, and layout file
  - Pick and place file
  - Assembly drawings
  - Gerber files



Sierra Circuits' Custom Quote tool

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Specifications that need to be documented

NOTES: UNLESS OTHERWISE SPECIFIED

1. Fabricate per IPC-600 Class 2.

2. Material: FR4
   Board shall be 4 layer construction in accordance with Detail A.

3. Impedance:
   Construct board so that the following trace width and spacing geometries will achieve the indicated impedances. The supplied artwork may or may not contain these trace width and spacing geometries on every layer specified.

   Layers 1: 8 mil traces are to be 50 OHM single ended +/- 10%
   Layers 4: 8 mil traces are to be 50 OHM single ended +/- 10%
   Fabricator may adjust trace width and spacing to meet the desired single ended and differential impedance requirements.

4. Finish: Plated through hole diameter as specified are after plating plus or minus .003 inches. The thickness of the copper plating on the wall of the hole shall be no less than .0008 inch.

5. External Layers Finish to be ENIG.

6. Soldermask: Green

7. Fabricator to clip silkscreens using solder mask layers.

8. Silkscreen: WHITE

9. Remove all burrs and sharp edges.

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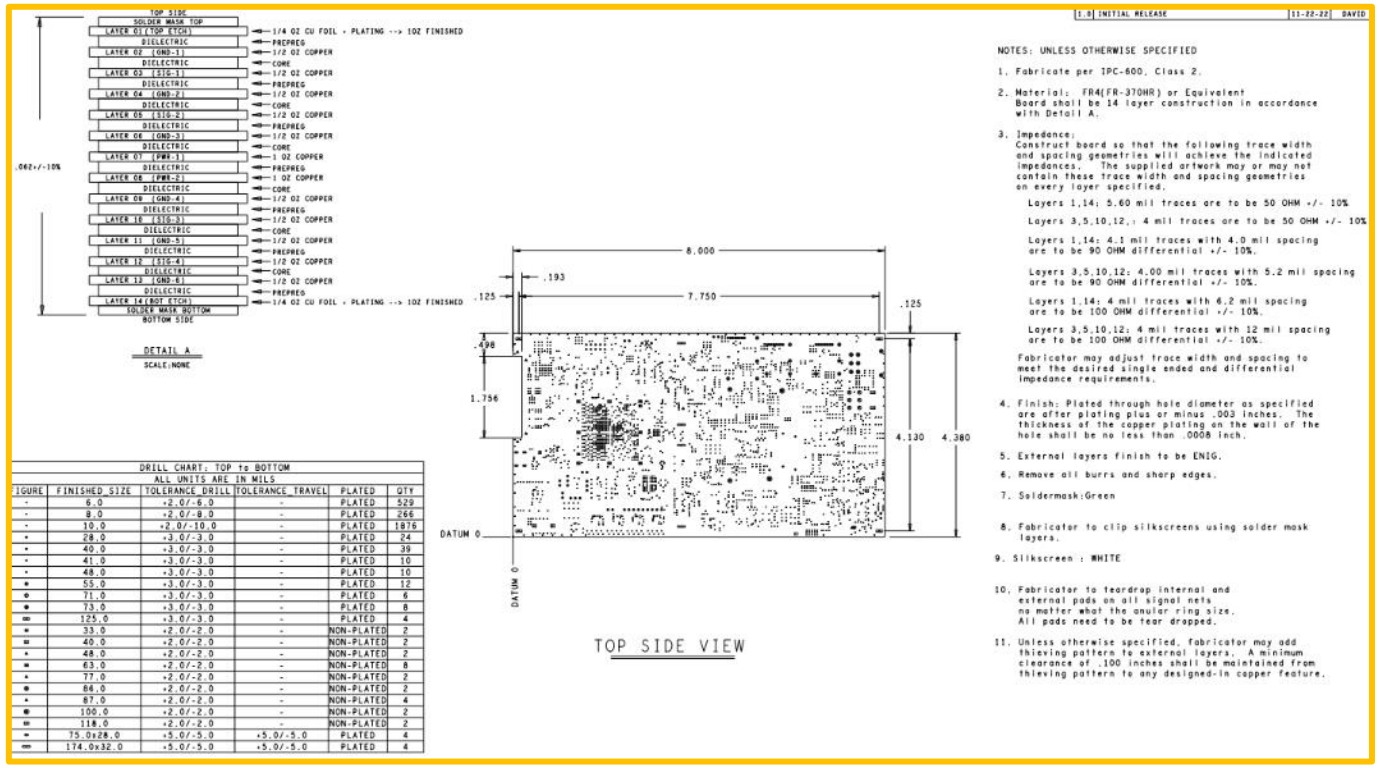
Primitive documentation for manufacturing

- Mention the class of the board (class 2 or 3)
- Include board outline in X-Y coordinates
- Specify slots, notches, and cutouts that need to be generated during fabrication
- Add the date, version, and the author of the drawing
- Company logo and name if required
- Clearly mention the orientation of pin 1/ cathode for polarized components



Fab drawing details (Click on the image to see the complete fab notes)

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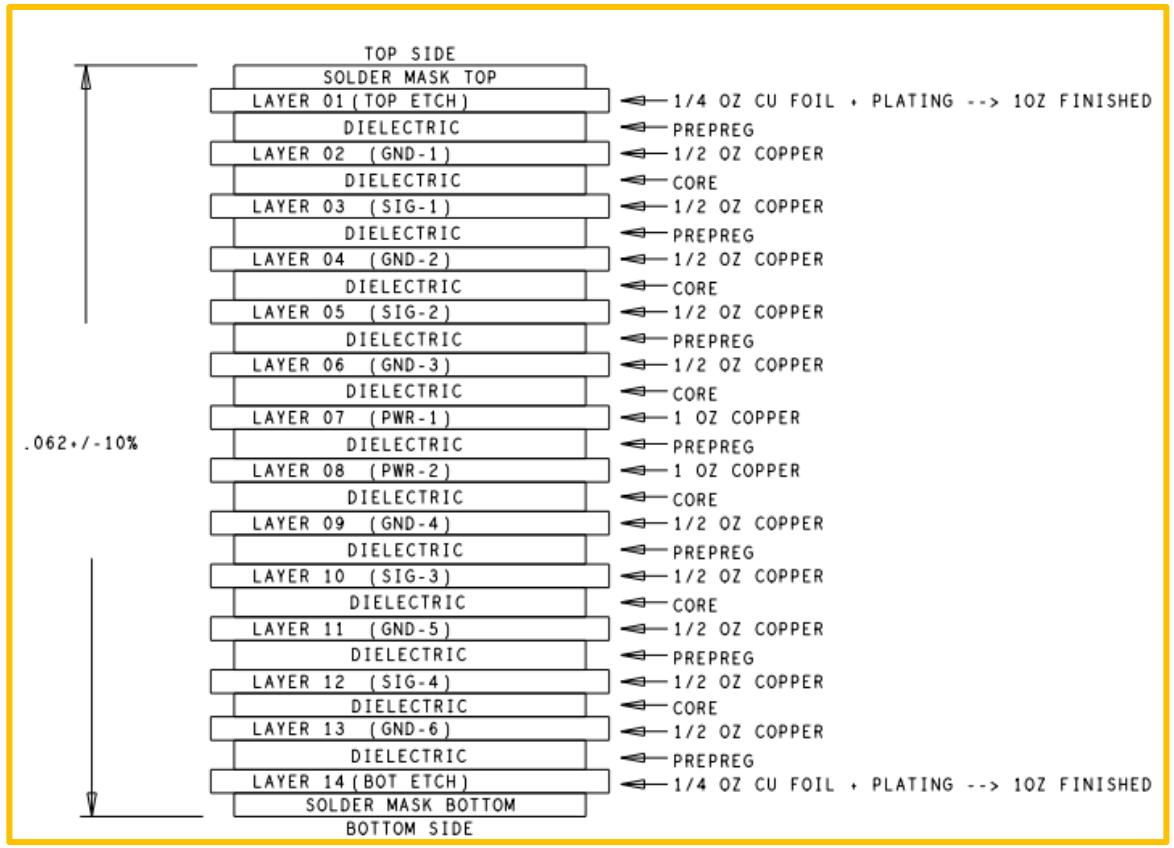
Stack-up information

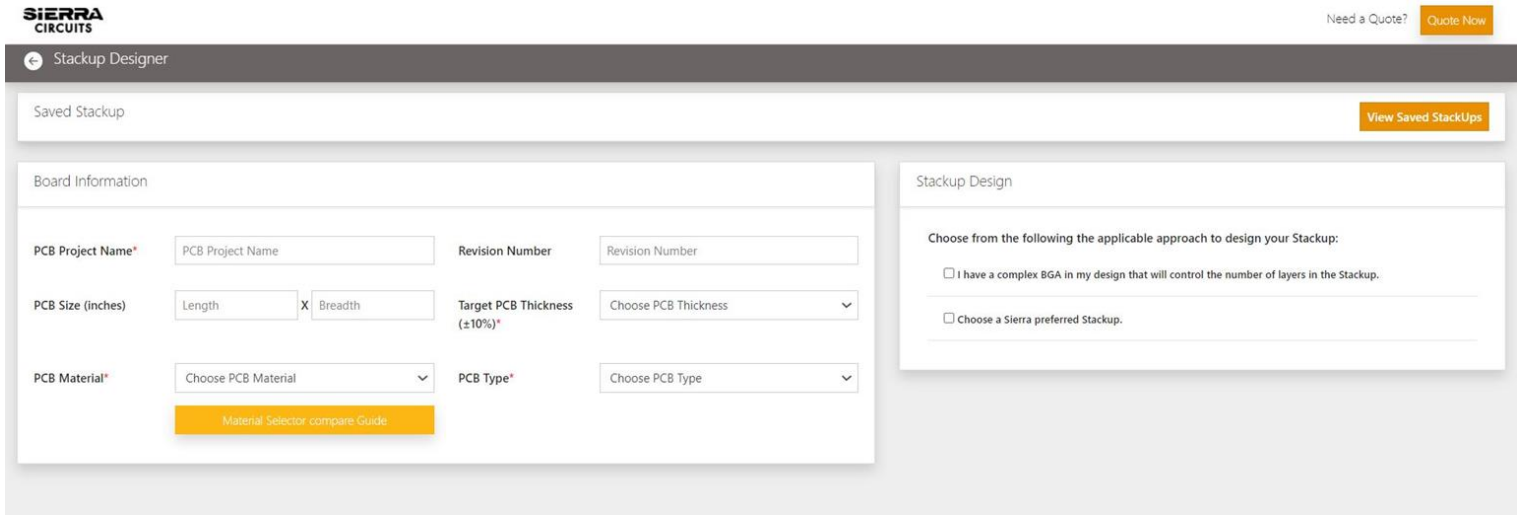
- Stack-up should provide information related to:
  - Number of signal and ground/power layers
  - Dielectric spacing and copper weight
  - Material type
  - Operating frequency
  - Sequence of the layers
  - Finished board thickness
- For HDI build-up, additional requirements are:
  - Type and layer arrangement of microvia
  - Number of BGAs
  - Number of lamination cycles



Stack-up requirements

Sierra Circuits' PCB Stackup Designer

- Includes library of stack-up with single and sequential lamination build-ups (HDI-1, HDI-2, HDI-3, and HDI-4)
- Involves a variety of material databases
- Automatically chooses the type of board construction
- Offers 3 technology levels (level I/II/III) with respect to different parameters such as trace geometry, drill sizes, spacing, and cost index



https://www.protoexpress.com/tools/pcb-stackup-designer/

Controlled impedance details

- Your CI data should include:
  - Target impedance
  - Trace width/height
  - Layers on which the impedance traces are present
  - Spacing between components on controlled traces (for coplanar or differential calculations)
  - Copper weights, and layer thicknesses
  - Differential pair spacing

- Include CI table to specify SE and differential pair impedance values

IMPEDANCE REQUIREMENT:
Construct board so that the following trace width and spacing geometries will achieve the indicated impedances. The supplied artwork may or may not contain these trace width and spacing geometries on every layer specified.

100 OHM DIFFERENTIAL IMPEDANCE:
Layer 10: 4.5 mil traces with 6.5 mil spacing are to be 100 ohm differential +/-10%.
Layer 3 and 7: 4.4 trace width with 6.2 spacing are to be 100 ohm differential pairs.

50 OHM SINGLE ENDED IMPEDANCE:
Layer 10: 6.5 mil traces are to be 50 ohm +/-10%.
Layer 3, 4, and 8: 4.75 mil traces are to be 50 ohm +/-10%.

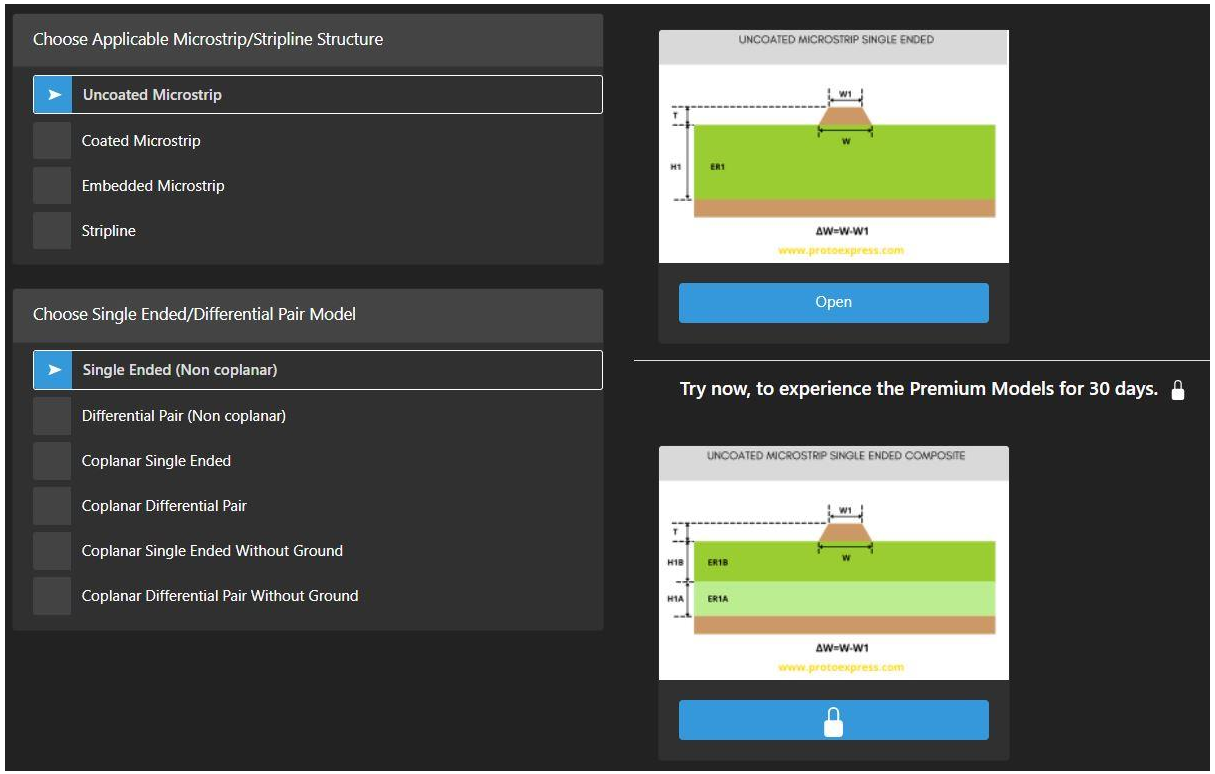
Impedance requirements in fab notes

LAYER	50 OHM	100 OHM	
	Trace	Trace	Space
3	4.75 Mils	4.40 Mils	6.20 Mils
4	4.75 Mils		
7		4.40 Mils	6.20 Mils
8	4.75 Mils		
10	6.50 Mils	4.50 Mils	6.50 Mils

Impedance table

Sierra Circuits' Impedance Calculator

- Uses 2D numerical solution of Maxwell's equations
- Calculates line parameters adding to the characteristic impedance
- Determines coupling coefficient, even and odd mode parameters for differential pairs
- Assures greater accuracy considering the trace's trapezoidal shape or the effect of multiple dielectric materials



https://www.protoexpress.com/tools/pcb-impedance-calculator/

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Plating and surface finish information

- For plating, you need to mention:
  - Maximum and minimum plating thickness
  - Plating material type
  - Hardness requirement
- Designers need to communicate about the type of surface finish as per their design demands
- At Sierra, we offer:
  - Lead-free HASL
  - Organic Solderability Preservative (OSP)
  - Immersion Silver
  - Immersion Tin
  - Electroless Nickel Immersion Gold (ENIG)
  - Electroless Ni/ Pd Immersion Au
  - Electrolytic Ni/Au (Hard/ Soft Bondable)

Type of surface finish	Planarity	Al wire bondable	Au wire bondable
Lead free HASL	Fair	No	No
Organic solderability preservative (OSP)	Good	No	No
Immersion Silver	Good	Yes	No
Immersion Tin	Good	No	No

Sierra Circuits' Surface Finish Capabilities

4. Finish: Plated through hole diameter as specified are after plating plus or minus .003 inches. The thickness of the copper plating on the wall of the hole shall be no less than .0008 inch.

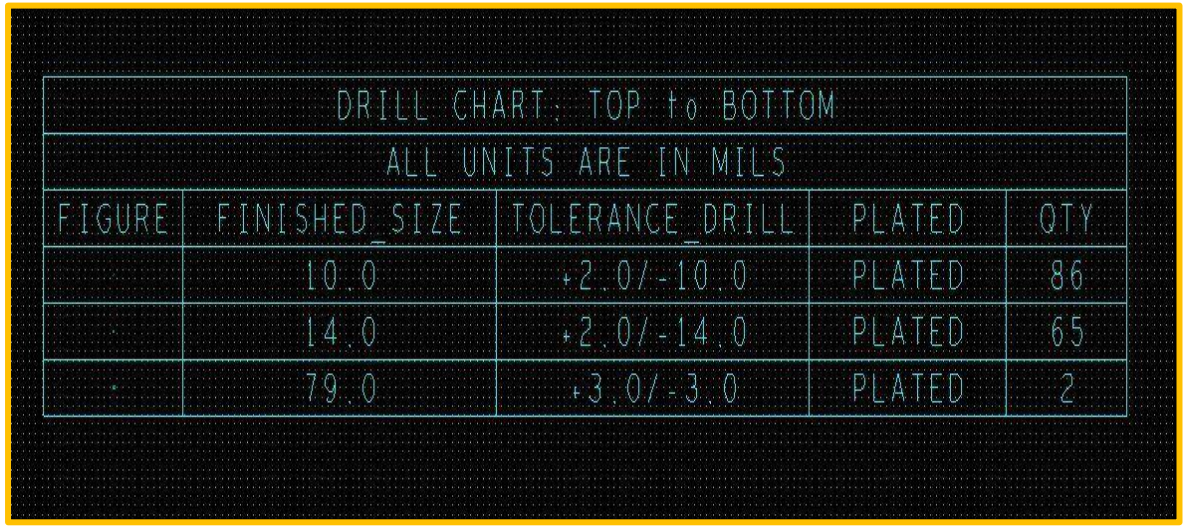
5. External layers finish to be ENIG.

Finished surface information

Drilling specifications

Include following drill details in your drill chart:

- Drill technology to be used (mechanical or laser)
- Type of drill: PTH or NPTH
- Drill location information with different drill symbols for each size
- Separate drill chart comprising the finished hole size with symbols
- Minimum drill to edge clearance
- Minimum annular ring size and plating thickness for PTH
- Drill tolerances:
  - PTH:+/- 0.003″,
  - NPTH: +/- 0.002”
  - Slots: +/- 0.005”



DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
	10.0	+2.0/-10.0	PLATED	86
	14.0	+2.0/-14.0	PLATED	65
	79.0	+3.0/-3.0	PLATED	2

Sample of a drill chart

Outer and inner layer specifications

- Calibrate trace width for external and internal layers accurately. This helps in efficient thermal management
- Determine the required minimum trace spacing under the IPC-2221 standard
- Add copper finish thickness in your fab notes, especially for high voltage, resistance, or impedance requirements

```
Construct board so that the following trace width
and spacing geometries will achieve the indicated
impedances.   The supplied artwork may or may not
contain these trace width and spacing geometries
on every layer specified.

  Layers 1,14: 5.60 mil traces are to be 50 OHM +/- 10%

  Layers 3,5,10,12,: 4 mil traces are to be 50 OHM +/- 10%.

  Layers 1,14: 4.1 mil traces with 4.0 mil spacing
  are to be 90 OHM differential +/- 10%.

  Layers 3,5,10,12: 4.00 mil traces with 5.2 mil spacing
  are to be 90 OHM differential +/- 10%.

  Layers 1,14: 4 mil traces with 6.2 mil spacing
  are to be 100 OHM differential +/- 10%.

  Layers 3,5,10,12: 4 mil traces with 12 mil spacing
  are to be 100 OHM differential +/- 10%.

Fabricator may adjust trace width and spacing to
meet the desired single ended and differential
impedance requirements.
```

Trace width and spacing specifications

Solder mask and silkscreen information

- Provide solder mask details such as:
  - Top and bottom solder mask thickness
  - Color and finish of the solder mask
  - Minimum solder mask dam
  - Clearance between copper pad and the solder mask

- For silkscreen requirements,
  - Mention the side, colour and font type for silkscreen printing
  - Specify the method to be used and the tolerance limit
  - Add if you need vendor's labelling and RoHS marking
  - Top and bottom legends (min 6 mils)

Defining solder mask and silkscreen requirements

Special manufacturing requirements

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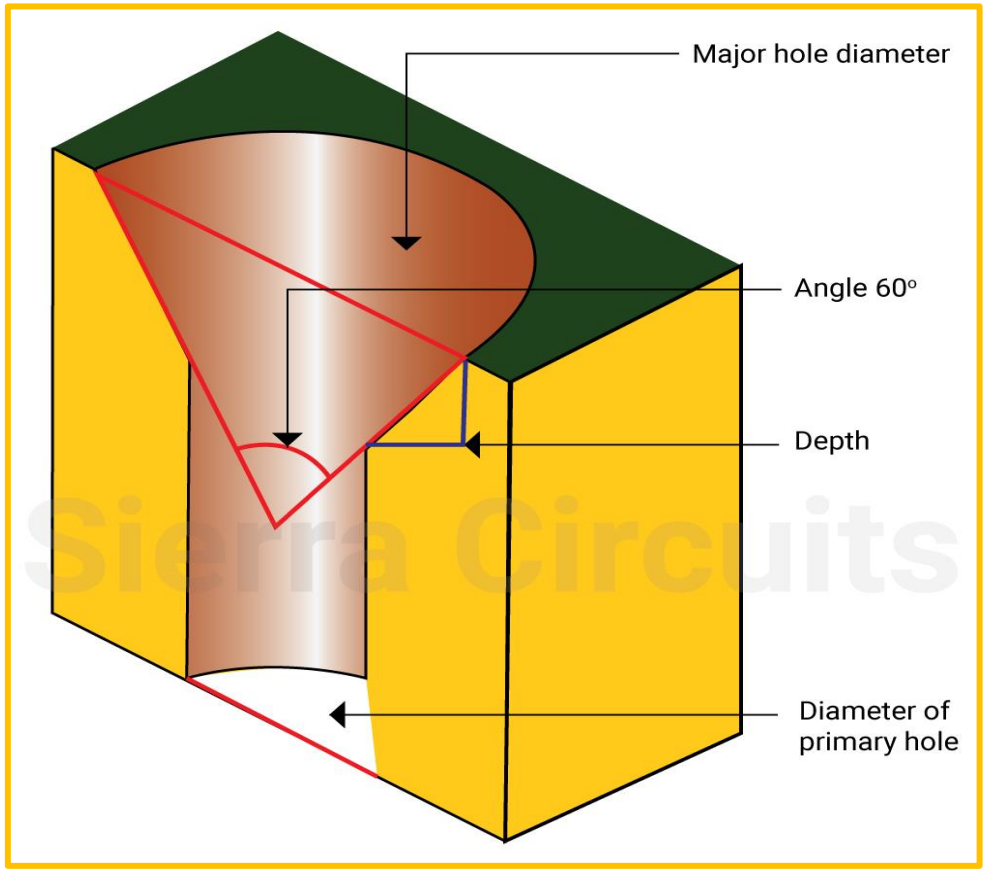
Countersink holes

To build a perfect countersink hole, convey the following information:

- Angle of the drill bit
- Countersink hole or major hole diameter
- Standard through-hole or primary hole diameter
- Side that needs a countersink hole
- Depth of the drill hole
- Whether the holes should be plated or non-plated

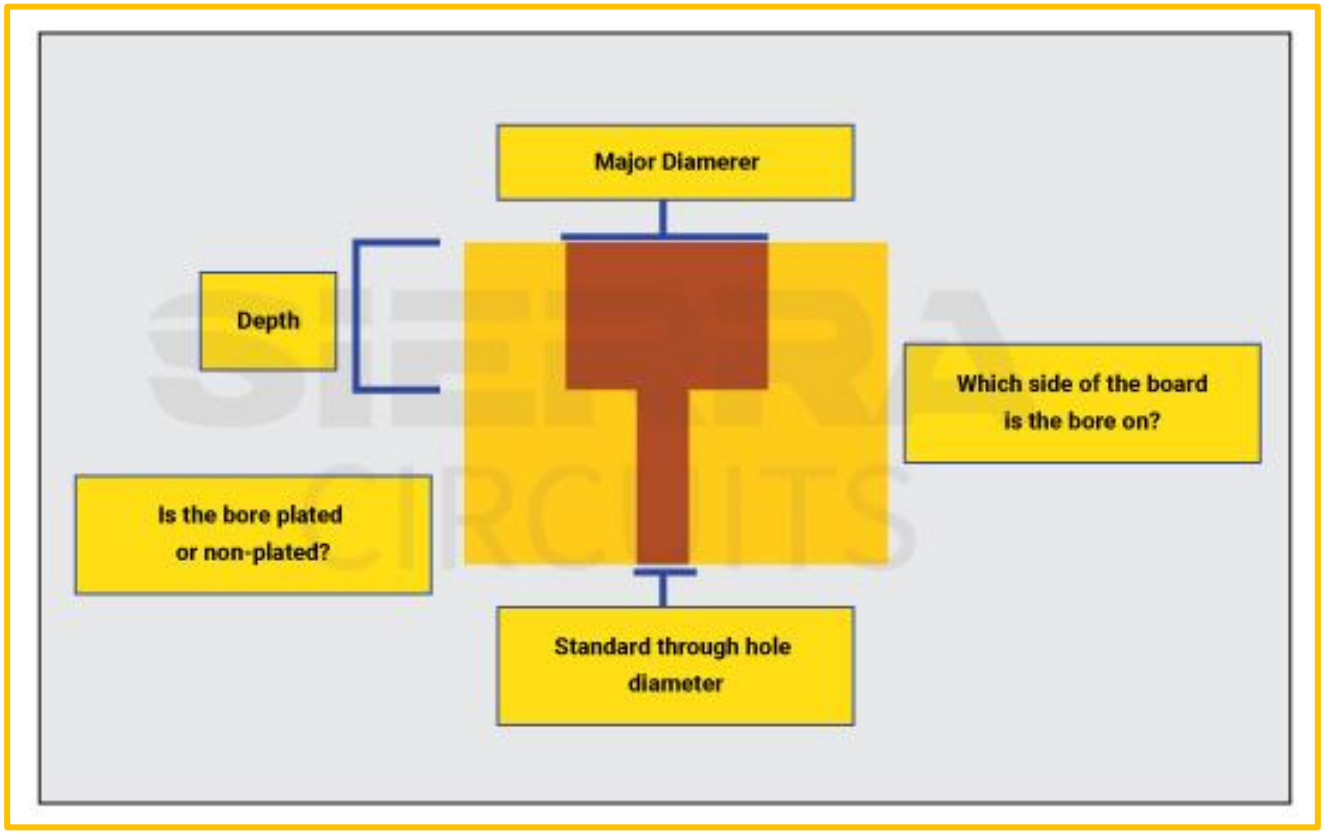


Countersink holes

Counterbore holes

Details required to fabricate counterbore are:

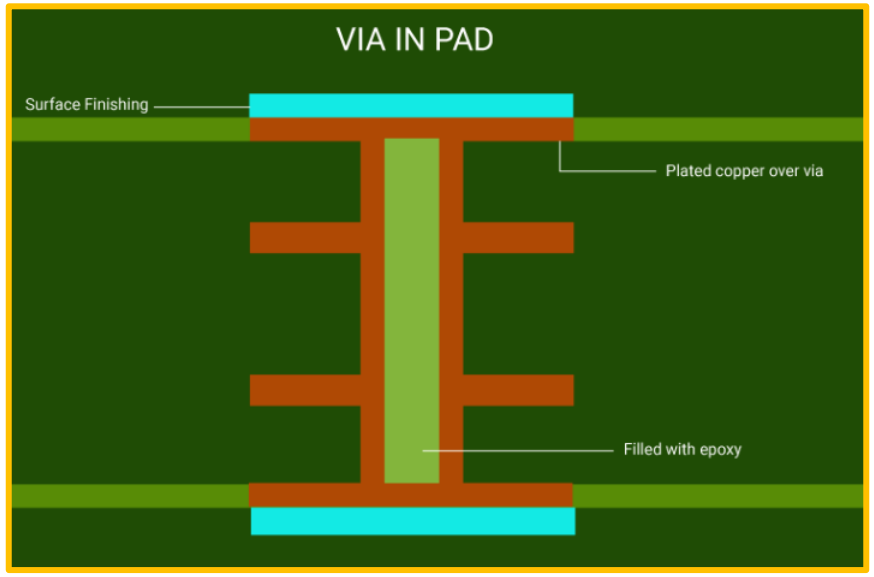
- Major diameter or finished diameter of the hole at the surface
- Drilling depth
- Where the bore needs to be drilled (from top or bottom)
- Finished diameter of the shaft
- Whether the bore and shaft are to be plated or non-plated



Counterbore holes

Via-in-pad or filled vias

- Provide the location, quantity and size of the holes that need to be via-in-pad
- If you require filled vias, specify the type of filling (conductive or non-conductive)



Via on Pad & Blind vias should be filled with conductive material.

Fab note with VIP details

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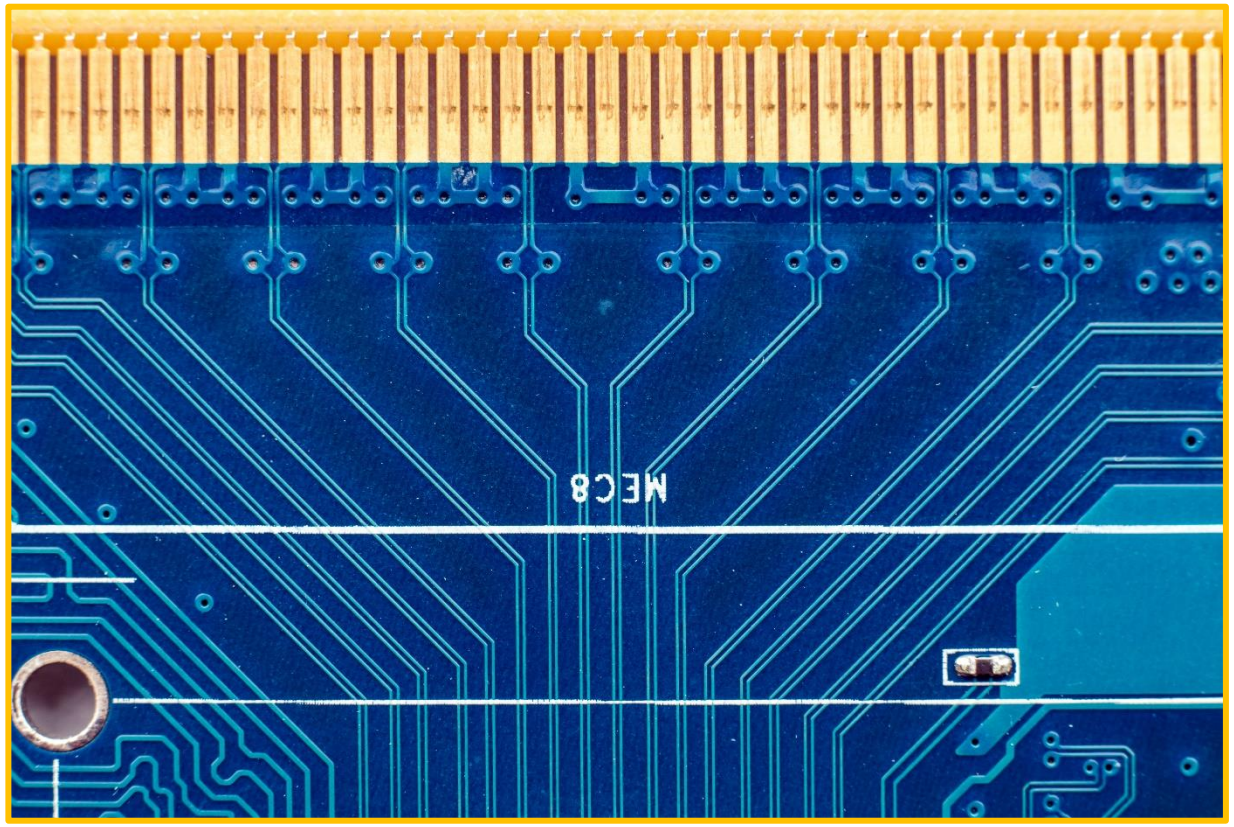
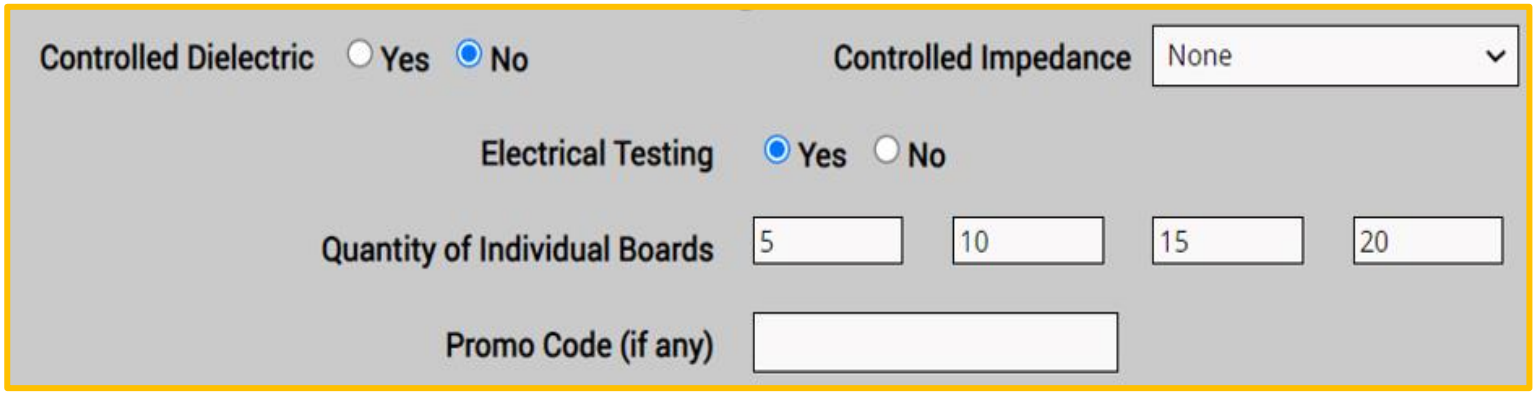
Gold fingers

- If you’re design features gold fingers, mention the following requirements:
- Type of gold plating:
  - ENIG
  - Electroplated hard gold
- Board side where gold plating is to be done
- Distance from the outer edge
- Chamfering angle (default angle: 45°)



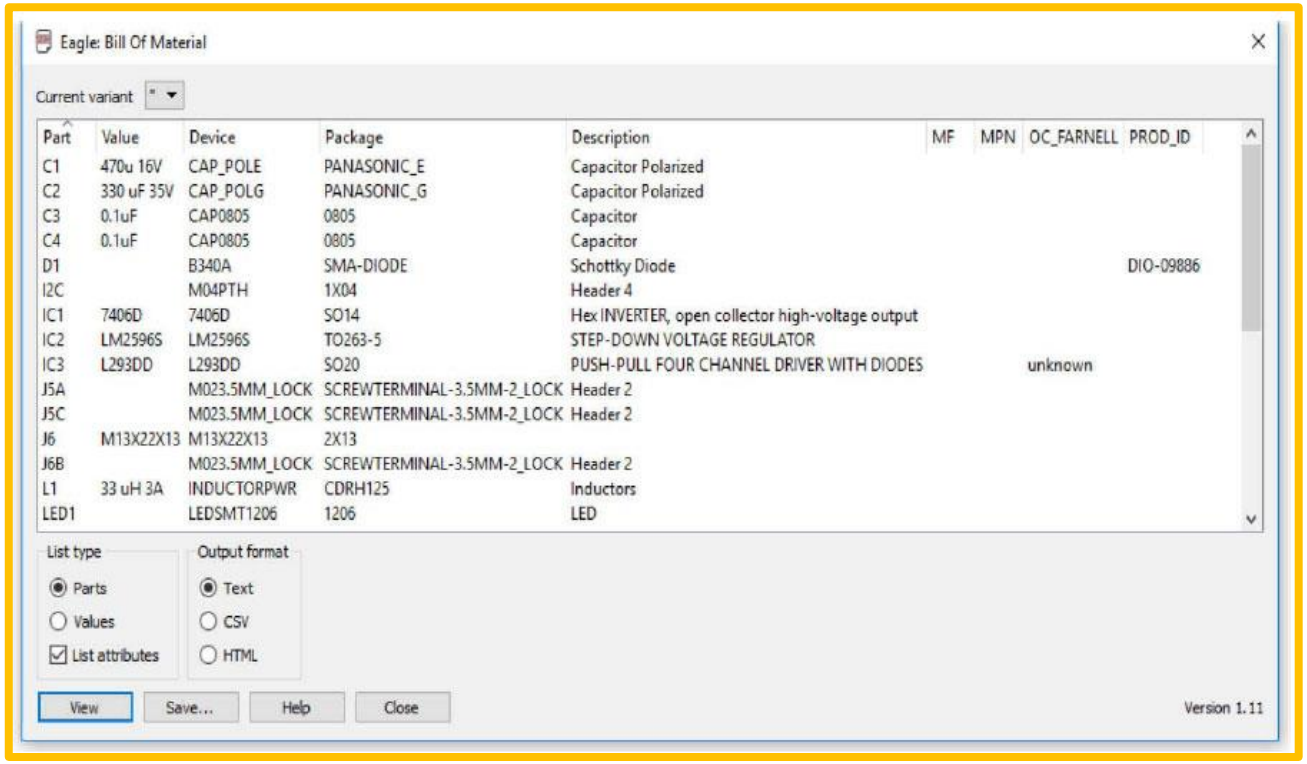
Controlled dielectric

- Provide the controlled dielectric stack-up to the manufacturer
- Mention the dielectric spacing you need between your copper layers
- Since impedance traces are not specified here, specify the tolerance limit



Defining controlled dielectric

Component assembly specifications



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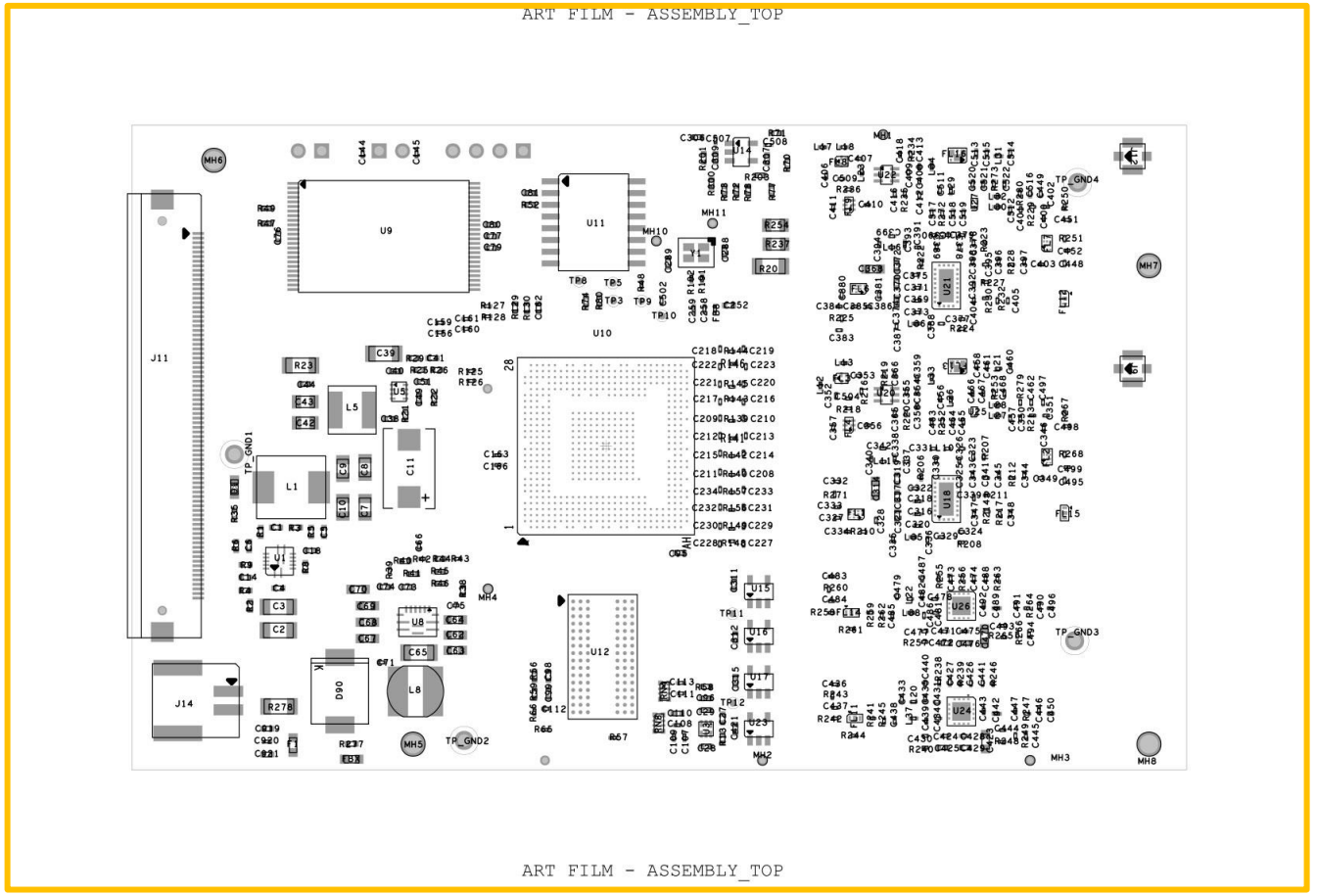
What to add in assembly drawing

Your assembly drawing should provide:

- Info related to primary and bottom side of the board
- Mounting instructions for critical components like connectors, heat sinks
- Details of additional hardware to be mounted such as stiffener bars, handles, or ejectors
- Enlarged view of critical areas of assembly
- Location of assembly stickers and labels

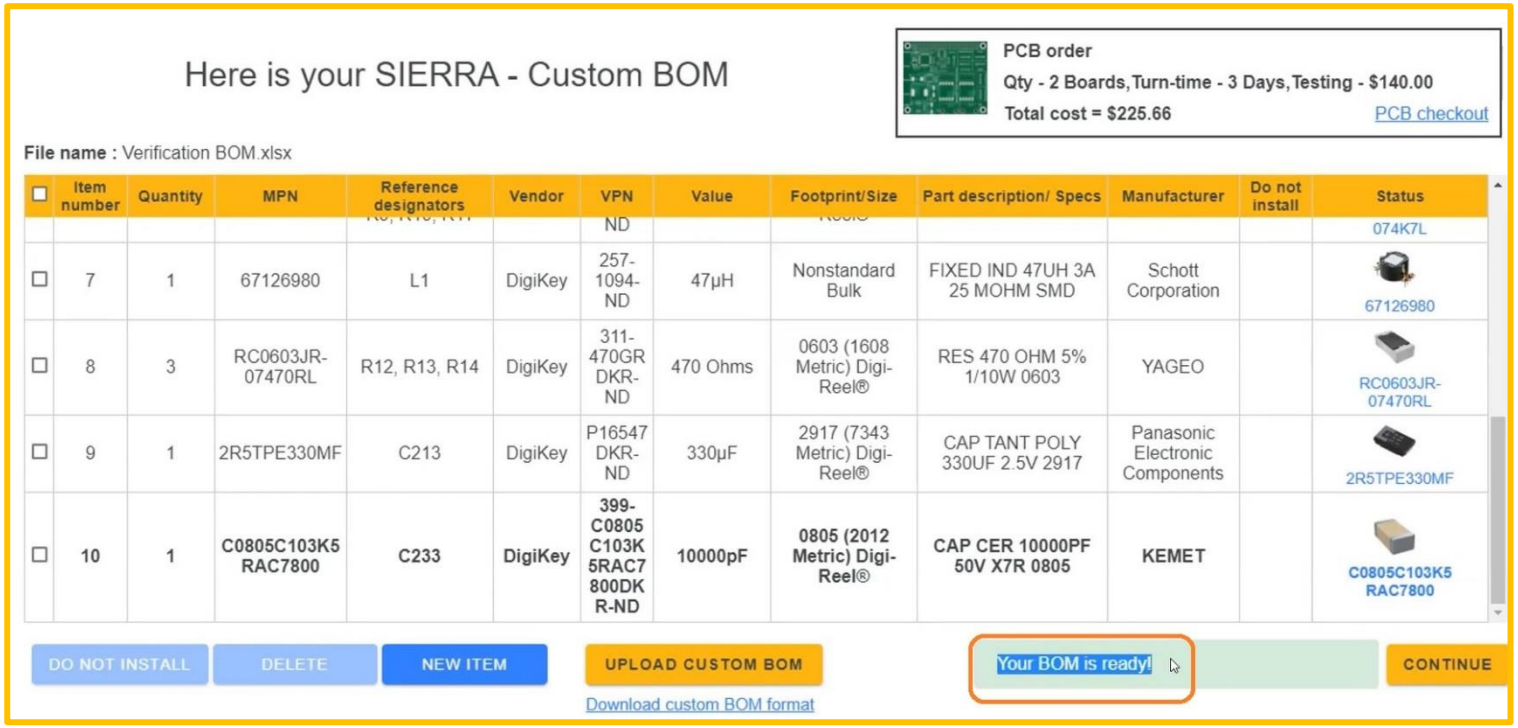


Assembly drawing

Information to keep in mind to prepare BOM file

BOM sheet should cover the following details:

- Quantity per board
- Manufacturer part number (MPN)
- Reference designators
- DNI/DNP
- Vendor (optional)
- Vendor part number (optional)
- Value (optional)
- Size/footprint
- Part description/specs
- Manufacturer (optional)
- Scope for alternative component
- Customer supplied parts

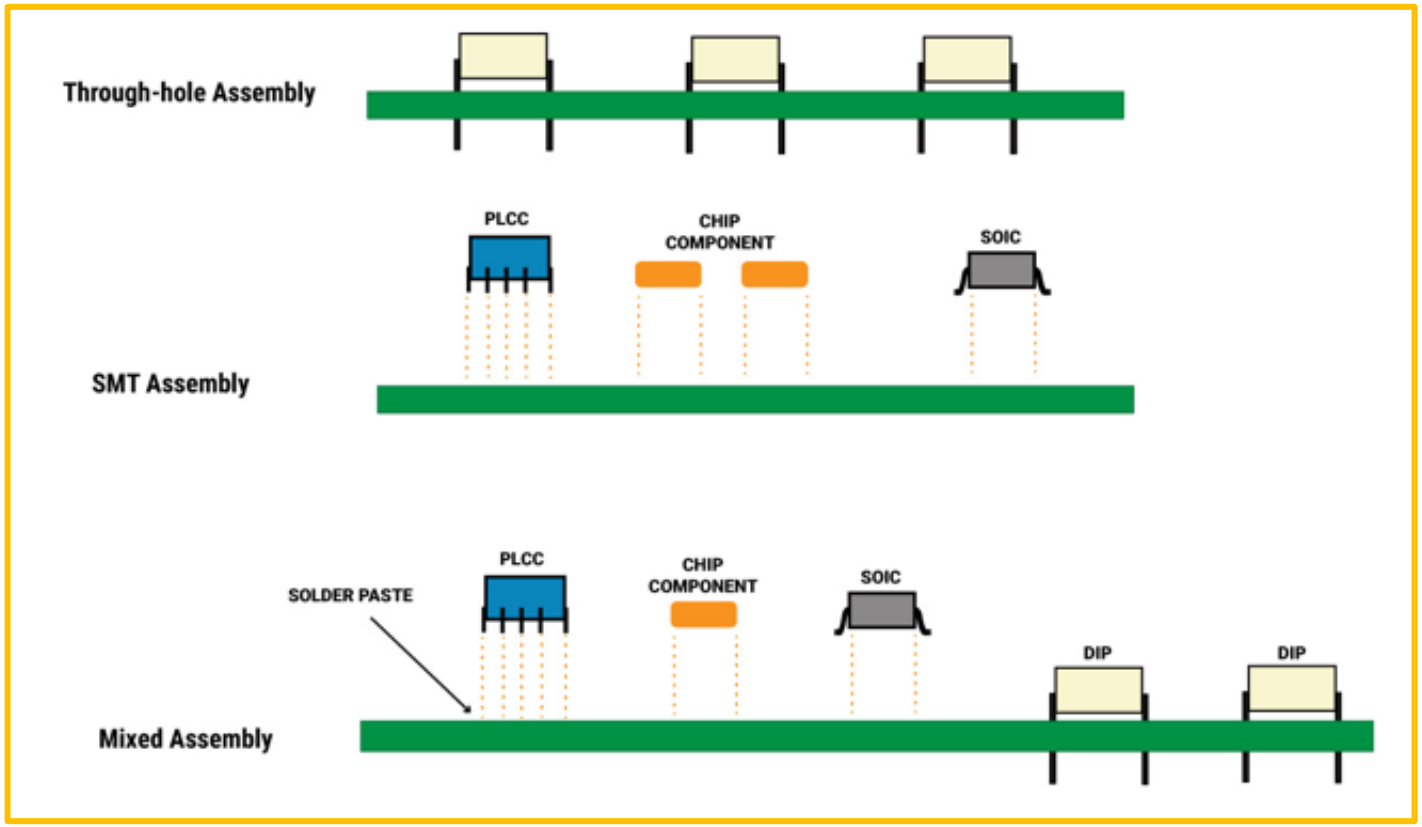


Bill of materials

Details of assembly notes

Your assembly notes should include:

- Number of SMT and through-hole components in your design
- Component sizes
- Component to component and component to board edge clearance
- Instructions related to customized part, if any
- Heat sink and shielding details
- Maximum height of the component or the total form factor
- Soldering instructions



Different types of components

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Design files manufacturers need

Customer Checklist		
Data Files		
ODB ++ or CAD files Required	☐ YES	☐ NO
Bills of Material with Mfg# and AVL required	☐ YES	☐ NO
Gerber files if ODB++ & CAD not available	☐ YES	☐ NO
XY Placement Data (Excel, CSV or Text format)	☐ YES	☐ NO
Assembly Drawing with Polarity marking (Pin 1)	☐ YES	☐ NO

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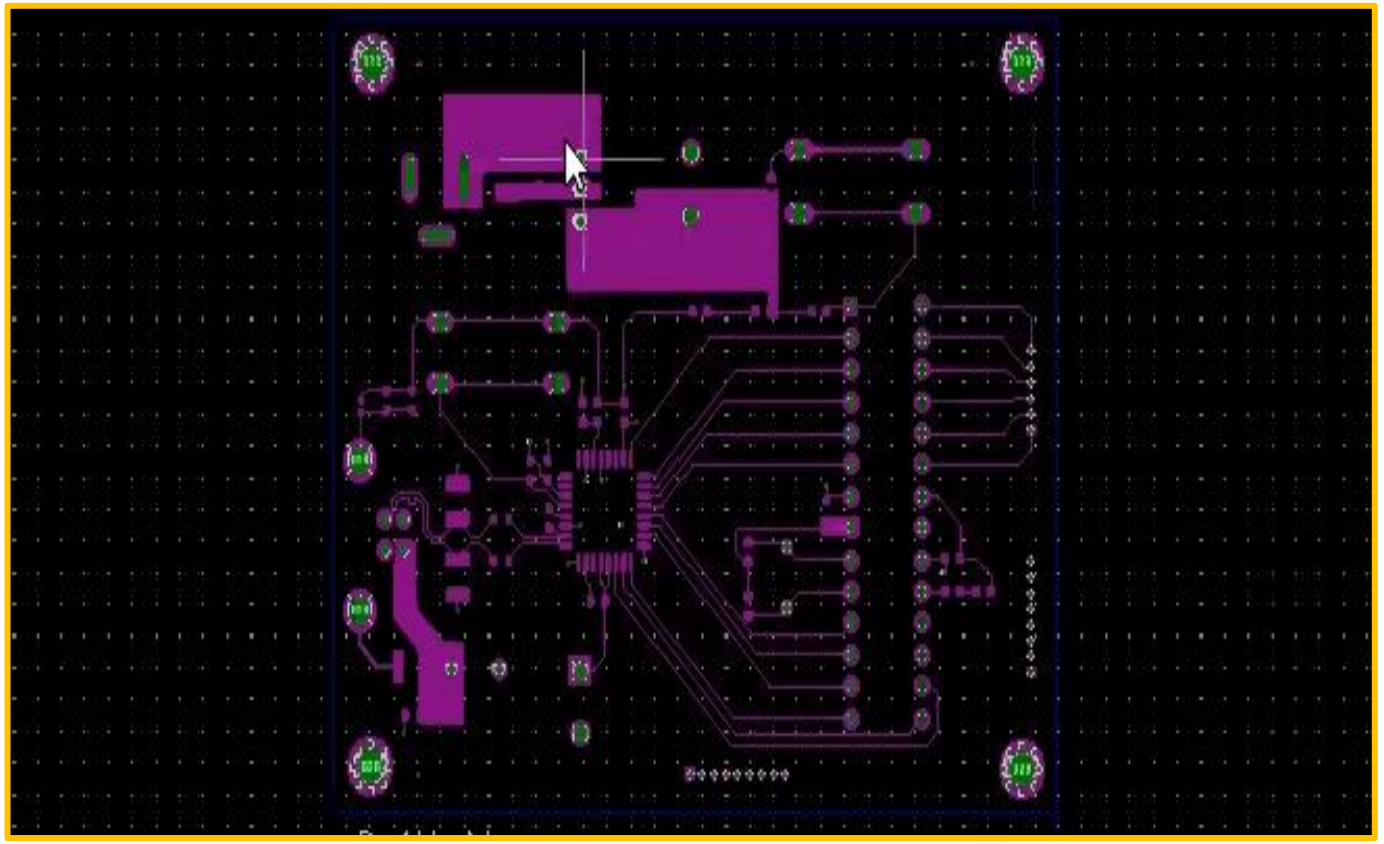
Gerber files

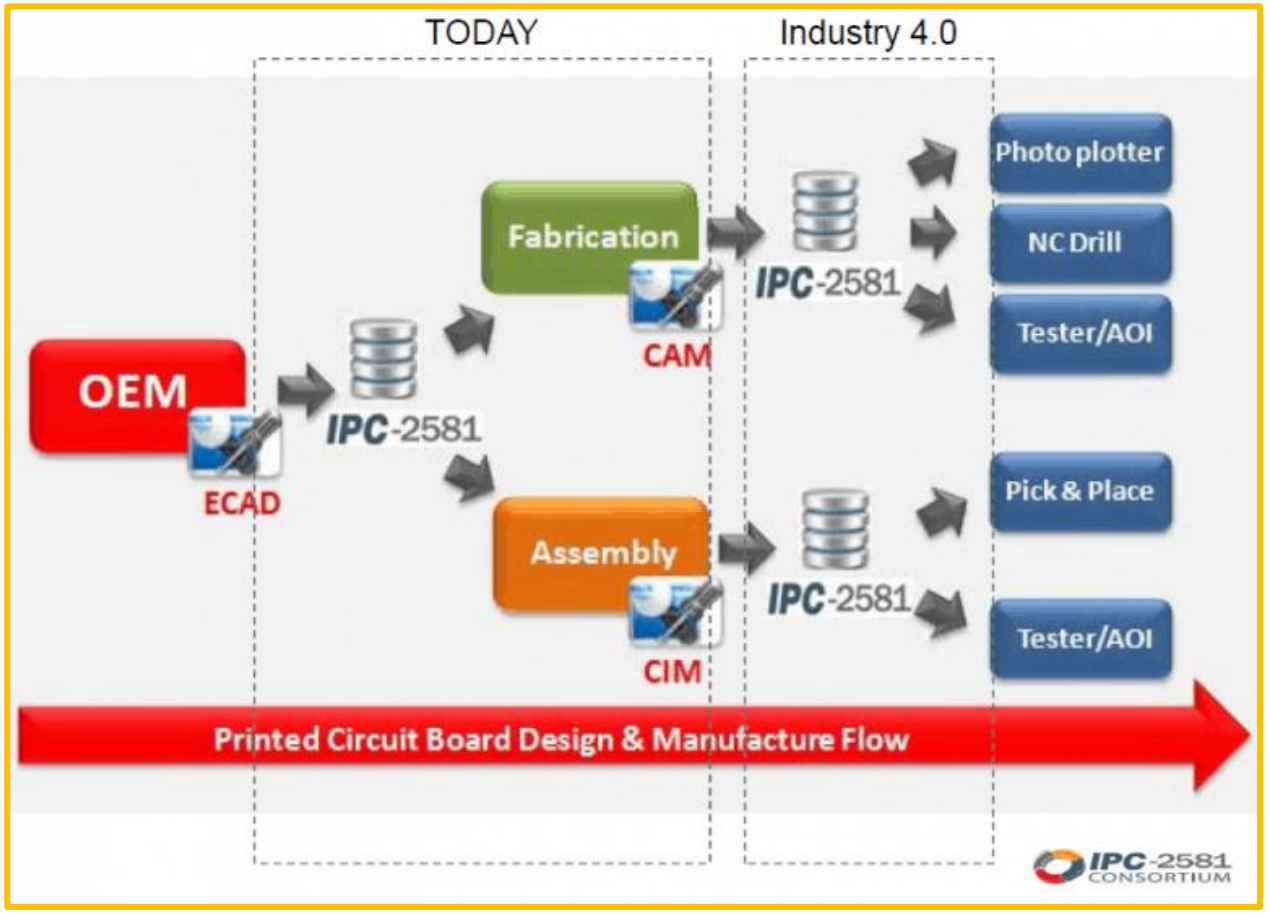
- Gerbers are most widely used file format for PCB manufacturing
- They provide 2D representation of copper layers, solder mask, and silkscreen details
- These files drive the photoplotter that creates the film to expose each conductor layer
- Standard extensions are “.GBR” “.GB”
- Gerber formats:
  - Standard Gerber (RS-274-D), first format, now obsolete
  - Extended Gerber, (RS-274X), currently in use
  - X2, extended Gerber updated to add meta-data about the files such as file attributes



Gerber file format

IPC-2581

- Defines a format for organizing and converting designs from CAD tools to CAM systems for fabrication and assembly
- Data embedded in IPC-2581 file includes:
  - Layer structure
  - Stack sub-groups
  - Dielectric and conductive materials
  - Coatings
- Uses single XML-based file
- Revised IPC-2581C supports automated bidirectional date exchange DFX intelligence capability



IPC-2581; Image credit: IPC-2581

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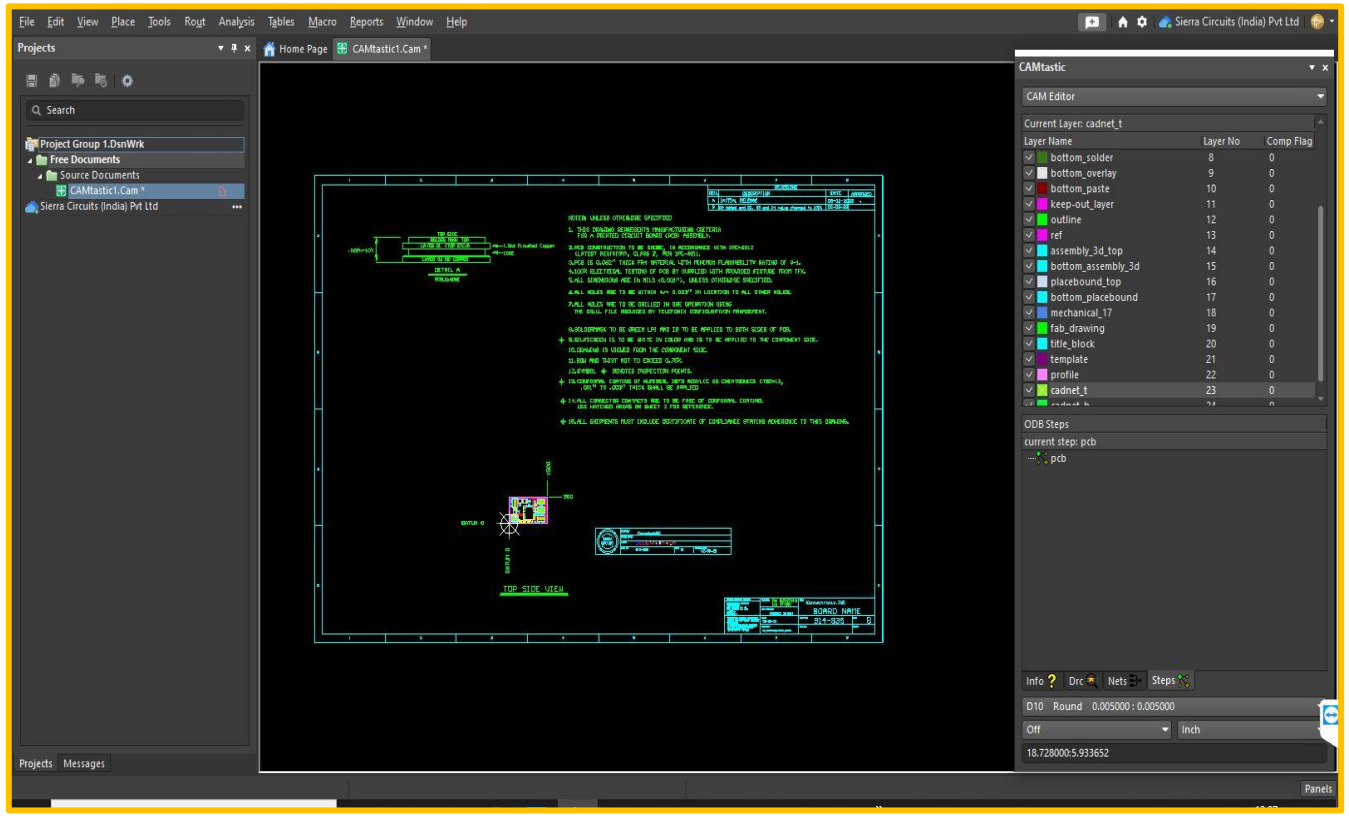
ODB++ files

- Transfer additional information than the standard layer artwork and drill data
- Data stored and arranged in multiple files and folders
- Operating system commands fuse all data into one compressed file
- Comprises material stack-up, BOM, component placement coordinates, dimension and fabrication details
- Can be accessed through most PCB design programs (Expedition, PADS, Allegro)



ODB++ file format

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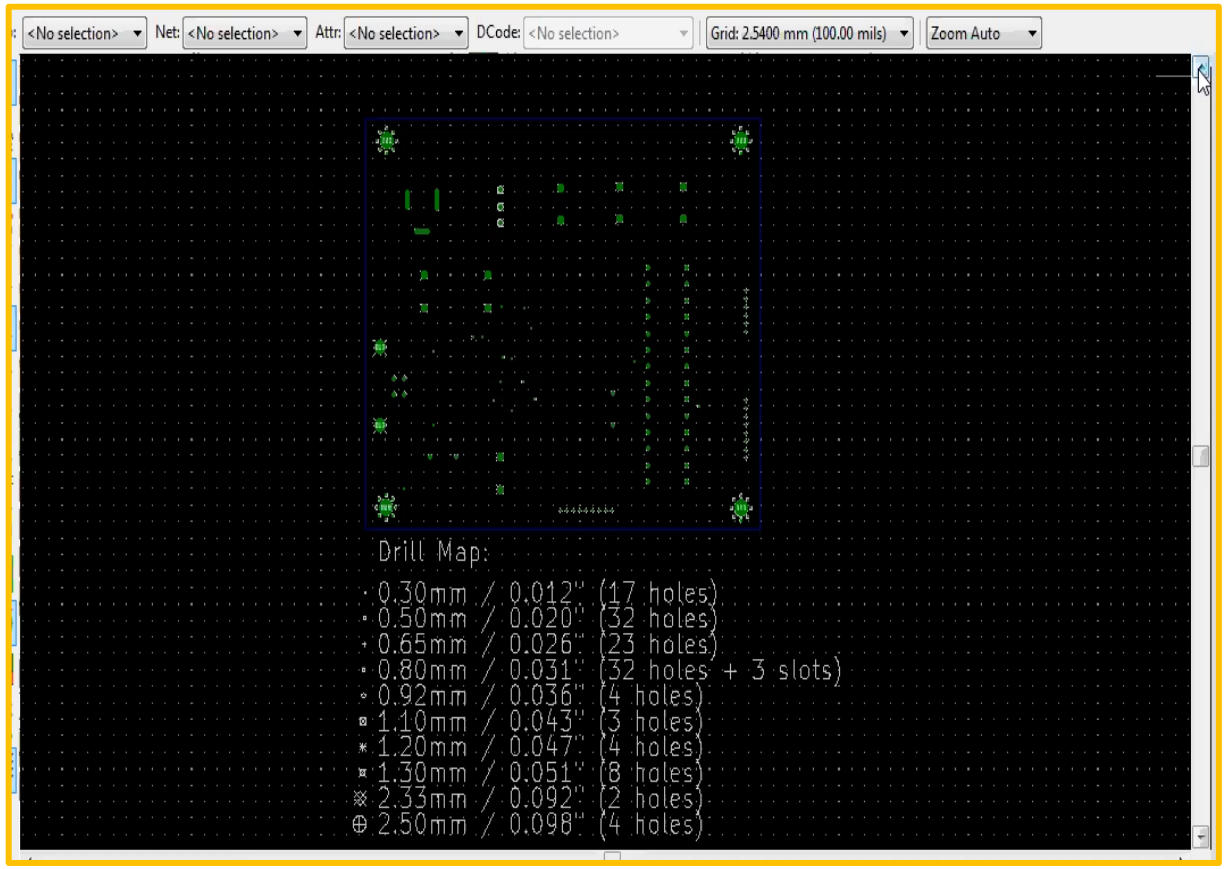
NC drill files

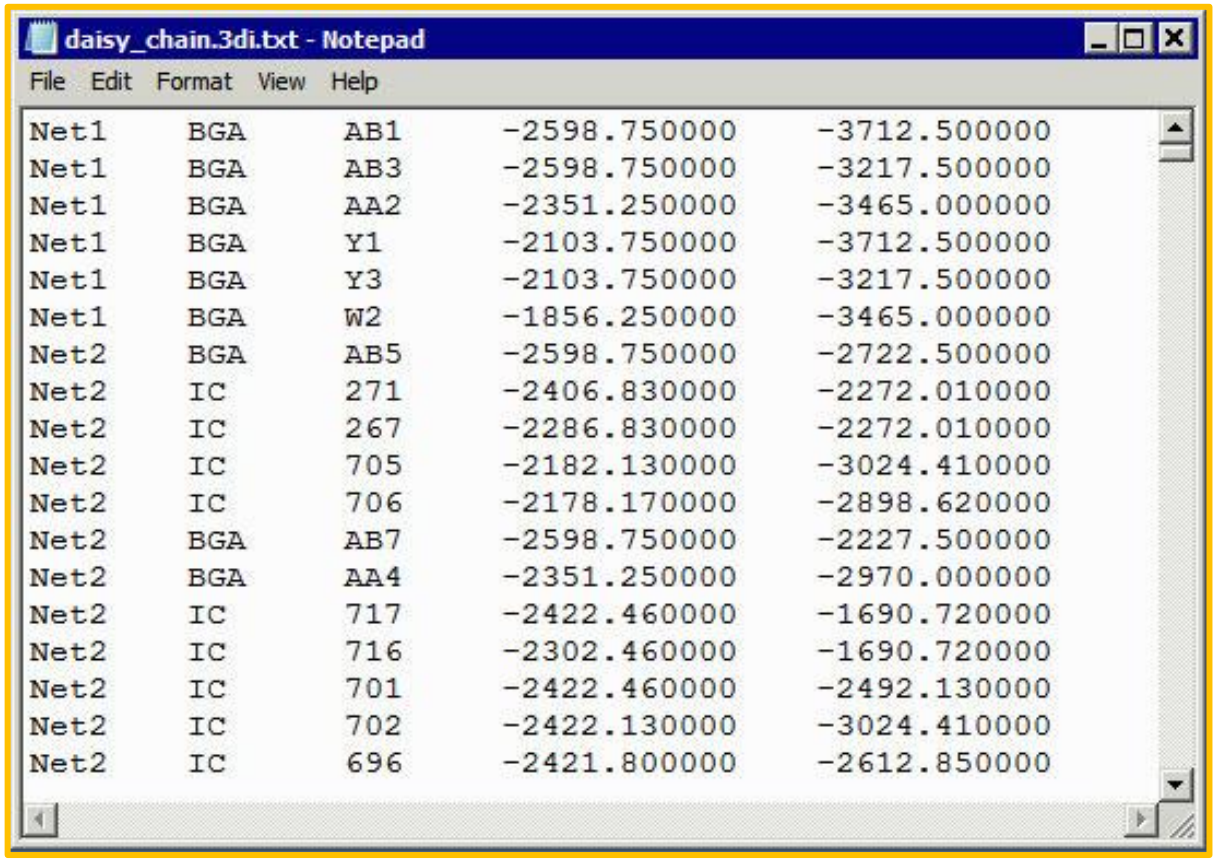
- Define board drilling and routing data, hole position, size, and number of holes
- Formats of drill files are:
  - IPC-NC-349
    - Refers to the machine-readable input format
    - Used by computer numerical control (CNC) drilling and routing tools
  - NC (XNC) format
    - Part of the IPC-NC-349 standard
    - Highly compatible with existing software for NC drill files
  - Excellon drill format
    - Includes necessary instructions to operate CNC drilling and routing machines
    - Default standard for drill files
    - Two types of Excellon drill files: Excellon 1 (older version) and Excellon 2



NC drill files

IPC netlist

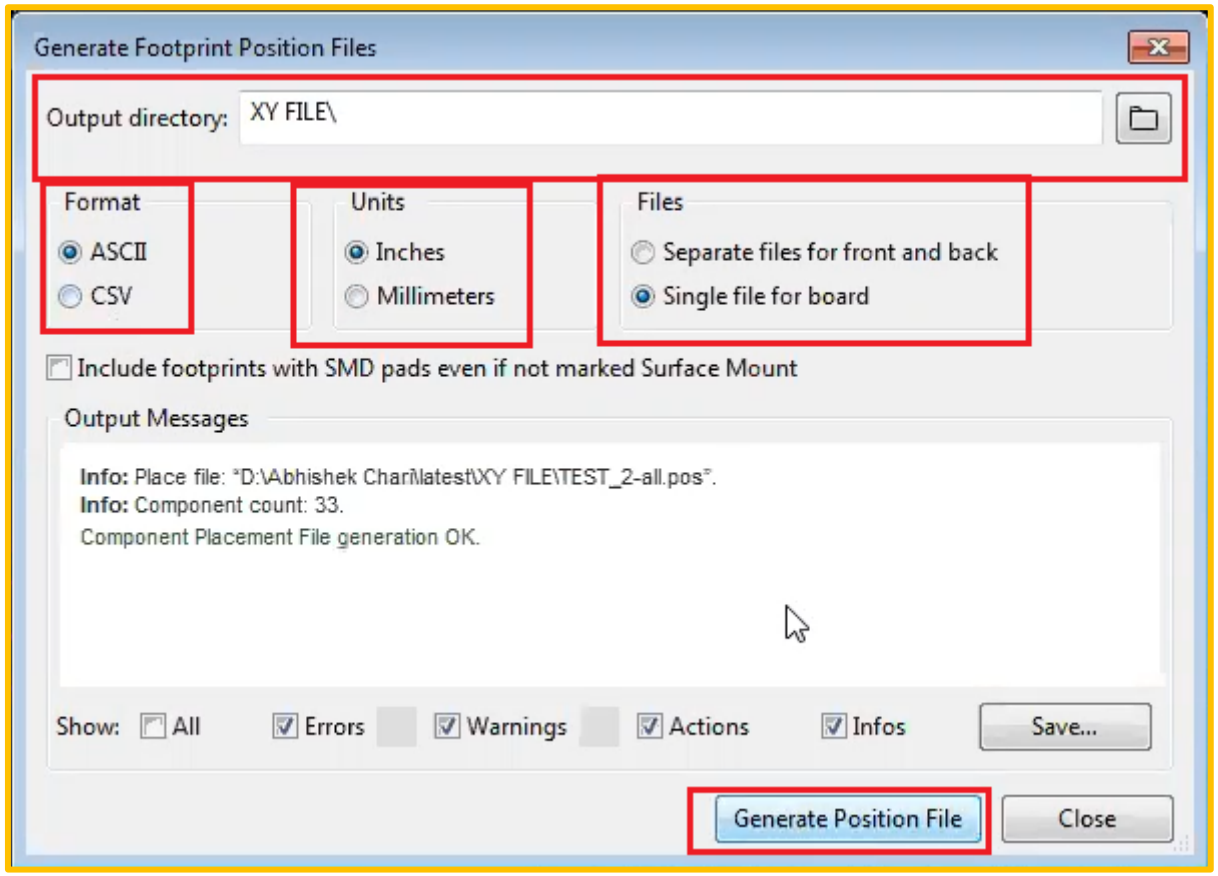
- Contains a list of networks that forms interconnection scheme of the board
- It is an ASCII text file with the PCB CAM system instructions
- Includes the net names, pins, and X-Y coordinates of the start and end point for each net/node



IPC netlist file

Pick and place files

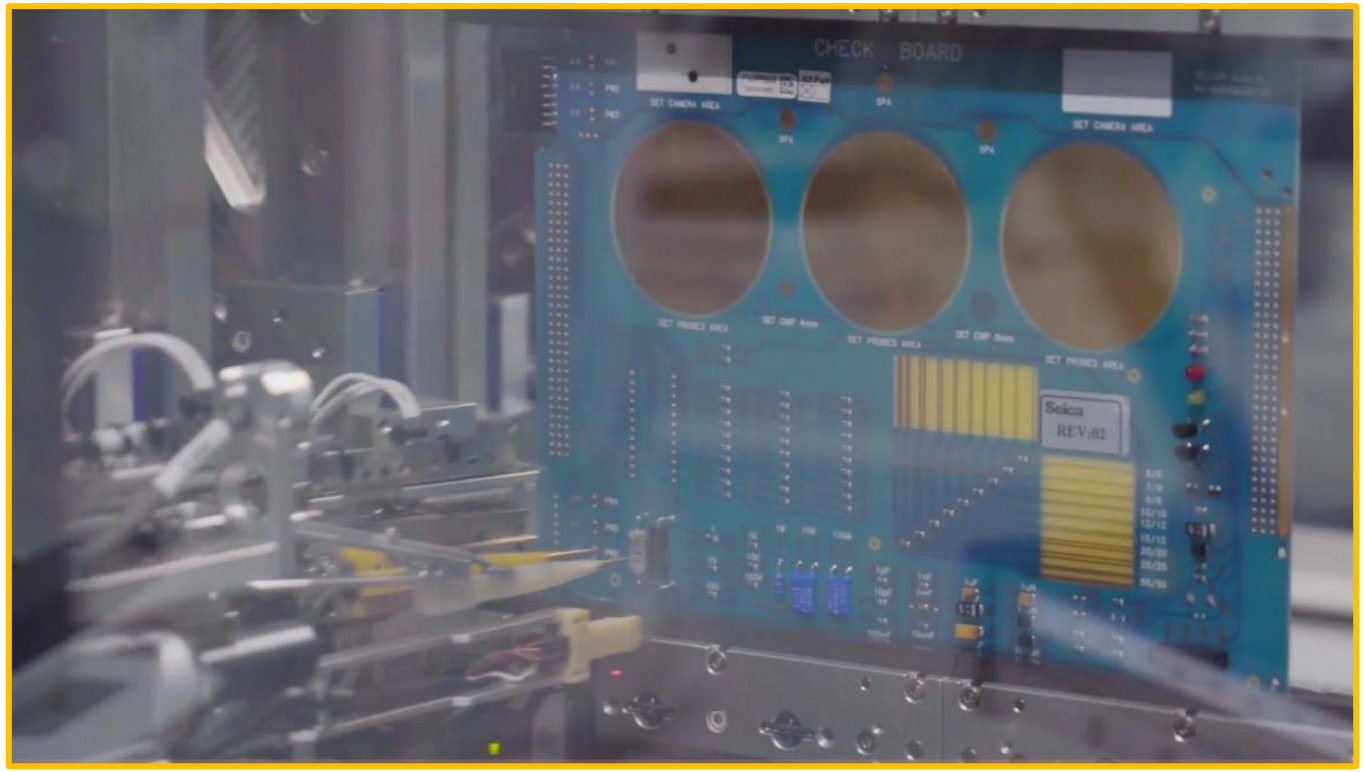
- These files are responsible to pick the right component and place it at the desired position during the assembly process
- Store data in ASCII format and can be generated by any design software
- Convey information about the position and orientation of all surface mount devices
- Define X-Y coordinates and rotation for each component to be assembled
- Define TOP and BOTTOM solder paste files



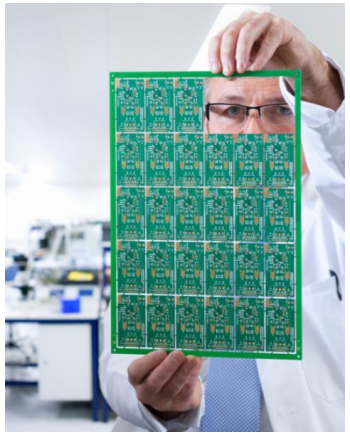
Pick and place file format

Design for testing analysis

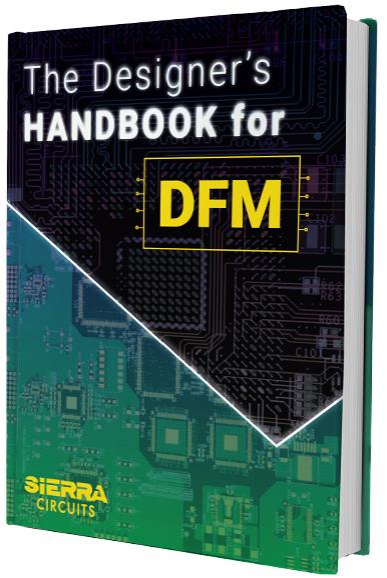
- Define the testing procedures to check the circuit performance
- Specify the parameters you want to measure
- Define test points to your layout where probe access points do not exist
- Mention the test points clearances from the edges
- Flying probe testing can check for:
  - Open traces and short connections
  - Misplacement of components
  - Value of capacitors, resistors, and inductors



Vertical FPT testing



SIERRA CIRCUITS RESOURCES



Download our DFM Handbook and other e-books.

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See our products and services.

Browse our knowledge base.