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CADENCE PCB SOLUTIONS

OrCAD Sigrity ERC

Electrically aware rule checking for signal quality challenges

OrCAD® Sigrity™ ERC (Electrical Rules Check) provides electrical rules checking technology that enables the PCB layout designer to easily and quickly identify signal quality issues and causes without the need for simulation models or extensive signal integrity expertise.

Built using industry- and market-leading Cadence Sigrity technology, OrCAD Sigrity ERC goes beyond simple geometry-based design-rule checking (DRC), identifying signal quality issues that have typically only been uncovered by advanced SI/PI tools.

OrCAD Sigrity ERC is fully integrated with the OrCAD PCB Editor, allowing PCB designers to see issues within the PCB canvas, make a change, and validate the ERC has been corrected.

Overview

OrCAD Sigrity ERC empowers PCB layout designers to check and address signal quality issues that in the past have required complex SI simulation tools and SI engineers. Using ERC and simulation-based rule checking (SRC) during PCB layout can reduce overall design time by enabling signal quality issues to be found and addressed during PCB layout design, reducing the burden for SI experts.

ERC- and SRC-based solutions are superior to DRC-based solutions in ensuring signal quality validation, identifying issues geometry-based DRCs often miss. OrCAD Sigrity ERC is specifically designed for PCB layout designers leveraging industry-leading Cadence Sigrity technology, providing an easy-to-use interface with minimal setup and cross-probes with the PCB layout design. OrCAD Sigrity ERC delivers actionable results that identify and quickly address signal quality issues.

Highlights

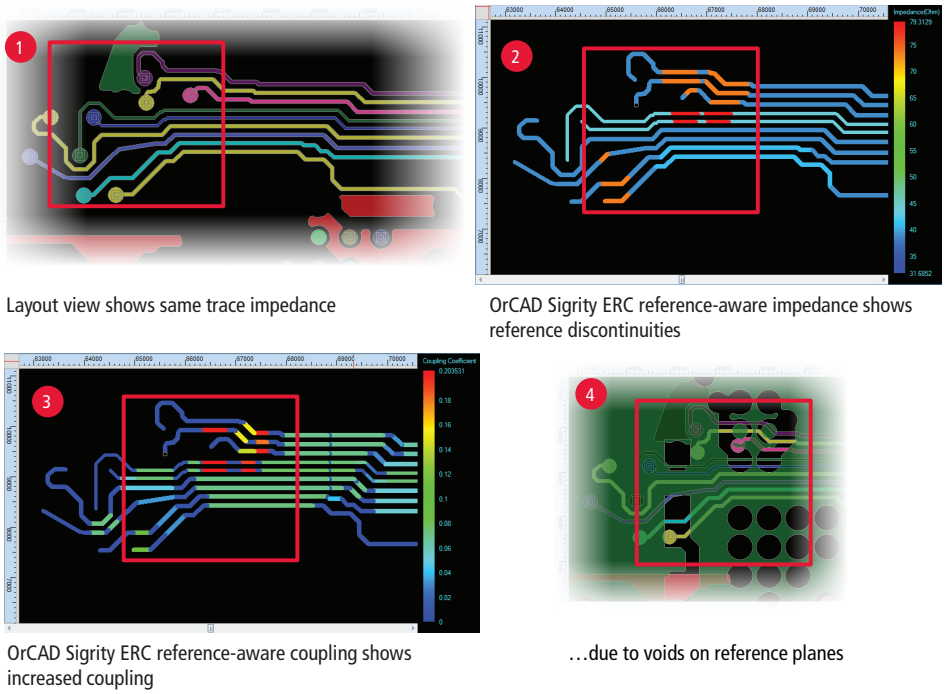
- No models required—easy to run by PCB layout designers
- Detects impedance discontinuities of routed PCB signals
- Detects excessive coupling between routed PCB signals
- Integrated with OrCAD PCB Designer for easy modification of problem signals

Why Is ERC Superior to DRC?

DRC-based signal quality checks usually use the design's dimensional information, such as length, width, distance, spacing, etc. They cannot validate the interconnect's electrical characteristics such as signals crossing split or different reference planes causing impedance changes. In contrast, ERC-based signal quality checks analyze at the individual, segment-level view in the geometry domain for signal quality, including:

- Trace reference
- Trace reference-aware impedance
- Trace reference-aware coupling
- Differential pair routing phase
- Number of vias and via locations

All analysis is organized for easy signal performance interpretation by the PCB layout designer, NOT the signal integrity (SI) expert.



Layout view shows same trace impedance

OrCAD Sigrity ERC reference-aware impedance shows reference discontinuities

OrCAD Sigrity ERC reference-aware coupling shows increased coupling

…due to voids on reference planes

Figure 1: OrCAD Sigrity ERC reference-aware impedance/coupling overlay

Features

Electrical rule check for PCB layout designers

OrCAD Sigrity ERC is an easy-to-use reference-aware trace impedance, coupling and reference check tool for advanced PCB layout signal quality checking. Three options are available:

- Check all nets
- Check selected nets
- Check by net groups

OrCAD Sigrity ERC produces the impedance and coupling overlay, where layout traces are color-coded with impedance and coupling coefficient values. The overlays clearly show increased impedance and coupling due to voids on reference planes, which would be practically impossible to identify on the board level with visual inspection. See Figure 1.

Comprehensive results tables

OrCAD Sigrity ERC also generate comprehensive results tables (see Figure 2):

- Trace segment-by-segment results
  - Reference-aware impedance
  - Reference-aware coupling
  - Upper/lower layer reference
  - Coplanar reference
- Net-level results
  - Impedance summary
  - Coupling summary
  - Length and delay
  - R, L, and C
  - Number of reference discontinuities
  - Number of no reference sections
  - Number of vias
- Board-level results
  - Routing area
  - Component placement area
  - Routing efficiency

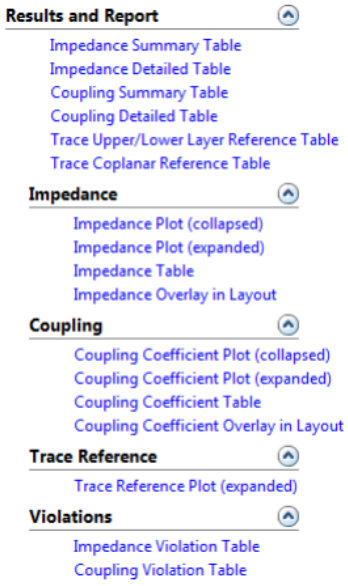
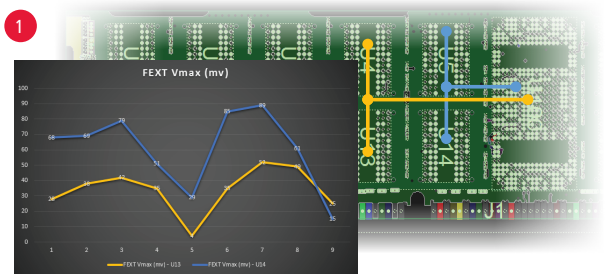
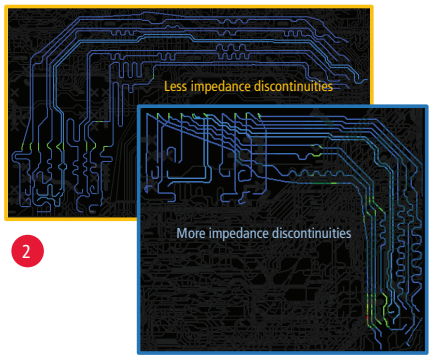


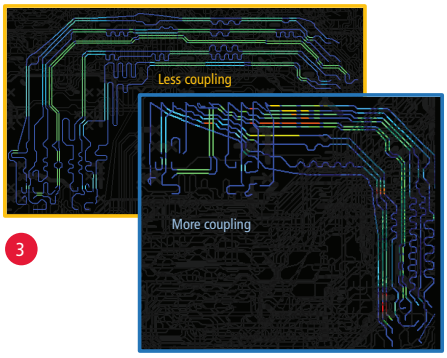
Figure 2: OrCAD Sigrity ERC delivers comprehensive results tables with actionable results



SRC shows the shorter (blue) data signals have more FEXT



ERC shows the shorter (blue) data signals have more impedance discontinuities ...



... And more coupling

Figure 3: SRC/ERC example

Advanced signal quality checking

OrCAD Sigrity ERC also includes a simulation-based rule checking (SRC) environment. This net-level PCB layout checking engine is based on time-domain simulation, and considers:

- Loss
- Delay
- Reflections due to termination and impedance discontinuities
- Trace couplings
- Via coupling

SRC setup is easy, with voltage pulses as stimulus representing signal amplitude, data rate, rise/fall time, and driver/receiver terminations. Device simulation models are not needed.

After SRC simulation, TX, RX, NEXT (near end xtalk), and FEXT (far end xtalk) waveforms are available, as well as SI metrics calculated using RX and FEXT waveforms as signal quality indicators.

ERC and SRC Solutions and Flows

With easy setup and fast simulation, OrCAD Sigrity ERC enables practical first-order screening of electrical issues before handing off to SI experts for final check (see Figure 3). For example:

- Use ERC to screen layout and identify the worst case for further SRC or SI analysis
- Use SRC to evaluate the SI impact of design rule violations and investigate tradeoffs
- Use ERC to find out how to fix SI problems shown in SRC or SI simulations
- Compare ERC and SRC results with known-good reference design and the part of the design that has been fully analyzed

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