DATASHEET

cadence

Xcelium Logic Simulator

Industry Leading Highest Performance Digital and Mixed-Signal Simulation Platform

Cadence® Xcelium™ Logic Simulator provides best-in-class core engine performance for SystemVerilog, VHDL, SystemC®, e, UVM, mixed-signal, low power, and X-propagation. Cadence simulator technology is known for innovation and technology leadership with a history of advancing digital and mixed-signal simulation and metric-based verification closure. Examples include the creation of the Verilog language in the mid-late 80s and its donation to the industry in the early 90s, the creation of the Verilog-AMS and Verilog-A languages, leading the SV-RNM language extensions in the late 2010s, and our many patents in our constraint solver and mixed-signal elaboration technology.

Key Benefits of Xcelium

- The industry's leading highest-performance and highest-capacity simulator
- The market's fastest unified front-end compiler across the entire verification flow from simulation to emulation
- Best-in-class multi-core engine to speed-up long-running test cases
- Automated parallel and incremental build technologies to support the compilation of the largest SoC designs
- Leading edge save/restore technology supporting digital and real number simulation in Xcelium and analog mixed-signal simulation with Spectre
- Dynamic test loading, constraint solver optimization, multi-threaded parallelism
- Advanced simulation profilers enable users to locate performance bottlenecks graphically
- History of continuous performance improvement across each release

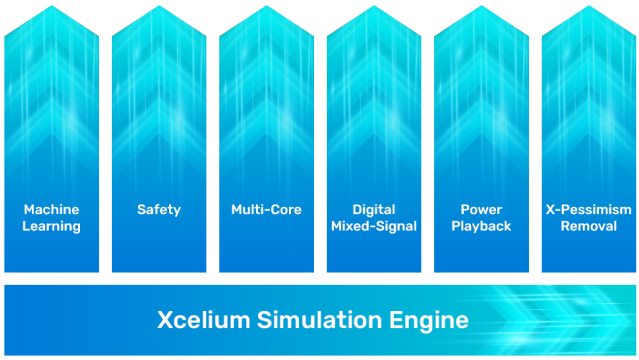


Figure 1: Apps natively integrated with the Xcelium Logic Simulator

Xcelium Apps are the next step in the evolution of logic simulation. These apps deliver domain-specific technologies to enable the highest levels of verification performance spanning from IP to SoC to chiplets covering the most complex of modern designs.

Key Benefits of Xcelium Apps

- Xcelium Machine Learning (ML) App
  - Leverage the power of machine learning for regression compression, accelerated coverage closure, and bug hunting
- Xcelium Digital Mixed-Signal (DMS)
  - The DMS App enables mixed-signal verification at RTL speeds using advanced SystemVerilog Real Number Modeling and native co-simulation with Cadence Spectre® SPICE analog simulation
- Xcelium Multi-Core (MC) App
  - Fastest GLS closure, up to 10X acceleration on DFT simulations
- Xcelium Safety App
  - Highest performance safety campaign execution for ISO 26262 compliance with Xcelium Safety App. The App enables both serial and concurrent fault simulation
- Xcelium Power Playback (PPB) App
  - Glitch-accurate power estimation of multi-billion gate SoC
- Xcelium X-Pessimism Removal App
  - Shorten Debug time, eliminate X's by bringing gate-level behavior to RTL

Xcelium Simulation Engine

Cadence Xcelium Logic Simulator provides best-in-class core engine performance for SystemVerilog, VHDL, SystemC®, e, UVM, mixed-signal, low power, X-propagation, parallel and incremental build. It provides the industry's highest-performance simulation and constraint solver engines. The simulation engine natively takes full advantage of multicore processors with multi-threaded technology, enabling users to quickly speed up high-activity, long-pole tests by allocating more cores at runtime. Xcelium simulator offers a significant speed-up at the IP level by leveraging over-constraint messages, constraint performance analysis, and debug capabilities. Xcelium parallel and incremental build flows can greatly decrease the build time, elaboration memory footprint, and storage space required to elaborate the design.

Xcelium Low-Power Engine

Mobile and handheld applications require advanced low-power design and verification techniques. To meet power targets, the manufacturers of these devices must use advanced low-power techniques, such as power shutoff (PSO), multi-supply voltage (MSV), and adaptive methods, such as dynamic voltage frequency scaling (DVFS). These methods must be used in the architectural phase, defining the power intent using the IEEE 1801 Unified Power Format (UPF). Low-power verification includes all the challenges of functional verification plus the following:

- RTL may contain behavioral constructs that are not synthesizable, and therefore, not appropriate for power-aware simulation
- Extremely complex power intent
- Debugging power-related problems
- Multiple sources of possible errors: RTL, Power Intent, Liberty and Power Models
- Increasing number of power states and complexity
- Low power with mixed signal
  - Include RNM, wreal, electrical, and SPICE models of analog devices in the low-power simulation
  - In-out ports are supported
  - Support for power supply modeling with custom resolution functions
- Power Intent
  - Comprehensive support for UPF 1.0, 2.0, 2.1. 3.1
  - Cadence actively participates in the IEEE-1801, aka UPF, low-power format standardization committee
- Xcelium isolation analysis at RTL
  - Add isolation without UPF. Enables the detection of isolation-related problems early in the verification cycle
- X-propagation
  - RTL can hide "X" values, which will appear much later in the gate-level simulation. X-propagation transformations RTL structures that synthesize to muxes and flip flops so that they mimic the processing of X values done by their gate-level equivalents but run at RTL without the need for a gate-level netlist
- Disable timing checks/assertions during power shutoff
- Support of Information model/checkers
- Hybrid isolation/retention flow
  - Support of mixed inferred/instantiated isolation and state retention
- Debug support
  - Differentiate "X" from low power vs. a functional "X"
  - Tightly coupled with the Verisium™ Debug App

Xcelium Mixed-Signal App

Cadence's mixed-signal verification solution continues to be the industry's "Gold Standard." The Xcelium Mixed-Signal App enables mixed-signal verification at RTL speeds with advanced SystemVerilog Real Number Modeling and native co-simulation with the Cadence Spectre SPICE analog simulation. The App features some of the industry's most significant mixed-signal verification features and methodologies.

- The dynamic user-defined resolution functions enable fault simulation with RNM
- The support for coverage with real numbers, real number constraints, and real assertions enables seamless metric-driven verification with traditional UVM and UPF (low power) methodologies
- Use the attribute-driven methodology to manage design flow and allow portability and maintainability of RNM. This technology also eases the transition from Verilog A/AMS to SystemVerilog RNM
- Mixed-network debug allows easy identification of incorrect system behavior at the analog/digital interface
- Extended SystemVerilog language support for RNM and connectivity to SPICE allows easy RNM development and validation
- Use enhanced RNM methodologies that yield SPICE-like accuracy but digital simulation speeds to identify bugs more rapidly and drive verification to closure with very high confidence
- Excellent AMS Rapid Adoption Kit (RAK) and Advanced Real Number Modelling Training courses
- Enhanced support for UPF with mixed signal designs allows seamless and efficient verification of critical low-power architectures in large SoCs. Such SoCs have many power domains that can be verified with accurate models and/or real implementation of power supplies

The Cadence mixed-signal verification solution additionally supports

- Build methods such as parallel and incremental build
- Simulation technologies such as Save/Restart and Dynamic Test Load
- Usability with Xcelium functional safety solutions

Xcelium Multi-Core App

Cadence's Xcelium Multi-Core App is the industry-leading solution for accelerating gate-level simulations.

The Xcelium Multi-Core App (Xcelium MC) shortens SystemVerilog design simulation time by breaking the design dependencies into independent parts and then simulating those parts on parallel cores of a server. It automatically partitions the design and dynamically allocates the independent parts across parallel cores of a socket to maximize their usage. The effect is a significant acceleration of simulation across active and large designs.

DFT simulations are the sweet spot for MC, as they are high-active tests with minimal activity in the testbench, and therefore, the entire design can be accelerated efficiently. The Xcelium MC App is a highly scalable solution, as simulation performance gains increase with more cores in cognizance of test activity. It can provide 2X – 10X performance gains for gate-level simulations and accelerate huge billion-gate complex designs with complete support for timing and debug capabilities, including full visibility of the design.

Xcelium Machine Learning App

All DV engineers running zillions of nightly regressions, struggling to achieve coverage goals faster, are looking for a plug-and-play solution—an automated solution that can help close coverage faster using minimal resources. The Xcelium Machine Learning (ML) App utilizes Cadence's

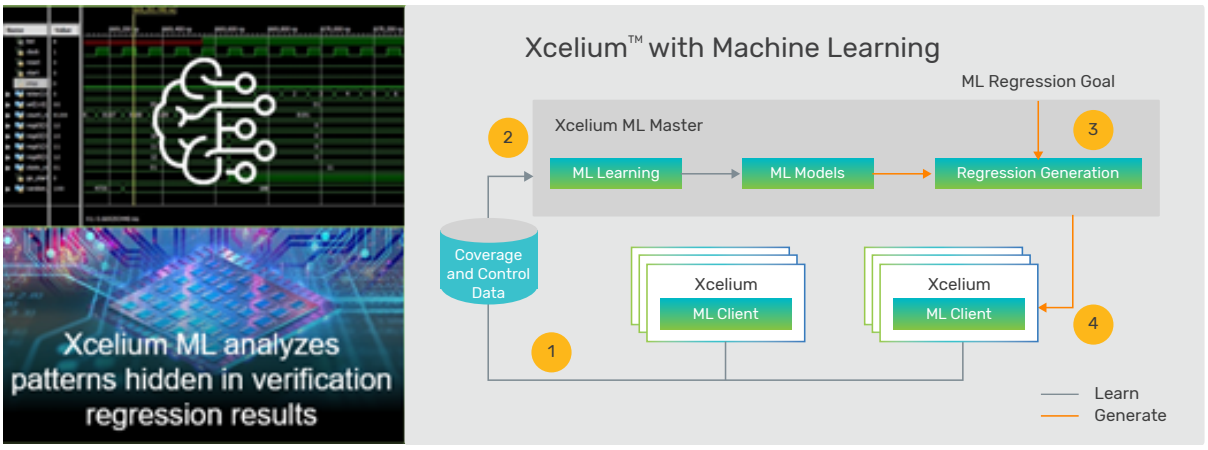
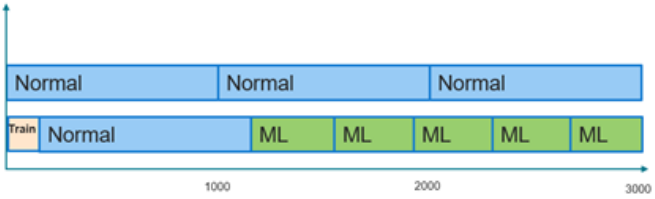


Figure 2: The Xcelium ML Flow

proprietary ML technology to reduce regression times up to 10X by learning from previous regression runs and guiding the Xcelium randomization kernel to achieve the same coverage with significantly fewer simulation cycles or expose more bugs around specific coverage points of interest.

Xcelium ML has the following use model:

1. Regression Compression – reduces compute resources
2. Targeted Regression – focuses runs on design changes
3. Bug Hunting – creates ML runs stressing more rare scenarios to fill bug hunting budgets



4. Accelerated Coverage Closure – start training on a small number of regression instances, then use ML runs to saturate coverage. Use iterative training to accelerate coverage closure. Xcelium ML targeted flow can increase runs around holes.

Xcelium Safety App

Xcelium delivers serial and concurrent fault injection; Xcelium is the only simulator with concurrent injection enabled in the main engine and meets the fault injection testing requirements in the ISO 26262 automotive safety standard.

The Xcelium Safety App enables serial and concurrent fault simulation, which, combined with Cadence's safety verification full flow comprising Jasper Safety, vManager Safety, and Midas Safety Planner, enables the highest performance safety campaign execution for ISO 26262 compliance. Cadence offers automotive Functional Safety Documentation Kits covering the full spectrum of semiconductor design and verification. The kits satisfy documentation requirements that automotive component suppliers must provide for their tools and flow to achieve ASIL certification. Additionally, the kits reduce the effort required to evaluate tool use cases within each of the supplier's automotive design projects and help them avoid costly tool-qualification activities.

The Jasper™ Functional Safety Verification (FSV) App offers structural fault analysis with structural fault connectivity, activatability, and relation analysis; formal fault analysis with formal activatability and propagability analysis; and custom safety and security analysis, which can create custom strobes and fault specifications to model attacks from hackers. The Jasper FSV App automatically annotates structurally safe faults in a given database of faults, and Xcelium runs all the other faults from that database.

The safety solution integrates the Spectre Simulation Platform, and Legato™ Reliability Solution automates the launching of analog and mixed-signal fault simulations for different failure modes.

Functional safety is a highly optimized flow, and the Cadence solution is the most comprehensive on the market. The complete flow can handle everything—from FMEDA capturing and optimized fault management to the fault injection and classification natively built into Jasper, Xcelium, and Palladium®, the Cadence safety flow suits all needs.

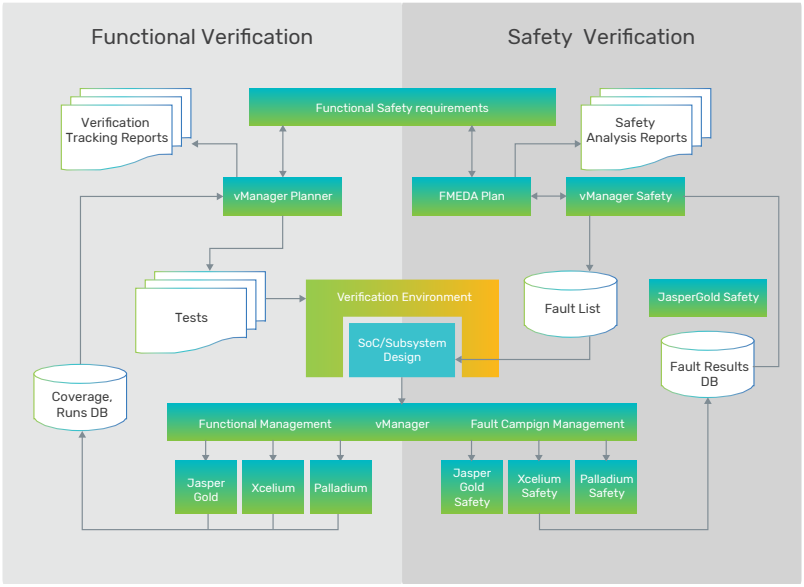


Figure 3: ISO 26262 Compliant Cadence Xcelium Fault Simulator Solution

Xcelium X-Pessimism Removal App

The Xcelium X-Pessimism Removal (XPR) App shortens debug time by using advanced algorithms to make the propagation of "X" values in simulation match hardware. This App is designed to help find X-related issues at RTL and reduce the requirement for lengthy gate-level simulations. The simulation semantics of conditional constructs in both HDL languages, Verilog and VHDL, cannot accurately model the ambiguity inherent in un-initialized registers and power on reset values. These issues are particularly problematic when the indeterminate states modeled as "X" values become control expressions.

Xcelium Power Playback App

The Xcelium PowerPlayback App enables the massively parallel Xcelium replay of waveforms captured by Palladium® emulation onto a timing-annotated gate-level netlist for creating glitch-accurate waveforms of multi-billion gate SoC designs. This alleviates the challenges designers face while estimating actual dynamic power; it becomes more critical as we move below 14nm, as a significant portion of dynamic power results from glitches.

The power estimation tool can use these glitch-accurate waveforms to obtain highly accurate dynamic power estimation. The Cadence Xcelium PowerPlayback helps estimate the dynamic power estimation accurately. The user can replay the original 0-delay waveforms (Palladium) and reconstruct the glitch-switching activities on signals/nodes of the netlist. Palladium's Dynamic Power Analysis (DPA) capabilities enable users to analyze power trends over very long emulation runs to identify time intervals for more accurate glitch-based power analysis.

Xcelium Simulator and Xcelium Apps are tightly integrated with Cadence's Verisium (AI-powered debug solution for fastest bug root cause analysis)

- Verisium Manager – Full flow IP and SoC-level verification management with verification planning, job scheduling, and multi-engine coverage, with AI-driven test suite optimization to improve compute farm efficiency.
- Verisium Debug – Comprehensive debug solution from IP to SoC and from single-run to multi-run, offering fast interactive and post-process debug with waveform, schematic, driver tracing, and SmartLog technologies
- Verisium AutoTriage – Helps automate the repetitive task of regression failure triage by predicting and classifying test failures with common root causes
- Verisium SemanticDiff – Helps pinpoint potential bug spots by comparing multiple source code revisions
- Verisium WaveMiner – Helps analyze waveforms across a full verification testsuite and determine the signals and times that are most likely to represent the root cause of test failures.
- Verisium PinDown – Integrates with industry-standard revision control systems to build AI models of source code changes, test reports, and log files to predict the source code check-ins that are most likely to have introduced specific failures.

Conclusion

Xcelium is the best-in-class high-performance and high-capacity simulator offering the following benefits:

- Comprehensive, high-performance Verilog, System Verilog, VHDL, e, and mixed-signal simulation for complex SoC designs
- Fast debug turnaround time with incremental compilation and elaboration
- Fastest coverage closure and project completion supporting coverage resilience, coverage analysis, and rapid debug

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