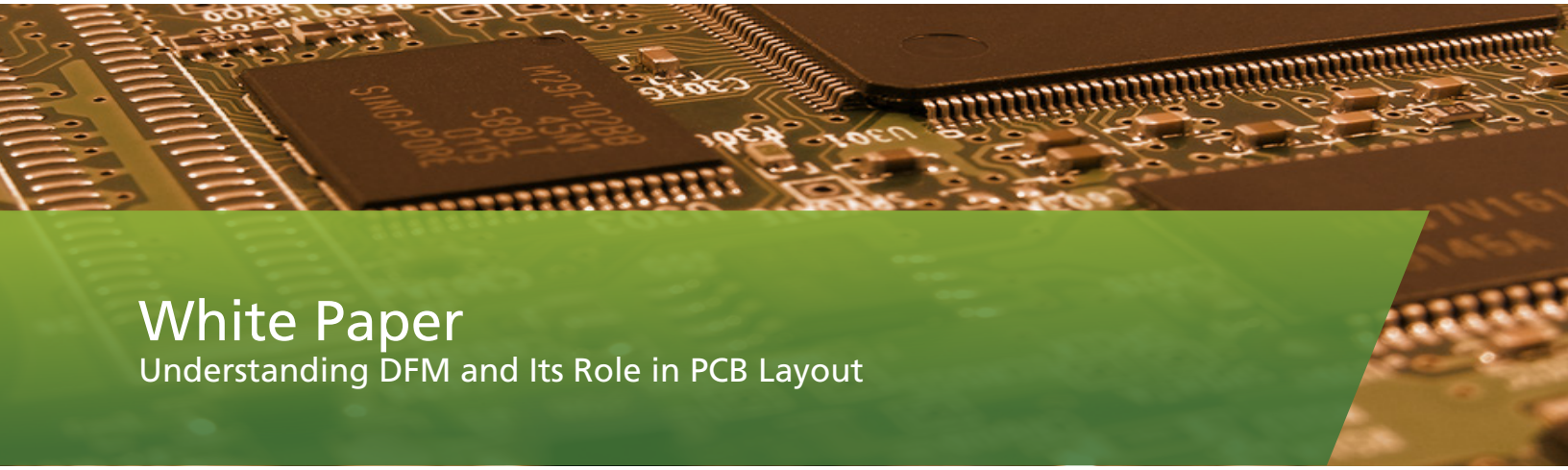
OrCAD™
CADENCE PCB SOLUTIONS



White Paper
Understanding DFM and Its Role in PCB Layout

Understanding DFM and Its Role in PCB Layout

DFM, DRC, DFF, DFA, DFwhat? All terms we hear used daily in the PCB design world regarding manufacturing analysis and often used interchangeably. But what exactly is DFM and why is it an important but often ignored aspect of the PCB design process?

Let's start by clarifying some terms. DFM is short for "Design for Manufacturability". It is the process of arranging a PCB layout topology to mitigate problems that could be encountered during the PCB fabrication and assembly processes required to manufacture an electronic system. Addressing fabrication issues is what's known as Design for Fabrication (DFF), and addressing assembly is known as DFA or Design for Assembly. The two together mostly make up DFM analysis. Mostly.

In many cases the term DRC, which actually stands for Design Rule Checking also gets used interchangeably and creates further confusion regarding DFM. That's understandable because DRC issues detected in manufacturing can indeed have a direct impact on the manufacturability of a PCB. However, DRC is markedly different from DFF and DFA.

Figure 1 These starved thermals pass electrical DRC, but in reality the connection to the actual source is insufficient for a good connection

> "Good DFM ensures that a design not only performs electrically as expected, but can be manufactured successfully in high volume quantities without increasing cost or risk, or adding unnecessary time to the design process"
>
> - Rick Almeida

Think of DRC as a hard "pass/fail" detection of a problem in a PCB. Either a problem exists or it doesn't. In engineering, DRC is used to ensure that PCB layout connectivity accurately reflect the connectivity definedin a board's associated schematic diagram. But connectivity is only one aspect of DRC. The "R" stands for "Rules". The "Rules" are used largely to definethe minimum spacing allowed between various PCB objects for the entire PCB or for individual layers, nets or areas on the PCB. In engineering, the spacing may have direct impact on circuit performance. In manufacturing, spacing may play a pivotal role in the ability to fabricate or assemble a PCB. As a result, DRC becomes a subset of DFM, but only if the rules used reflec a manufacturer's requirements for spacing. Otherwise, DRC is used solely for electrical verification.

DFM's two primary components, DFF and DFA, are more nuanced than DRC. While DRC detects very specificdiscrepancies from the intended interconnect, DFM identifiesissues in the PCB topology that have the "potential" to create manufacturing problems. What's more, a DRC defect will be present in every copy of the PCB built, so if there is a short missed in DRC, every PCB will contain the short, no matter how many PCBs are produced. By contrast, if the same PCB quantities contain DFM issues, problems may only manifest in some of the PCBs

while others perform correctly as expected. For example, a PCB layout containing very thin pieces of copper created in the design tool by rule would be correct per the schematic. And if spaced properly it would pass DRC. However that same slivers, being so thin, could potentially detach on the physical PCB and inadvertently connect itself to other copper elements during assembly, thus creating shorts on some PCBs but not on others. So the sliver would pass DRC verifiction, but in real-world manufacturing the sliver could cause some PCBs to fail. Without DFM, this problem would go on undetected and would result in scrap or rework.

Until recently, DFM analysis was either left to the PCB fabricator or assembly engineer to manage, or could only be performed by companies that had the financial resources to purchase high-end DFM analysis software and support a dedicated staff to run DFM analysis. Most PCB designers would perform only a DRC analysis and visual inspection of the design before submitting the design to be manufactured. Manufacturers who know that DFM issues like acid traps, slivers and starved thermal pad connections can decrease manufacturing yields and increase costs take it upon themselves to analyze the design, often making modificationsto ensure that the design can be built with maximum yields and lowest costs. So long as the finished PCB functioned properly, the design engineer was content. So why move DFM into the PCB design flow There are several reasons: cost of finished PCBs, maintaining design intent, and the potential for future design failure.

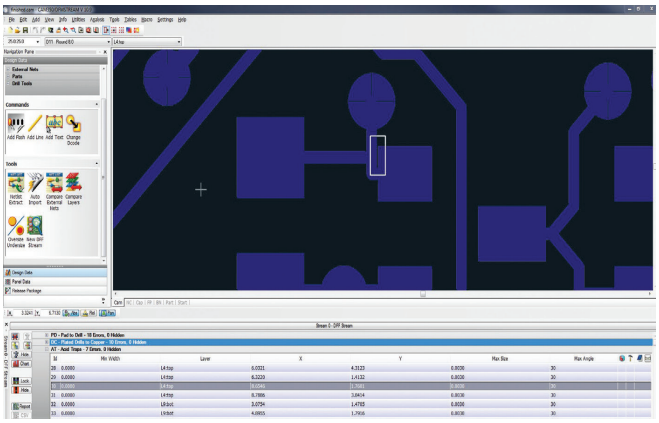


Figure 2 Acid traps have the potential of trapping acid during the PCB etching process longer than intended and can eat away a connection, making the circuit defective.

It can cost a PCB manufacturer as much as 20% of the cost of the PCBs for CAM engineering, the processing and tooling of design data to prepare it for manufacture. This additional cost is built into the end price that users pay to have physical PCBs fabricated. So, theoretically, designs submitted without DFM defects are less expensive to manufac-turer than ones with DFM defects. One could deduce that it's better to pay a little more to have a manufacturer ensure the design can be built. However, this creates other issues that are not so desirable.

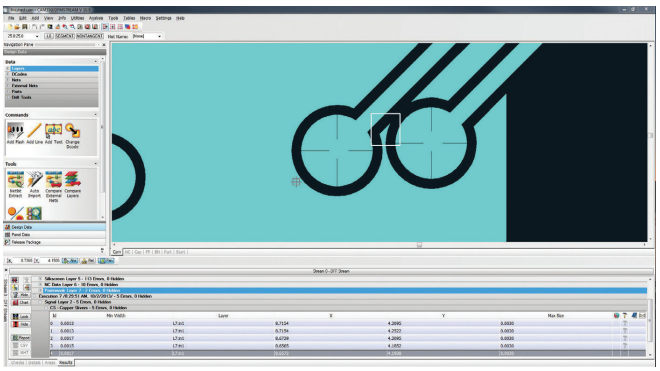


Figure 3 Small copper slivers can detach themselves during assembly, float aound during soldering and inadvertently reconnect themselves anywhere on the PCB, potentially tying multiple nets together.

To take a design that has DFM issues and make it comply with the manufactur-ing process, a CAM engineer may need to modify the design data. What this means is that the layout provided to manufacturing may not be 100% consistent with the finished PCB. Issues with electromagnetic interference, signal integrity, cross talk, etc., which are commonplace in today's high-tech electronics and are addressed in design engineering, may be unknowingly re-introduced into the design as it's reworked for manufacturing. There is also no guarantee that a CAM engineer will communicate the design changes back to engineering to be incorporated into the original PCB design database. So not only is the design layout different between engineering and manufacturing, but what happens when a second manufacturing build is required or the design is released to a different manufacturer for volume production?

Consider this real-life scenario: a design engineer designs a PCB, runs DRC analysis and determines that the design is correct. He creates PCB manufacturing filesand sends the filesoff to a manufacturer to have prototypes made. The manufacturing engineer runs his analysis on the PCB filesto ensure the design can be fabricated and identifiesdefects in the design that could result in scrap or low yields. Wanting to deliver a good product, the manufacturer fixs the issues, builds the PCBs and ships back the finishedprototypes without communicating what changes were made. Back in the lab, the design engineer tests the prototypes and they work successfully. That's great; however, unbeknownst to the design engineer, his prototypes are different from his PCB manufacturing fies. Now the design engineer releases the manufacturing fils for high volume production from a different manufacturer who specializes in production PCBs. This manufacturer, for one reason or another, chooses not to run an analysis prior to manufacturing and therefore doesn't detect the same issues as the prototype manufacturer. They build and ship the finished PCBs back to the customer. The boards are assembled and tested and, oddly enough, some, most, or all of the PCBs fail. Why? Because the design data still contained the original DFM errors in the manufacturing filethat were corrected in prototype, but never incorporated for production. The result was thousands of dollars in material being scrapped but – even

worse and more costly – lost time-to-market. Had the design engineer had the ability to perform his own DFM analysis prior to prototype, the same issues could have been detected and addressed in engineering and incorporated in the PCB design where they belong, lowering the cost, maintaining design intent, and ensuring that follow-on builds also work correctly. Just a few more minutes with the design in engineering would have prevented a whole design and manufacturing iteration, and the costs associated with it.

So what are DFM issues? Mostly these are issues in the PCB topology that create adverse effects in manufacturing and are typically not detected in the engineering CAD software that creates the design. The table below is a short list of typical DFM issues that pass detection in the CAD system but result in PCB failures in the real world.

DFM Defect	Description
Starved Thermals	Plane connections that are tied correctly to a plane layer in a CAD system but inadvertently isolated from the rest of the plane.
Acid Traps	Acute angles that allow acid to build up in the fabrication process and over-etch a trace, potentially creating an open in the circuit.
Slivers	Narrow wedges of copper or solder mask that can peel off and either reconnect to other pieces of copper or expose copper that should be covered with solder mask.
Insufficient Annular Ring	A drill size is specified that exceeds the size of the pad being drilled and can result in a disconnect of the pin or short in a voltage plane.
Missing Clearance Pads on Planes	Pins that are missing a clearance pad will be connected to a plane layer. If clearance pads are missing from all plane layers for the pin, it will tie together all of the voltage planes as well.
Copper too close to board edge	When there is insufficient clearance of plane layers from board edges it's very likely that the voltage planes will be connected together when the PCB form factor is routed. The copper on each voltage layer is inadvertently "mashed" together.
Missing Solder-mask Pads	End user failed to define a solder mask pad for a pin or component. This exposes more copper and creates the potential for bridging pins together during assembly.

These are but a short list of DFM issues. Good DFM tools will analyze for not only the above issues, but also many more that most PCB design systems are not architecturally designed to detect.

Until recently, having DFM analysis in-house has been very costly, creating an obstacle for many companies to adopt a pre-manufacturing DFM process. Previous DFM analysis software also came with a very high price point, ran on expensive hardware, and required dedicated users to run the analysis, making it very difficultfor adoption in the majority of the electronics market. The good news is that more mainstream DFM tools are now available in the market and can provide the same in-depth analysis, but instead have a very low cost of ownership to procure and, more importantly, maintain. These tools are also much easier for the everyday design engineer to use and deploy in the PCB layout process, without really having to be a manufacturing expert. Several of these new offerings allow users to model the rules that their intended manufacturer uses, to ensure that PCBs can be built by a particular manufacturer, and then rule sets can be switched to model different manufacturers when the design moves from prototype to production. Because these tools are designed as DFM tools and are free from the constraints of PCB CAD, they can detect problems in a design that are not supported by core PCB CAD tools. Good DFM ensures that a design not only performs electrically as expected, but can be manufactured successfully in high volume quantities without increasing cost or risk, or adding unnecessary time to the design process.

Sales, Technical Support, and Training

For the latest product or release information, visit us at www.orcad.com or contact your local Cadence Channel Partner.

The OrCAD product line is owned by Cadence Design Systems, Inc., and is supported by a worldwide network of Cadence Channel Partners (VARs). For sales, technical support, or training, contact your local channel partner. For a complete list of authorized channel partners, visit www.orcad.com/CCP-Listing.