OLogic

PRODUCTS

FROM CONCEPT TO REALITY

Presentation by: Ted Larson

Introduction/Agenda

1. What is OLogic - What do we do
2. Experience using Altium with Cadence tools
3. Post-layout validation workflow of MediaTek Genio designs and why it is critical to our design process
4. Signal integrity validation of high-speed signals
    a. *USB example*
    b. *Compliance examples: PCIe, HDMI, MIPI, DDR4, USB3*
    c. *PDN analysis*

Our Mission

OLOGIC PARTNERS WITH ITS CUSTOMERS FROM PRODUCT CONCEPT TO REALITY.

OLogic is Silicon Valley's premier engineering consultancy, specializing in robotics, IoT, and consumer electronics. With over two decades of experience, we've engineered the core technology behind hundreds of innovative products.

Our expert team covers all aspects of robotics engineering, including electrical, mechanical, hardware/software, and industrial design. Whether you're starting with an idea, a prototype, or something in between, OLogic can step in to bring your product to market readiness.

Misty Robotics

OLogic Specializes in

Robotic and consumer electronic products to provide

ELECTRONICS DESIGN

SOFTWARE ENGINEERING

DESIGN FOR MANUFACTURING

CONSUMER ELECTRONICS

Dash & Dot

Nvidia Kaya

Project Tango AR/Core

Happiest Baby Snoo

Force Trainer

A.M.P

ROBOTICS

Dusty Robotics

Relay Robotics

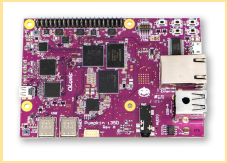
Bear Robotics

Knightscope

Cobalt Robotics

Simbe Robotics

IoT



Pumpkin Genio 350

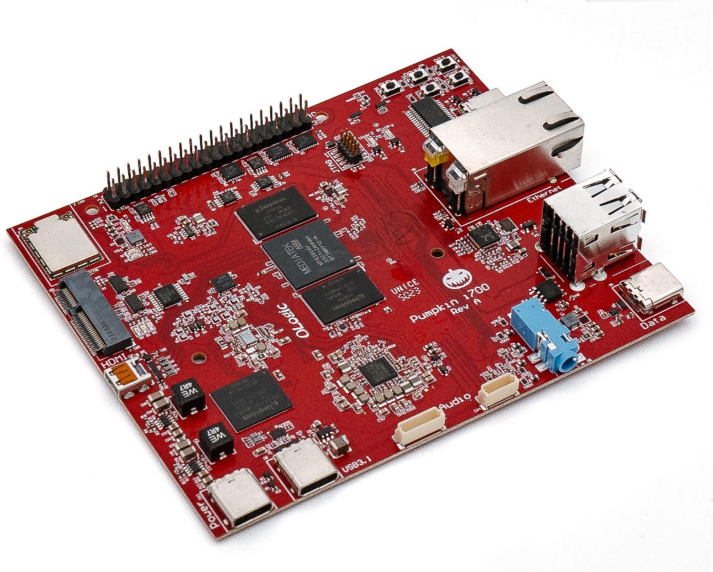
Pumpkin Genio 500

Angie Hospitality

Stealth Matrix

Snorble

Why Signal Integrity Simulation?



- We work heavily in the fields of robotics where the reliability of high-speed signals, such as MIPI, ethernet, PCIe, etc. are crucial.
- Simulation allows us to deliver designs to our clients with high confidence of industry-level performance, prior to the fabrication of the prototypes.
- Simulations provide critical data for high-density interconnect (HDI) designs in which space constraints and specific stackups highly influence routing and component placement, at times at the expense of high-speed routing.

USB 3 Example

Summary of Issue:

- Unable to communicate through USB from poorly designed flex cable

In-Lab Testing:

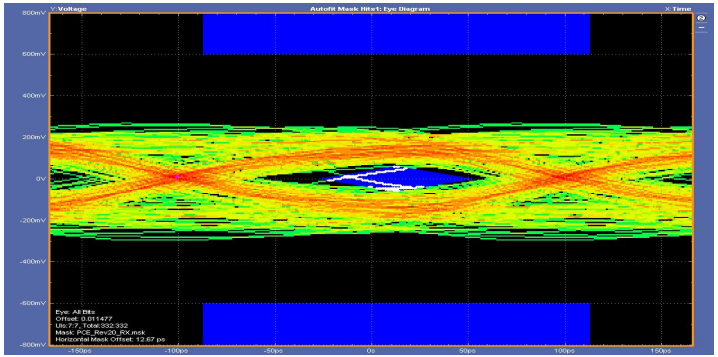
- Eye diagram analysis of USB 3.0 using off-the-shelf cable with our MediaTek board vs with a standard RPI dev board

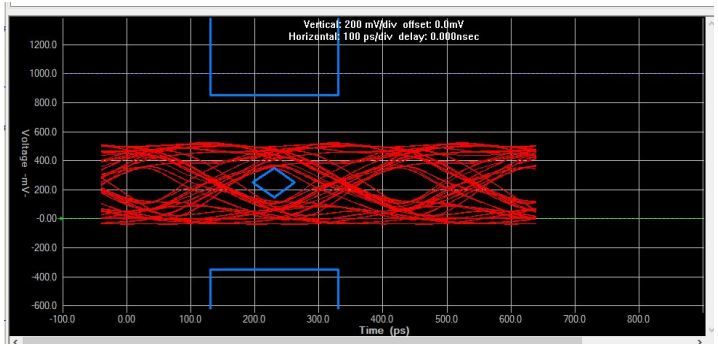
Replicating in Simulation:

- Able to replicate the observed real results in simulation

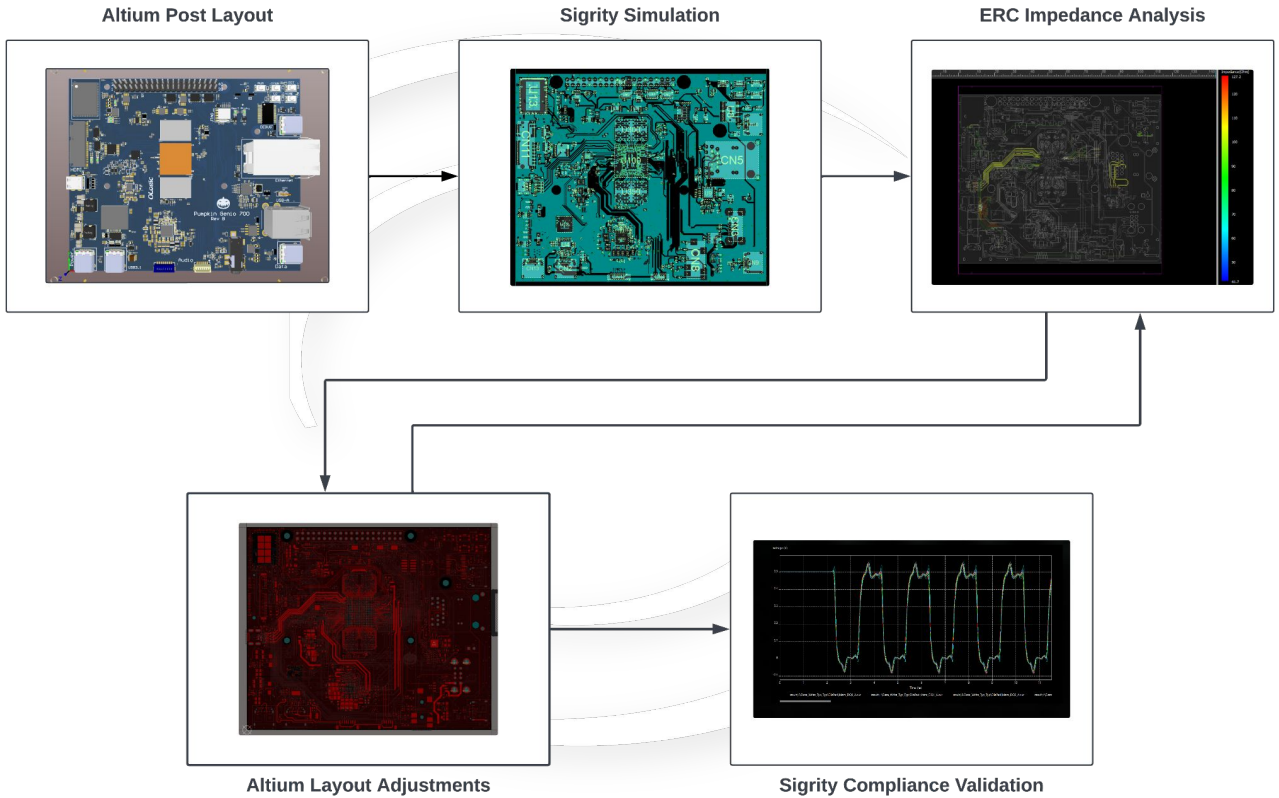
Takeaways:

- The issue was in fact the layout, not the cabling





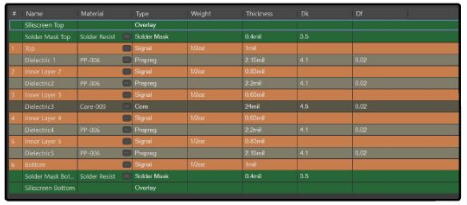
Altium Sigrity Workflow



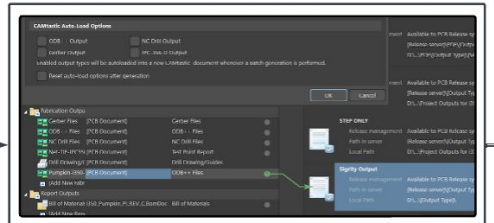
Initial Project Preparation in Altium

- Must use Altium Designer 21 or higher.
- Launch the Layer Stack Manager and make sure it is configured correctly: layer thicknesses; copper weights; material DKs.
- Add an ODB++ section to your OutJob and configure it so that only the electrical layers are on; turn off all the non-plated holes, and any drills that are not needed for conductivity, or which may not be connected to the electrical nets of the design. Turn off all the drill drawing layers.
- This will generate a .tgz file that is imported to Sigrity.

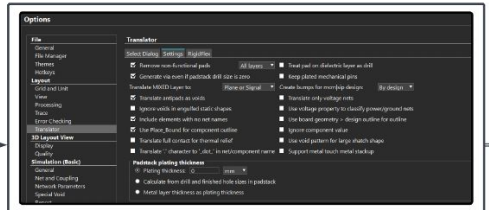
How to Integrate Altium with Sigrity



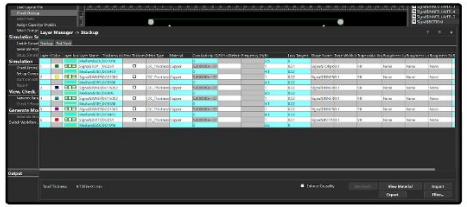
In Altium: Verify PCB design has updated stack up (this could affect results)



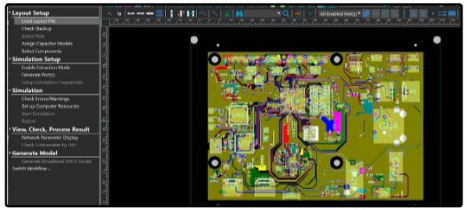
Update outjob files to include ODB++ generation and configure



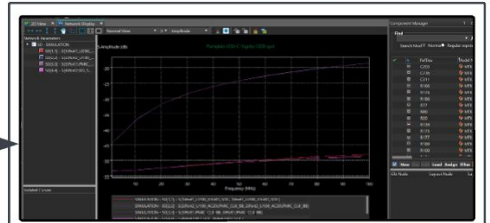
In Sigrity: Change the translator options to preferred settings



Verify the stack up in Sigrity matches the one in Altium

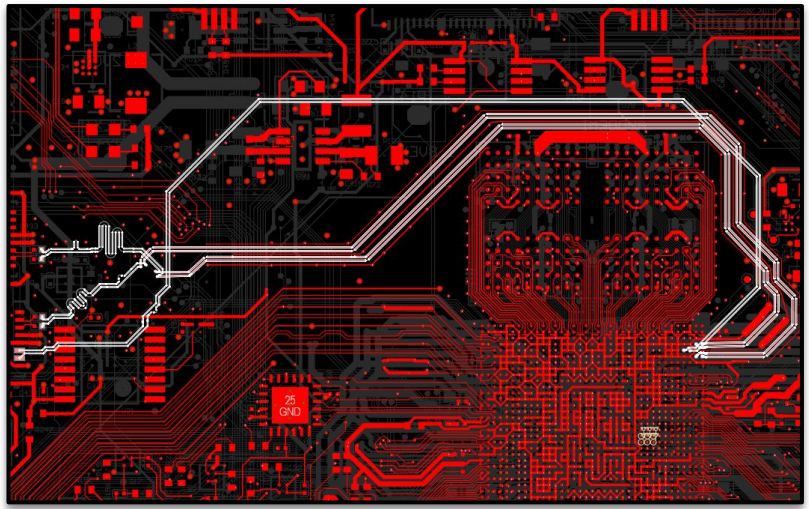


Select Model Extraction workflow:

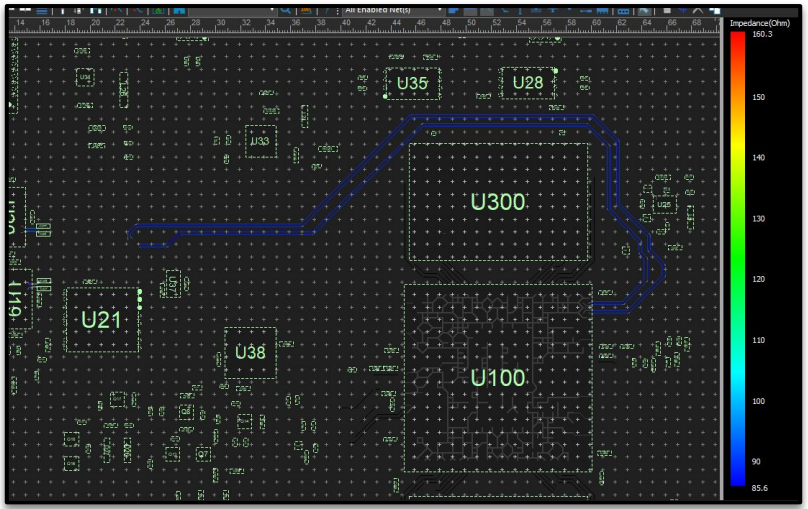


Enable the nets you want to analyze, create ports, and run simulation

PCIe

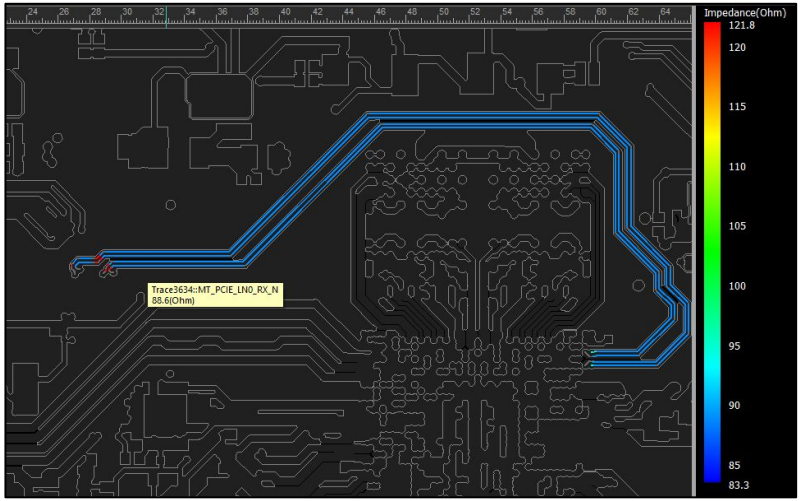


Altium Viewer of i700 PCIe from MediaTek CPU to PCIe Switch Mux.

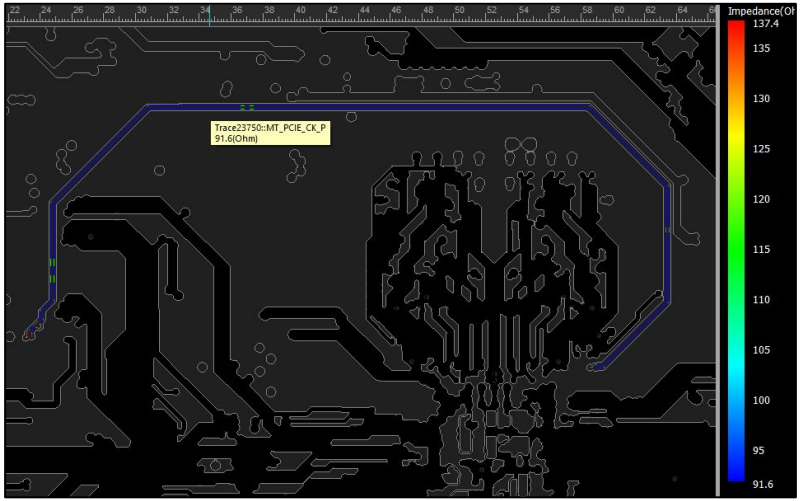


Sigrity PowerSI View of i700 PCIe Impedance Overlay Map.

PCIe (2)



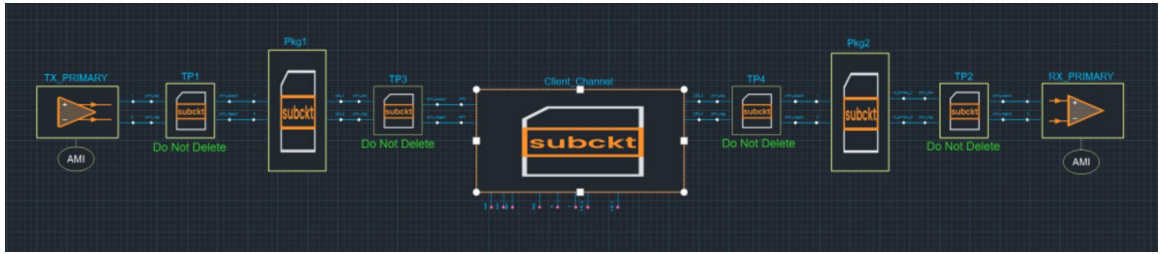
Differential Impedance Simulation ERC Workflow for Layer 1.
Diff Pairs Matched to 85 ohm.



Differential Impedance Simulation ERC Workflow for Layer 3.
Diff Pairs Matched to 85 ohm.

PCIe (3)

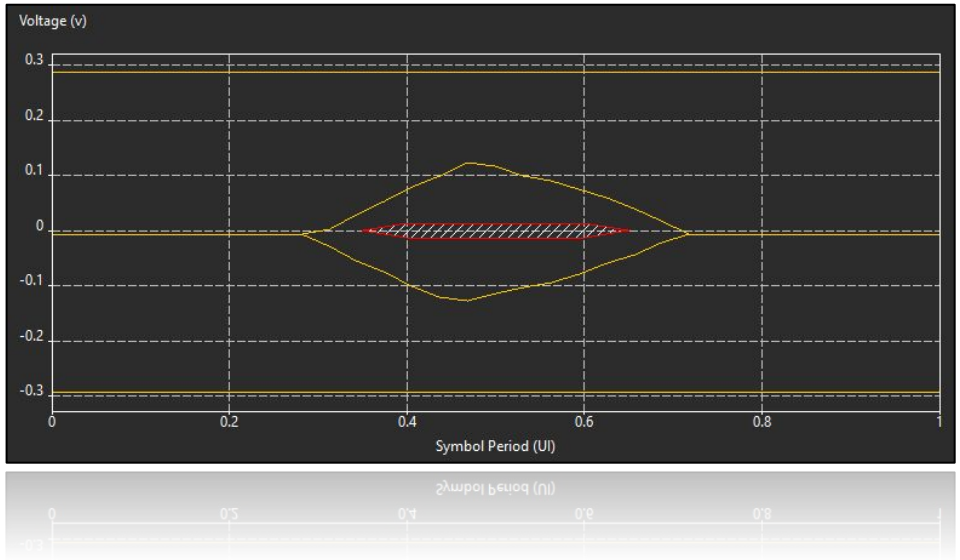
- This particulate i700 SoC had 1 PCIe channel available. In order to accommodate for the various peripherals using PCIe, we used a dedicated Mux Switch.
- To validate that the Mux and corresponding routing would not negatively affect the performance of the periphery devices, we utilized Sigrity simulation.



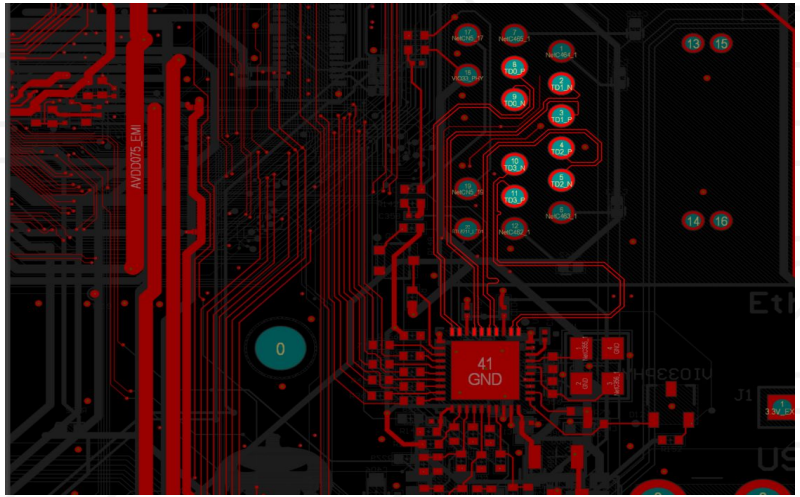
- Because there is a Mux in-line, I broke up the simulation of the PCIe traces into two sections. It is also possible to keep the component active in the simulation and adding in the a spice model for it, but I was not able to source the exact part's model.
- From there, I was able to bring the .subckt file output from PowerSI to the Topology Workbench.

PCIe (4)

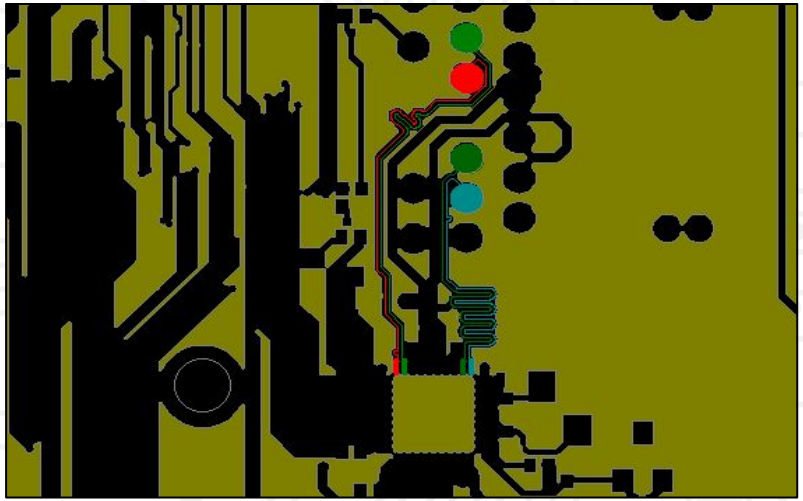
- Sigrity Topology Workbench View of PCIe Compliance Simulation Results.
- Simulation done for all 3 differential pairs, from MTK CPU to the Mux to the WiFi module and M.2 connector.
- Eye mask results show the voltage amplitude as well as the timing sequence of the routing is within specifications.
- Insertion loss check also indicates that the loss that is experienced is within the allowable tolerance.



Ethernet

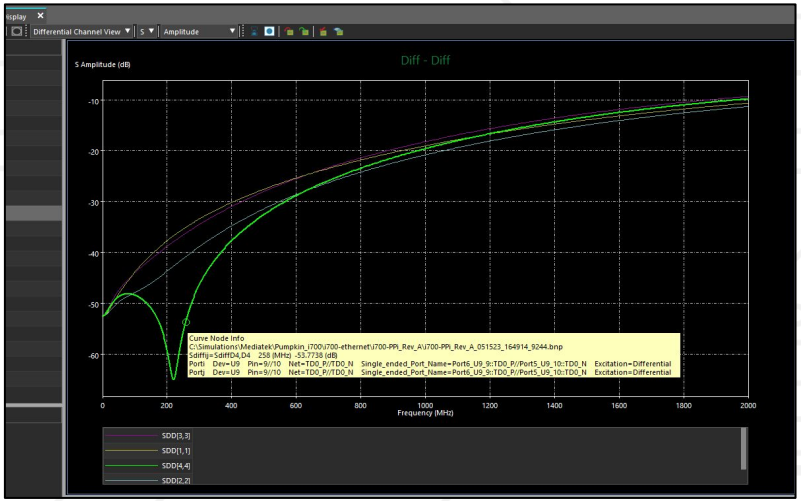


Altium Viewer of i700 Ethernet from Transceiver to RJ45 Connector

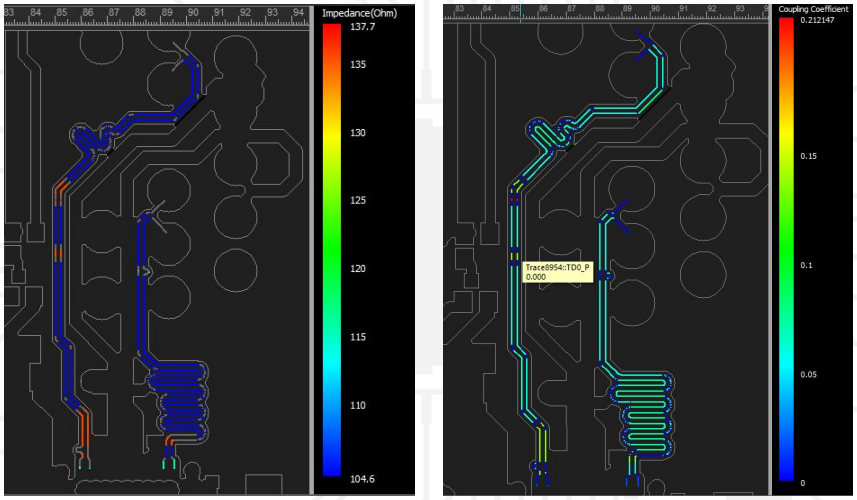


Sigrity PowerSI View of i700 Ethernet Impedance Overlay Map.

Ethernet (2)

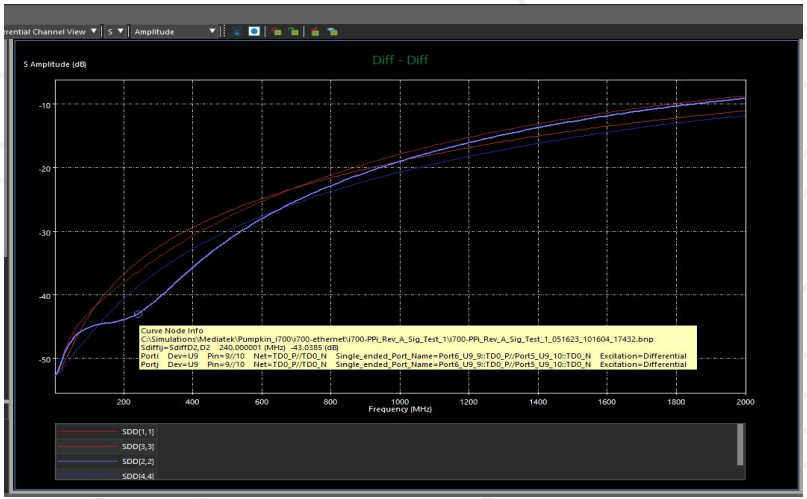


Sigrity Model Extraction Workflow Showing Area of Concern

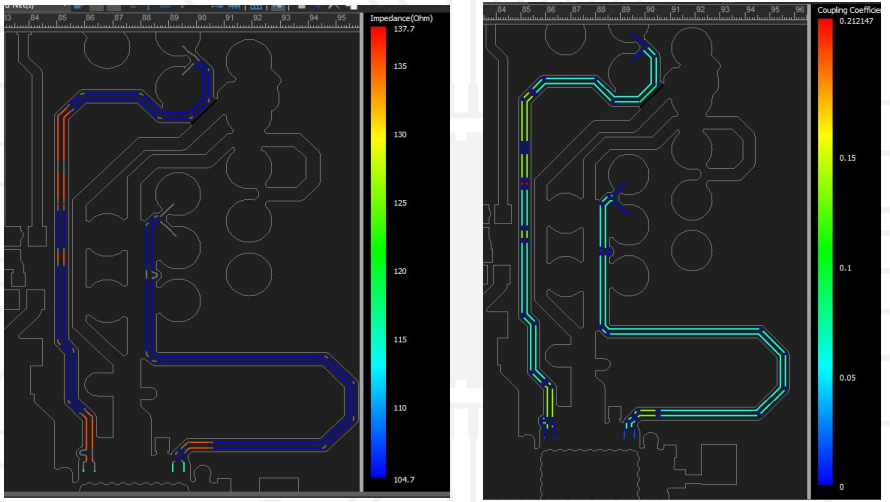


Sigrity PowerSI ERC Analysis Showing Breaks in Impedance Matching

Ethernet (3)

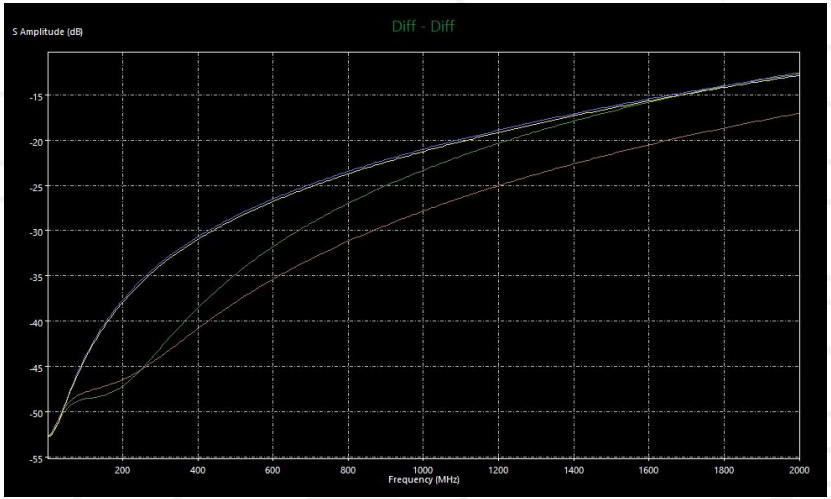


Sigrity Model Extraction Workflow Showing Area of Concern

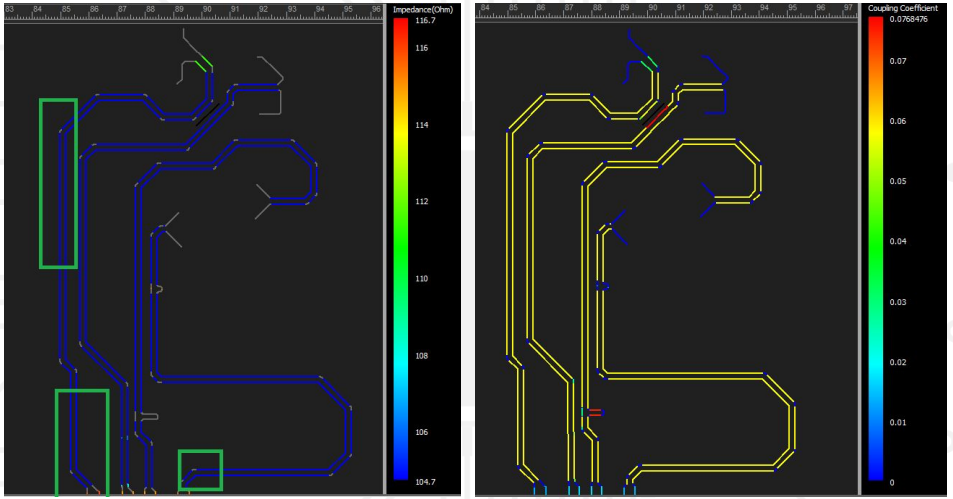


Sigrity PowerSI ERC Analysis Showing Breaks in Impedance Matching

Ethernet (4)



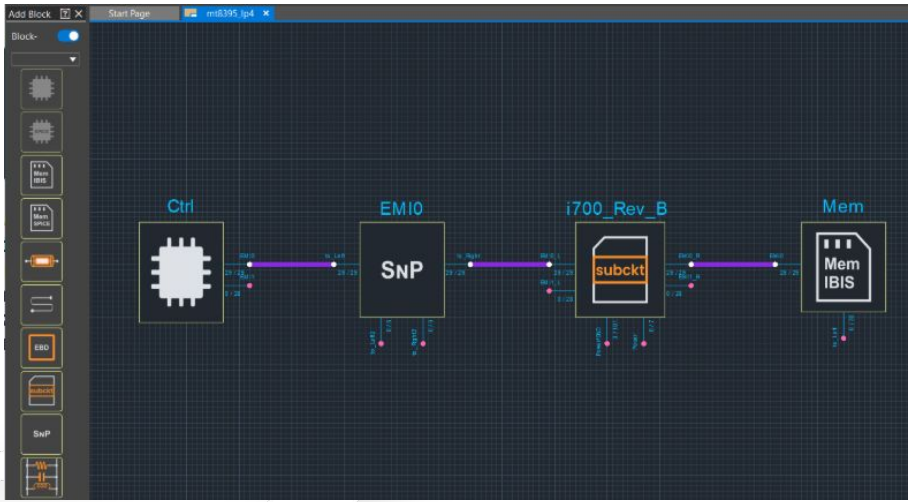
Sigrity Model Extraction Workflow Showing Area of Concern



Sigrity PowerSI ERC Analysis Showing Breaks in Impedance Matching

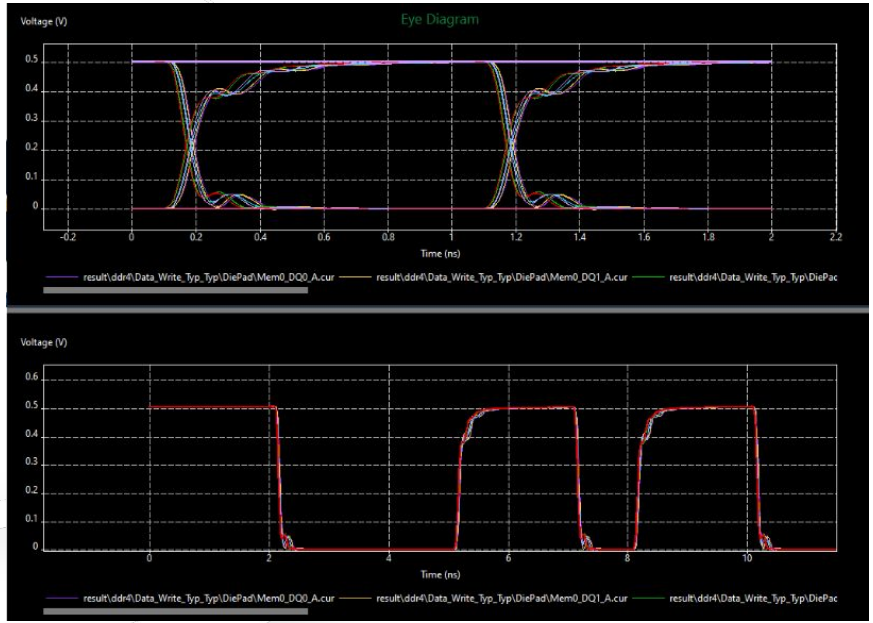
Example: DDR4 (Parallel Bus)

- Validation of the routing between the SoC (controller) and the DDR (memory) is imperative in designing a functional system.
- For my analysis, I used the Sigrity Topology Workbench parallel bus compliance.
- Different blocks in custom template included:
  - Controller - this includes the pin mapping and basic pin definitions
  - S-parameter - this IBIS model was provided by the MediaTek and contains the pin specific characteristics
  - .subckt - this block contains the PCB layout s-parameter model extraction of the DUC
  - Memory - this is the pin mapping and pin definitions of the controller



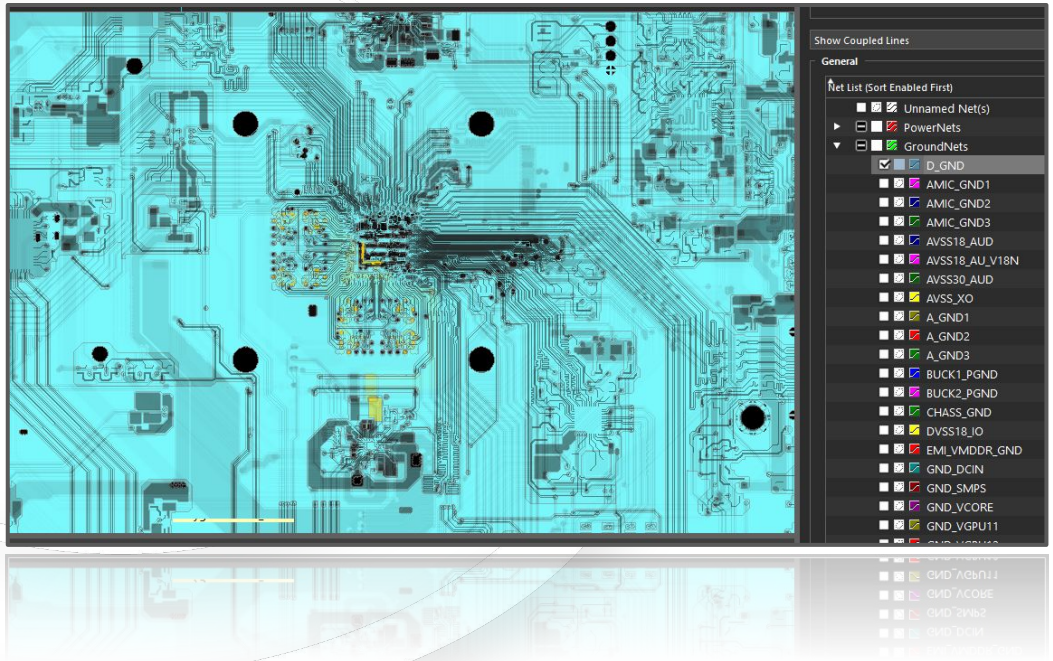
Example: DDR4 (Parallel Bus)

- Interpreting the Results:
  - Although there is some jitter on the RX eye diagram, the results were consistent with the MTK results
  - This jitter could be caused by the memory block itself. That block contained only generic pin descriptions, not the IC specific IBIS model, which limited the accuracy of the simulation results

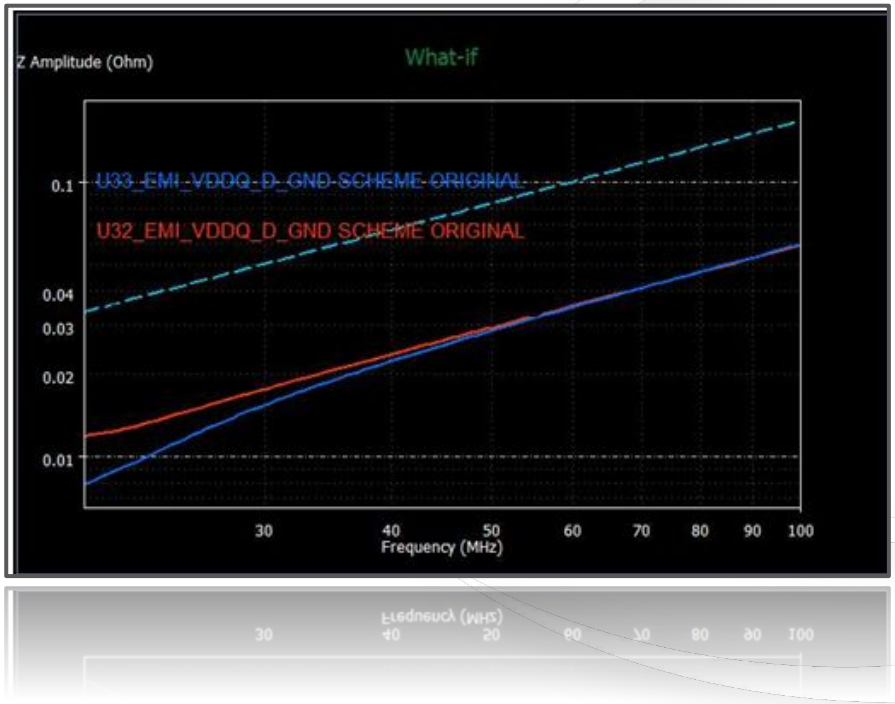


Power Delivery Network Impedance Analysis

- Sigrity's PDN Impedance Analysis workflow provides confidence in the design's ability to meet EMI compliance requirements.
- Impedance mismatches in PDN can often result in high resonances which can affect performance, signal integrity, etc.
- Failures in the PDN impedance found during this post-layout analysis.



Example: PDN Analysis



- For the i700 design, we were able to acquire the target PDN impedance profiles for all the power rails.
- Using the “What-If” analysis workflow, we were able to compare our board layout’s simulated results with the target profile and verify that it was within the expected results.
- Using the customizable capacitor library, we were also able to simulate for the exact capacitor packages used in the actual board design.
- This allowed us to simulate using varying capacitor values/sizes in order to get the desired results.

CONTACT US

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