# DESIGN GUIDE

# cādence°



# OrCAD X Constraint Management Guide

Part 2 of 5



# Contents

Part 2 - Standard Constraints
Physical and Spacing Constraints3
Trace Width: Minimum and Maximum Width for Signal And Power Traces3
Via Size: Diameter and pad size for vias, including microvias and blind/buried vias6
Differential Pairs (Basic Setup)8
Creating a Diff Pair11
Spacing Constraints
Creepage and Clearance: Minimum Distances Between Conductive Elements to Prevent Electrical Arcing12
Component Spacing: Minimum Distances Between Components to Avoid Interference and Facilitate Cooling15
Manufacturing Constraints23
Fabrication Tolerances: Allowable Variations in Dimensions for Manufacturing
Board Outline Dimensions: Tolerances for Overall Board Size and Shape23
Trace Width for Manufacturing: Minimum Copper Width for Traces23
Trace Spacing: Minimum Distance Between Copper Features24
Annular Ring: Minimum Width of Copper Surrounding a Hole26

	Drill to Copper Spacing	28
	Teardrops (Fillets)	31
	Pad To Mounting Hole Spacing: Minimum Distance Between Pads and Mounting Holes	31
	Acid Traps: Avoiding Acute Angles in Copper Feature That Can Trap Etching Chemicals	s 33
	Minimum Copper Area: Smallest Allowable Area of Isolated Copper Features	34
Ass Orie	embly Constraints: Rules for Component Placement, entation, and Soldering	35
	Outlines and Cut Outs	35
Whe	ere to Apply the Constraint Set	36
	Package to Package Spacing	36
	Component Spacing to PCB Features	36
	Pastemask	36
	Silkscreen and Solder Mask: Specifications for Text and Mask Application on The PCB	88
Des	ign for Test (DFT) Constraints	10
	Test Points: Placement and Minimum Distances From Other Test Points and Components	n 10
3D (	Constraints	41
Rigi	d Flex PCB Constraints	13
	Teardrops (Fillets)	13
	Component to Flex PCB	13
Con	clusion	15

# Part 2 - Standard Constraints

Welcome to the second part of this Constraint Management Guide. This section covers the common constraints you will need to set for most printed circuit boards (PCBs). Below is a general list of the format we will be following:

- Purpose: Briefly states the purpose of the constraint. Example: Ensures minimum spacing to prevent electrical interference.
- 2. **Visual Aid:** Relevant images or screenshots to illustrate the process. *Example: Diagram of Constraint Manager with highlighted options.*
- 3. **Steps:** Outlines the steps to implement the constraint in OrCAD X Presto PCB Editor. *Example: Open Constraint Manager > Select Category > Set Parameters > Apply.*
- 4. **Reason**: Explains why this constraint is important. *Example: Critical for maintaining signal integrity in high-speed designs.*
- 5. **Impact:** Describe the impact of implementing this constraint. *Example: Reduces risk of signal crosstalk, improving overall design reliability.*

For more details on constraints, please refer to online documentation and training.

# **Physical and Spacing Constraints**

Trace Width: Minimum and Maximum Width for Signal And Power Traces.



Top view of PCB traces with different widths

**Purpose**: Defines minimum and maximum trace widths for signal and power traces.

#### Steps:

1. Open Constraint Manager. Select Physical > Physical Constraint Set > All Layers > Create a Constraint Set if necessary.

Worksheet Selector 🗗	X P3449_B01_Alle	gro_layout_BGA-RE	GION				
🕴 Electrical			Objects		Line		
🔸 Physical 🚺			Nerra	Referenced Physical	Min	Max	Min W
▼ 📄 Physical Constraint Set	Туре	5	Name		mm	mm	mn
🔚 All Layers 😢	•			•		•	•
🖽 By Layer	Dsn		▼ P3449_B01_Allegro_layout_BGA-R	E DEFAULT	0.100:0.080:0.080	2.540	0.100:0.080
▼ 🛄 <u>N</u> et	PCS		AREATEST		0.100:0.080:0.080	2.540	0.100:0.080
All Layers	PCS		BGA-REGION-PCS		0.100:0.080:0.080	2.540	0.100:0.080
▼ Region	PCS		► CSI_NCLS		0.101:0.080:0.080	0.101:0.080:0.080	0.101:0.080
I All Layers	PCS		DAP_SIGNALS		0.112:0.084:0.084	0.112:0.084:0.084	0.112:0.084
	PCS		🔻 DEFAULT ( 3)		0 100.0 000.0 000	2.540	0.100:0.080
	LTyp		Conductor	Analyze		.540	0.100
	Līyp		► Plane	Cross Probe		.540	0.080
	Līyp		Conductor/EXTERNAL	Find	Ctrl+F	.540	0.100
	PCS		▼ DEFAULT_Z	Bookmark	,	.540	0.125:0.090
	LTyp		Conductor	Expand		.540	0.125
	LTyp		► Plane	Expand All		.540	0.090
	LTyp		Conductor/EXTERNAL	Collapse		.540	0.125
	PCS		DP_SIGNALS	Create		Physical CSet.	4 .080
	0.00	00000000000000				102.0 090.0 090	0 102-0 090

2. Name the constraint set of interest (e.g., USB\_SIGNALS)

Create PhysicalCSet								
PhysicalCSet:	USB_SIGN	ALS						
Copy Constraints from:								
	Ok	Cancel	Help					

3. The constraint set has been created (you will see it in the worksheet).

×1			
×	► POWER1	0.254:0.080:0.080	2.540
8	▼ USB_SIGNALS ◆	0.101:0.080:0.080	0.101:0.08
8	Conductor	0.101	0.101
8	► Plane	0.080	0.080
8	Conductor/EXTERNAL	0.101	0.101
×.	VIA IN PAD AREA	0.100:0.080:0.080	2.540

4. Next, apply the constraint set to the appropriate nets or net classes by going to the **Physical - Net - All Layers** worksheet (USB\_SIGNALS application shown below).

→ ← Physical				Referenced Physical	
Physical Constraint Set	Туре	S	Name	CSet	
All Layers	•	*	*	•	*
ि By Layer ▼ ■ Net	NCIs		GENERIC_DEZ2	GENERIC_DEZ2	0.102:
All Lavers 1	NCls		GENERIC_DEZ3	GENERIC_DEZ3	0.100:
▼ Region	NCls		GENERIC_SEZ1	GENERIC_SEZ1	0.137:
	NCls		GENERIC_SEZ2	GENERIC_SEZ2	0.137:
	NCls		► HDMI_SIGNALS(4)	HDMI_SIGNALS	0.102:
	NCls		PEXGEN3_SIGNALS(3)	PEXGEN3_SIGNALS	0.101:
	NCls		► POWER(6)	POWER1	0.254:
	NCIs 2		▼ USB_SIGNALS(5)	USB_SIGNALS 3	0.101:
	DPr		USB_PEX_RX6	USB_SIGNALS	0.101:
	DPr		► USB_PEX_TX6	USB_SIGNALS	0.101:
	DPr		► USB0_AP	USB_SIGNALS	0.101:
	DPr		► USB1_AP	USB_SIGNALS	0.101:
	DPr		► USB2_AP	USB_SIGNALS	0.101:
	NCls		400HM_NETCLASS1	400HM_NETCLASS1	0.170:
	NCIs		400HM NETCLASS2	400HM NETCLASS2	0.170:

- 5. Then click the dropdown and select the appropriate Physical CSet (USB\_SIGNALS) you created (shown above in step 3).
- 6. Finally, if you need to, you can set specific trace widths for any net without having to apply a constraint set by typing values directly into the cells. Those values will appear blue and bold, like in the image below.

	DLIAOLI	0.100.0.080.0.080	2.340
UART2_RXD_LS	DEFAULT	0.100:0.080:0.080	2.540
UART2_TXD_LS	DEFAULT	0.100:0.080:0.080	2.540
USB0_VBUS_DET*	DEFAULT	0.100	2.540
UUSB_DMODE	DEFAULT	0.100:0.080:0.080	2.540
UUSB_ILIM	DEFAULT	0.100:0.080:0.080	2.540
V N			

7. Set a value in the spreadsheet column named Line Width - Max value for USB0\_VBUS\_DET\*, which will override the constraint set you just applied to the class, group, or net and turn it blue (shown above).

**Tip:** You can repeat this general procedure for any number of nets: Set the constraints/rule set, then apply to the appropriate net, net class, or net group.

You may also directly type in/apply to specific nets or classes by typing them in, but that is not recommended as the first option. Manage what you can through constraint sets only.

Reason: Trace width ensures proper current-carrying capacity and signal integrity.

Impact: Balances manufacturability with electrical performance.

**Note**: Setting the trace width in the Physical section does not necessarily mean you meet the manufacturer's minimum trace width limits. Please be mindful that you can set any value in the Physical domain for trace (line) width. But if you do not follow the rules for your manufacturer, you can have a rude awakening that will force you to reroute the entire PCB again.

**Related Constraints**: Design for Manufacturing - Trace width.

Neck mode: Minimum trace width when routing into smaller spaces



**Purpose**: Allow traces to enter a smaller area (e.g., a BGA Constraint region, shown in Part 1 of this document) by becoming thinner momentarily and for a certain distance.

#### Steps to Create a Neck Mode Constraint:

1. Open Constraint Manager.

Worksheet Selector	×	P3449_B01_Allegro_layout_BGA-REGION							
🕴 Electrical			Ођ	cts		Neck			
🔸 Physica				Nama	Max	Min Width	Max Length		
🔻 📗 Physical Constraint Set		Туре	3	Name	mm	mm	mm		
🔚 All Layers 🔶		•		*		*	*		
🖩 By Layer		Dsn		▼ P3449_B01_Allegro_layout_BG		0.100:0.080:0.080:0.100	1270.000	0.0	
▼ Net		PCS		► AREATEST		0.100:0.080:0.080:0.100	1270.000	0.0	
All Layers		PCS		BGA-REGION-PCS		0.100:0.080:0.080:0.100	1270.000	0.0	
▼ Region		PCS		► CSI_NCLS	080:0.080	0.101:0.080:0.080:0.101	1270.000	0.1	
II Layers		PCS		DAP_SIGNALS	084:0.084	0.112:0.084:0.084:0.112	1270.000	0.0	

- 1. Navigate to the spreadsheet Physical > Physical Constraint Set > All Layers.
- You will see all the constraint sets that were created. You can create your own by right-clicking the cell containing the design name P3349\_B01\_Allegro\_layout\_BG (the name of your .BRD file/Design), then choosing Create -Physical CSet.

Create PhysicalCSet							
PhysicalCSet:	PCS1						
	Ok	Cancel	Help				
		Curicei	Theip				

3. In the pop-up window, give the PhysicalCSet an appropriate name.

Neck Max Length Neck Min Neck Min Width (Line Width)

4. After that, you can set whichever neck mode rules you want. The two main parameters are: **1. Neck - Min Width**, and

2. Neck - Max Length (see below).

Objects			Nec	k	1
	Nama		Min Width	Max Length	м
	Name		mm	mm	
			*	*	
	▼ P3449_B01_Allegro_layout_BG	$\otimes$	0.100:0.080:0.080:0.100	1270.000	0.000
***	► AREATEST		0.100:0.080:0.080:0.100	1270.000	0.000
***	BGA-REGION-PCS		0.100:0.080:0.080:0.100	1270.000	0.000
***	► CSI_NCLS	30	0.101:0.080:0.080:0.101	1270.000	0.118:0
	DAP_SIGNALS	34	0.112:0.084:0.084:0.112	1270.000	0.000
***	▼ DEFAULT		0.100:0.080:0.080:0.100	1270.000	).000
	Conductor				0.000
***	ТОР		0.100	1270.000	0.000
	воттом		0.100	1270.000	0.000
***	Plane		0.080	1270.000	0.000
333	Conductor/EXTERNAL		0.100	1270.000	0.000
***	▼ DEFAULT_Z		0.125:0.090:0.090:0.125	1270.000	0.000

Via Size: Diameter and pad size for vias, including microvias and blind/buried vias.

Purpose: Defines the diameter and pad size for various types of vias to ensure proper connectivity between layers.





#### Steps:

- 1. Open Constraint Manager.
- 2. Select the Physical worksheet tab and click on Net All.



3. Go to the Vias column, then click **once** on the cell for the row of rules you want to assign specific vias to. The **Edit Via List** new window will appear.



- 4. Set via types you want from the library (vias found on the left), then double-click to place them among the list of usable via the list on the right. These vias will be applied to the specific row net, class, group, or region to be selected when you open the window from the CM.
- 5. Once the list is satisfactory, you may organize the vias by highlighting the via name (on the list to the right) and using the **Up** and **Down** buttons in the window.
- 6. Use the above steps to apply specific via types (through-hole, blind, buried, or microvias) to any net classes, groups, and constraint regions.

**Note:** While you can modify padstacks within OrCAD X PCB Editor, you cannot directly create them. You will need to use the Padstack Editor tool to create them, and then you can use the Constraint Manager to add padstacks to your design.

**Reason for Padstacks**: Proper padstack selection ensures reliable layer-to-layer connections while optimizing board space and manufacturability.

Impact: Balances electrical performance with manufacturing constraints and cost considerations.

Related to: Aspect Ratio, Annular Ring

#### Differential Pairs (Basic Setup)

**Purpose**: Defines the minimum and maximum widths and spacing for differential pair traces to maintain signal integrity. We will focus on the physical constraints in this example. In the high-speed section(s), we will encounter differential pairs again and address the high-speed constraints.



Top view of a differential pair showing some width and spacing parameters

**Reason for Physical Constraints**: Setting up physical constraints and forcing symmetry in differential pairs ensures consistent impedance and reduces the chances of signal issues in high-speed signal transmission. In OrCAD X Presto PCB Editor, you want to use physical rules to control your differential pairs as much as possible.

#### Steps:

- 1. Open Constraint Manager.
- 2. Navigate to the Physical Constraint Set tab.
- 3. Select "All Layers" from the dropdown.
- 4. Similar to the previous creation of constraint classes, you can right-click the main Dsn name at the top of the list, make a Physical Cset, then navigate to the CSet. In our example, we have one named USB\_SIGNALS expanded (shown below).

🔸 Physical					Min Width	Max Length	Min Line Spacing
🔻 📗 Physical Constraint Set	Type	Type S Name		mm	mm	mm	
🔚 All Layers	*	*	*		*	*	*
🖩 By Layer	Dsn		▼ P3449_B01			4070.000	0.000
▼ Net	PCS	¥XX	► AREATE	Cross Dro			0.000
All Layers	PCS		► BGA-RE	Cross Pro	эде	C+rl + E	0.000
Region	PCS	****	► CSI_NC	e Fina Poolemae	de .	Cuitr	0.118:0.000:0.000:0.118
I All Layers	PCS		► DAP_SI	Evened A	K		0.000
	PCS		► DEFAUL	Croate	<b>MI</b>		Dhusical CSat
	PCS		► DEFAUL	Denemo		52	
	PCS	1000	▼ DP_SIG	Delete		F2 Del	0.100:0.000:0.000:0.100
	LТур		▼ Cor	Compare	<b>a</b>	Dei	0.100
	Lyr	1	-	Constrair	nt Set References		0.100
	Lyr	4			nstraints from		0.100
		<u>4000</u>	N	cob) co			



Worksheet Selector 🗗 🛪	P3449	_B01_/	Allegro_layout_BGA-REGION								
🕴 Electrical			Objects	Neck		Differential Pair					
🔶 Physical				Min Width	Max Length	Min Line Spacing	Primary Gap	Neck Gap	(+)Tolerance	(-)Tolerance	Vias
🔻 🚞 Physical Constraint Set	Тур	, 5	Name	mm	mm	mm	mm	mm	mm	mm	
🔚 All Layers 🛛 🛻 🔤	•										
🖩 By Layer	rea		TOMI SIGNALS	0.102.0.000.0.00	1270.000	0.111.0.000.0.000.0.111	0.119.0.000.0.000.	0.119.0.000.0.000	0.002	0.002	vin_043C020F1vin_040C02
🔻 🛅 Net	Цур		▼ Conductor	0.102	1270.000	0.177	0.179	0.179	0.002	0.002	
All Layers	Lyr	1	ТОР	0.102	1270.000	0.177	0.179	0.179	0.002	0.002	
▼ 📄 Region	Lyr		BOTTOM	0.102	1270.000	0.177	0.179	0.179	0.002	0.002	
All Layers	Llyp		Plane	0.080	1270.000	0.000	0.000	0.000	0.002	0.002	
	LTyp		Conductor/E		1270.000				0.002	0.002	
	PCS		PEXGEN3_SIGNALS ).	0.101:0.080:0.08	1270.000	0.118.0.000.0.000.0.118	0.120.0.000.0.000	0.120:0.000:0.000	0.002	0.002	VTH_045C020P:VTH_048C02
	PCS		► POWER1	0.100:0.080:0.08	1270.000	0.000	0.125	0.000	0.000	0.000	VTH_045C020P:VTH_048C02
	PCS		USB_SIGNALS	0.101:0.080:0.08	1270.000	0.118:0.000:0.000:0.118	0.120.0.000.0.000	0.120:0.000:0.000	0.002	0.002	VTH_045C020P:VTH_048C02
	LTyp		Conductor	0.101	1270.000	0.118	0.120	0.120	0.002	0.002	
	Lyr	1	ТОР	0.101	1270.000	0.118	0.120	0.120	0.002	0.002	
	Lyr		BOTTOM	0.101	1270.000	0.118	0.120	0.120	0.002	0.002	
	LTyp		▼ Plane	0.080	1270.000	0.000	0.000	0.000	0.002	0.002	
	Lyr	2	L2	0.080	1270.000	0.000	0.000	0.000	0.002	0.002	
	lyr	3	LI LI	0.080	1270.000	0.000	0.000	0.000	0.002	0.002	
2	LTyp		Conductor/E		1270.000				0.002	0.002	
	PCS		► VIA_IN_PAD_AREA	0.100:0.080:0.08	1270.000	0.000	0.125	0.000	0.000	0.000	VTH_045C020P;VTH_048C02
	PCS		► VIA_IN_PAD_ARE	0.125:0.090:0.09	1270.000	0.000	0.125	0.000	0.000	0.000	VTH_048C023P:VTH_050C02
	PCS		► 400HM_NETCLA )	0.170:0.080:0.08	1270.000	0.000	0.125	0.000	0.000	0.000	VTH 045C020P:VTH 048C02
	PCS		► 400HM_NETCLA )	0.170:0.080:0.08	1270.000	0.000		0.000	0.000	0.000	VTH_045C020P:VTH_048C02
	PCS		► 400HM_NETCLA ).	0.170:0.080:0.08	1270.000	0.000	0.125	0.000	0.000	0.000	VTH_045C020P:VTH_048C02
	pre		ASOUND NETCLA	0.1270.000.0.00	1270.000	0.000	0.125	0.000	0.000	0.000	

5. Set values for Min Width, Max Width, Min Space, and Max Space (shown above).



Top View of Differential Pair

Differential pairs have many parameters to consider.

- Line Width (Min, Max) The trace width for a single diff pair trace not in Neck Mode. Min is the thinnest the trace is allowed to be, and Max is the thickest the trace is allowed to be.
- Neck When in Neck Mode (narrower traces)
  - Min Width the thinnest that a single-ended trace of the diff pair can be
  - Max Length the longest distance allowed for diff pairs to be in neck mode before going into regular diff pair mode
- > Uncoupled Length When diff pairs are not close enough to each other to be electrically coupled, i.e., separated
  - Gather control During the time diff pairs are uncoupled to connect to or from pads, you can ignore or include the distance where diff pairs momentarily separated
  - Max the maximum distance you will allow diff pair traces to be uncoupled for
- Static Phase Tolerance a high-speed timing-related constraint that determines the allowed skew in timing between the two differential signals arriving at the receiver simultaneously.
- Dynamic Phase high-speed timing and EMC-related constraint that determines the amount of common mode voltage and signal attenuation allowed at any distance along the trace path before reaching the receiver pins
  - Max Length maximum time of flight to allow signals to propagate out of phase
  - Tolerance some +/- margin for signals to be out of sync

#### Differential Pair

- Referenced Intra-DP Spacing CSet diff pair trace to diff pair trace spacing
- Min Line Spacing the thinnest diff pair trace can be
- Primary Gap the edge-to-edge distance between the + and diff pair traces during regular routing
- Neck Gap the edge-to-edge distance between the + and diff pair traces during Neck Mode routing
- (+)Tolerance added trace width on any trace, whether in neck mode or not
- (-)Tolerance the subtracted/minimal gap spacing width, whether in Neck mode or not. Note that the narrowest gap (during neck mode) minus the Tolerance must be equal to or greater than the Min Line Spacing rule/constraint, else you get an error
- **Vias** vias that are allowed on the differential pair traces
- BB Via Stagger the allowed parameters for blind and buried vias for the diff pair traces
  - Min the closest distance between two blind/buried vias
  - Max the furthest distance between two blind/buried vias
- Pad-Pad Connect Basically for allowing via in pad connections typical for tight spacing conditions and via in pad technology
- Etch
- > Ts T-points this allows you to make a T-junction between another trace and one of the traces of your diff pair

#### Creating a Diff Pair

Before continuing with this example, let's create a differential pair.

- 1. To create a differential pair:
  - a. Go to the Physical > Net > All Layers worksheet
  - b. Select the two nets you want to pair
  - c. Right-click and choose Create > Differential Pair
  - d. The Create Differential Pair window will appear
  - e. Name the pair and click Create
  - f. You can also remove a differential pair you might have made by mistake by clicking the Clear button
  - g. Once you have created all your differential pairs, click Close

Create Differential Pair							×
Xnet		•		<u></u>			Create
All Xnets	Diff Pair		Diff Pair Name: DPI Selections:			[	Modify
CAM_MUX_SEL			Name	• Туре	Diff Pair		Delete
CAM0_12C_SDA		-   <u> </u> [	CAN_TX	Net			Clear
CAM0_MCLK CAM0_PWDN			CAN_RX	Net			
CAM1_I2C_SCL							
CAM1_IZC_SUX							
CAM1_PWDN							
CAN_TX							
CSI0_CLK_N CSI0_CLK_P	CSI A C						
CSI0_D0_N	CSLA_D	Shift	+ Sele	ect			
CSI0_D0_P CSI0_D1_N	CSI_A_D CSI_A_D						
CCID D1 D							

2. At this point, you can create a net class or group within the Physical > Net > All Layers worksheet (follow the instructions in Part 1 on how to create Net classes and groups).

3. After creating your net classes and groups, apply the differential pair Physical Constraint Set you made earlier to a Net Class, Net Group, or Differential Pair (NCls, NGrp, DPr), as shown below.

Worksheet Selector	ъ×	P3449_B01_Alle	gro_layout_BGA-REGI	ON		
🗲 Electrical			o			
🔸 Physical					Referenced Physical	Min
🔻 📄 Physical Constraint Set		Туре	5	Name	Coct	mm
🖩 All Layers		*	*	•	*	*
🖩 By Layer		Dsn		▼ P3449_B01_Allegro_layout_BGA-RE	DEFAULT	0.100:0.080:
▼ 🖢 Net		NCls		► CSI_NCLS(6)	CSI_NCLS	0.101:0.080:
🖩 All Layers 🥌		NCls		PEXGEN3_SIGNALS(3)	PEXGEN3_SIGNALS	0.101:0.080:
Region		NCls		▼ USB_SIGNALS(5)	USB_SIGNALS	0.101:0.080:
I All Layers		DPr		▼ USB_PEX_RX6	USB_SIGNALS	0.101:0.080:
		XNet		USBSS_RX6_N	USB_SIGNALS	0.101:0.080:
		XNet		USBSS_RX6_P	USB_SIGNALS	0.101:0.080:

4. The Net Class, USB\_SIGNALS(5), adopts the Physical Constraint Set (which we also named USB\_SIGNALS) and the application is done.

**Note:** While it may be implicitly understood, know that constraint sets are **different** from the objects, groups, classes, and regions they are applied to. They may be named the same as the net groups they're applied to, but that is simply for convenience. There is no relation between the names of your constraints and what they are applied to.

**Important Tip**: Please be careful with the worksheet being selected. All constraint sets are made in the Constraint set category (e.g., Physical Constraint Set - All Layers in this case)

**Impact**: Differential pair use and constraints are popular for carrying important signals that need some protection against noise. Managing the constraints for your differential pairs improves signal integrity and enhances overall performance. Differential pair signaling is popular in high-speed designs.

Related Constraints: Differential Pair Static Phase Tolerance, Differential Pair Dynamic Phase

# **Spacing Constraints**

#### Creepage and Clearance: Minimum Distances Between Conductive Elements to Prevent Electrical Arcing

**Purpose**: Defines minimum distances between conductive elements to prevent electrical arcing and ensure insulation integrity.



Clearance between two traces on a PCB across an air gap





Creepage between traces on a PCB surface

Cadence OrCAD X Presto PCB Editor does not support creepage and clearance rules, but Allegro X does. However, you can at least set a spacing rule to control your creepage if you don't have coatings on the PCB. Notice how it addresses spacing in this image below.



We cannot distinguish between clearance or creepage with this constraint, because coatings are not taken into account.

Therefore, this distance could be the distance midway between the creepage distance and the clearance distance, thus giving an average clearance, which could in effect violate the creepage, clearance or both.

Hence, if you do use this as a substitute for creepage or clearance, consider using creepage and only when a coating is not present.

If a coating is present and you still use this constraint in OrCAD X, at least increase the distance more than usual with an acceptable tolerance to address both your creepage and clearance needs. However, using Allegro X is recommended at this stage.

Nonetheless, we need some kind of spacing rule for traces, so, to manage the spacing between traces on the PCB do the following:

#### Steps

1. In Constraint Manager, create a Spacing Constraint set.

t s	pacing							mm
-	Spacing Constraint Set	*				*		*
	All Layers 🔶	Dsn	_	P3449_B01_All	egro layout BGA-RE	DEFAULT		
	🖩 By Layer	SCS		► CSI_NCI	Analyze			***
▼ 🗎	Net	SCS		► DAP_SI	Cross Probe			***
	🔲 🖩 All Layers	SCS		🕨 🕨 DEFAUL	Find	Ctrl+F		***
▼ 🛯	Net Class-Class	SCS		► DEFAUL	Bookmark	•		***
	🖩 All Layers	SCS		► DP_SIG	Expand All			
	🔚 CSet assignment matrix	SCS		► ETH_SIC	Create		Spaci	ng CSet
▼ 🗋	Region	SCS		► GENERI	Rename	F2	7	***
	🖩 All Layers	SCS		► GENERI	Delete	Del		***
▼ 🛯	Inter Layer	SCS		► GENERI	Compare			***
	🖩 Spacing	SCS		► GENERI	Constraint Set Refere	nces		***
		SCS		► GENERI	Copy Constraints from	n		***
		SCS			Change all design un	it attributes		***



2. For that Spacing CSet (SCS), apply a value in the Line to Line column (you need to double-click and expand the Line To column at the top) for the spacing you want between the traces.

P3449_B01_Alleg	ro_layou	t_BGA-REGION							
		Objects					Line To		
Tuna		Daubla aliala				All	Line	Thru Pin	
Type I		Double click	to exp	and this column		mm	mm	mm	
*	*	*		*	*		*	*	*
Dsn		▼ P3449_B01_Allegro_layout_B	GA-RE	DEFAULT	***		0.100	0.125:0.100:0.100	0.125
SCS		► CSI_NCLS			***		0.270:0.100:0.100	0.125:0.100:0.100	0.125
SCS		DAP_SIGNALS			***		0.270:0.100:0.100	0.125:0.100:0.100	0.125
SCS		▼ DEFAULT			***		0.100	0.125:0.100:0.100	0.125
LTyp		Conductor			***		0.100	0.125	0.125
Lyr	1	тор	Male	a far Line to Line Once			0.100	0.125	0.125
Lyr	4	воттом	Valu	le for Line to Line Spac	ing		0.100	0.125	0.125
LTyp		► Plane					0.100	0.100	0.10
LТур		Conductor/EXTERNA	AL		***		0.100	0.125	0.12
SCS		► DEFAULT_Z			***		0.125	0.150:0.125:0.125	0.150
SCS	10000	DP_SIGNALS			***		0.330.0.100.0.100	0.125:0.100:0.100	0.125

3. Apply this new Spacing CSet to your desired net, net class, group or region by selecting the appropriate worksheet in the CM, e.g. Spacing > Spacing Constraint Set > Net > All Layers.

4. Let's say you want to apply it to the Net Class named POWER(6) - Click the dropdown in the Referenced Spacing CSet column, then select your preferred spacing constraint set. In this case, we go with DEFAULT (see below).

Worksheet Selector & 🛪 🗙	P3449_B01_Alleg	ro_layout_BGA-REGI	ON					
🕴 Electrical		a	bjects			Line To		
🖡 Physical				Referenced Spacing	All	Line	Thru Pin	SMD Pin
1 Spacing	Туре	s	Name	Cart	mm	mm	mm	mm
▼ Spacing Constraint Set				*				•
All Layers	Dsn		▼ P3449_B01_Allegro_layout_BGA-RE	DEFAULT	***	0.100	0.125:0.100:0.100	0.125:0.100:0.10
🛱 By Layer	NCIs		► CSI_NCLS(6)	CSI_NCLS	•••	0.270.0.100.0.100	0.125:0.100:0.100	0.125:0.100:0.10
🔻 📗 Net	NCIs		DAP_SIGNALS(18)	DAP_SIGN			0:0.100	0.125:0.100:0.10
🛱 All Layers 🗕	NCIs		DP_SIGNALS(4)	DP_SIGNA			0:0.100	0.125:0.100:0.10
▼ 📗 Net Class-Class	NCIs		► ETH_SIGNALS(4)	ETH SIGN			0:0.100	0.125:0.100:0.10
🖩 All Layers	NEIs		GENERIC_DEZ1	GENERIC	100SE	e a Nei	0:0.100	0.125:0.100:0.10
CSet assignment matrix	NCIs		GENERIC_DEZ2	GENERIC			0:0.100	0.125:0.100:0.10
▼ Egion	NCIs		GENERIC_DEZ3	GENERIC NO	t grou	ip or N	et 0:0.100	0.125:0.100:0.10
All Layers	NCIs		GENERIC_SEZ1	GENERIC	41-	·	0:0.100	0.125:0.100:0.10
▼ Inter Layer	NCIs		GENERIC_SEZ2		SS, IN	en ap	OIV 0:0.100	0.125:0.100:0.10
I Spacing	NCIs		▼ HDMI_SIGNALS(4)	HDMI_SIG	0		0:0.100	0.125:0.100:0.10
	DPr		HDMI_TXD0	HDMI_SIGT	Spac	ing Ut	Del 0:0.100	0.125:0.100:0.10
	DPr		► HDMI_TXD1	HDMI_SIC			0:0.100	0.125:0.100:0.10
_	DPr		HDMI_TXD2_CON	HPMI_SIG			0:0.100	0.125:0.100:0.10
5	DPr		► HDMI_TXD3	HDMI_SIGNALS		0.338:0.100:0.100	0.125:0.100:0.100	0.125:0.100:0.10
<u> </u>	NCIs		PEXGEN3_SIGNALS(3)	PEXGEN3_SIG VALS	•••	0.270.0.100:0.100	0.125:0.100:0.100	0.125:0.100:0.10
	NCIs		POWER(6)	DEFAULT				0.125:0.100:0.10
	Net		VDD_3V3_EDP	DEFAULT	•••	0.100	0.125:0.100:0.100	0.125:0.100:0.10
	Net		VDD_3V3_HDMI	DEFAULT		0.100	0.125:0.100:0.100	0.125:0.100:0.10
	Net		VDD_3V3_SYS	DEFAULT		0.100	0.125:0.100:0.100	0.125:0.100:0.10
	Net		VDD_5V_IN	DEFAULT		0.100	0.125:0.100:0.100	0.125:0.100:0.10
	Net		VDD_5V_USB	DEFAULT	•••	0.100	0.125:0.100:0.100	0.125:0.100:0.10
	Net		VDD_5V0_HDMI_CON	DEFAULT	•••	0.100	0.125:0.100:0.100	0.125:0.100:0.10
	NCIs		▼ USB_SIGNALS(5)	USB_SIGNALS	***	0.270:0.100:0.100	0.125:0.100:0.100	0.125:0.100:0.10
	DPr		V USB PEX RX6	USB SIGNALS	***	0 270 0 100 0 100	0 125 0 100 0 100	0 125 0 100 0 10

**Reason**: Clearance and creepage are crucial for electrical safety, especially in high-voltage designs and harsh environments. Creepage travels along the surface of the PCB while clearance involves the space between in the air above the PCB.

**WARNING**: As stated above, specific clearances and creepages are **not** addressed in OrCAD X. However, some kind of spacing needs to be established.

Impact: Enhances product safety, reliability, and compliance with safety standards.

#### Component Spacing: Minimum Distances Between Components to Avoid Interference and Facilitate Cooling

Purpose: Ensures adequate spacing between components for assembly processes and thermal dissipation.



#### Package to package spacing

This constraint defines the minimum allowable distance between two packages with various orientations. The format of the constraint value is like "SS:EE:SE:ES", where SS stands for Side to Side, EE stands for Edge to Edge, SE stands for Side to Edge and ES stands for Edge to Side. Example constraint value may look like 10:12:20:21. Each of the distance values are captured in design unit. DRC will be reported if any two packages placed in a given orientation violates the constraint value. The constraint can be different for different type of packages, and hence a triangular matrix is used to represent constraints among different packages.

**Image**: Diagram showing minimum spacing requirements between different component types on a PCB. Please follow IPC 2221 for spacing requirements, i.e. Edge-to-Edge (EE), Side to Edge (SE), Edge to Side (ES) and Side to Side (SS).

**Reason**: Proper component spacing is crucial for manufacturing processes and thermal management of the PCB, especially during automatic soldering processes, manual soldering, and PCB Assembly. We will address both the 2D and 3D aspects of component spacing.

#### Steps:

- 1. Open Constraint Manager.
- 2. Navigate to the Design for Assembly category.
- 3. Select the PkgToPkg Spacing section.
- 4. Set minimum distances between different component types (see below).

of P3449_B01_Allegro_layout_BGA-REGION - P0	CB Constraints - [Manufac	cturing / Design fo	r Assembly / DFA (	onstraint Set]							- 0	×
File Edit Objects Column View	Analyze Audit	Tools Window	Help									- 8
					👝 .   💷 «	L A. C. II.	. <mark></mark> 🗐					
		0 i . 🕲 . 🔘		<b>e .</b> @   <u>&gt;</u> .	<b>~ •</b>		2 👬 🛄					
Worksheet Selector 🛃 🗙	DFAPKGCS_BOTTOM	DFAPKGCS_TOP										
Electrical			_									
++ Physical	Name		DFAPKGCS_TOP									
1 Specing	Constraint set usag	ge	Spacing									
1 Same Nat Spacing	Package to packag	je spacing	01005									
Same rvet spacing												
Manufacturing		,										
Design for Fabrication	DFA Spread Sheet	ormat: (Side to Sid	le):(End to End):(Sid	le to End):(End to S	ide)							
UHine	Default: 25:25:25:2	25										
III Mask	DFA Table											
Annular Ring												m
Copper Features	Package Name 🔺	01005	0603	0402	0201	Хзор	Thru_Hole_Sm_Hd	r Thru_Hole	Sot	Smtmisc2	Smtmisc	
E Copper Spacing	24	1.0:1.0:1.0:1.0	0.4:0.4:0.4:0.4	0.4:0.4:0.4:0.4	0.35:0.35:0.35:0.35	0.6.0.6.0.6			0.35:0.35:0.35:0.35	0.60.60.60.6	0.60.60.60.5	
III Silkscreen	66-05	1.0:1.0:1.0:1.0	0.4:0.4:0.4:0.4	0.4:0.4:0.4:0.4	0.35:0.35:0.35:0.35	0.6:0.6:0.6:0.6	0.7:0.7:0.7:0.7	0.7:0.7:0.7:0.7	0.35:0.35:0.35:0.35	0.6:0.6:0.6:0.6	0.6.0.6:0.6:0.5	
▼ 🛅 Design	Bas (850	1.0:1.0:1.0:1.0	0.4:0.4:0.4:0.4	0.4.0.4.0.4.0.4	035035035035	06060606	0.7:07:0.7:0.7	0.7.0.7.0.7.0.7	0.35:0.35:0.35:0.35	0.60.60.60.6	0.60.60.60.5	
0utline	500300CCC	0.25:0.25:0.25:0.25	0.25:0.25:0.25:0.25	0.25:0.25:0.25:0.25	025025025025	035035035035	0.37:0.37:0.37:0.37	0.4:0.4:0.4:0.4	0.35:0.35:0.35:0.35	0.4:0.4:0.4:0.4	0.35:0.35:0.35:0.35	
III Mask		1.0:1.0:1.0:1.0	0.35:0.35:0.35:0.35	0.35:0.35:0.35:0.35	0.35:0.35:0.35:0.35	05:05:05:05	0.5:05:05:05	0.5:0.5:0.5:0.5	0.35:0.35:0.35:0.35	0.4:0.4:0.4:0.4	0.40.40.40.4	
🖽 Annular Ring	20000	1.0:1.0:1.0:1.0	0.37.0.37.0.37.0.37	0.33.0.33.0.33.0.33	0.3.0.3.0.3.0.3	0.4.0.4.0.4.0.4	0.35.0.35.0.35.0.35	0.35:0.35:0.35:0.35	0.35.0.35.0.35.0.35	0.4.0.4:0.4.0.4	0.4.0.4.0.4.0.4	
Copper Features	GENERADE	0.25:0.25:0.25:0.25	0.25:0.25:0.25:0.25	0.25:0.25:0.25:0.25	025025025025	0.3:0.3:0.3:0.3	0.3:0.3:0.3:0.3	0.3:0.3:0.3:0.3	0.25:0.25:0.25:0.25	0.3:0.3:0.3:0.3	0.3.0.3:0.3:0.3	
Copper Spacing	80900000	02020202	0.2:0:2:0:2:0:2	0.20.20.20.2	02:02:02:02	02:02:02:02	02:02:02:02	02020202	0.2.0.2.02:02	0.20.2:0.2:02	0.20.20.202	
E Declar for Assembly	No.sep	0.3:0.3:0.3:0.3	0.3:0.3:0.3:0.3	0.3:0.3:0.3:0.3	03:03:03:03	0.4:0.4:0.4:0.4	0.35:0.35:0.35:0.35	0.4:0.4:0.4:0.4	0.3:0.3:0.3:0.3	0.4:0.4:0.4:0.4	0.3:0.3:0.3:0.3	
Design for Assembly	000000	0.3:0.3:0.3:0.3	0.3:0.3:0.3:0.3	0.3:0.3:0.3:0.3	03:03:03:03:03	04:04:04:04	0.35:0.35:0.35:0.35	0.4:0.4:0.4:0.4	0.3:0.3:0.3:0.3	0.4:0.4:0.4:0.4	0.30.30.30.3	
Outline /	200000000000000000000000000000000000000	02020202	0.1:0.1:0.1:0.1	0.2:0.2:0.2:0.2	02:02:02:02	0.1:0.1:0.1:0.1	0.05:0.05:0.05:0.05	0.05:0.05:0.05:0.05	0.1:0.1:0.1:0.1	0.1:0.1:0.1:0.1	0.1.0.1:0.1:0.1	
		1.0:1.0:1.0:1.0	0.35:0.35:0.35:0.35	0.35:0.35:0.35:0.35	0.35:0.35:0.35:0.35	0.5:0.5:0.5:0.5	0.5:05:05:05	0.5:0.5:0.5:0.5	0.35:0.35:0.35:0.35	0.4:0.4:0.4:0.4	0.40.40.40.4	
III Specing	CONTRACTO	0.4.0.40.4.0.4	0.4:0.4:0.4:0.4	0.4.0.4.0.4.0.4	04:0.4:0.4:0.4	0.4:0.4:0.4:0.4	0.4:0.4:0.4:0.4	0.4:0.4:0.4:0.4	0.4:0.4:0.4:0.4	0.4:0.4:0.4:0.4	0.40.40.40.4	
Pastemask	Sections	1.0:1.0:1.0:1.0	0.4:0.4:0.4:0.4	0.4:0.4:0.4:0.4	0.35:0.35:0.35:0.35	0.45:0.45:0.45:0.45	0.45:0.45:0.45:0.45	0.5:0.5:0.5:0.5	0.45:0.45:0.45:0.45	0.4:0.4:0.4:0.4	0.40.40.40.4	
Design	Southerners	1.0:1.0:1.0:1.0	0.4:0.4:0.40.4	0.4.0.4.0.40.4	0.35:0.35:0.35:0.35	0.45:0.45:0.45:0.45	0.5:05:05:05	0.5:0.5:0.5:0.5	0.4.0.4.0.4	0.4:0.4:0.4:0.4	0.40.40.40.4	
🕶 🛅 Design for Test	Service Contraction	1.0:1.0:1.0:1.0	0.4:0.4:0.4:0.4	0.4:0.4:0.4:0.4	0.35:0.35:0.35:0.35	0.45:0.45:0.45:0.45	0.4:0.4:0.4:0.4	0.45:0.45:0.45:0.45	0.45:0.45:0.45:0.45	0.5:0.5:0.5:05	0.5:0.5:0.5:0.5	
DFT Constraint Set	Success	1.0:1.0:1.0:1.0	0.4:0.4:0.40.4	0.4:0.4:0.4:0.4	0.35:0.35:0.35:0.35	0.45:0.45:0.45:0.45	0.45:0.45:0.45:0.45	0.45:0.45:0.45:0.45	0.45:0.45:0.45:0.45	0.5:0.5:0.5:05	0.50.50.50.5	
🕨 🛅 Design	Excellence of the second	10101010	10 3541 3540 3541 35	10 35/0 35/0 35/0 35	n 35n 85n 85n 85	04040404	035035035035	0.350.350.350.35	0.850.850.850.85	04020404	0 350 350 350 35	
	Symbol names:		/									
Va 3D	Browse for Symbo	Is Show symb	ool classifications	Purge classifie	d symbols Purg	e unused symbols						
Properties												
M DRC	Outline PkgToPkg Space	cing Spacing Pa	stemask									

- 5. To set the component spacing, choose the Show symbol classifications ... button at the bottom, categorize your components into different DFA Package Classes.
- 6. For 3D constraints, go to the Constraint Manager 3 Dimensional category and adjust component clearances.
- 7. Create a Package to Package 3D Constraint Set and for the CSet Usage, choose Spacing3D.

Worksheet Selector 🗗 🗙	
🖡 Electrical	Press "+" to create new cset
→ ← Physical	
1 Spacing	Create PkgToPkg3DCset X
Same Net Spacing	PkgToPkg3DCset: PKG3DCS2
🗢 Manufacturing	CSet Usage Spacing3D ▼
🔯 3D	
🔻 🛄 3D Clearance 🧳	
🔻 🖩 Constraint Set 🛛 🖌	
Component to Component	
E Component to Board	
🖽 Component to Rigid-Flex	
🖽 Component to Board Edge	

8. You can now check the symbol classifications and classify your symbols as necessary to make the next part easier (see below).

	•					•		•
	A Symbol Browser							×
Avai	able packages				Selected packages			
VIR	TUAL_SHORT			> <	<ul> <li>0402</li> <li>0603</li> <li>DISCRETE</li> <li>LOGO</li> <li>NO-POP2</li> <li>QF</li> <li>SMT-TH-MIX-</li> <li>SMTMISC</li> <li>SOT</li> <li>THRU_HOLE</li> <li>lab_test_point</li> <li>outline</li> <li>smtconn2</li> </ul>	NP P		
F	ilter Packages		Creat	te DFA Dev Package	e Class Ok	Cance	el Help	
Add Row	Show symbol c	lassifications						

9. After symbol classification, choose Add Row to start setting up specific 3D spacing rules that meet your design requirements (see below).

FIGI			To Component	
	A Component 0402 0603 DISCRETE LOGO NO-POP2 QF SMT-TH-MIX-NP SMT-TH-MIX-P SMTMISC SOT THRU_HOLE Iab_test_point outline smtconn2 0402 0603 0603 0605 1206 2016MM CAP_SMD_048X048 T	Geometry to Check ✓ 3D ■ Place Bound ■ DFA Bound	To Component 0402 0603 DISCRETE LOGO NO-POP2 QF SMT-TH-MIX-NP SMT-TH-MIX-P SMTMISC SOT THRU_HOLE Iab_test_point outline smtconn2 0402 0603 0805 1206 2016MM CAP_SMD_048X048	Geometry to C 30 Place Bour DFA Bound
J J J Hori Vert	Show Packages from library Show Packages from database Show Package Classes Clearances: izontal 0 ical 0		Show Packages from library Show Packages from database Show Package Classes	

10. You can also create and sort by entire package classes to make package class to package class spacing available (it pulls up the classification list you would have created in previous steps depending on your needs). This means that as long as a component falls within a class, it will space itself a certain distance away from any component found in another component class.



Component-to-component spacing in 3D

Once your 3D spacing constraints have been created, you can go to the worksheet found under 3D > 3D Clearance >
 Design > Component to Component, then select the dropdown option under the Referenced package to package 3D
 CSet column to apply your constraint set (shown below).

Worksheet Selector	×			
Flectrical		1	Name	Referenced package to package 3D CSet
→ Physical				
1 Spacing			*	*
Same Net Spacing			P3449_B01_Allegro_lay	PKG3DCS2 3
😂 Manufacturing				
🔌 3D 🚹				
▼ 📕 3D Clearance				
🔻 🖩 Constraint Set				
Component to Compone	nt			
🔠 Component to Board				
🔠 Component to Rigid-Flex				
🔠 Component to Board Edg	e			
🔻 🖩 Design				
🔁 🌐 Component to Compone	nt			
📕 Component to Board				

**Impact**: Improves manufacturability, reduces assembly errors, and enhances thermal performance of the PCB by keeping components sufficiently separate from each other to avoid overheating and other thermal related issues (proximity to other components, primarily).

Related to: Surface placement of components (top vs. bottom).

Differential Pairs Spacing (Class to Class Spacing for Crosstalk Mitigation)

We addressed the physical constraints of differential pairs, but we must address their classes for spacing purposes so we can avoid crosstalk and signal degradation.

In this section we will analyze the spacing differences in differential pairs and how that is executed in the Constraint Manager.

#### Steps:

Just like how you created a physical constraint set earlier in this guide, you can set the values for inter pair and intra pair skew. We won't make a constraint but will instead modify an existing one.

- 1. Open the Constraint Manager.
- 2. Instead of making constraint sets then applying them we will navigate to an existing applied constraint set, simply navigate to our existing Spacing Constraint set USB\_SIGNALS, in the Physical Physical Constraint Set > All Layers worksheet.

Worksheet Selector 🗗	×	P3449_B01_Alleg	ro_layout_BGA-REGIO		
🗲 Electrical					
→ ← Physical				News	Referenced Spacing CSet
Spacing		Туре	<b>S</b>	Name	
▼ Spacing Constraint Set		*	•	*	*
All Layers		Net		VDD_3V3_EDP	DEFAULT
By Laver		Net		VDD_3V3_HDMI	DEFAULT
▼ Net		Net		VDD_3V3_SYS	DEFAULT
🔚 All Layers 🔶		Net		VDD_5V_IN	DEFAULT
▼ 📗 Net Class-Class		Net		VDD_5V_USB	DEFAULT
🖩 All Layers		Net		VDD_5V0_HDMI_CON	DEFAULT
🖩 CSet assignment matrix		NCIs		▼ USB_SIGNALS(5)	USB_SIGNALS
▼ 📕 Region		DPr		▼ USB_PEX_RX6	USB_SIGNALS
All Layers		XNet		USBSS_RX6_N	USB_SIGNALS

- 3. Notice that the USB\_SIGNALS(5) cell name is a net class (shown on the far left as NCIs).
- 4. As shown in the 3D component spacing constraint set, we can make class to class rules. Let's say we want any different pair net class to be at least 40 mils away from any other differential pair net class go to the worksheet under Net Class-Class > All Layers, right click the USB\_SIGNALS(5) Net class, then create a Net Class to Class spacing constraint (see below).

1 Spacing	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	ľ	- Internet			mm	mm	mm	
Spacing Constraint Set	•			•					•
	Dsn		▼ P3449_B01_Allegro_layout_BGA	-RE DE	FAULT		0.100	0.125:0.100:0.100	0.125
By Layer	NCIs		CSI_NCLS	CSI	NCLS	***	0.270:0.100:0.100	0.125:0.100:0.100	0.125
▼ III Net	NCls		DAP_SIGNALS	DA	P_SIGNALS	***	0.270:0.100:0.100	0.125:0.100:0.100	0.125
I All Layers	NCIs		DP_SIGNALS	DP	SIGNALS	***	0.338:0.100:0.100	0.125:0.100:0.100	0.125
Net Class-Class	NCIs		ETH_SIGNALS	ETI	H_SIGNALS		0.338:0.100:0.100	0.125:0.100:0.100	0.125
🕅 All Layers 📕	NCIs		GENERIC_DEZ1	GE	NERIC_DEZ1	***	0.338:0.100:0.100	0.125:0.100:0.100	0.125
CSet assignment matrix	NCIs		GENERIC_DEZ2	GE	NERIC_DEZ2	***	0.203:0.100:0.100	0.125:0.100:0.100	0.125
▼ 🛄 Region	NCIs		GENERIC_DEZ3	GE	NERIC_DEZ3	***	0.100	0.125:0.100:0.100	0.125
All Layers	NCIs		GENERIC_SEZ1	GE	NERIC_SEZ1		0.338:0.100:0.100	0.125:0.100:0.100	0.125
Inter Layer	NCIs		GENERIC_SEZ2	GE	NERIC_SEZ2	***	0.203:0.100:0.100	0.125:0.100:0.100	0.125
Spacing	NCIs		HDMI_SIGNALS	HD	MI_SIGNALS		0.338:0.100:0.100	0.125:0.100:0.100	0.125
	NCIs		PEXGEN3_SIGNALS	PE	XGEN3_SIGNALS	***	0.270:0.100:0.100	0.125:0.100:0.100	0.125
	NCIs		POWER	DE	FAULT		0.100	0.125:0.100:0.100	0.125
_	NCIs		🔻 USB_SIGNALS(1) 📕 🚃	Analasi			7.270:0.100:0.100	0.125:0.100:0.100	0.125
6	CCls		USB_SIGNALS	Analyze					
<u> </u>	NCIs		400HM_NETCLASS1	Cross Pro	bbe	C+1. F	.338:0.100:0.100	0.125:0.100:0.100	0.125
	NCIs		400HM_NETCLASS2	Find		Ctrl+F	).203:0.100:0.100	0.125:0.100:0.100	0.125
	NCIs		400HM_NETCLASS3	BOOKMAR	K		).125:0.100:0.100	0.125:0.100:0.100	0.125
	NCls		450HM_NETCLASS1	Expand			.338:0.100:0.100	0.125:0.100:0.100	0.125
	NCIs		450HM_NETCLASS2	Collapse	41		).203:0.100:0.100	0.125:0.100:0.100	0.125
	NCls		450HM_NETCLASS3	Create			Croate Class in	Physical Domain	<u>المل</u>
	NCIs.		500HM_NETCLASS1	Net Class	members		Class-Class	Physical Domain	9
	NCIs		500HM_NETCLASS2	Rename	interno er s	F2	Spacing Chet.		5
	NCIs		500HM_NETCLASS3	Delete		Del	).125:0.100:0.100	0.125:0.100:0.100	0.125
	NCIs		60V_SPACING_NETCLAS	Compare			1.250	1.250	1.250
	NCIs		60V_SPACING_NETCLAS	Constrain	nt Set References		).700	0.700	0.700
1 Same Net Spacing	NCIs		90DIFF_NETCLASS1	Change a	ll design unit attrib	outes	.338:0.100:0.100	0.125:0.100:0.100	0.125
		A0000000000000	×1					a subscription of the second	

5. You will get a new window where you set the first class and then the second class you want to make rules between.

6. Choose the USB\_SIGNALS net class on the left then the USB\_SIGNALS net class on the right so we can make rules from USB to USB (shown below).

Create ClassClasses				×
NetClasses:		NetClasses:		
HDMI_SIGNALS		GENERIC_DEZ3		
PEXGEN3_SIGNALS		GENERIC_SEZ1		
POWER		GENERIC_SEZ2		
		HDMI_SIGNALS		
400HM_NETCLASS1		PEXGEN3_SIGNALS		
400HM_NETCLASS2		POWER		
400HM_NETCLASS3		USB_SIGNALS 2		
450HM_NETCLASS1		400HM_NETCLASS1		
450HM_NETCLASS2		400HM_NETCLASS2		
450HM_NETCLASS3	I*I	400HM_NETCLASS3		
50OHM_NETCLASS1		450HM_NETCLASS1		
50OHM_NETCLASS2		450HM_NETCLASS2		
	Ok <mark>4</mark>	Apply 3	Close	Help

- 7. Click Apply, then Ok.
- 8. The USB\_SIGNALS Net Class gets added underneath itself and is listed as a Class-to-Class constraint (CCls). Click the cell next to it, then select USB\_SIGNALS (this is the spacing constraint set, not the class).
- 9. Now go to the Net Class-Class > CSet assignment matrix worksheet. Scroll right until you see the classes overlapping in that matrix.

Worksheet Selector	₽×	Row filter:	Column filter:		
👎 Electrical					
→← Physical		Class Name 🔺	400HM_NETCLAS	USB_SIGNALS	
1 Spacing		CSI NCLS			
Spacing Constraint Set		DAP_SIGNALS			
All Layers		DP_SIGNALS			
u⊞ by Layer		ETH_SIGNALS			
		GENERIC_DE			
▼ ■ Net Class-Class ≁		GENERIC_DE			
All Layers		GENERIC_DE			
CSet assignment matrix		GENERIC_SEZ1			
▼ ■ Region		GENERIC_SEZ2			
🖩 All Layers		HDMI_SIGNA			
🔻 📕 Inter Layer		PEXGEN3_SI			
🖩 Spacing		POWER			
		USB_SIGNALS		USB_SIGNALS	
		400HM_NET			

10. What this means is that any object within the USB\_SIGNALS class will have USB\_SIGNALS spacing constraints active in relation to any other object within the USB\_SIGNALS class. This is inter pair spacing.

11. Alternatively, you can use this matrix directly to apply Class to Class spacing constraints between various classes. For example, in the POWER row, select the cell found in the USB\_SIGNALS column, then choose DEFAULT.

Worksheet Selector 🗗 🗙	Row filter:	Column	filter:		
🗲 Electrical					
+∲+ Physical	Class Name		400HM_NETCLAS	USB_SIGNALS	POWER PI
‡ Spacing	CSI_NCLS				
Spacing Constraint Set	DAP_SIGNALS				
IIIII All Layers	DP_SIGNALS				
u⊞ by Layer	ETH_SIGNALS				
	GENERIC_DEZ1				
▼ Net Class-Class	GENERIC_DEZ2				
All Lavers	GENERIC_DEZ3				
CSet assignment matrix	GENERIC_SEZ1				
▼ 📄 Region	GENERIC_SEZ2				
🛱 All Layers	HDMI_SIGNALS				
▼ 📄 Inter Layer	PEXGEN3_SIGNALS				
🖩 Spacing	POWER			DEFAULT	DEFAULT
	USB_SIGNALS			USB_SIGNALS	

- 13. When you click on the worksheet Net Class-Class > All Layers again, you can scroll down/up to find the POWER Net class, then see that it now has rules for POWER to POWER and POWER to USB\_SIGNALS.

While this setting handles inter pair spacing, we also don't want these rules to cause traces and an error among themselves within their own classes. So, we need intra pair spacing.

- 1. Create an intra pair differential pair spacing constraint set by making a regular constraint set in **Spacing > Spacing Constraint Set > All Layers**. Right-click the top Dsn cell, Create Spacing Constraint Set, and name it **SCS\_INTRA\_DP**.
- 2. Once created, you can set the Line To Line spacing and other parameter values as you would like.

Worksheet Selector 🗗 🗙	P3449_B01_Alleg	ro_layou	t_BGA-REGION				
🖗 Electrical			Objects				
→ Physical			Name	Referenced Spacing CSet	All	Line	Thru
🚺 Spacing 🛛 🕇	Туре		Name		mm	mm	m
Spacing Constraint Set	•			•			•
🛱 All Layers 🔶	Dsn		▼ P3449_B01_Allegro_layout_BGA-RE	DEFAULT	***	0.100	0.125:
🖩 By Layer	SCS		► CSI_NCLS		***	0.270:0.10	0.125:
🔻 🛅 Net	SCS		► DAP_SIGNALS		***	0.270:0.10	0.125:
🛱 All Layers	SCS		► DEFAULT			0.100	0.125:
▼ 📄 Net Class-Class	SCS		► DEFAULT_Z		***	0.125	0.150:
🛱 All Layers	SCS		DP_SIGNALS			0.338:0.10	0.125:
CSet assignment matrix	SCS		► ETH_SIGNALS			0.338:0.10	0.125:
Region	SCS		► GENERIC_DEZ1			0.338:0.10	0.125:
All Layers	SCS		► GENERIC_DEZ2			0.203:0.10	0.125:
▼ Inter Layer	SCS		► GENERIC_DEZ3			0.100	0.125:
I Spacing	SCS		► GENERIC_SEZ1			0.338:0.10	0.125:
	SCS		► GENERIC_SEZ2			0.203:0.10	0.125.
	SCS		HDMI_SIGNALS			0.338:0.10	0.125:
_	SCS		▶ PEXGEN3_SIGNALS		***	0.270:0.10	0.125:
5	SCS		► SCS_BGA-REGION		0.076	0.076	0.076
<u> </u>	SCS		SCS_INTRA_DP			0.100	0.125:
	LТур		Conductor			0.100	0.125
	LTyp		Plane		***	0.100	0.100
	LТур		Conductor/EXTERNAL			0.100	0.125
	SCS		► USB_SIGNALS			0.270:0.10	0.125:

 Return to the Physical > Net > All Layers worksheet, find USB\_SIGNALS(5), scroll horizontally down to the Differential Pair > Referenced Intra-DP Spacing CSet, select the drop down cell and choose the spacing constraint set we just created, SCS\_INTRA\_DP.

Worksheet Selector 🛛 🗗 🕽	P3449_B01_Alleg	ro_layout_BGA-RI	EGION			
🕺 Electrical			Objects	Dynami	ic Phase	
🔸 Physical			Name	Max Length	Tolerance	Referenced Intra-DP Spacing
▼ 📗 Physical Constraint Set	Туре	8	Name	mm	mm	CSet
🛱 All Layers	•	*	•	•		*
🖩 By Layer	Net		VDD_3V3_EDP			
▼ ■ Net	Net		VDD_3V3_HDMI			
All Layers	Net		VDD_3V3_SYS			
▼ ■ Region	Net		VDD_5V_IN			
I All Layers	Net		VDD_5V_USB			
	Net		VDD_5V0_HDMI_CON			
	NCIs		USB_SIGNALS(5)			SCS_INTRA_DP
	DPr		▼ USB_PEX_RX6			SCS_INTRA_DP
	XNet		USBSS_RX6_N			
	XNet		USBSS_RX6_P			
	DPr		► USB_PEX_TX6			SCS_INTRA_DP
	DPr		▼ USB0_AP			SCS_INTRA_DP
	Net		USB0_AP_N			
	Net		USB0_AP_P			
5	DPr		► USB1_AP			SCS_INTRA_DP
	DPr		► USB2_AP			SCS_INTRA_DP

4. Now our differential pairs within the USB\_SIGNALS class have their own spacing constraints for their inner traces.

Visually we're talking about what you see in the image below:



**Reason for these Constraints:** We want to avoid other signals (whether differential pair or not) from creating crosstalk on our differential pairs. We achieve that by spacing them far enough apart and enforcing that spacing rule. However, the traces within the differential pairs themselves need to be close to each other, so they have their own special intra pair spacing constraint, which is shown in the image above. This intra pair spacing constraint makes it so the differential pairs don't violate their own spacing rules.

Impact: Reduced chances of crosstalk by preventing the designer from allowing signals to get too close.

Related Constraints: Class to Class Spacing, Net Class Spacing Constraints

# Manufacturing Constraints

#### Fabrication Tolerances: Allowable Variations in Dimensions for Manufacturing

Here is a list of common fabrication tolerances for PCB manufacturing, excluding silkscreen and solder mask, that can be addressed in the Constraint Manager. For a complete list, please refer to the Appendix section of this document.

# 

Board Outline Dimensions: Tolerances for Overall Board Size and Shape

**Purpose**: To define the physical boundaries of the PCB and objects near it.

**Impact**: Creating proper constraints for board-edge ensures that all components and traces fit within the specified board dimensions, crucial for manufacturing and assembly, especially for panelization of multiple board designs from one copper sheet.

#### Steps:

You can set various outline-to-object rules within a constraint set. To do so:

- 1. Open the Constraint Manager.
- 2. Go to Manufacturing > Design for Fabrication > DFF Constraint Set > Outline spreadsheet.

#### Trace Width for Manufacturing: Minimum Copper Width for Traces



Conductor/Trace width on a PCB

#### Steps:

- 1. Open the Constraint Manager.
- 2. Go to the worksheet shown below.



- 3. Left click <Create new> and the Create DFFCopperFeatureCSet will appear.
- 4. Click Ok.
- 5. In the Line Width column, set the minimum to what your manufacturer can make within the allowed budget (4 mils, 0.102 mm).

**Note**: This manufacturing rule may seem redundant if we already set the trace width in the Physical Constraints section. However, not all manufacturers have the same criteria. We want to be able to have our design without influence from the manufacturer's capabilities. We also want a modular way to swap out manufacturers without having to change our original design trace widths every time. Hence the 'redundancy'.

#### Trace Spacing: Minimum Distance Between Copper Features



Copper feature distances from each other

#### Steps:

- 1. Open the Constraint Manager.
- 2. Navigate to the Manufacturing > Copper Spacing worksheet.
- 3. Click New CSET and name it, then click Ok. You will get a window like below if you expand the rows.



- 4. There are way too many copper to copper spacing features to demonstrate here, but feel free to set rules for anything your manufacturer is capable of doing.
- 5. The final step is to choose this constraint set and **apply** it to your Design. Navigate to the worksheet, Manufacturing > Design for Fabrication > Design > Copper Spacing.
- 6. Click the dropdown cell under the **Conductor All** column.
- 7. Select the constraint set we just created. It will apply all the rules you wanted to add for spacing constraints for your manufacturer (DFFCSCS1).



**Impact:** By applying these robust sets of rules to your design, you will make your manufacturing DFM CAM engineers happy by designing **with** DFM spacing instead of it being an afterthought post layout. Proper spacing reduces the chances of unintended shorts from copper slivers on the PCB.

#### Annular Ring: Minimum Width of Copper Surrounding a Hole

**Purpose**: Defines the minimum width of copper surrounding a drilled hole to ensure proper electrical connection and mechanical strength.



Cross-sectional diagram of a via showing the annular ring measurement

# Pin Hole to Pad

Checks the minimum distance of the pin padstack hole from the outermost edge of the pad geometry.



Legal Values: Design Units DRC Code: oP Applicable Objects: DFFAnnularRingCSet Attribute Name: DFF\_AR\_PNHL\_TOPD

Diagram showing annular ring (pad hole edge to pad edge).

#### Steps:

1. Open Constraint Manager.

Same Net Spacing     Manufacturing     Design for Exprication 2	Create new> 4	•	•	*		*	
✓		1	Create DFFAnnu	ularRingCSet			×
III Mask			DFFAnnularRingCS	Set: DFFACS1 5			
Copper Features			CSet Usa	ige Etch			
Copper Spacing			6	Ok	Cancel	Help	
IIII Silkscreen         ▶       Image: Design							

- 2. Navigate to this worksheet shown in the image above: Manufacturing > Design for Fabrication > DFF Constraint Set > Annular Ring.
- 3. Create a DFFConstraint Set by clicking <Create new>.
- 4. Choose a name for this Design for Fabrication Annular Ring Constraint Set (DFFACS1).
- 5. Set the Hole to pad dimension to whatever your manufacturer recommends for the Annular ring or drill hole edge to edge of pad spacing (e.g. below is 5 mils = 0.127 mm).

		All	pins		All vias			
Name	ame Constraint set usage	mask	Hole to pad	Hole to antipad	Mining work	Pad to mask	Hole to pad	
		n	mm	mm	Missing mask	mm	mm	
							•	
<create new=""></create>								
DFFACS1	Etch		0.127				0.127	

6. Now apply this DFFACS1 constraint set to the Design. Go to Manufacturing > Design > Annular Ring worksheet.



🎢 P3449\_B01\_Allegro\_layout\_BGA-REGION - PCB Constraints - [Manufacturing / Design for Fabrication

7. Expand the PRIMARY Cell, then to the right of the Conductor Cell, choose the above constraint set and apply it (DFFACS1).

Now your pads and vias will throw a design rule error if they have any less than 5 mils (0.127 mm) of Annular ring available.

**Reason**: Ensures reliable connections between layers and prevents manufacturing defects like breakouts.



**Impact**: Affects manufacturability, reliability, and overall PCB performance. Pads may rip up. The board may result in incomplete connections and a non-functional mess of circuitry.

#### **Drill to Copper Spacing**



Top view of a pad with drill hole edge to copper trace edge spacings

**Purpose**: Defines the minimum distance between the edge of a drilled hole and the nearest copper feature to prevent manufacturing issues and ensure manufacturing reliability by preventing short circuits. May even require X-ray analysis through the PCB to adjust for scaling of PCB size and layers.

## Trace to Pin Pad

Checks the spacing between copper-object trace and pin pad.



Legal Values: Design Units DRC Code: tp Applicable Objects: DFFCopperSpacingCSet, DFFCopperSpacingAcceptableCSet Attribute Name: DFF\_CS\_TRCTO\_PNPD

#### Steps:

1. Open the Constraint Manager.



- As shown above, navigate to the Manufacturing Constraints section > Design for Fabrication > DFF Constraint Set > Copper Spacing spreadsheet.
- 3. Look for a setting called All pin pads to > Trace.
- 4. Add a new Fabrication Constraint Set by clicking on the New CSET column.
- 5. You get the Create DFFCopperSpacingCSet window.
- 6. With the options above (CSet Usage = Etch), click Ok.

7. The Constraint Set will create a column where you can populate values (see below).

Worksheet Selector	ð	×	Name	DFFCSCS1	
🐓 Electrical			•	*	New CSET
→ ← Physical			Constraint set usage	Etch	
I Spacing			► Trace to		
🚺 Same Net Spacing			Shape to		
🗧 Manufacturing			All pin pads to		
▼ 📄 Design for Fabrication			Trace Trace	0.203 🔶	
▼			Shape		
🔠 Outline			All pin pads		
🔛 Mask			All via pads		
🔠 Annular Ring			All non plated hole		
🔠 Copper Features			All non signal geometry		
🖽 Copper Spacing			All via pads to		
🗮 Silkscreen			All non plated holes to		
🕨 🔚 Design			All non signal geometry to		
Design for Assembly			► Holes		
▶ 🖩 DFA Constraint Set			Non plated		

- 8. Set the minimum clearance value (typically 8 mils (0.2032 mm), as per Sierra Circuits manufacturer recommendation).
- 9. Apply the constraint to the entire design by going to Manufacturing > Design for Fabrication > Design > Copper Spacing.

Worksheet Selector	ъ×	PRIMARY			
🕈 Electrical				Canalustan b	
→ ← Physical		Name		Conductor P	
I Spacing			All	тор	
🚺 Same Net Spacing			*	*	
Sea Manufacturing		Referenced DFF CSet	DFFCSCS1	DFFCSCS1	
Design for Fabrication		► Trace to			
▼ 🖩 DFF Constraint Set		Shape to			
0utline		<ul> <li>All pin pads to</li> </ul>			
🛄 Mask		Trace	0.203	0.203	
🇮 Annular Ring		Shano	0.205		
Copper Features		All pip pade			
Copper Spacing		All via pada			
🔡 Silkscreen		All via pads			
🔻 🖩 Design 🔫 💳		All non plated hole			
🔠 Outline		All non signal geometry			
🗰 Mask		All via pads to			
Annular Ring		All non plated holes to			
Copper Features		All non signal geometry to			
Copper Spacing		► Holes			
III Silkscreen		Non plated			

- 10. Then in this spreadsheet, in the All column, set the 'Referenced DFF CSet' field to the one we just created (DFFCSCS1).
- 11. The value for the 'All pin pads to Trace' rule will populate (0.203 mm / 8 mils) as intended.

Now all pin pads will flag an error in the PCB design rule check if closer than 8 mils to a trace.

**Impact**: Adequate spacing helps prevent issues like short circuits or weakened connections due to misalignment during drilling. Therefore getting this correct ensures manufacturability, improves yield, and enhances the overall reliability of the PCB.

#### Teardrops (Fillets)

**Purpose:** Ease the stress on copper traces and pads, especially for signal integrity and flex PCBs.

#### Steps:

- 1. Open the Constraint Manager and go to the worksheet in Manufacturing > Design for Fabrication > DFF Constraint Set > Copper Features.
- 2. Then you can see a constraint set (or create one similar to previous methods).
- 3. Under the Flex section, you have options for turning on the checks for **Missing pad fillets** and **Missing T fillets** and **Missing trace tapers** (see below).

Worksheet Selector & X	l		Minimum 🕨			Flex		۲	
🕈 Electrical	Name	Constraint set usage	Line width	Min radius on all trace corners	Max solid fill on shapes	Missing trace			
++ Physical			mm	mm	sq.mm	tapers	Missing pad fillets	Missing I fillets	
L Spacing						·	•	•	
Manufacturing	<create new=""></create>					•		•	
Design for Fabrication	DFFCFCS1	Etch	0.102			On	On	On	
▼ 🖩 DFF Constraint Set									
III Outline									
🔠 Annular Ring 🥜									
E Copper Features									
Copper Spacing									
Copper Features Copper Spacing									

- 4. Apply the constraint set by clicking the **Design > Copper Features** worksheet below.
- 5. Then you will already have the DFFCFCS1 constraint set applied to your Conductor layer (or you can apply it), and the values for the fillets will populate if you have any to add.

Worksheet Selector & X	l		Minimum 🕨			Flex		1
Flectrical	Name	Referenced DFF CSet	Line width	Min radius on all trace corners	Max solid fill or shapes	Missing trace	Missing and fillets	Missing T fillets
+ Physical			mm	mm	sq.mm	tapers	missing pad fillets	Missing T filets
1 Spacing						•	•	•
L Same Net Spacing	🔻 PRIMARY 🤟	L						
Manufacturing	▼ Conductor	DFFCFCS	0.102			On	On	On
Design for Fabrication	тор	DFFCFCS1	0.102			On	On	On
Guttine	BOTTOM	DFFCFCS1	0.102			On	On	On
III Mask	Plane							
Annular Ring								
Copper Features								
E Copper Spacing								
Silkscreen								
▼ 🔚 Design								
Outline								
🛄 Mask								
🔠 Annular Ring								
Copper Features								

If any fillets (Teardrops) are missing, especially for flex PCBs, you know where to add them because the DRC tool flags an error if they're missing.

**Impact**: More reliable pads and traces, less breakage and damage on regular and flex PCBs after bending, and improved signal integrity by reducing the abrupt change in characteristic impedance.

#### Pad To Mounting Hole Spacing: Minimum Distance Between Pads and Mounting Holes

**Purpose:** You want to avoid placing traces to mounting holes to avoid unintended shorts. Mounting holes often have metal bolts/screws used to mount the PCB which may or may not be connected to ground or some signal or power. By ensuring the mounting holes are far enough away from your traces and pads, you reduce the chance of unintended shorts and a smoking PCB.

We won't explore the entire procedure but will just highlight where to find the constraint set option and where it can be applied.

#### **Constraint Set Category**

- 1. Manufacturing > Design for Fabrication > Copper Spacing.
- 2. Create the constraint set by clicking in the New CSET column, then name it and click Ok.
- 3. Set values in the categories below:
  - a. Holes > Plated mechanical hole: Set to desired value (e.g. 100 mils or 2.540 mm).
  - b. Non plated holes > Non plated mechanical hole: Set value (e.g. 100 mils or 2.540 mm).

Worksheet Selector 🗗 🗙	Name	DFFCSCS1	
🖗 Electrical	*	*	New CSET
🔸 Physical	Mit via paus		
Spacing	All non signal geometry		
Samo Not Spacing	▼ Shape to		
	Trace		
Manufacturing	Shape		
Design for Fabrication	► Holes		
▼ IIII DFF Constraint Set	All non plated holes		
Utline	All pin pads		
	All via pads		
	All non signal geometry		
	All pin pads to		
	Trace	0.203	
▼ I Design	Shape		
Outline	All pin pads		
Hask	All via pads		
Annular Ring	All non plated hole		
Copper Features	All non signal geometry		
Copper Spacing	All via pads to		
III Silkscreen	<ul> <li>All non plated holes to</li> </ul>		
🔻 🚞 Design for Assembly	Trace		
▼ 🔚 DFA Constraint Set	Shape		
0utline	All pin pads		
PkgToPkg Spacing	All via pads		
Spacing	All non plated hole		
Pastemask	All non signal geometry		
▶ IIII Design	All non signal geometry to		
Design for Test	▼ Holes		
DFT Constraint Set	Plated mechanical hole to		
	▼ Holes		
	Plated mechanical hole	2.540	
	Non plated holes		
<b>3</b> D	Non plated mechanic	2.540	

#### Where to Apply It

As per the image below, you would apply your mechanical hole spacing constraints in the Design > Copper Spacing worksheet. Select the rule in the dropdown option, and you will see that they are applied (expand the **Holes** row if they are not visible).

Worksheet Selector B X PRIMARY									
Electrical		Conductor							
t Spacing	Name	All	тор	BOTTOM					
Same Net Spacing									
Manufacturing			DEFECCE						
Design for Fabrication     DFF Constraint Set     Outline     Mask     Annular Ring	<ul> <li>Trace to</li> <li>Shape to</li> <li>All pin pads to</li> <li>All via pads to</li> </ul>								
Copper Features Copper Spacing Silkscreen	<ul> <li>All non plated holes to</li> <li>All non signal geometry to</li> <li>Holes</li> <li>Plated mechanical hole to</li> </ul>								
<ul> <li>Image: Design</li> <li></li></ul>	<ul> <li>✓ Holes</li> <li>Plated mechanical hole</li> <li>✓ Non plated holes</li> <li>Non plated mechanic</li> </ul>	2.540 2.540	2.540	2.540 2.570 2.5400 2.5400 2.5400 2					
Copper Spacing     Silkscreen	Same Net     Non plated								

Downstream Impact: Fewer short circuits to your mounting chassis, cables, etc. Fewer concerns during testing.

#### Acid Traps: Avoiding Acute Angles in Copper Features That Can Trap Etching Chemicals

**Purpose:** While many manufacturers have updated their processes to avoid acid traps regardless of copper angles, some manufacturers can still have this problem. You can use the constraint manager to check for unintended acid traps.



Potential spacing issues that can commonly create acid traps

#### Where to find the Constraint Set

- 1. In the constraint manager, go to Manufacturing > Design for Fabrication > Copper Features.
- 2. Choose <Create new> for your desired constraint set and name it, then click Ok.
- 3. You can then set your values in the Acid Traps column under Minimum angle (45 degrees or less is typical) and Minimum area (entirely up to your design). See the example below.

Worksheet Selector 🗗 🖓	<			•	Ant	enna	Acid traps		
🕈 Electrical	Name	Constraint set usage					Minimum angle	Minimum area	
+ + Physical			Missing pad fillets	Missing T fillets	Traces	Via	deg	sq.mm	
1 Spacing	• \				•	•			
Same Net Spacing	«Croate now»							L	
Se Manufacturing	DFFCFCS1	Etch	On	On			45	0.250	
Design for Fabrication									
Im DFF Constraint Set									
Outline     Mack									
Annular Ring									
E Copper Features									
Copper Spacing									
III Silkscreen									

#### Where to Apply the Constraint Set

- 1. Go below this section to Design > Copper Features.
- 2. Click the dropdown next to Conductor to choose your desired DFFCFCS1. Notice that the rules for Acid traps get applied to your Conductor layer.

Worksheet Selector 🛃	9 X				4 Ar		enna	Acid traps	
🗲 Electrical		Name	Referenced DFF CSet	renced DFF CSet			Via	Minimum angle	Minimum area
+++ Physical					Missing T fillets	Traces		dea	sa.mm
\$ Spacing									
Same Net Spacing								·	
S Manufacturing		PRIMARY							
		Conductor	DFFCFCS1	On	On			45	0250
Design for Fabrication		TOP	DFFCFCS1	On				45	0.250
Im DFF Constraint Set		воттом	DFFCFCS1	On	On			45	0250
		► Plane							
Angular Bing									
Conner Forturer									
The Device									
• IIII Design									
Mask /									
🖽 Annular Ring									
E Copper Features									

#### Minimum Copper Area: Smallest Allowable Area of Isolated Copper Features

**Purpose**: Avoid unintended copper slivers. Slivers are hairline shavings of copper that can cause unintended shorts on the PCB and are very challenging to detect without full testing of the board and can often be intermittent.

#### Where to Find:

Similar to the steps in the Acid traps section, minimum copper area can be set as well. Please refer to that section for Acid traps.



#### How to Apply

Check the Acid Traps section and follow the same steps, but apply to the Minimum area instead.

Whitehast Salactor								
				•	Ant	tenna	Acid	traps
🕴 Electrical	Name	Referenced DFF CSet			_		Minimum angle	Minimum area
++ Physical			Missing pad fillets	Missing T fillets	Traces	Via	deg	sq.mm
L Spacing			•	•		•	•	•
Same Net Spacing								
Manufacturing	Conductor	DFFCFCS1	On	On			45	0.250
Design for Fabrication	TOP	DFFCFCS1					45	0.250
▼ I DFF Constraint Set	BOTTOM	DFFCFCS1	On	On			45	0.250
	Plane							
Annular Ping								
Copper Features								
Copper Spacing								
III Silkscreen								
🔻 🔚 Design								
III Outline								
🌐 Mask 🌈								
🌐 Annular Ring 🚽								
Copper Features								

# Assembly Constraints: Rules for Component Placement, Orientation, and Soldering

#### **Outlines and Cut Outs**

Component to Outline constraints can be set and applied in the following sections shown below.

You can set rules for:

- Component to Cut Out
- Pastemask to outline
- Paste Mask to cut out

#### Where to Find and Create the Constraint Set



## Where to Apply the Constraint Set



Component to Component Spacing (Edge and Side Spacing)

#### Package to Package Spacing

Use the constraint manager to establish Package to Package Spacing for all your components. For more information, please refer to the Component to Component Spacing Class section earlier in this document.

#### **Component Spacing to PCB Features**

Use the constraint manager to create and apply the following constraints.

- Component Body to
  - All pin pads
  - All holes
  - Edge fingers

**Purpose**: The purpose of these constraints is to avoid shorts and challenges in automatic and manual assembly, which can significantly drive up costs (especially for manual testing and assembly).

Impact: You also can hurt yield if the boards are too challenging or costly to assemble, even if they are easy to fabricate.

#### Pastemask

Use the constraint manager to establish Package to Package Spacing for all your components.



Typical solder paste to soldered component flow for surface mount and through-hole devices on a PCB

**Purpose**: Pastemask is extremely important for automatic assembly of components onto your PCB. Solder paste is metallic material with a moderately high melting point used to adhere the components to a PCB copper pad surface using wave soldering or an oven. The paste mask is a film manufactured to create a negative image to squeegee the solder paste onto your PCB (for surface mount soldering preparation).

You can set constraints for various paste mask options including:

- Pastemask to pad
- Missing pastemask
- Pastemask to other mask types
- Pastemask to
  - Pastemask
  - Via pad
  - Other Mask
  - Component Body

To access, create, and apply paste mask rules onto your design:

- 1. Open the constraint manager and you'll find your constraint creation options under Manufacturing > Design for Assembly > Pastemask.
- 2. You can click <Create new> to make your DFAMCS1 constraint, set your required values as per your manufacturing requirements and tolerances (see below).

Worksheet Selector 🛛 🗗 🗙			Pastemask to pad		Pastemask to other mask types
🕴 Electrical	Name	Constraint set usage	%	Missing pastemask	mm
→ ← Physical	•		*	•	
Spacing	<create news<="" td=""><td></td><td></td><td></td><td></td></create>				
1 Same Net Spacing	DFAMCS1	Non-Etch	90	On	0.076
Se Manufacturing	1	4			
🖽 Outline				N	
🗰 Mask _		•	► <b>`</b>		
🛄 Annular Ring					
Copper Features					
Copper Spacing					
→ Silkscreen					
▼ IIII Design					
Annular Ring					
Copper Features					
Copper Spacing					
🔠 Silkscreen					
Design for Assembly					
▼ 🖩 DFA Constraint Set					
0utline					
PkgToPkg Spacing					
U Spacing					
Pastemask					

3. Once that constraint has been created, apply it to your design that has paste mask layers. For example, the section below: Manufacturing > Design for Assembly > Design > Pastemask.

P3449_B01_Allegro_layout_BGA-REGION - P	CB Constraints - [Manufact	uring / Design for Assemb	ly / Design]		
File Edit Objects Column View	Analyze Audit To	ools Window Help			
🛞 📮 🏮 🍢 🛛 via_in_pad		5 🚡 🚡 🏹	To To S	• 🔊 - 🗏 😽 🐇	o 😘 🍋 🔆 🖬
Worksheet Selector 🗗 🗙	News		Pastemask to pad		Pastemask to other mask types
👎 Electrical	Name	Referenced DFA CSet	%	wissing pastemask	mm
+ ← Physical	•	•		]•	•
J Spacing		· · · · · · · · · · · · · · · · · · ·	L		
C Same Net Spacing	Pastemask layers				
Search Manufacturing	Not in stackup				
0utline					
🗮 Mask 🔤					
🖽 Annular Ring					
Copper Features					
E Silkscreen					
▼ I Design					
III Outline					
III Mask					
🌐 Annular Ring					
Copper Features					
Copper Spacing					
Silkscreen     Design for Assembly					
▼					
🔠 Outline					
🗰 PkgToPkg Spacing					
III Spacing					
Pastemask					
▼ IIII Design					
Spacing					
Pastemask					

4. Then, choose **Referenced DFA CSet** and then rules from the CSet get applied.

**Impact**: You also can hurt yield if the boards are too challenging or costly to assemble due to unreliable paste, missing paste or paste that is too close to other objects on the PCB.

### Silkscreen and Solder Mask: Specifications for Text and Mask Application on The PCB.

**Purpose**: Silkscreen is used to write notes on the PCB for easier assembly.



Silkscreen reference designators on a PCB layout

- All pin pads
- All via pads
- All non plated holes
- Min width (line, arc, shape)
- Min length (line, arc)

- Text overlap
- Text under component
- Text to line
- Text to shape
- Text to text

**Impact**: There is risk with having silkscreen in the wrong areas, though, like close to or under pads. There can be slivers and fabrication and manufacturing defects created by misplaced silkscreen. In addition, if the silk screen is missing in critical areas, it can significantly or gradually add on more cost for assembly.

#### Where to Find:

- 1. In the constraint manager, navigate to the Manufacturing > Design for Fabrication > Silkscreen worksheet.
- 2. Then hit the <Create new> button to create a new constraint set. That gets created.
- 3. Then populate the values based on what your design and manufacturer need (see image below).

Worksheet Selector	e ×			All pin pads	All via pads	All non plated holes	Min width(line,arc,shape)	Min length(line,arc)	Text	Text under	Text to line	Text to shape	Text to text
Électrical		Name	Constraint set usage	mm	mm	mm	mm	mm	overlap	component	mm	mm	mm
🔸 Physical									•	•	•		
1 Spacing		<create new=""></create>											
Same Net Spacing		DFFSCS1	Non-Etch	0.127	0.127	0.127	0.152	0.127	Off	Off	0.127	0.127	0.127
Sector Manufacturing													
Design for Fabrication													
Im DFF Constraint Set													
III Mask													
🛄 Annular Ring													
Copper Features													
Copper Spacing													
🔠 Silkscreen 🦰													

- 4. Once the constraints are set, you are ready to apply them.
- 5. Go to Manufacturing > Design for Fabrication > Design > Silkscreen.
- 6. Click and apply your constraint set onto the cell next to your **PRIMARY** design.

File Edit Objects Column View	v Analyze Audit To	ools Window Help				
🛠 📮 🝺 🔯 🛛 via_in_pad	<b>▼ ∧</b> ∧	) 🚡 🚡 🏹 🍾	To To To 🛇	/ 🔊 - 🛯 = <sub>0</sub> 🔏 👌	ə 😘 🍋 🔆 🔚	
Worksheet Selector 🛛 🗗 🗙			All pin pads	All via pads	All non plated holes	•
🗲 Electrical	Name	Referenced DFF CSet	mm	mm	mm	1
+ Physical	•				•	
\$ Spacing						
(1) Same Net Spacing	Mask					
Se Manufacturing	Not in stackup					
<ul> <li>Design for Fabrication</li> <li>DFF Constraint Set</li> <li>Outline</li> <li>Mask</li> <li>Annular Ring</li> <li>Copper Features</li> <li>Copper Spacing</li> <li>Silkscreen</li> <li>Design</li> <li>Outline</li> <li>Mask</li> <li>Annular Ring</li> <li>Copper Features</li> <li>Copper Spacing</li> <li>Silkscreen</li> <li>Silkscreen</li> <li>Silkscreen</li> </ul>						

While we have constraints for all fabrication and assembly concerns, we need another for testing and test points. This is addressed in the next section.

# Design for Test (DFT) Constraints

Test Points: Placement and Minimum Distances From Other Test Points and Components



Visual Aid: Test point on pad.

**Purpose:** Defines the placement and spacing requirements for test points to ensure proper testing and debugging of the PCB. **Steps:** 

- 1. Open the Constraint Manager.
- 2. Navigate to the Design for Test (DFT) section.
- 3. You would create the constraint set for your design (upper red box in image below).
- 4. Then apply that constraint set to appropriate objects within the design (lower red box in image below). Set a minimum distance between test points.



In the constraint manager you can set constraints for various parameters such as:

- Outline
  - Test point to outline
  - Test point to cut out
- Mask and Silkscreen
  - Test point on solder mask
  - Test point to silkscreen
- Spacing
  - Test point to test point
  - Test point to component
  - Test point to pin pad
  - Test point to via pad
  - Test point to non plated hole
  - Test point under component
- Probe
  - Test point minimum pad size

**Reason**: Proper test point placement ensures accessibility for automated testing equipment and manual probing, facilitating efficient testing and troubleshooting processes.

**Impact**: Improves testability, reduces testing time, and enhances the overall quality assurance process for the PCB. Well-placed test points can significantly reduce debugging time and improve manufacturing yield.

# **3D** Constraints

Purpose: 3D constraints have become a mandatory requirement in the modern PCB design and assembly process.

#### **Component to Component**



#### **Component to Board**



#### **Component to Rigid Flex**



#### Component to Board Edge



#### Steps: To access 3D constraints

- 1. Open the Constraint manager and navigate to the '3D' section > 3D Clearance > Constraint Set.
- 2. Choose the category within the constraint set that applies to your situation (e.g. Component to Component, Component to Board, Component to Rigid-Flex, Component to Board Edge).
- 3. Click the + Button to create a new cset and apply your constraint values.

Worksheet Selector 🗗 🗙	-
🗲 Electrical	Pres "+" to create new cost
+++ Physical	Fiest + to cleate new cset
Spacing	
Same Net Spacing	
🗢 Manufacturing	
🔯 3D 🛛 🖊 🖊 🙀	
<ul> <li>▼ ■ 3D Clearance</li> <li>▼ ■ Constraint Set</li> <li>Component to Component</li> <li>Component to Board</li> <li>Component to Rigid-Flex</li> <li>Component to Board Edge</li> <li>▼ ■ Design</li> <li>Component to Component</li> <li>Component to Board</li> <li>Ecomponent to Board</li> <li>Component to Board</li> <li>Ecomponent to Board</li> <li>Ecomponent to Board</li> <li>Ecomponent to Board</li> <li>Ecomponent to Board</li> </ul>	

4. Once you're happy with your constraints, go to the 3D Clearance > Design section and apply the appropriate constraint to the relevant objects (e.g. Component to Component, Component to Board, etc.)

Worksheet Selector 🛛 🗗 🗙		
🖡 Electrical	Name	Referenced package to package 3D CSet
→ ← Physical		
1 Spacing	·	
Same Net Spacing	P3449_B01_Allegro_layout	
anufacturing		<b>†</b>
🔯 3D 🔶		
▼ 📕 3D Clearance		
🔻 🖩 Constraint Set		
🔠 Component to Component		
🔠 Component to Board		
🗰 Component to Rigid-Flex		
🗰 Component to Board Edge		
🔻 🖩 Design		
Component to Component		
🗱 Component to Board		
🗰 Component to Rigid-Flex		
🔛 Component to Board Edge		

**Impact:** Components, cables and connectors can cause an otherwise functional PCB to not be viable for product use because of lack of ability to fit into a larger system. You may also have components that, due to their spacing, make it difficult or impossible to place them on the PCB without going in a certain order. Poorly 3D constrained boards are also at risk of components and your design enclosures colliding.

## **Rigid Flex PCB Constraints**

#### Teardrops (Fillets)

Please see the Teardrops (Fillets) section in the Manufacturing Section.

#### Component to Flex PCB

Purpose: Components need to maintain a certain distance from the flexible parts of a PCB.

The Constraint manager gives you granular control over components to rigid-flex placement and positioning. To explore that:

- 1. Open the constraint manager.
- 2. Go to the worksheet found in 3D > 3D Clearance > Constraint Set > Component to Rigid-Flex.



3. In this worksheet, you can choose Add Row at the bottom of the window to open the Create Component to Rigid-Flex Clearances window.

4. Set your 3D clearances and other parameters as shown below, then click Ok.

P Create Com	nponent to Rigid-Flex Cle	earances ×
From Compor	nent	
0402 0603 <b>4</b> DISCRETE		Geometry to Check
Show Pack	<ul><li>Place Bound</li><li>DFA Bound</li></ul>	
🛃 Show Pack	kage Classes	
3D Clearances		
Horizontal	0	
Vertical	0	
dd Package (	Classe Ok	Cancel

5. You can set your values even after placing the constraints.

Worksheet Selector 🗗		<mark>S1</mark> +				
🐓 Electrical						
🔸 Physical			3D Clearances			
Spacing	Component	20	Dis es Bernad		Horizontal	Vertical
(     Same Net Spacing		30	Place Bound	DFA Bound	mm	mm
nanufacturing	•	*				*
🔯 3D	0603				0.254	0.508
<ul> <li>▼ ■ 3D Clearance</li> <li>▼ ■ Constraint Set</li> <li>■ Component to Component</li> <li>■ Component to Board</li> <li>■ Component to Rigid-Flex</li> </ul>						

6. Now you can apply the constraint set by choosing the 3D > 3D Clearance > Design > Component to Rigid-Flex worksheet.

Worksheet Selector 🗗 🗙		
🐔 Electrical	Name	Referenced package to rigid-flex 3D CSet
+ 🕂 Physical		
1 Spacing	*	<u>*</u>
🚺 Same Net Spacing	P3449_B01_Allegro_lay	COMPTORGDFLEXCS1
😂 Manufacturing		<b>↑</b>
🔯 3D 🚄		
▼ 📄 3D Clearance		
▼ 🖩 Constraint Set		
E Component to Component		
🖽 Component to Board		
Component to Rigid-Flex		
🖽 Component to Board Edge		
🔻 🖩 Design 🍡		
E Component to Componer		
🌐 Component to Board		
Component to Rigid-Flex		
🔛 Component to Board Edge		

**Impact**: Similar to component 3D assembly constraints, your component to Rigid Flex constraints can cause product issues if they collide, even if the fabrication and assembly go well. This is especially true when it comes to the folding behavior of flexing and folding on a PCB.

Modern hardware and PCB layout require a more holistic approach than traditional methods, and only the most robust set of constraint management tools enable today's top technology.

## Conclusion

In Part 2 of the OrCAD X Constraint Manager Guide, we explored the essential standard constraints and rules that form the backbone of PCB design. These constraints, ranging from physical and spacing rules to manufacturing considerations, ensure a reliable and high-quality PCB layout.

By understanding and applying these constraints, designers can effectively manage component placement, electrical integrity, and manufacturing processes, ultimately leading to a robust design that meets industry standards.

As we transition into Part 3, Advanced Constraints, we will delve deeper into more complex design considerations that accommodate cutting-edge technologies and intricate layouts.

This next section will empower you with the knowledge to tackle challenging design environments and push the boundaries of PCB design innovation.

# cādence<sup>®</sup>

Cadence is a pivotal leader in electronic design and computational expertise, using their Intelligent System Design Strategy to turn design concepts into reality. Cadence customers are the world's most creative and innovative companies, delivering extraordinary electronic products from chips to boards to systems in the most dynamic market applications. www.cadence.com

© 2025 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, the Cadence logo, and the other Cadence marks found at www.cadence.com/go/trademarks are trademarks or registered trademarks of Cadence Design Systems, Inc. All other trademarks are the property of their respective owners. 02/25 DB/CP6/DG-ORCDX-CNSTMG-PT2/PDF