DESIGN **GUIDE**

cadence®

OrCAD X Constraint Management Guide

Part 2 of 5

Contents

Part 2 - Standard Constraints

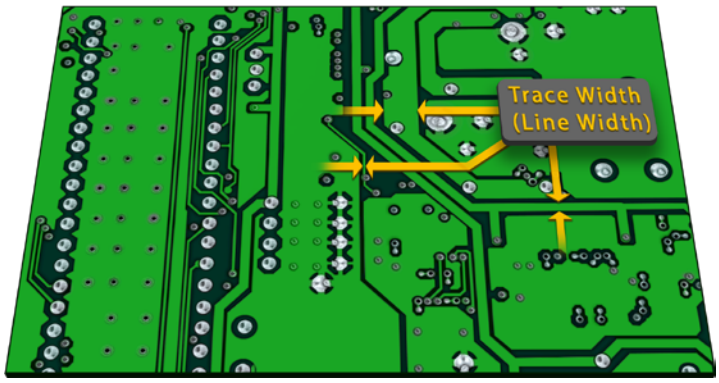
Welcome to the second part of this Constraint Management Guide. This section covers the common constraints you will need to set for most printed circuit boards (PCBs). Below is a general list of the format we will be following:

1. **Purpose:** Briefly states the purpose of the constraint.
   Example: Ensures minimum spacing to prevent electrical interference.
2. **Visual Aid:** Relevant images or screenshots to illustrate the process.
   Example: Diagram of Constraint Manager with highlighted options.
3. **Steps:** Outlines the steps to implement the constraint in OrCAD X Presto PCB Editor.
   Example: Open Constraint Manager > Select Category > Set Parameters > Apply.
4. **Reason**: Explains why this constraint is important.
   Example: Critical for maintaining signal integrity in high-speed designs.
5. **Impact:** Describe the impact of implementing this constraint.
   Example: Reduces risk of signal crosstalk, improving overall design reliability.

For more details on constraints, please refer to online documentation and training.

Physical and Spacing Constraints

Trace Width: Minimum and Maximum Width for Signal And Power Traces.

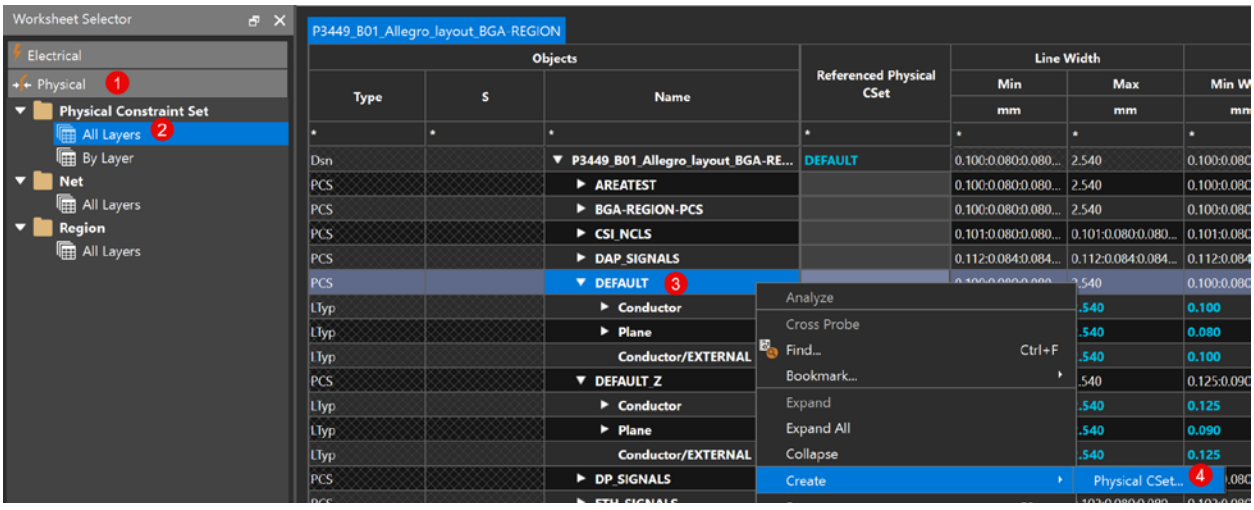


Top view of PCB traces with different widths

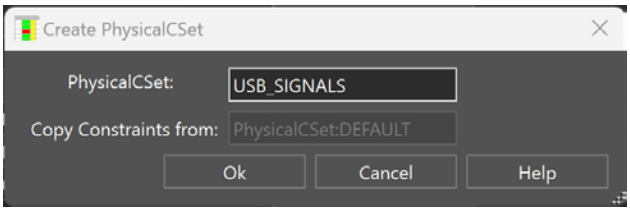
Purpose: Defines minimum and maximum trace widths for signal and power traces.

Steps:

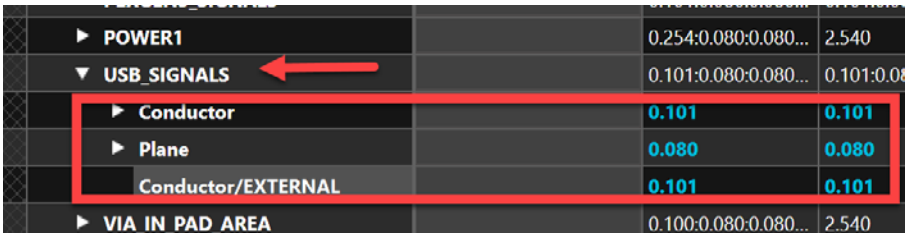
1. Open Constraint Manager. Select Physical > Physical Constraint Set > All Layers > Create a Constraint Set if necessary.



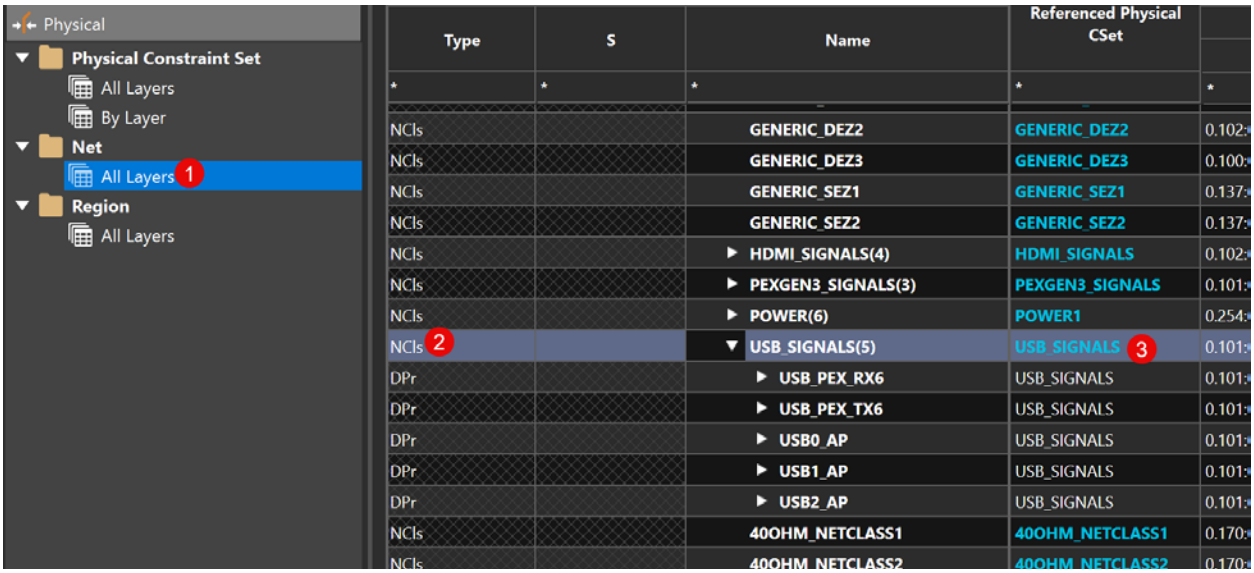
2. Name the constraint set of interest (e.g., **USB_SIGNALS**)



3. The constraint set has been created (you will see it in the worksheet).

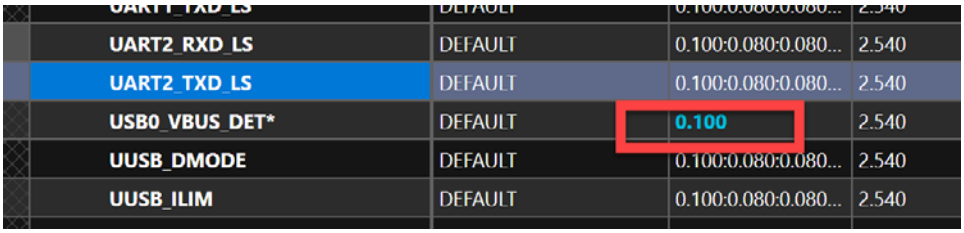


4. Next, apply the constraint set to the appropriate nets or net classes by going to the **Physical - Net - All Layers worksheet** (USB_SIGNALS application shown below).



5. Then click the dropdown and select the appropriate Physical CSet (USB_SIGNALS) you created (shown above in step 3).

6. Finally, if you need to, you can set specific trace widths for any net without having to apply a constraint set by typing values directly into the cells. Those values will appear blue and bold, like in the image below.



7. Set a value in the spreadsheet column named **Line Width - Max** value for **USB0_VBUS_DET***, which will override the constraint set you just applied to the class, group, or net and turn it blue (shown above).

Tip: You can repeat this general procedure for any number of nets: Set the constraints/rule set, then apply to the appropriate net, net class, or net group.

You may also directly type in/apply to specific nets or classes by typing them in, but that is not recommended as the first option. Manage what you can through constraint sets only.

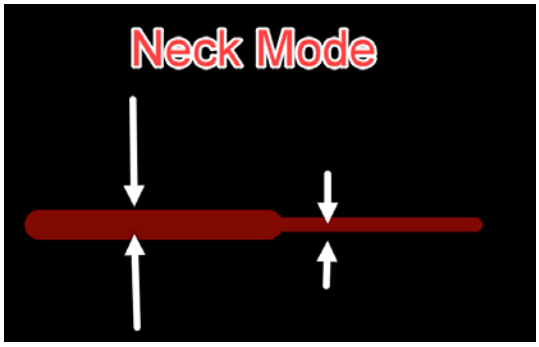
Reason: Trace width ensures proper current-carrying capacity and signal integrity.

Impact: Balances manufacturability with electrical performance.

Note: Setting the trace width in the Physical section does not necessarily mean you meet the manufacturer's minimum trace width limits. Please be mindful that you can set any value in the Physical domain for trace (line) width. But if you do not follow the rules for your manufacturer, you can have a rude awakening that will force you to reroute the entire PCB again.

Related Constraints: Design for Manufacturing - Trace width.

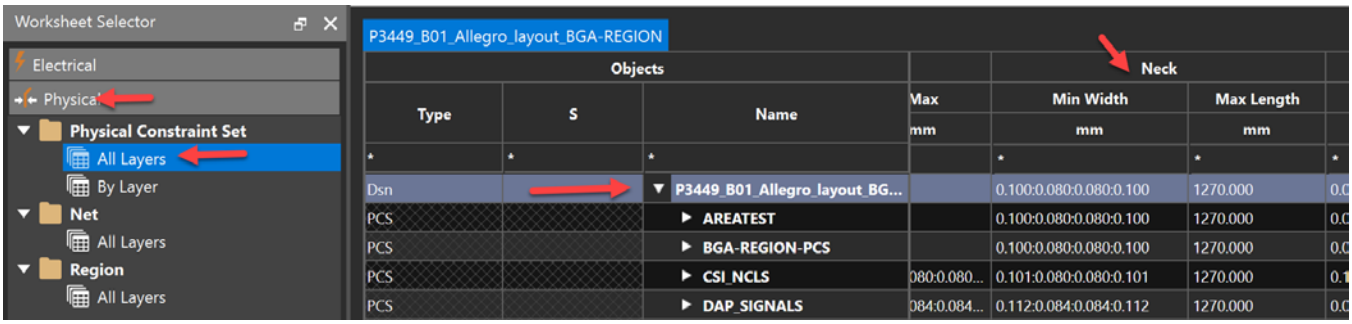
Neck mode: Minimum trace width when routing into smaller spaces



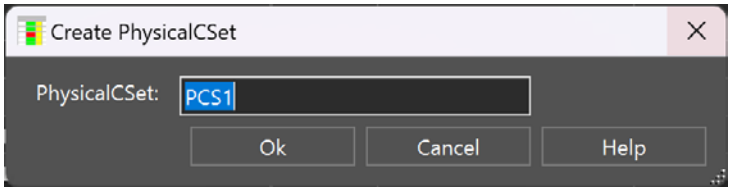
Purpose: Allow traces to enter a smaller area (e.g., a BGA Constraint region, shown in Part 1 of this document) by becoming thinner momentarily and for a certain distance.

Steps to Create a Neck Mode Constraint:

1. Open Constraint Manager.

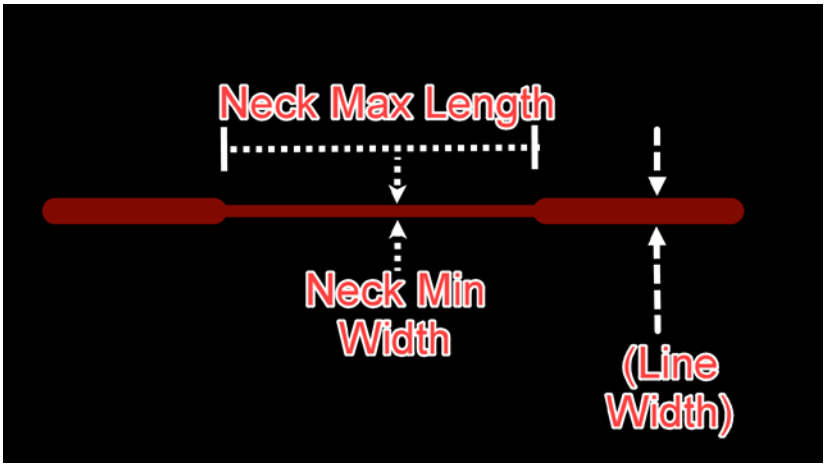


1. Navigate to the spreadsheet Physical > Physical Constraint Set > All Layers.
2. You will see all the constraint sets that were created. You can create your own by right-clicking the cell containing the design name **P3349_B01_Allegro_layout_BG** (the name of your .BRD file/Design), then choosing Create - Physical CSet.



3. In the pop-up window, give the PhysicalCSet an appropriate name.

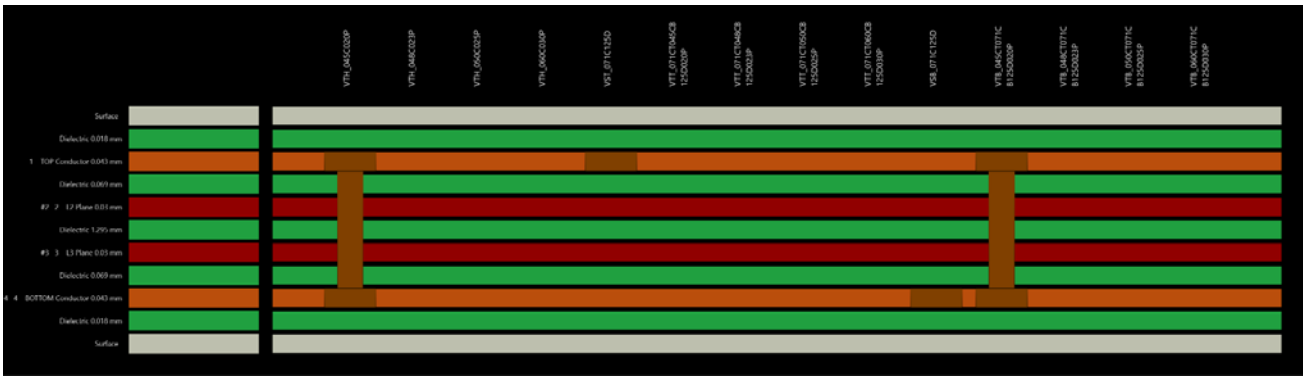
4. After that, you can set whichever neck mode rules you want. The two main parameters are: **1. Neck - Min Width**, and **2. Neck - Max Length** (see below).



Objects	Name	Neck		
		Min Width	Max Length	Mi
		mm	mm	
	*	*	*	*
▼	P3449_B01_Allegro_layout_BG...	0.100:0.080:0.080:0.100	1270.000	0.000
▶	AREATEST	0.100:0.080:0.080:0.100	1270.000	0.000
▶	BGA-REGION-PCS	0.100:0.080:0.080:0.100	1270.000	0.000
▶	CSI_NCLS	0.101:0.080:0.080:0.101	1270.000	0.118:0.0
▶	DAP_SIGNALS	0.112:0.084:0.084:0.112	1270.000	0.000
▼	DEFAULT	0.100:0.080:0.080:0.100	1270.000	0.000
▼	Conductor	0.100	1270.000	0.000
	TOP	0.100	1270.000	0.000
	BOTTOM	0.100	1270.000	0.000
▶	Plane	0.080	1270.000	0.000
	Conductor/EXTERNAL	0.100	1270.000	0.000
▼	DEFAULT_Z	0.125:0.090:0.090:0.125	1270.000	0.000

Via Size: Diameter and pad size for vias, including microvias and blind/buried vias.

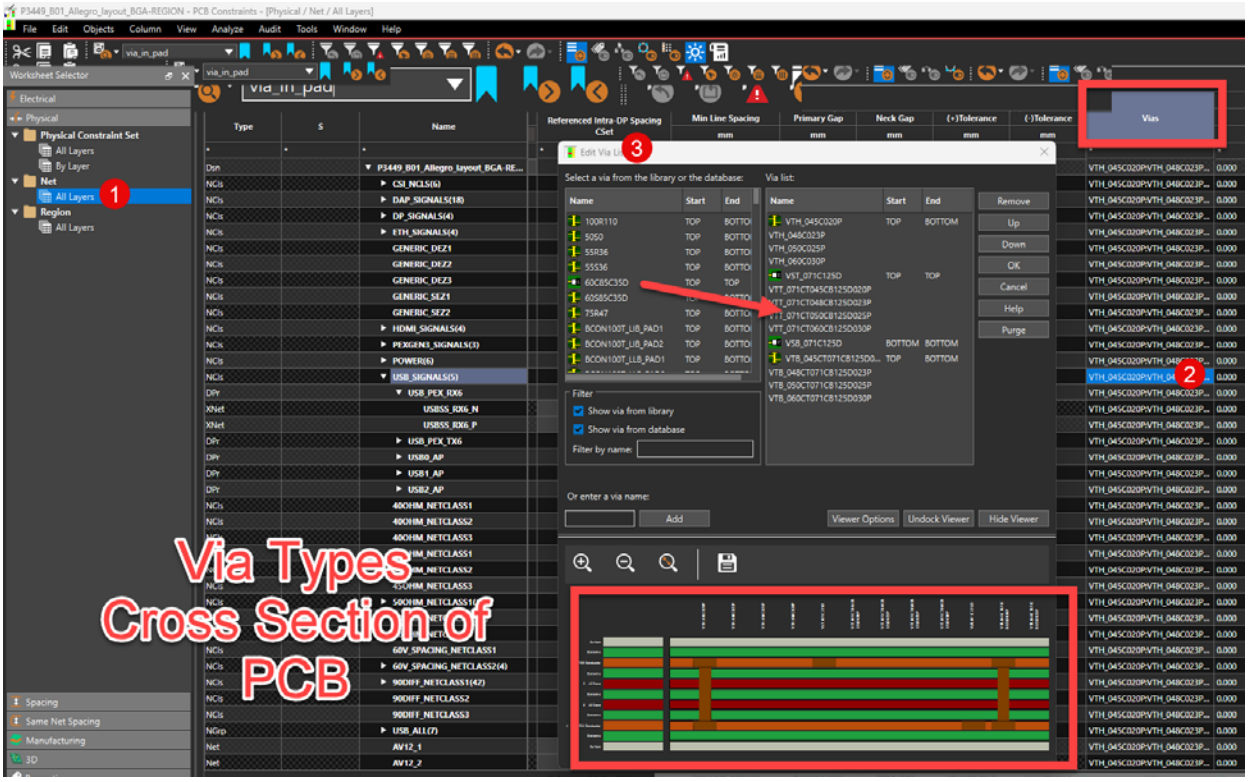
Purpose: Defines the diameter and pad size for various types of vias to ensure proper connectivity between layers.



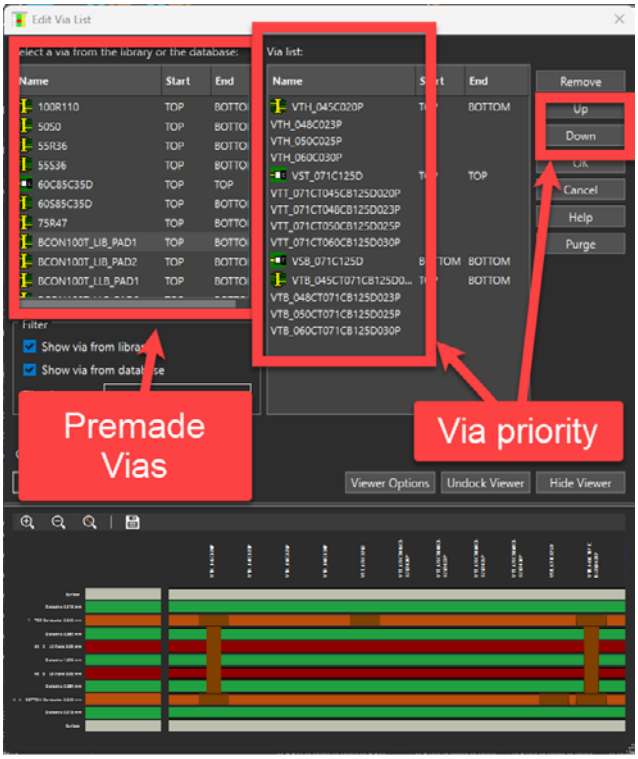
Cross-sectional diagram showing different via types.

Steps:

1. Open Constraint Manager.
2. Select the Physical worksheet tab and click on Net - All.



3. Go to the Vias column, then click **once** on the cell for the row of rules you want to assign specific vias to. The **Edit Via List** new window will appear.



4. Set via types you want from the library (vias found on the left), then double-click to place them among the list of usable via the list on the right. These vias will be applied to the specific row net, class, group, or region to be selected when you open the window from the CM.
5. Once the list is satisfactory, you may organize the vias by highlighting the via name (on the list to the right) and using the **Up** and **Down** buttons in the window.
6. Use the above steps to apply specific via types (through-hole, blind, buried, or microvias) to any net classes, groups, and constraint regions.

Note: While you can modify padstacks within OrCAD X PCB Editor, you cannot directly create them. You will need to use the Padstack Editor tool to create them, and then you can use the Constraint Manager to add padstacks to your design.

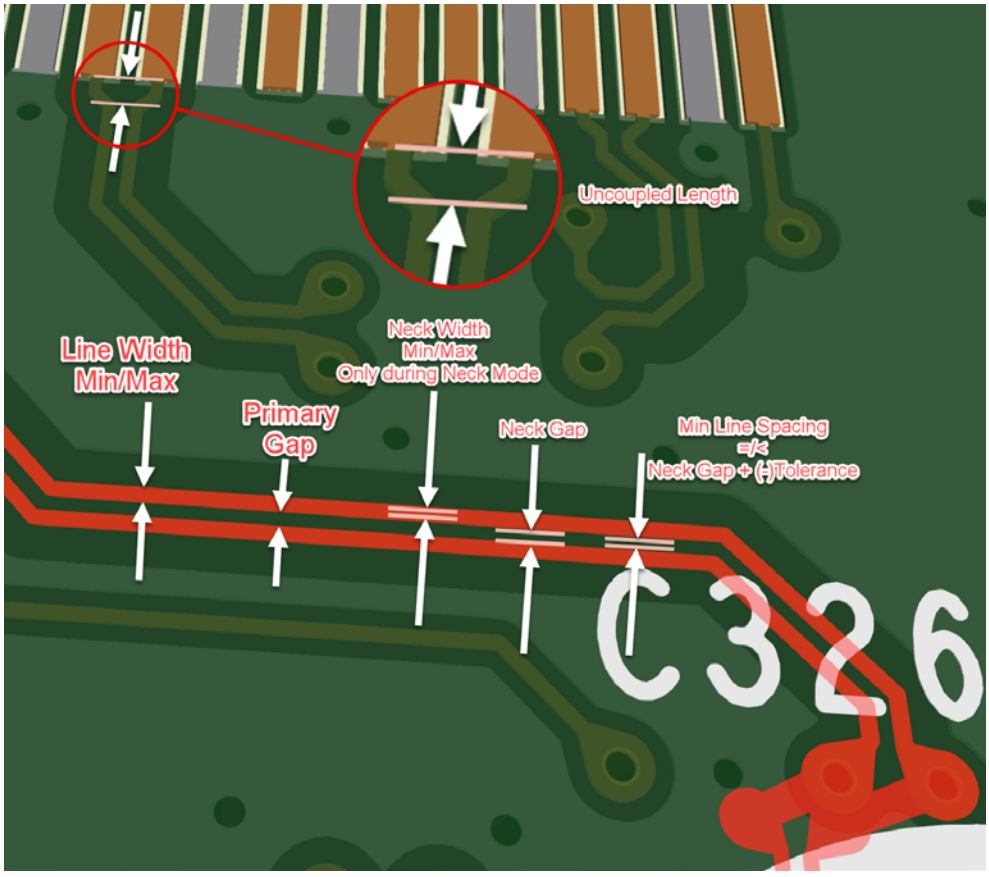
Reason for Padstacks: Proper padstack selection ensures reliable layer-to-layer connections while optimizing board space and manufacturability.

Impact: Balances electrical performance with manufacturing constraints and cost considerations.

Related to: Aspect Ratio, Annular Ring

Differential Pairs (Basic Setup)

Purpose: Defines the minimum and maximum widths and spacing for differential pair traces to maintain signal integrity. We will focus on the physical constraints in this example. In the high-speed section(s), we will encounter differential pairs again and address the high-speed constraints.

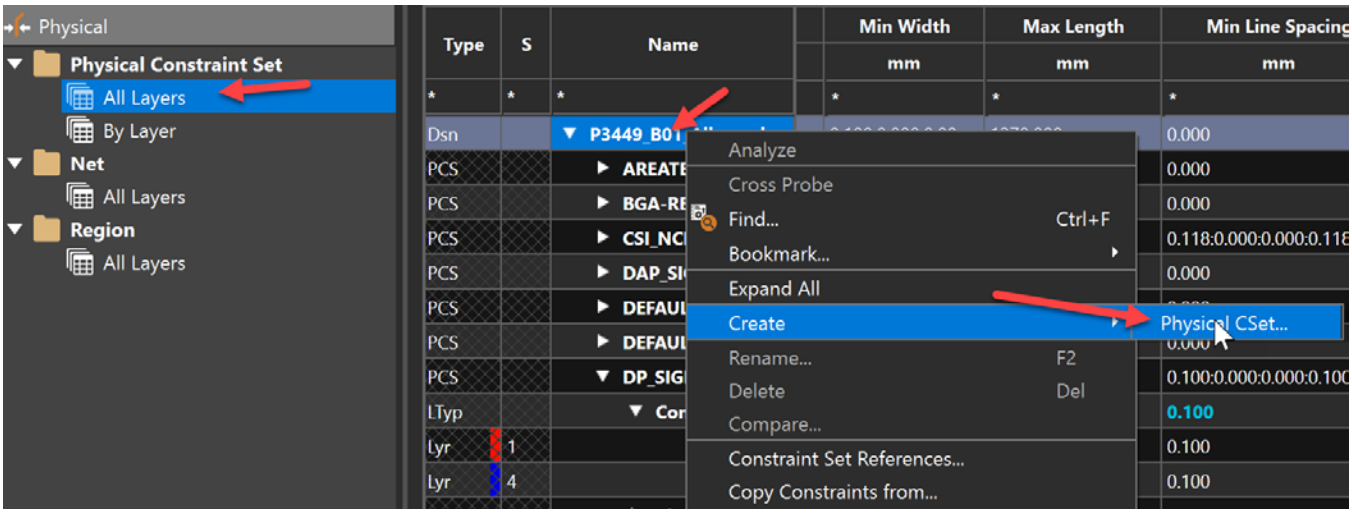


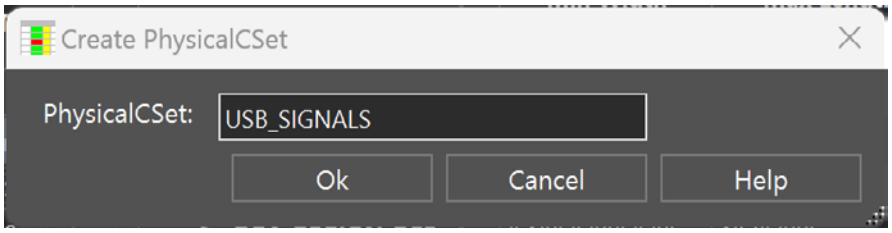
Top view of a differential pair showing some width and spacing parameters

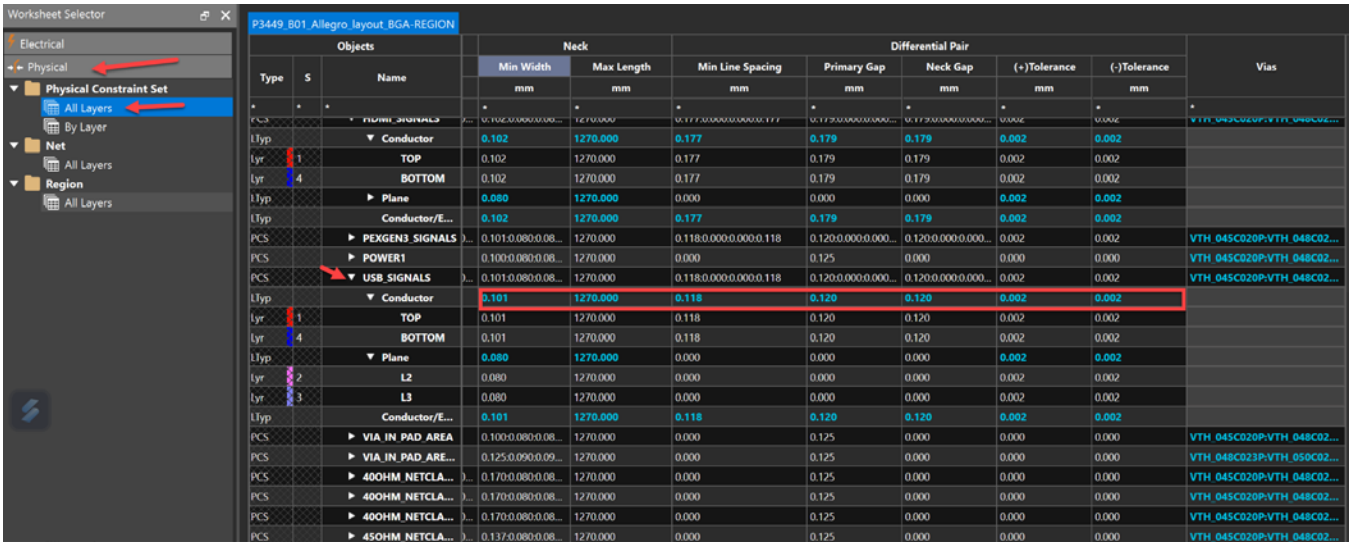
Reason for Physical Constraints: Setting up physical constraints and forcing symmetry in differential pairs ensures consistent impedance and reduces the chances of signal issues in high-speed signal transmission. In OrCAD X Presto PCB Editor, you want to use physical rules to control your differential pairs as much as possible.

Steps:

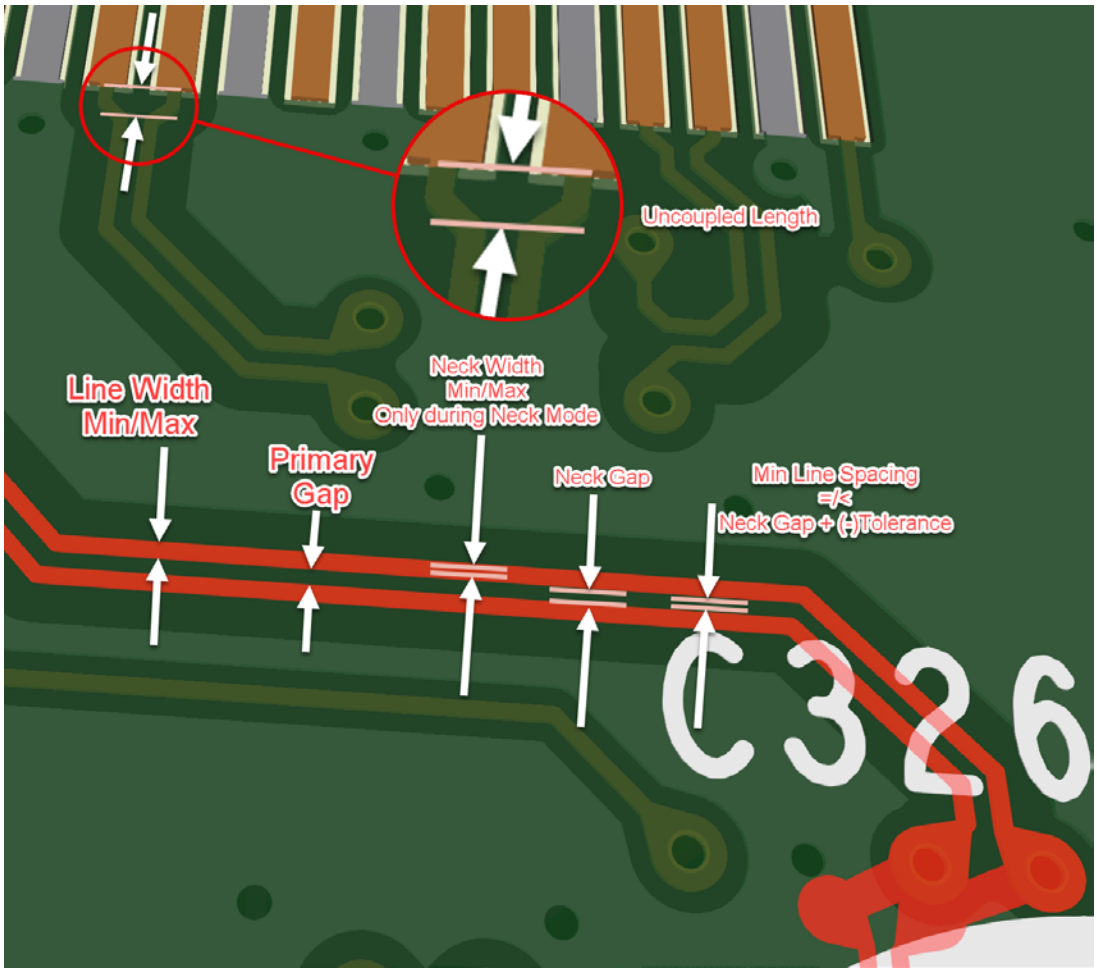
1. Open Constraint Manager.
2. Navigate to the Physical Constraint Set tab.
3. Select "All Layers" from the dropdown.
4. Similar to the previous creation of constraint classes, you can right-click the main Dsn name at the top of the list, make a Physical Cset, then navigate to the CSet. In our example, we have one named USB_SIGNALS expanded (shown below).







5. Set values for Min Width, Max Width, Min Space, and Max Space (shown above).



Top View of Differential Pair

Differential pairs have many parameters to consider.

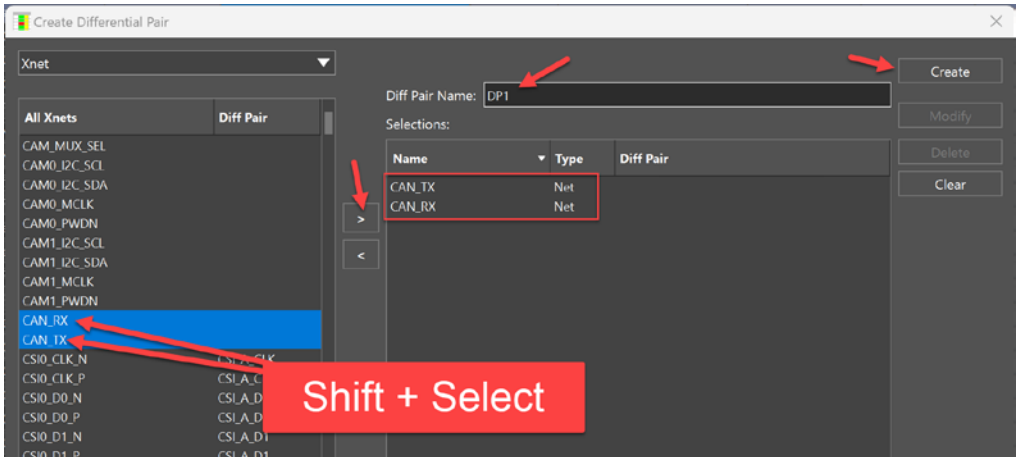
- **Line Width (Min, Max)** - The trace width for a single diff pair trace not in Neck Mode. Min is the thinnest the trace is allowed to be, and Max is the thickest the trace is allowed to be.
- **Neck** - When in Neck Mode (narrower traces)
  - Min Width – the thinnest that a single-ended trace of the diff pair can be
  - Max Length - the longest distance allowed for diff pairs to be in neck mode before going into regular diff pair mode
- **Uncoupled Length** - When diff pairs are not close enough to each other to be electrically coupled, i.e., separated
  - Gather control - During the time diff pairs are uncoupled to connect to or from pads, you can ignore or include the distance where diff pairs momentarily separated
  - Max - the maximum distance you will allow diff pair traces to be uncoupled for
- **Static Phase Tolerance** – a high-speed timing-related constraint that determines the allowed skew in timing between the two differential signals arriving at the receiver simultaneously.
- **Dynamic Phase** - high-speed timing and EMC-related constraint that determines the amount of common mode voltage and signal attenuation allowed at any distance along the trace path before reaching the receiver pins
  - **Max Length** - maximum time of flight to allow signals to propagate out of phase
  - **Tolerance** - some +/- margin for signals to be out of sync

- **Differential Pair**
  - **Referenced Intra-DP Spacing CSet** - diff pair trace to diff pair trace spacing
  - **Min Line Spacing** - the thinnest diff pair trace can be
  - **Primary Gap** - the edge-to-edge distance between the + and - diff pair traces during regular routing
  - **Neck Gap** - the edge-to-edge distance between the + and - diff pair traces during Neck Mode routing
  - **(+)Tolerance** - added trace width on any trace, whether in neck mode or not
  - **(-)Tolerance** - the subtracted/minimal gap spacing width, whether in Neck mode or not. Note that the narrowest gap (during neck mode) minus the Tolerance must be equal to or greater than the Min Line Spacing rule/constraint, else you get an error
- **Vias** - vias that are allowed on the differential pair traces
- BB Via Stagger - the allowed parameters for blind and buried vias for the diff pair traces
  - Min - the closest distance between two blind/buried vias
  - Max - the furthest distance between two blind/buried vias
- Pad-Pad Connect - Basically for allowing via in pad connections - typical for tight spacing conditions and via in pad technology
- Etch
- Ts - T-points - this allows you to make a T-junction between another trace and one of the traces of your diff pair

Creating a Diff Pair

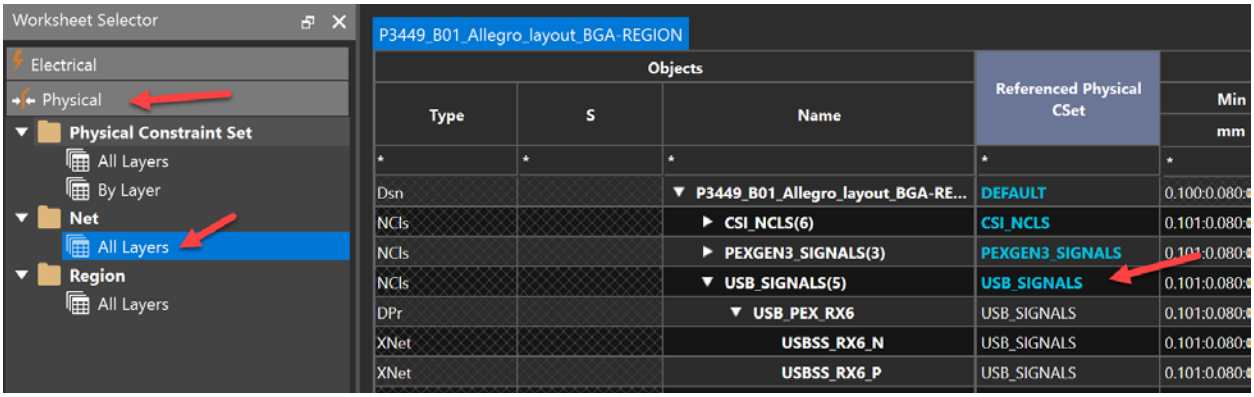
Before continuing with this example, let's create a differential pair.

1. To create a differential pair:
   a. Go to the Physical > Net > All Layers worksheet
   b. Select the two nets you want to pair
   c. Right-click and choose Create > Differential Pair
   d. The Create Differential Pair window will appear
   e. Name the pair and click Create
   f. You can also remove a differential pair you might have made by mistake by clicking the Clear button
   g. Once you have created all your differential pairs, click Close



2. At this point, you can create a net class or group within the Physical > Net > All Layers worksheet (follow the instructions in Part 1 on how to create Net classes and groups).

3. After creating your net classes and groups, apply the differential pair Physical Constraint Set you made earlier to a Net Class, Net Group, or Differential Pair (NCls, NGrp, DPr), as shown below.



4. The Net Class, USB_SIGNALS(5), adopts the Physical Constraint Set (which we also named USB_SIGNALS) and the application is done.

Note: While it may be implicitly understood, know that constraint sets are **different** from the objects, groups, classes, and regions they are applied to. They may be named the same as the net groups they're applied to, but that is simply for convenience. There is no relation between the names of your constraints and what they are applied to.

Important Tip: Please be careful with the worksheet being selected. All constraint sets are made in the Constraint set category (e.g., Physical Constraint Set - All Layers in this case)

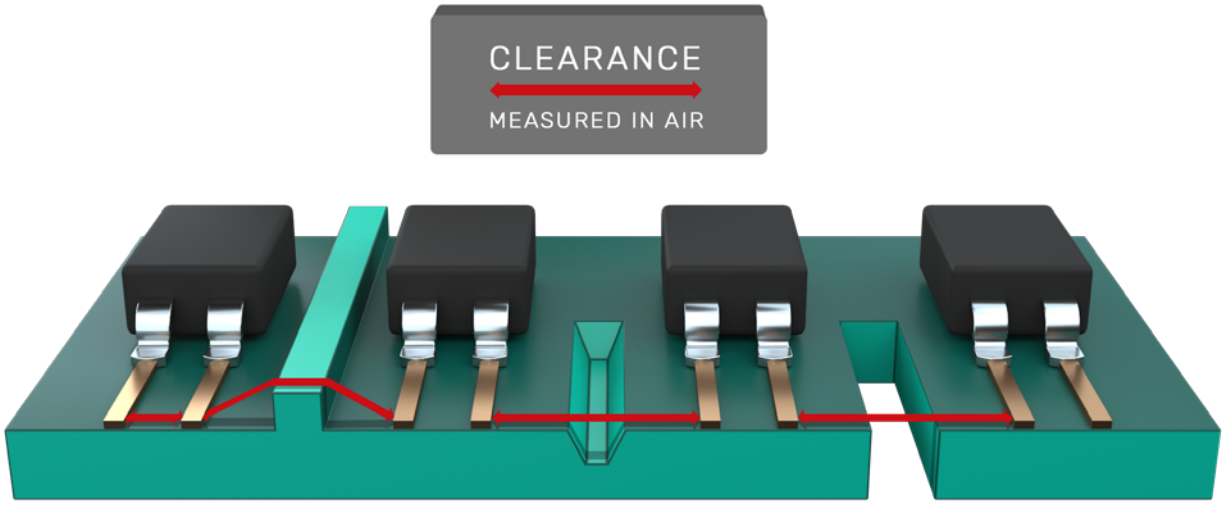
Impact: Differential pair use and constraints are popular for carrying important signals that need some protection against noise. Managing the constraints for your differential pairs improves signal integrity and enhances overall performance. Differential pair signaling is popular in high-speed designs.

Related Constraints: Differential Pair Static Phase Tolerance, Differential Pair Dynamic Phase

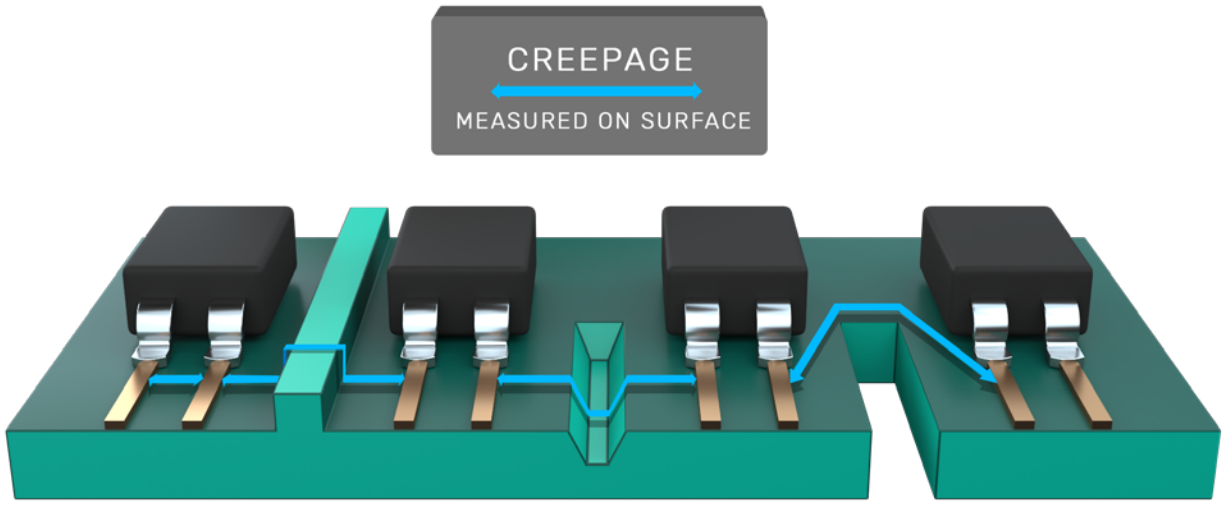
Spacing Constraints

Creepage and Clearance: Minimum Distances Between Conductive Elements to Prevent Electrical Arcing

Purpose: Defines minimum distances between conductive elements to prevent electrical arcing and ensure insulation integrity.

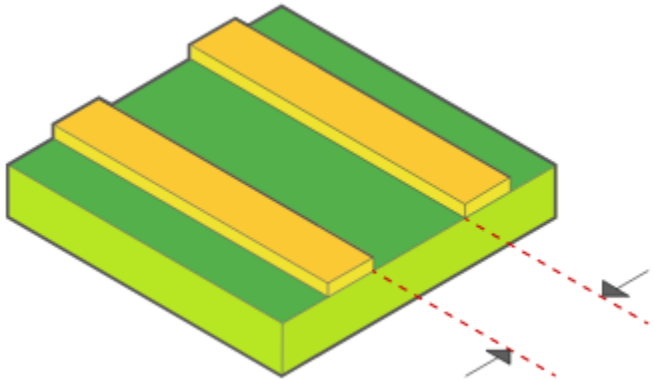


Clearance between two traces on a PCB across an air gap



Creepage between traces on a PCB surface

Cadence OrCAD X Presto PCB Editor does not support creepage and clearance rules, but Allegro X does. However, you can at least set a spacing rule to control your creepage if you don't have coatings on the PCB. Notice how it addresses spacing in this image below.



We cannot distinguish between clearance or creepage with this constraint, because coatings are not taken into account.

Therefore, this distance could be the distance midway between the creepage distance and the clearance distance, thus giving an average clearance, which could in effect violate the creepage, clearance or both.

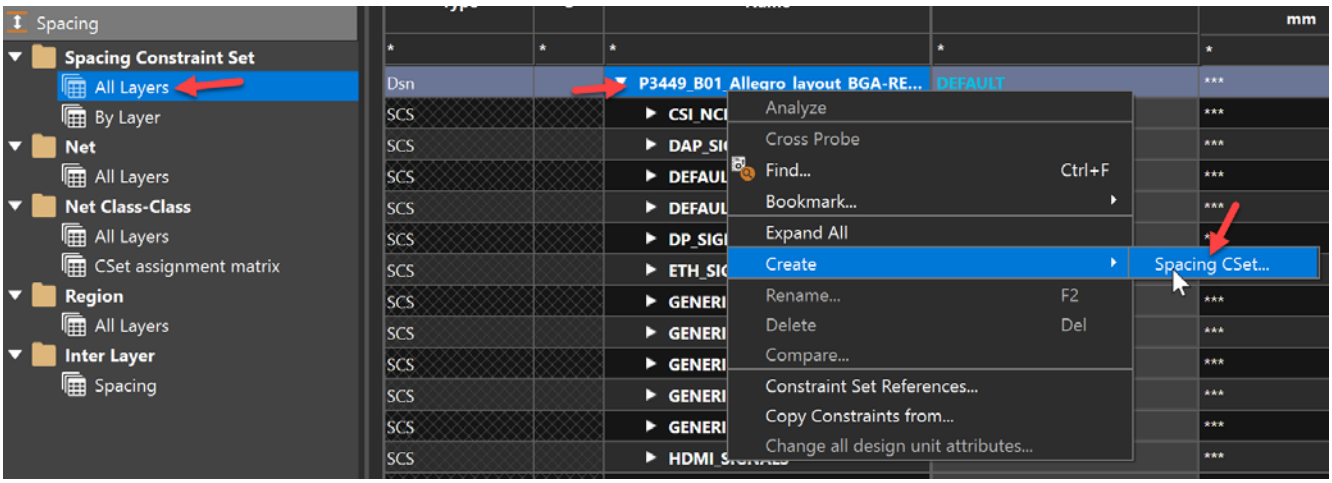
Hence, if you do use this as a substitute for creepage or clearance, consider using creepage and only when a coating is not present.

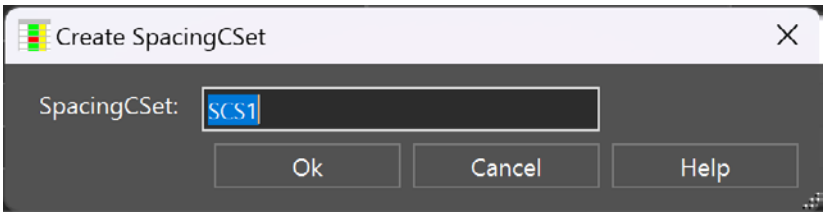
If a coating is present and you still use this constraint in OrCAD X, at least increase the distance more than usual with an acceptable tolerance to address both your creepage and clearance needs. However, using Allegro X is recommended at this stage.

Nonetheless, we need some kind of spacing rule for traces, so, to manage the spacing between traces on the PCB do the following:

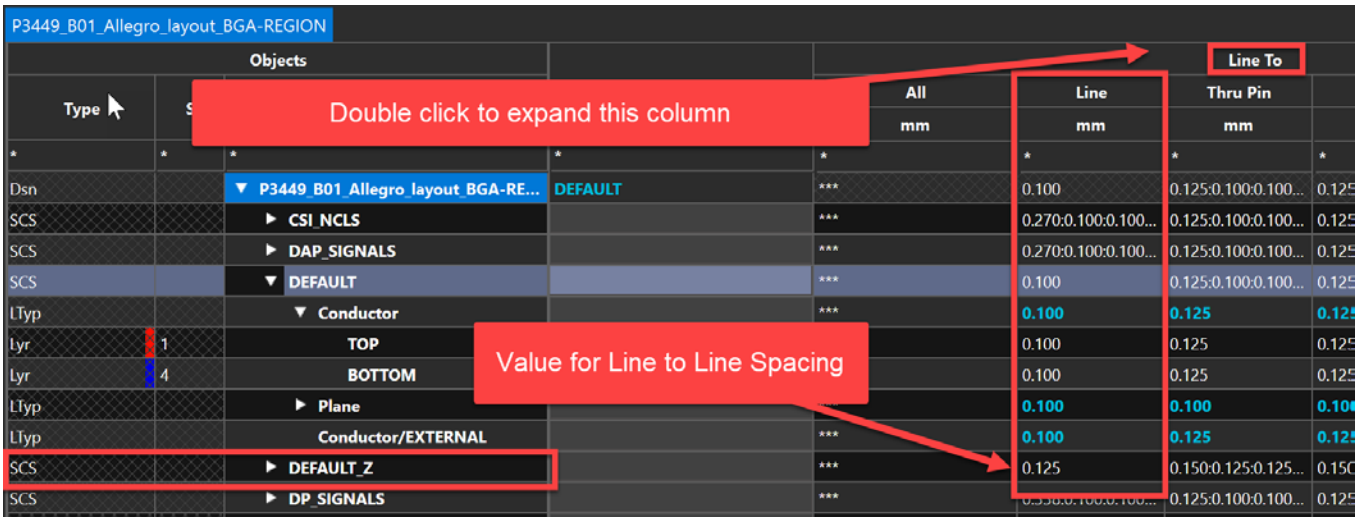
Steps

1. In Constraint Manager, create a Spacing Constraint set.



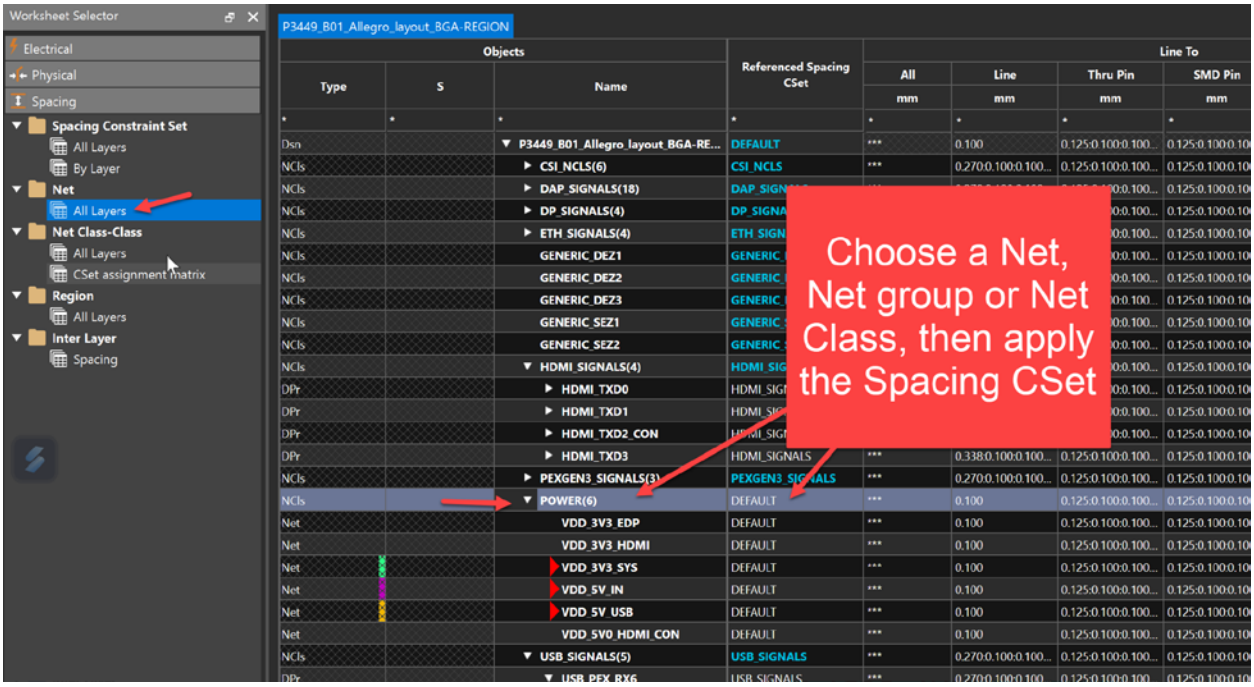


2. For that Spacing CSet (SCS), apply a value in the Line to Line column (you need to double-click and expand the Line To column at the top) for the spacing you want between the traces.



3. Apply this new Spacing CSet to your desired net, net class, group or region by selecting the appropriate worksheet in the CM, e.g. Spacing > Spacing Constraint Set > Net > All Layers.

4. Let's say you want to apply it to the Net Class named POWER(6) - Click the dropdown in the Referenced Spacing CSet column, then select your preferred spacing constraint set. In this case, we go with DEFAULT (see below).



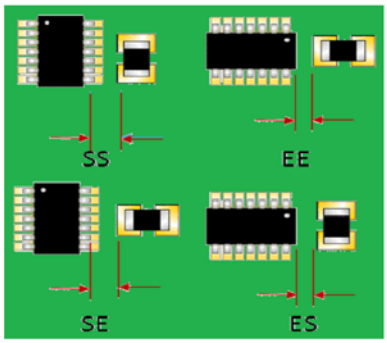
Reason: Clearance and creepage are crucial for electrical safety, especially in high-voltage designs and harsh environments. Creepage travels along the surface of the PCB while clearance involves the space between in the air above the PCB.

WARNING: As stated above, specific clearances and creepages are **not** addressed in OrCAD X. However, some kind of spacing needs to be established.

Impact: Enhances product safety, reliability, and compliance with safety standards.

Component Spacing: Minimum Distances Between Components to Avoid Interference and Facilitate Cooling

Purpose: Ensures adequate spacing between components for assembly processes and thermal dissipation.



Package to package spacing

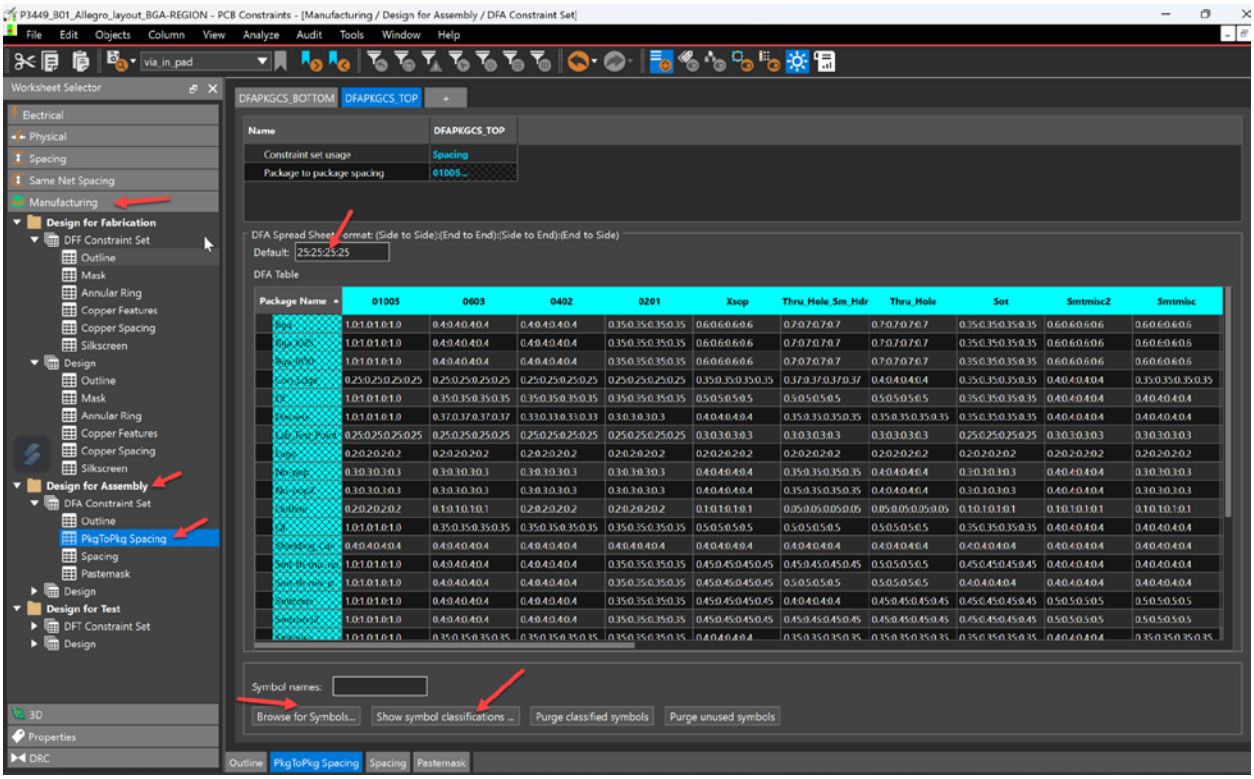
This constraint defines the minimum allowable distance between two packages with various orientations. The format of the constraint value is like "SS:EE:SE:ES", where SS stands for Side to Side, EE stands for Edge to Edge, SE stands for Side to Edge and ES stands for Edge to Side. Example constraint value may look like 10:12:20:21. Each of the distance values are captured in design unit. DRC will be reported if any two packages placed in a given orientation violates the constraint value. The constraint can be different for different type of packages, and hence a triangular matrix is used to represent constraints among different packages.

Image: Diagram showing minimum spacing requirements between different component types on a PCB. Please follow IPC 2221 for spacing requirements, i.e. Edge-to-Edge (EE), Side to Edge (SE), Edge to Side (ES) and Side to Side (SS).

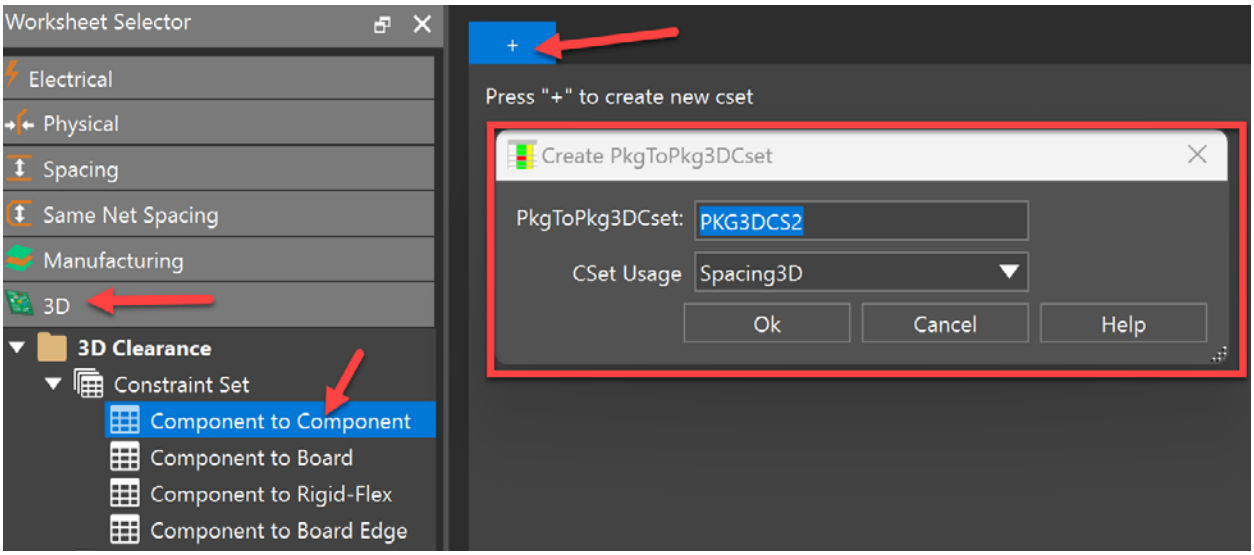
Reason: Proper component spacing is crucial for manufacturing processes and thermal management of the PCB, especially during automatic soldering processes, manual soldering, and PCB Assembly. We will address both the 2D and 3D aspects of component spacing.

Steps:

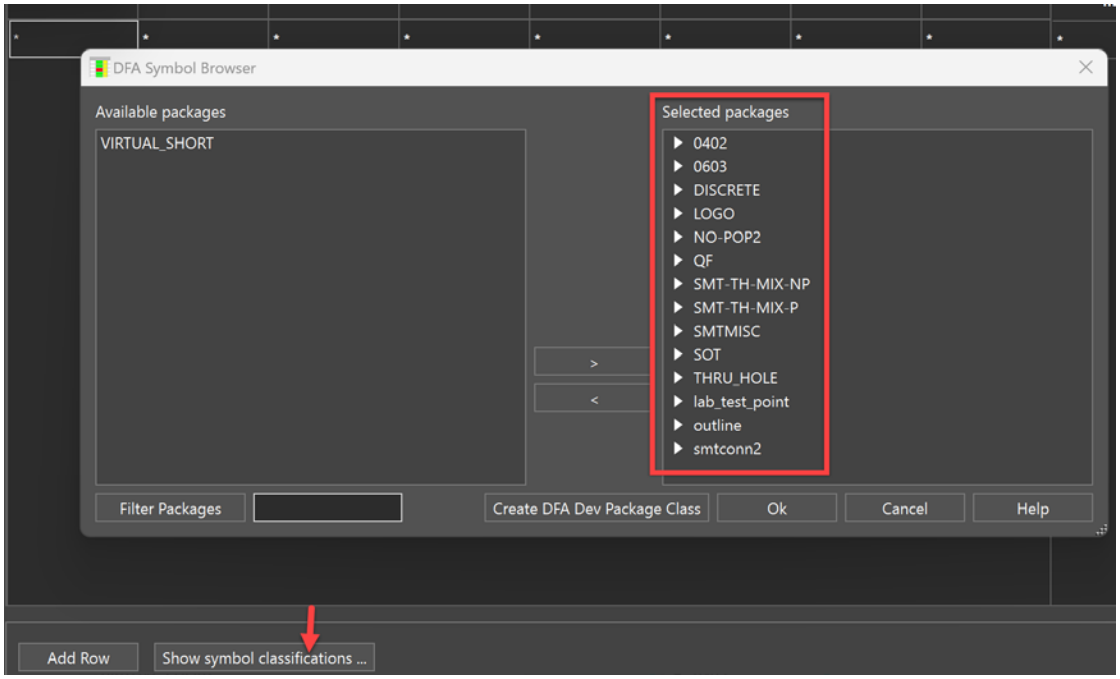
1. Open Constraint Manager.
2. Navigate to the Design for Assembly category.
3. Select the PkgToPkg Spacing section.
4. Set minimum distances between different component types (see below).



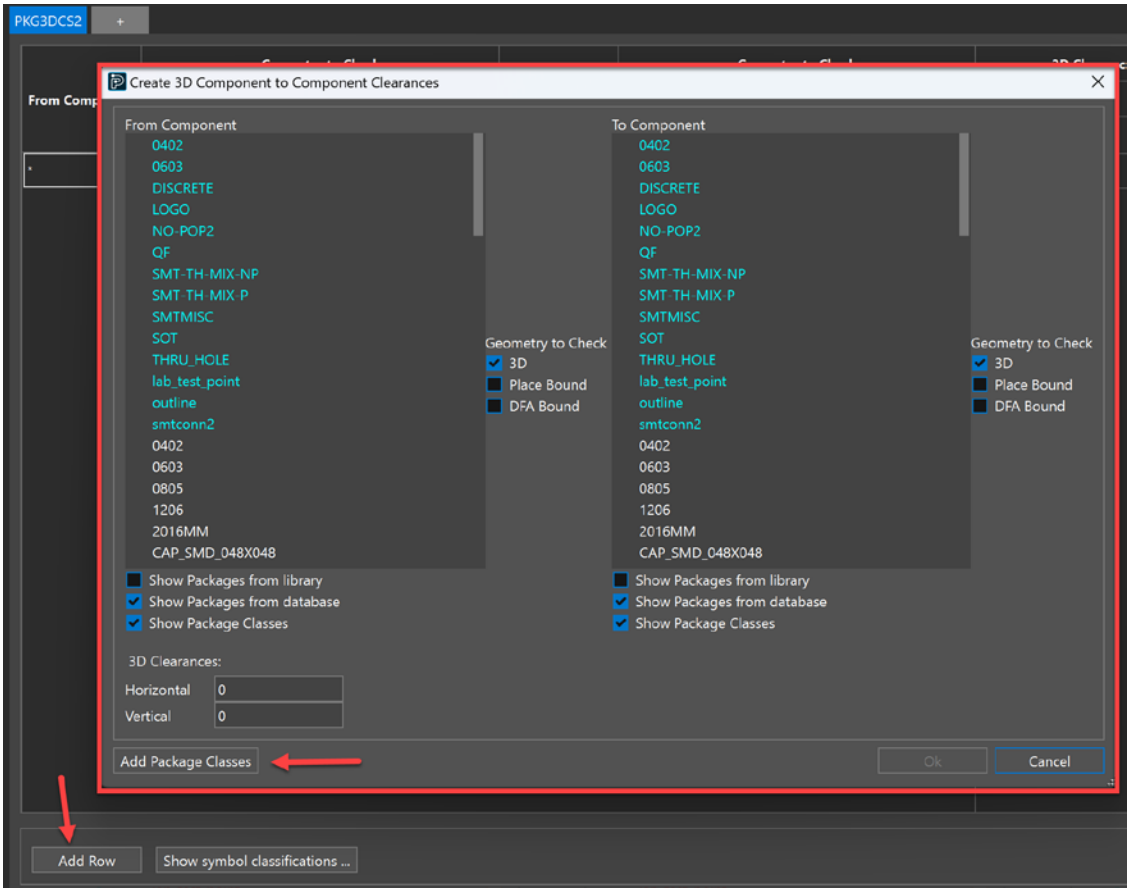
5. To set the component spacing, choose the Show symbol classifications … button at the bottom, categorize your components into different DFA Package Classes.
6. For 3D constraints, go to the Constraint Manager 3 Dimensional category and adjust component clearances.
7. Create a Package to Package 3D Constraint Set and for the CSet Usage, choose Spacing3D.



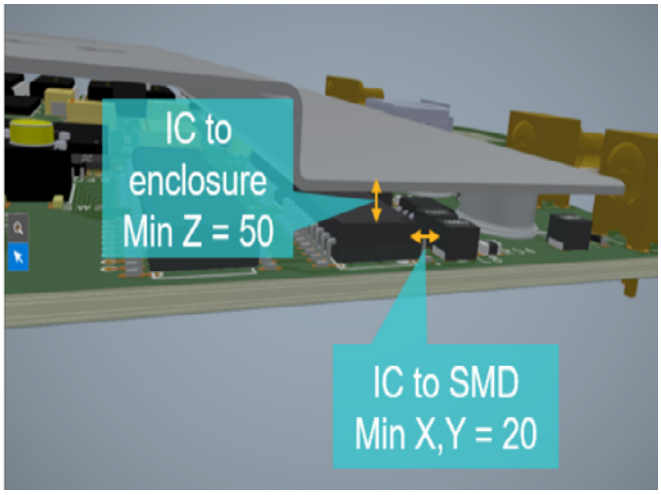
8. You can now check the symbol classifications and classify your symbols as necessary to make the next part easier (see below).



9. After symbol classification, choose Add Row to start setting up specific 3D spacing rules that meet your design requirements (see below).

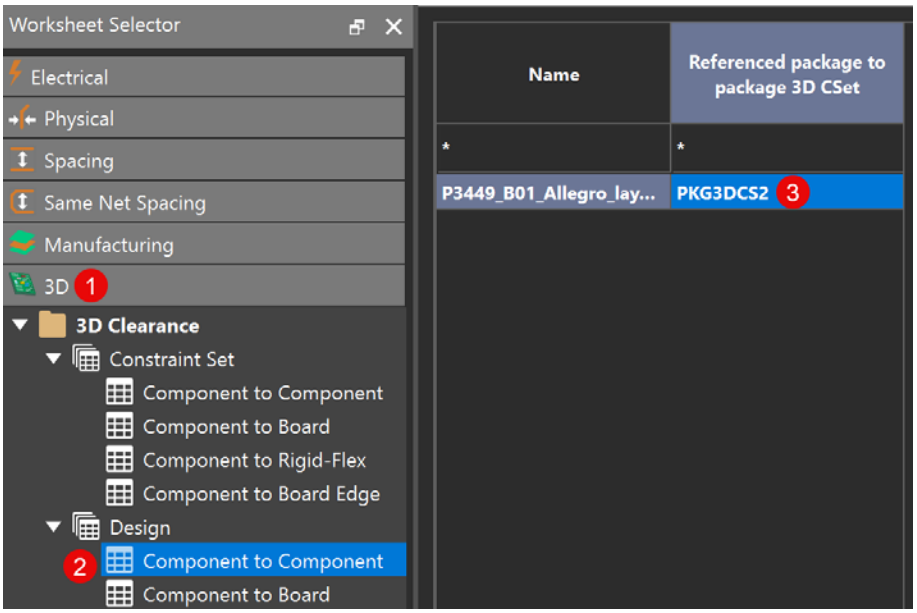


10. You can also create and sort by entire package classes to make package class to package class spacing available (it pulls up the classification list you would have created in previous steps depending on your needs). This means that as long as a component falls within a class, it will space itself a certain distance away from any component found in another component class.



Component-to-component spacing in 3D

11. Once your 3D spacing constraints have been created, you can go to the worksheet found under **3D > 3D Clearance > Design > Component to Component**, then select the dropdown option under the **Referenced package to package 3D CSet** column to apply your constraint set (shown below).



Impact: Improves manufacturability, reduces assembly errors, and enhances thermal performance of the PCB by keeping components sufficiently separate from each other to avoid overheating and other thermal related issues (proximity to other components, primarily).

Related to: Surface placement of components (top vs. bottom).

Differential Pairs Spacing (Class to Class Spacing for Crosstalk Mitigation)

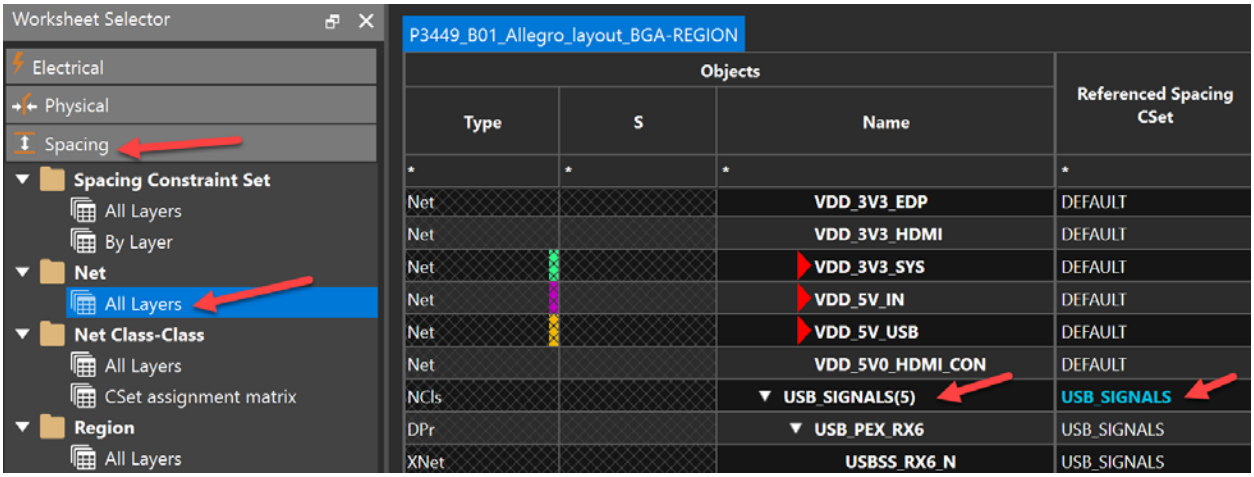
We addressed the physical constraints of differential pairs, but we must address their classes for spacing purposes so we can avoid crosstalk and signal degradation.

In this section we will analyze the spacing differences in differential pairs and how that is executed in the Constraint Manager.

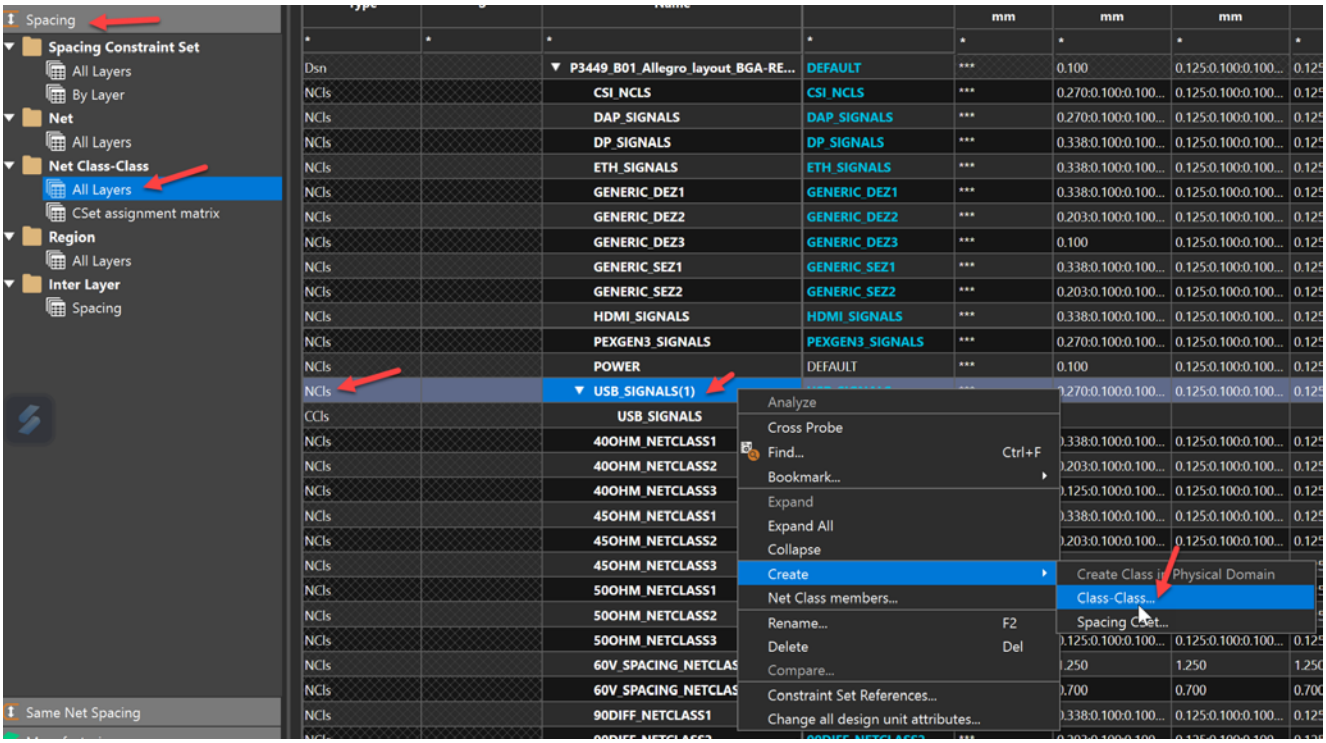
Steps:

Just like how you created a physical constraint set earlier in this guide, you can set the values for inter pair and intra pair skew. We won't make a constraint but will instead modify an existing one.

1. Open the Constraint Manager.
2. Instead of making constraint sets then applying them we will navigate to an existing applied constraint set, simply navigate to our existing Spacing Constraint set USB_SIGNALS, in the Physical Physical Constraint Set > All Layers worksheet.

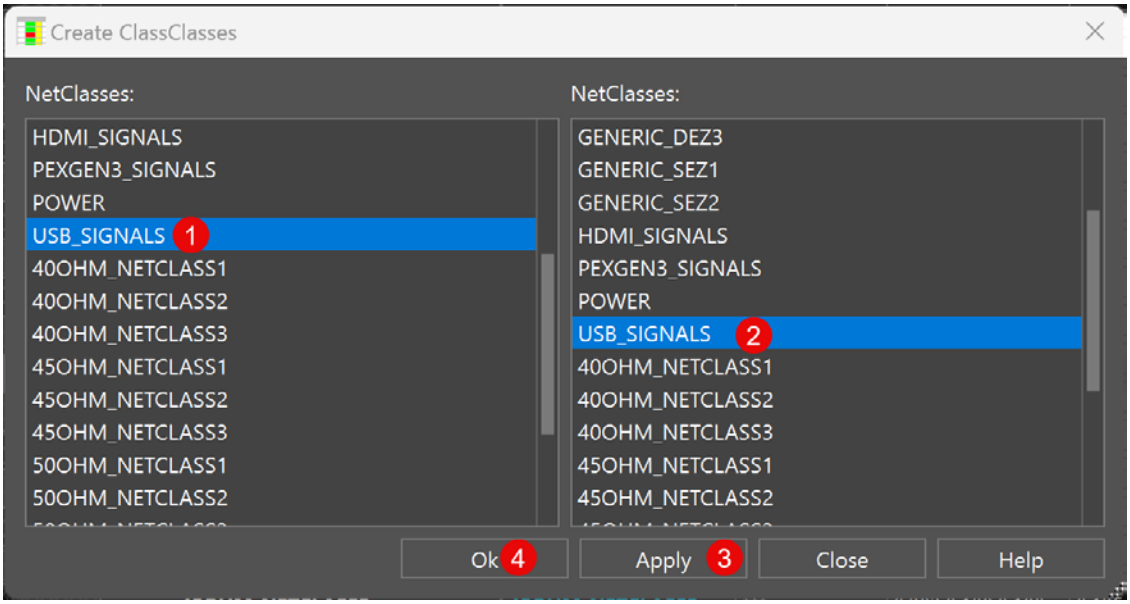


3. Notice that the USB_SIGNALS(5) cell name is a net class (shown on the far left as NCls).
4. As shown in the 3D component spacing constraint set, we can make class to class rules. Let's say we want any different pair net class to be at least 40 mils away from any other differential pair net class - go to the worksheet under Net Class-Class > All Layers, right click the USB_SIGNALS(5) Net class, then create a Net Class to Class spacing constraint (see below).

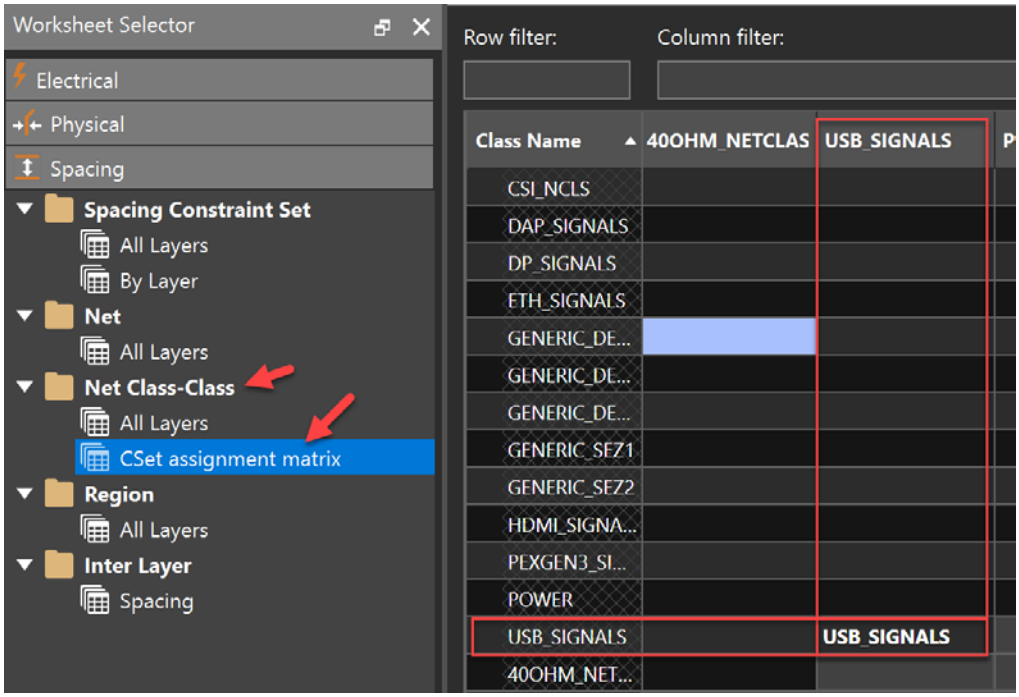


5. You will get a new window where you set the first class and then the second class you want to make rules between.

6. Choose the USB_SIGNALS net class on the left then the USB_SIGNALS net class on the right so we can make rules from USB to USB (shown below).

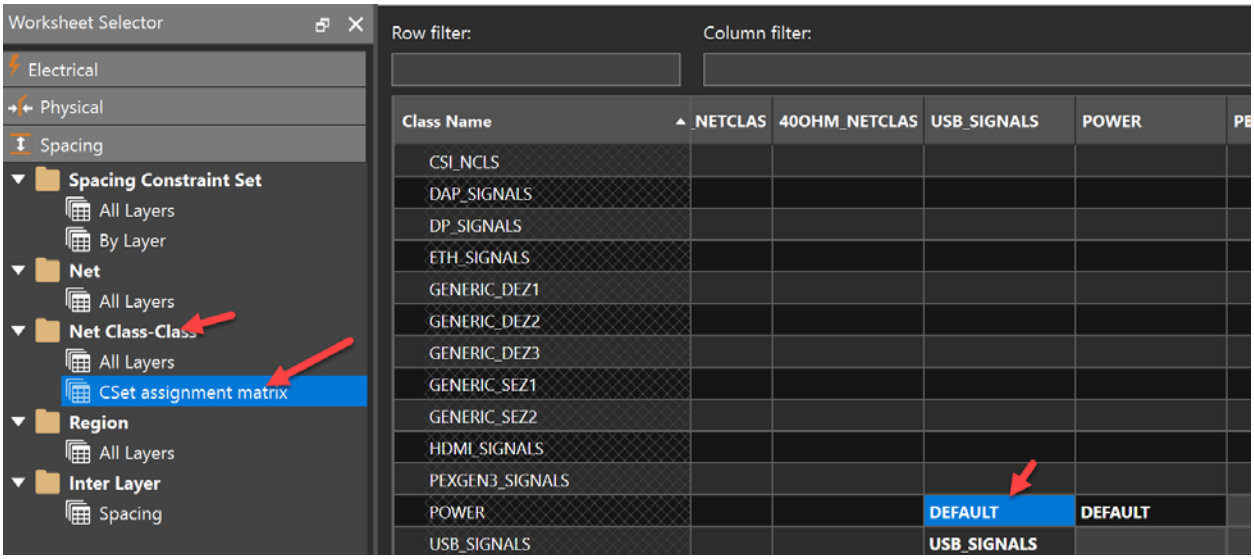


7. Click Apply, then Ok.
8. The USB_SIGNALS Net Class gets added underneath itself and is listed as a Class-to-Class constraint (CCIs). Click the cell next to it, then select USB_SIGNALS (this is the spacing constraint set, not the class).
9. Now go to the Net Class-Class > CSet assignment matrix worksheet. Scroll right until you see the classes overlapping in that matrix.



10. What this means is that any object within the USB_SIGNALS class will have USB_SIGNALS spacing constraints active in relation to any other object within the USB_SIGNALS class. This is inter pair spacing.

11. Alternatively, you can use this matrix directly to apply Class to Class spacing constraints between various classes. For example, in the POWER row, select the cell found in the USB_SIGNALS column, then choose DEFAULT.



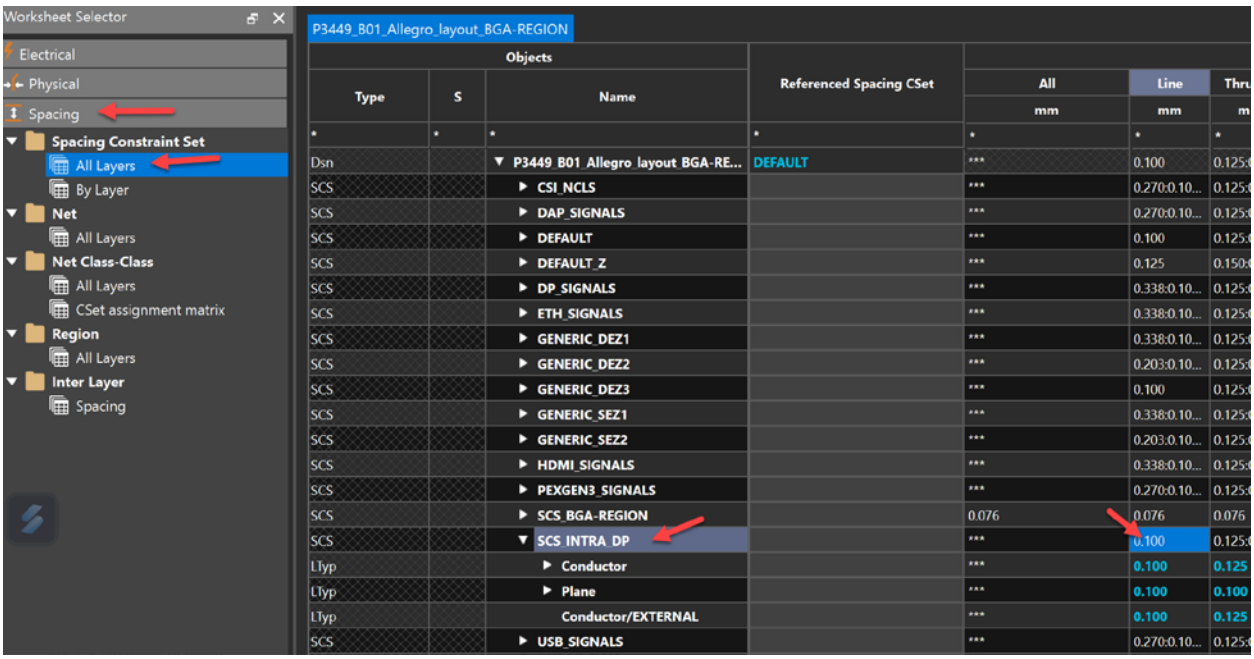
12. This will set for every net in the POWER class to be the DEFAULT rule spacing away from everything in the USB_SIGNALS class.

13. When you click on the worksheet Net Class-Class > All Layers again, you can scroll down/up to find the POWER Net class, then see that it now has rules for POWER to POWER and POWER to USB_SIGNALS.

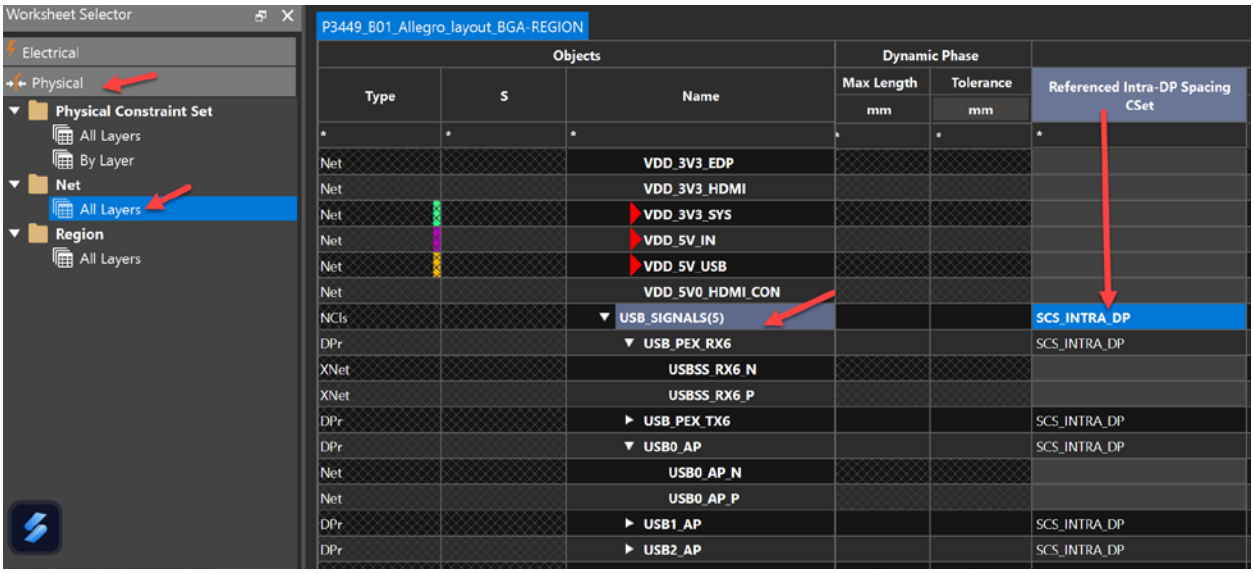
While this setting handles inter pair spacing, we also don't want these rules to cause traces and an error among themselves within their own classes. So, we need intra pair spacing.

1. Create an intra pair differential pair spacing constraint set by making a regular constraint set in **Spacing > Spacing Constraint Set > All Layers**. Right-click the top Dsn cell, Create Spacing Constraint Set, and name it **SCS_INTRA_DP**.

2. Once created, you can set the **Line To Line** spacing and other parameter values as you would like.

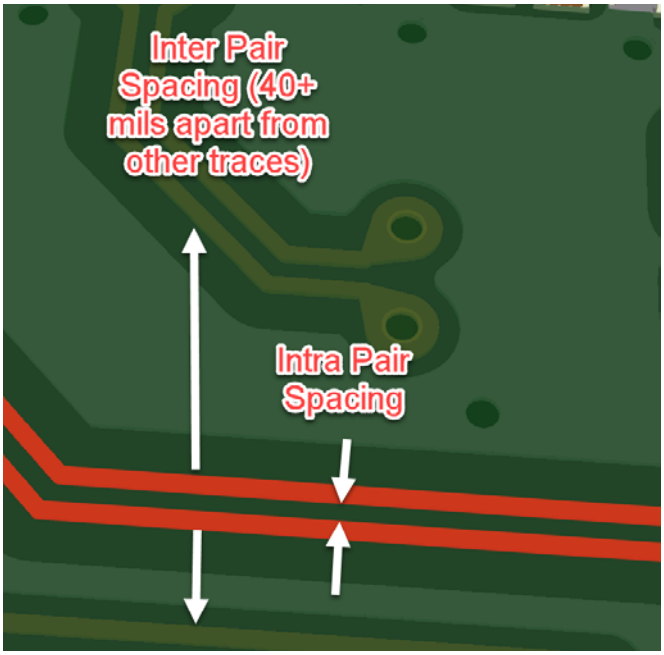


3. Return to the Physical > Net > All Layers worksheet, find USB_SIGNALS(5), scroll horizontally down to the **Differential Pair** > **Referenced Intra-DP Spacing CSet**, select the drop down cell and choose the spacing constraint set we just created, SCS_INTRA_DP.



4. Now our differential pairs within the USB_SIGNALS class have their own spacing constraints for their inner traces.

Visually we're talking about what you see in the image below:



Reason for these Constraints: We want to avoid other signals (whether differential pair or not) from creating crosstalk on our differential pairs. We achieve that by spacing them far enough apart and enforcing that spacing rule. However, the traces within the differential pairs themselves need to be close to each other, so they have their own special intra pair spacing constraint, which is shown in the image above. This intra pair spacing constraint makes it so the differential pairs don't violate their own spacing rules.

Impact: Reduced chances of crosstalk by preventing the designer from allowing signals to get too close.

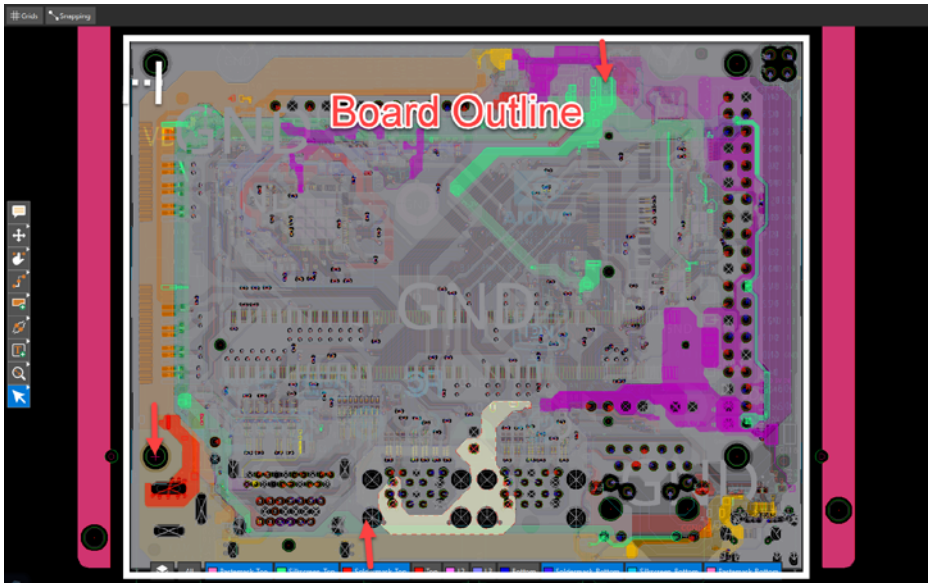
Related Constraints: Class to Class Spacing, Net Class Spacing Constraints

Manufacturing Constraints

Fabrication Tolerances: Allowable Variations in Dimensions for Manufacturing

Here is a list of common fabrication tolerances for PCB manufacturing, excluding silkscreen and solder mask, that can be addressed in the Constraint Manager. For a complete list, please refer to the Appendix section of this document.

Board Outline Dimensions: Tolerances for Overall Board Size and Shape



Purpose: To define the physical boundaries of the PCB and objects near it.

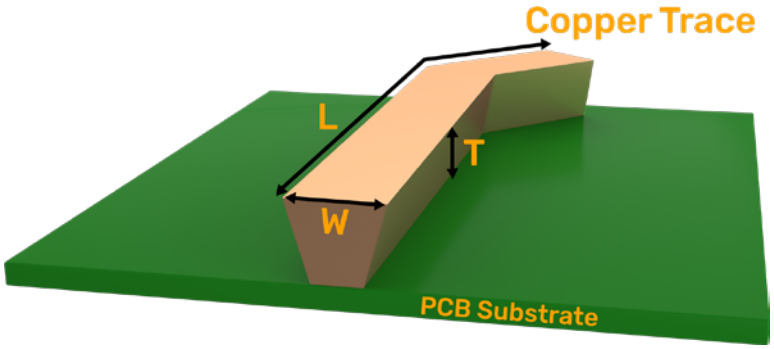
Impact: Creating proper constraints for board-edge ensures that all components and traces fit within the specified board dimensions, crucial for manufacturing and assembly, especially for panelization of multiple board designs from one copper sheet.

Steps:

You can set various outline-to-object rules within a constraint set. To do so:

1. Open the Constraint Manager.
2. Go to Manufacturing > Design for Fabrication > DFF Constraint Set > Outline spreadsheet.

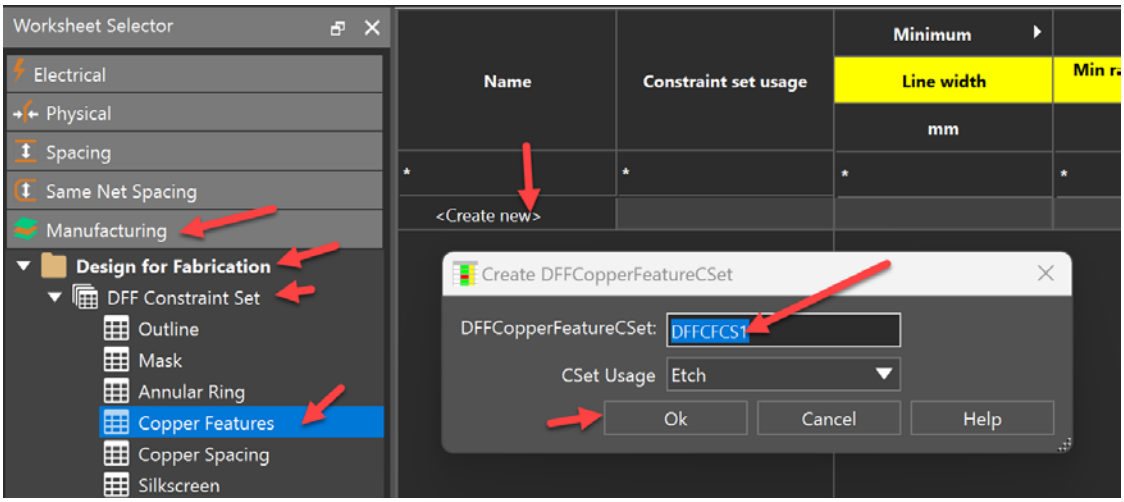
Trace Width for Manufacturing: Minimum Copper Width for Traces



Conductor/Trace width on a PCB

Steps:

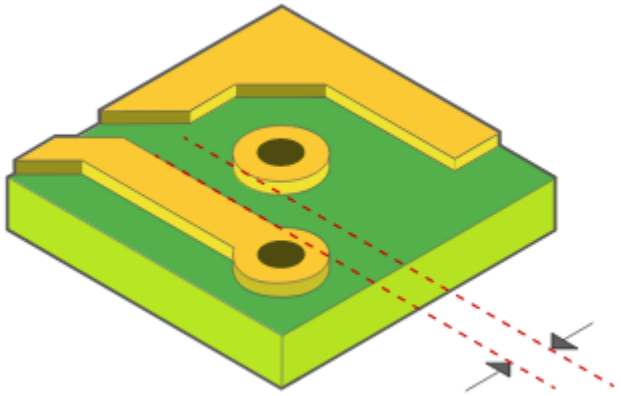
1. Open the Constraint Manager.
2. Go to the worksheet shown below.



3. Left click <Create new> and the Create DFFCopperFeatureCSet will appear.
4. Click Ok.
5. In the Line Width column, set the minimum to what your manufacturer can make within the allowed budget (4 mils, 0.102 mm).

Note: This manufacturing rule may seem redundant if we already set the trace width in the Physical Constraints section. However, not all manufacturers have the same criteria. We want to be able to have our design without influence from the manufacturer's capabilities. We also want a modular way to swap out manufacturers without having to change our original design trace widths every time. Hence the 'redundancy'.

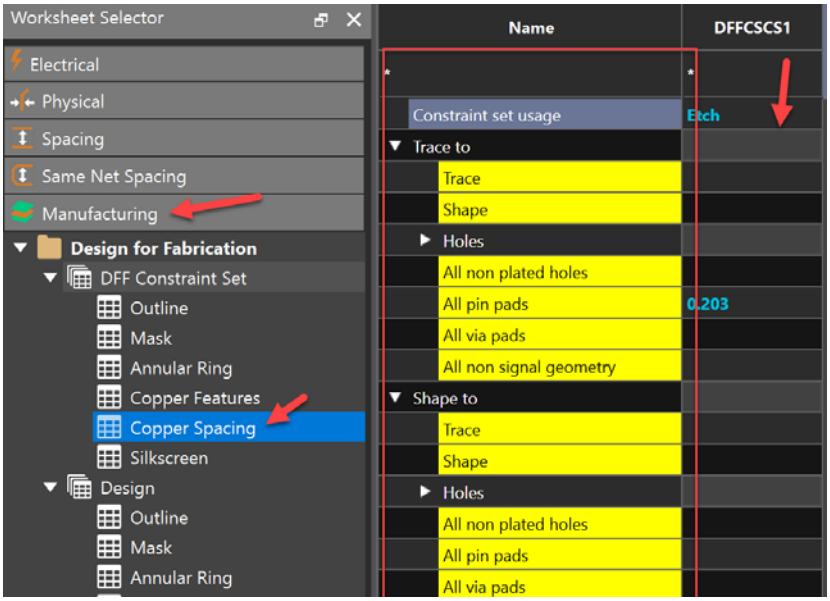
Trace Spacing: Minimum Distance Between Copper Features



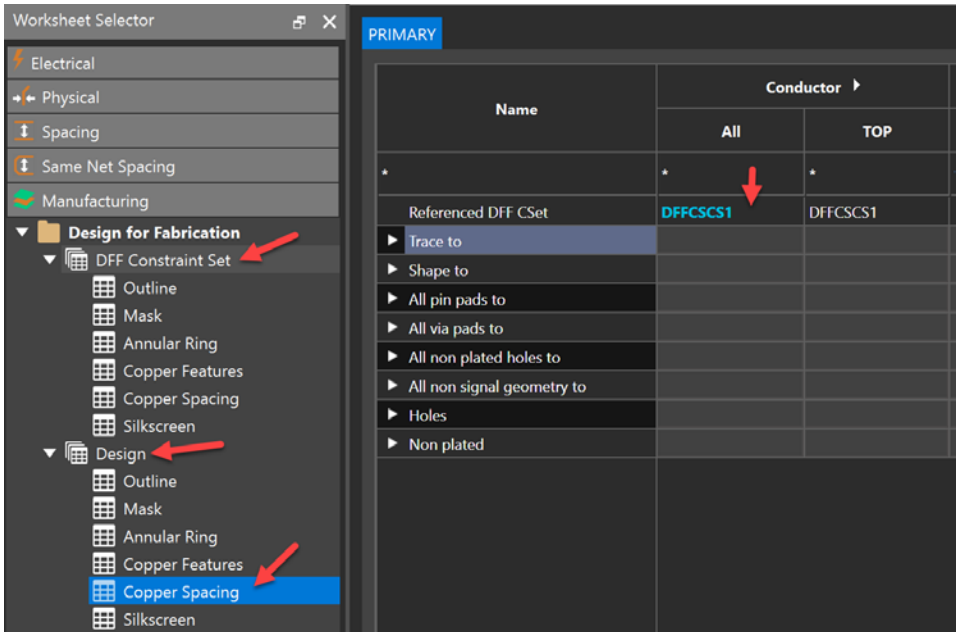
Copper feature distances from each other

Steps:

1. Open the Constraint Manager.
2. Navigate to the Manufacturing > Copper Spacing worksheet.
3. Click New CSET and name it, then click Ok. You will get a window like below if you expand the rows.



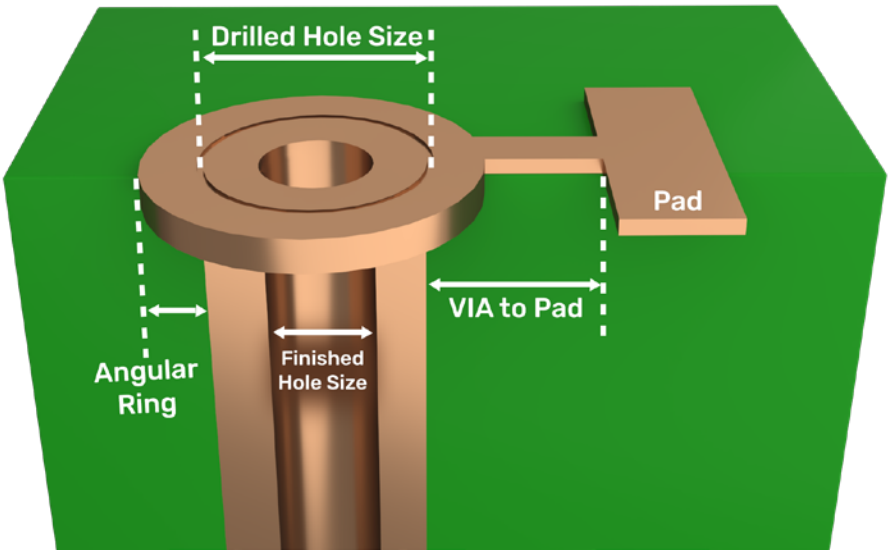
4. There are way too many copper to copper spacing features to demonstrate here, but feel free to set rules for anything your manufacturer is capable of doing.
5. The final step is to choose this constraint set and **apply** it to your Design. Navigate to the worksheet, Manufacturing > Design for Fabrication > Design > Copper Spacing.
6. Click the dropdown cell under the **Conductor - All** column.
7. Select the constraint set we just created. It will apply all the rules you wanted to add for spacing constraints for your manufacturer (DFFCSCS1).



Impact: By applying these robust sets of rules to your design, you will make your manufacturing DFM CAM engineers happy by designing **with** DFM spacing instead of it being an afterthought post layout. Proper spacing reduces the chances of unintended shorts from copper slivers on the PCB.

Annular Ring: Minimum Width of Copper Surrounding a Hole

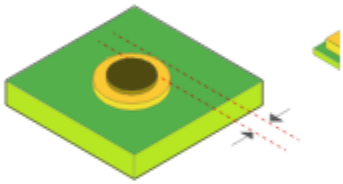
Purpose: Defines the minimum width of copper surrounding a drilled hole to ensure proper electrical connection and mechanical strength.



Cross-sectional diagram of a via showing the annular ring measurement

Pin Hole to Pad

Checks the minimum distance of the pin padstack hole from the outermost edge of the pad geometry.



Legal Values: Design Units
DRC Code: oP
Applicable Objects: DFFAnnularRingCSet
Attribute Name: DFF_AR_PNHL_TOPD

Diagram showing annular ring (pad hole edge to pad edge).

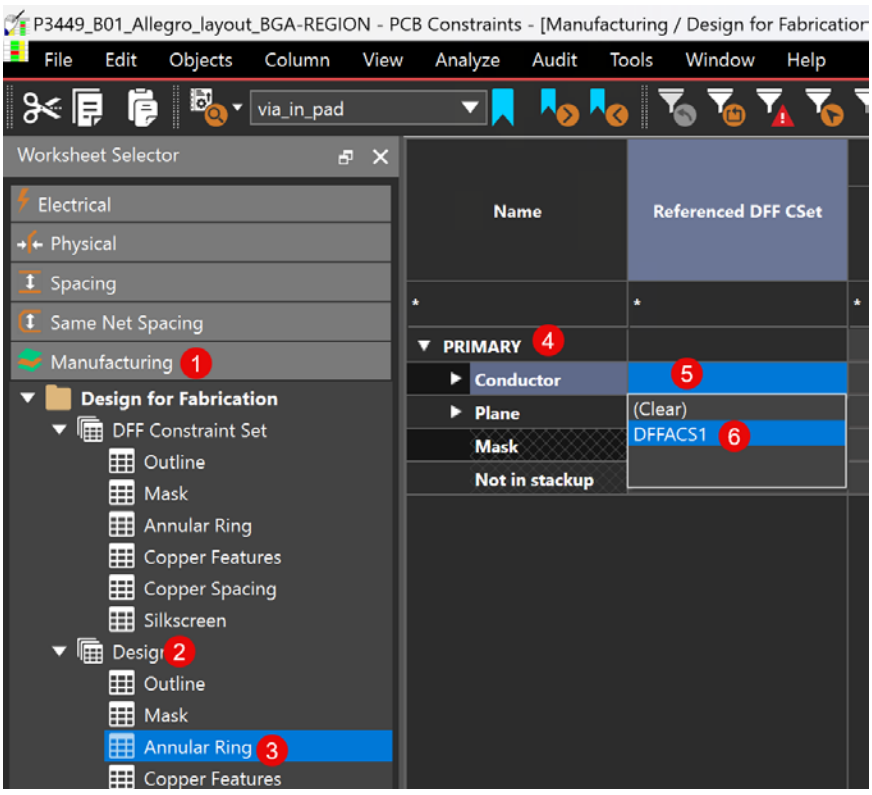
Steps:

1. Open Constraint Manager.

2. Navigate to this worksheet shown in the image above: Manufacturing > Design for Fabrication > DFF Constraint Set > Annular Ring.
3. Create a DFFConstraint Set by clicking <Create new>.
4. Choose a name for this Design for Fabrication Annular Ring Constraint Set (DFFACS1).
5. Set the Hole to pad dimension to whatever your manufacturer recommends for the Annular ring or drill hole edge to edge of pad spacing (e.g. below is 5 mils = 0.127 mm).

Name	Constraint set usage	All pins			All vias		
		mask	Hole to pad	Hole to antipad	Missing mask	Pad to mask	Hole to pad
			mm	mm		mm	mm
	*		*	*	*	*	*
<Create new>							
DFFACS1	Etch		0.127				0.127

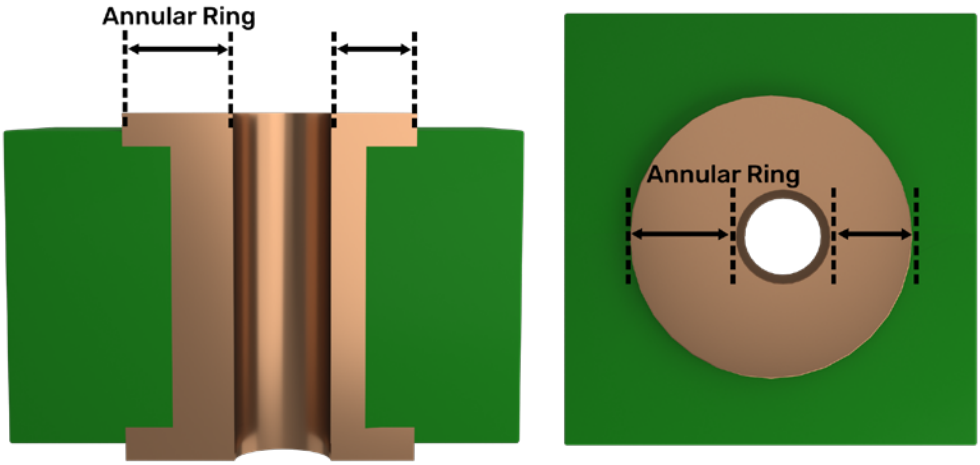
6. Now apply this DFFACS1 constraint set to the Design. Go to Manufacturing > Design > Annular Ring worksheet.



7. Expand the PRIMARY Cell, then to the right of the Conductor Cell, choose the above constraint set and apply it (DFFACS1).

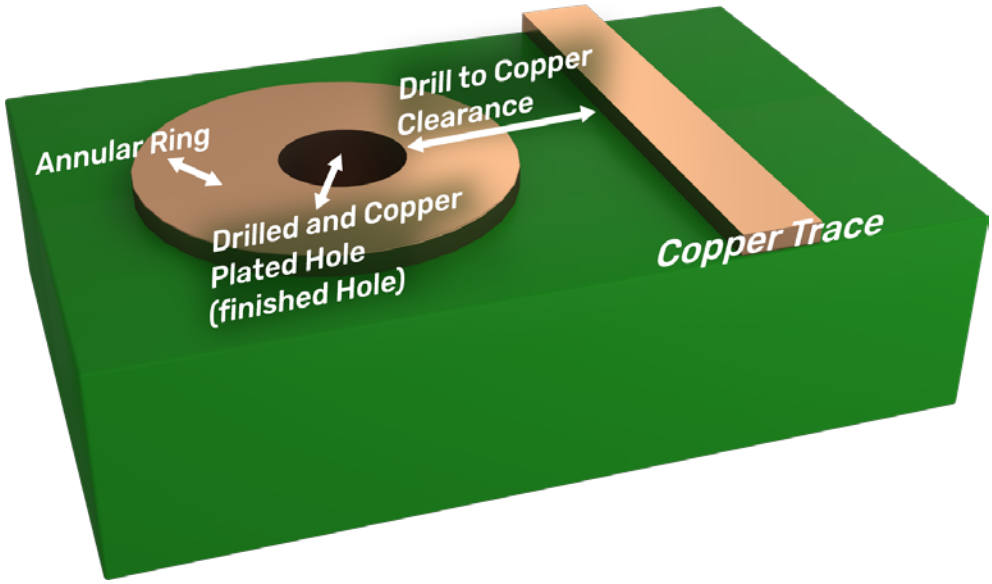
Now your pads and vias will throw a design rule error if they have any less than 5 mils (0.127 mm) of Annular ring available.

Reason: Ensures reliable connections between layers and prevents manufacturing defects like breakouts.



Impact: Affects manufacturability, reliability, and overall PCB performance. Pads may rip up. The board may result in incomplete connections and a non-functional mess of circuitry.

Drill to Copper Spacing

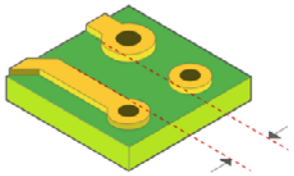


Top view of a pad with drill hole edge to copper trace edge spacings

Purpose: Defines the minimum distance between the edge of a drilled hole and the nearest copper feature to prevent manufacturing issues and ensure manufacturing reliability by preventing short circuits. May even require X-ray analysis through the PCB to adjust for scaling of PCB size and layers.

Trace to Pin Pad

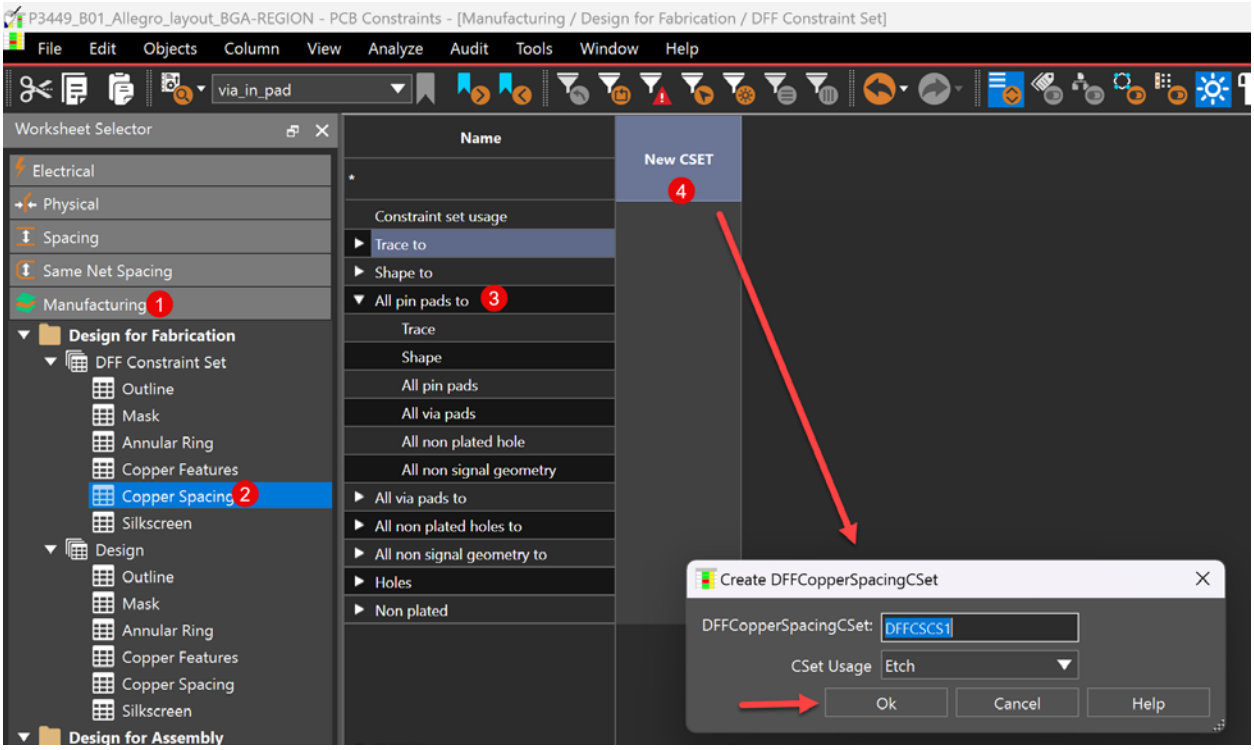
Checks the spacing between copper-object trace and pin pad.



Legal Values: Design Units
DRC Code: tp
Applicable Objects: DFFCopperSpacingCSet, DFFCopperSpacingAcceptableCSet
Attribute Name: DFF_CS_TRCTO_PNPD

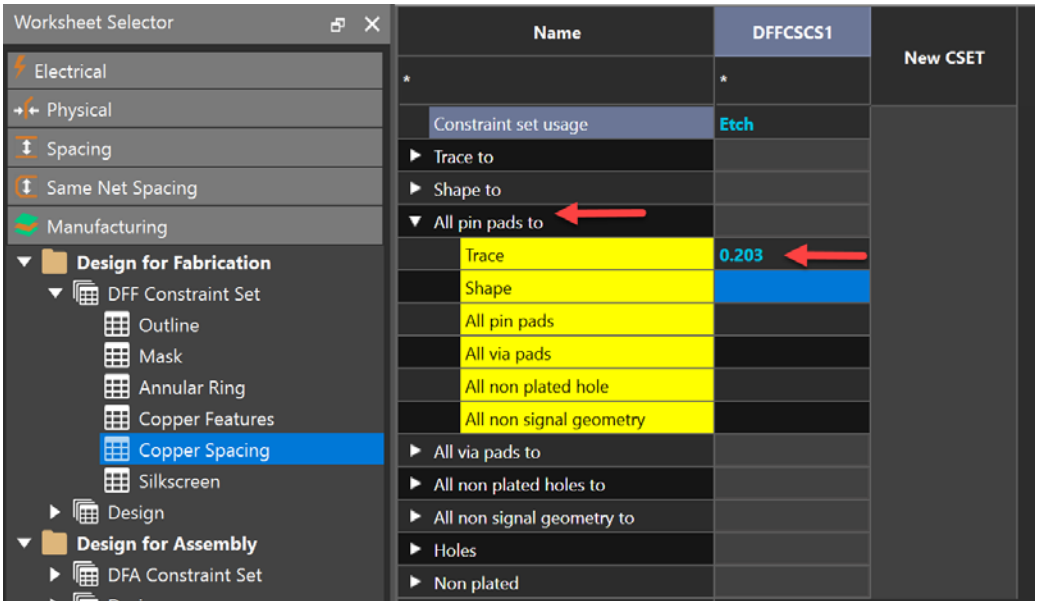
Steps:

1. Open the Constraint Manager.

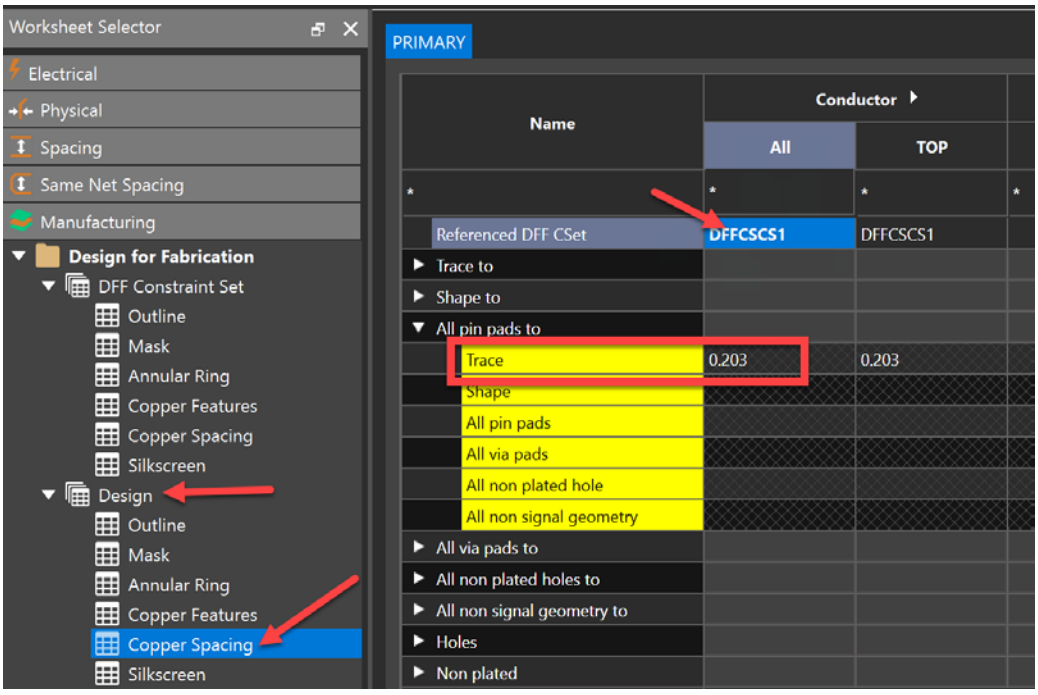


2. As shown above, navigate to the Manufacturing Constraints section > Design for Fabrication > DFF Constraint Set > Copper Spacing spreadsheet.
3. Look for a setting called All pin pads to > Trace.
4. Add a new Fabrication Constraint Set by clicking on the New CSET column.
5. You get the Create DFFCopperSpacingCSet window.
6. With the options above (CSet Usage = Etch), click Ok.

7. The Constraint Set will create a column where you can populate values (see below).



8. Set the minimum clearance value (typically 8 mils (0.2032 mm), as per Sierra Circuits manufacturer recommendation).
9. Apply the constraint to the entire design by going to Manufacturing > Design for Fabrication > Design > Copper Spacing.



10. Then in this spreadsheet, in the All column, set the 'Referenced DFF CSet' field to the one we just created (DFFCSCS1).
11. The value for the 'All pin pads to Trace' rule will populate (0.203 mm / 8 mils) as intended.

Now all pin pads will flag an error in the PCB design rule check if closer than 8 mils to a trace.

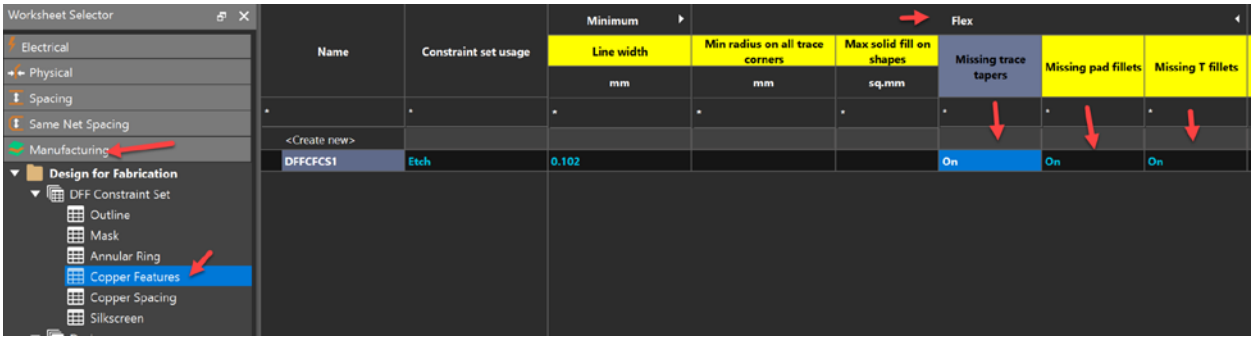
Impact: Adequate spacing helps prevent issues like short circuits or weakened connections due to misalignment during drilling. Therefore getting this correct ensures manufacturability, improves yield, and enhances the overall reliability of the PCB.

Teardrops (Fillets)

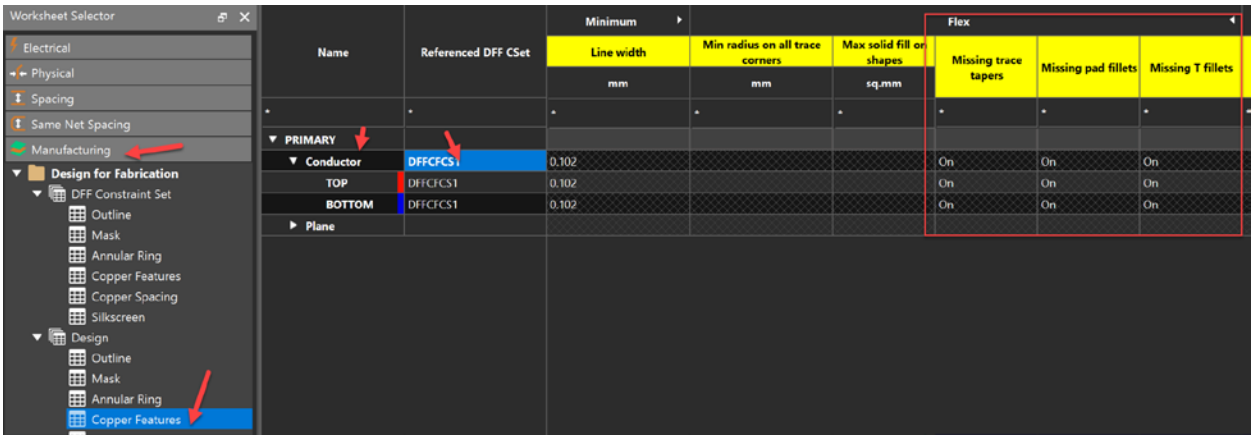
Purpose: Ease the stress on copper traces and pads, especially for signal integrity and flex PCBs.

Steps:

1. Open the Constraint Manager and go to the worksheet in Manufacturing > Design for Fabrication > DFF Constraint Set > Copper Features.
2. Then you can see a constraint set (or create one similar to previous methods).
3. Under the Flex section, you have options for turning on the checks for **Missing pad fillets** and **Missing T fillets** and **Missing trace tapers** (see below).



4. Apply the constraint set by clicking the **Design > Copper Features** worksheet below.
5. Then you will already have the DFFCFCS1 constraint set applied to your Conductor layer (or you can apply it), and the values for the fillets will populate if you have any to add.



If any fillets (Teardrops) are missing, especially for flex PCBs, you know where to add them because the DRC tool flags an error if they're missing.

Impact: More reliable pads and traces, less breakage and damage on regular and flex PCBs after bending, and improved signal integrity by reducing the abrupt change in characteristic impedance.

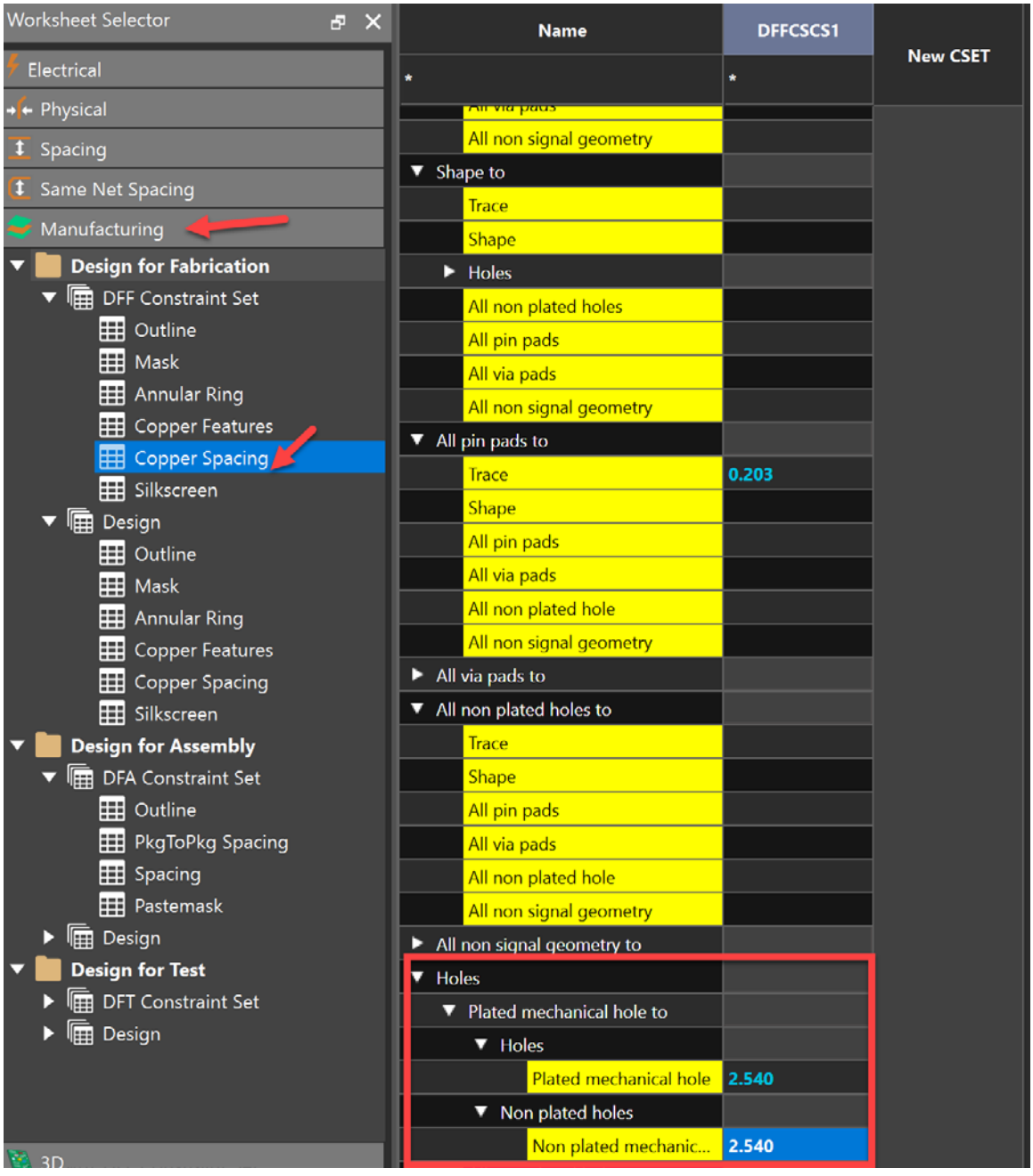
Pad To Mounting Hole Spacing: Minimum Distance Between Pads and Mounting Holes

Purpose: You want to avoid placing traces to mounting holes to avoid unintended shorts. Mounting holes often have metal bolts/screws used to mount the PCB which may or may not be connected to ground or some signal or power. By ensuring the mounting holes are far enough away from your traces and pads, you reduce the chance of unintended shorts and a smoking PCB.

We won't explore the entire procedure but will just highlight where to find the constraint set option and where it can be applied.

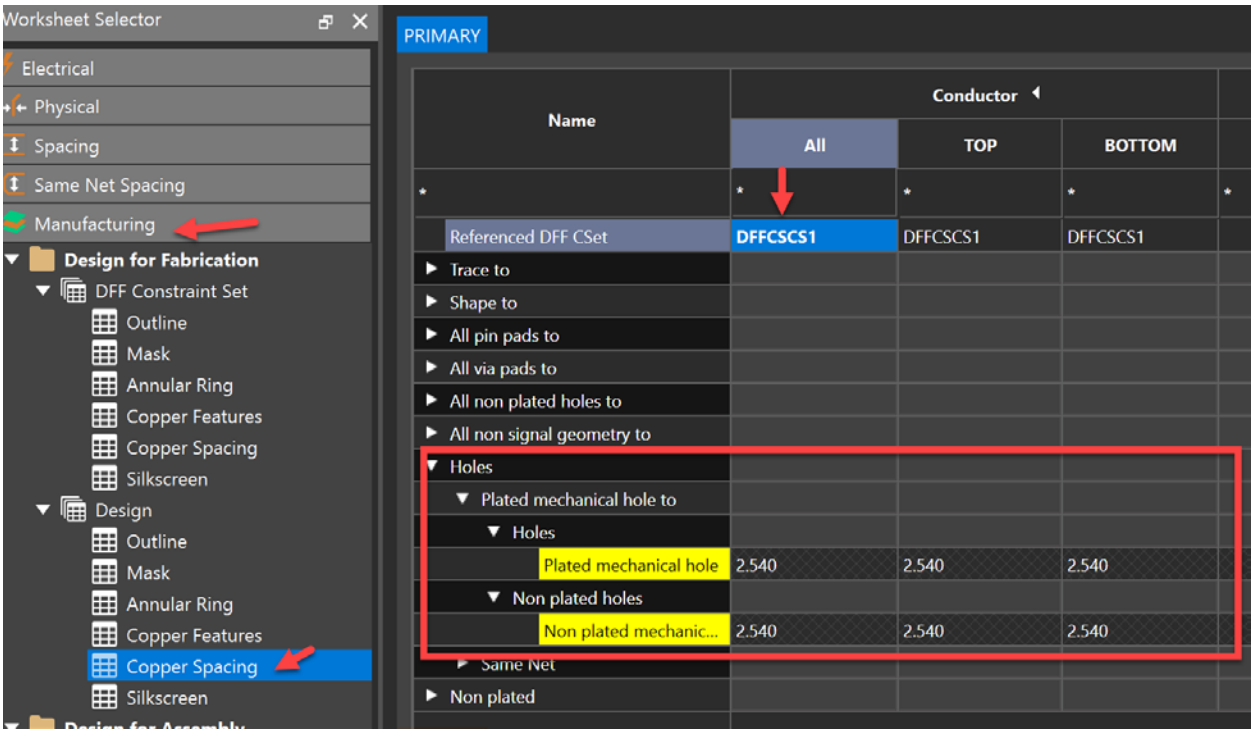
Constraint Set Category

1. Manufacturing > Design for Fabrication > Copper Spacing.
2. Create the constraint set by clicking in the New CSET column, then name it and click Ok.
3. Set values in the categories below:
   a. Holes > Plated mechanical hole: Set to desired value (e.g. 100 mils or 2.540 mm).
   b. Non plated holes > Non plated mechanical hole: Set value (e.g. 100 mils or 2.540 mm).



Where to Apply It

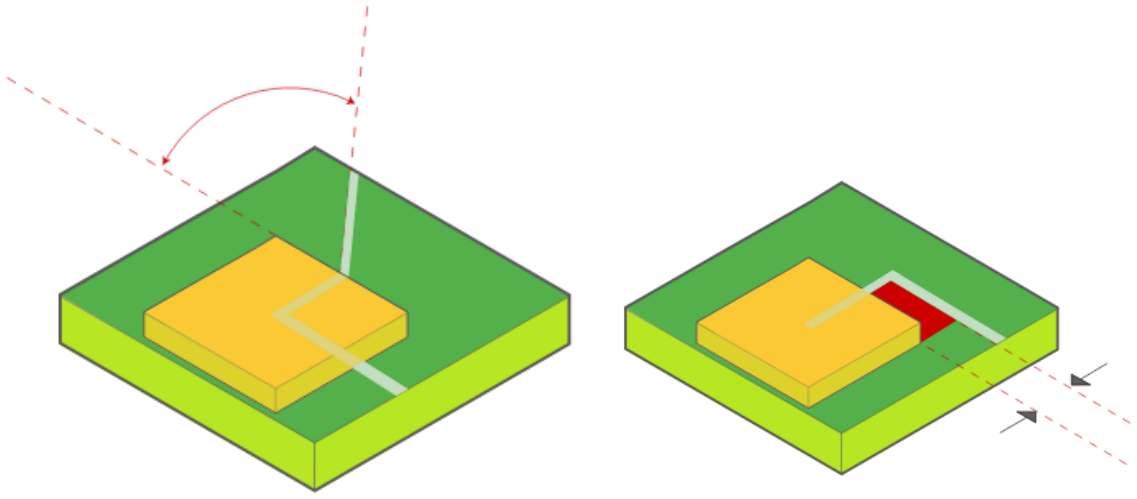
As per the image below, you would apply your mechanical hole spacing constraints in the Design > Copper Spacing worksheet. Select the rule in the dropdown option, and you will see that they are applied (expand the **Holes** row if they are not visible).



Downstream Impact: Fewer short circuits to your mounting chassis, cables, etc. Fewer concerns during testing.

Acid Traps: Avoiding Acute Angles in Copper Features That Can Trap Etching Chemicals

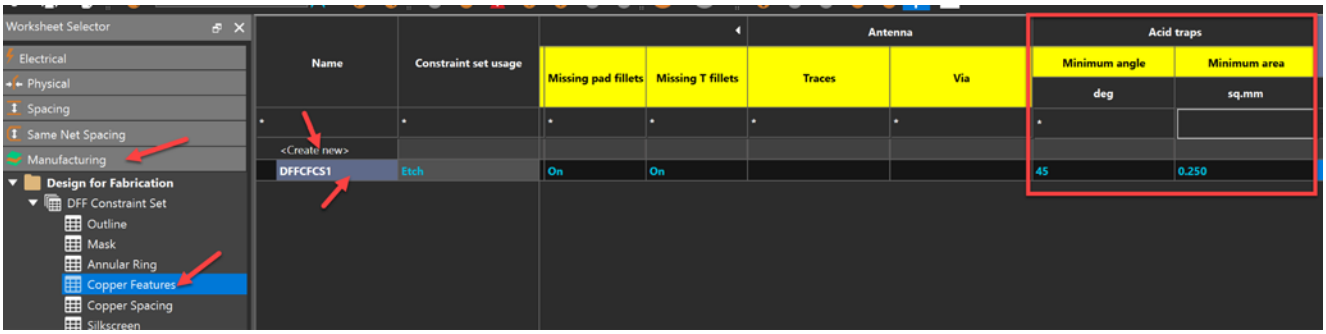
Purpose: While many manufacturers have updated their processes to avoid acid traps regardless of copper angles, some manufacturers can still have this problem. You can use the constraint manager to check for unintended acid traps.



Potential spacing issues that can commonly create acid traps

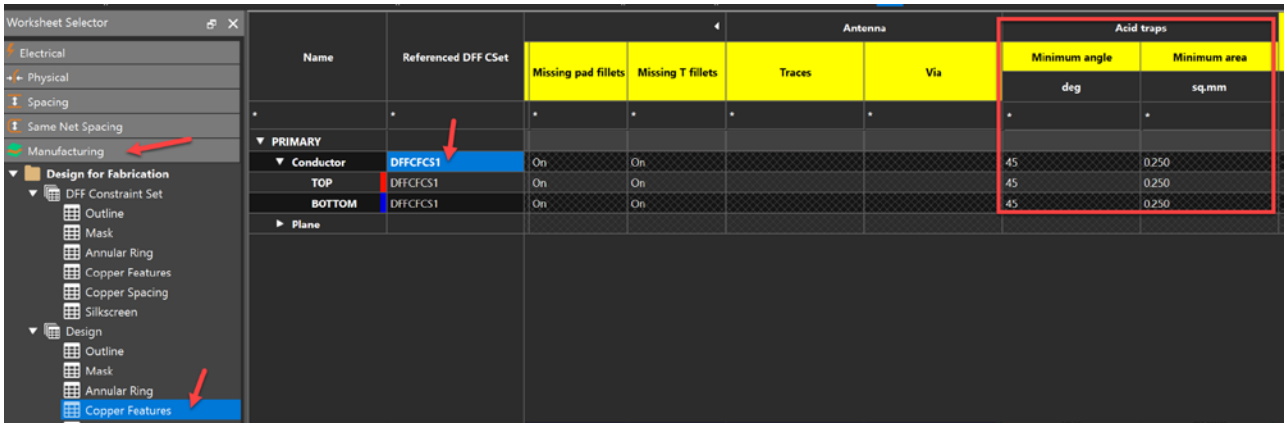
Where to find the Constraint Set

1. In the constraint manager, go to Manufacturing > Design for Fabrication > Copper Features.
2. Choose <Create new> for your desired constraint set and name it, then click Ok.
3. You can then set your values in the Acid Traps column under Minimum angle (45 degrees or less is typical) and Minimum area (entirely up to your design). See the example below.



Where to Apply the Constraint Set

1. Go below this section to Design > Copper Features.
2. Click the dropdown next to Conductor to choose your desired DFFCFCS1. Notice that the rules for Acid traps get applied to your Conductor layer.

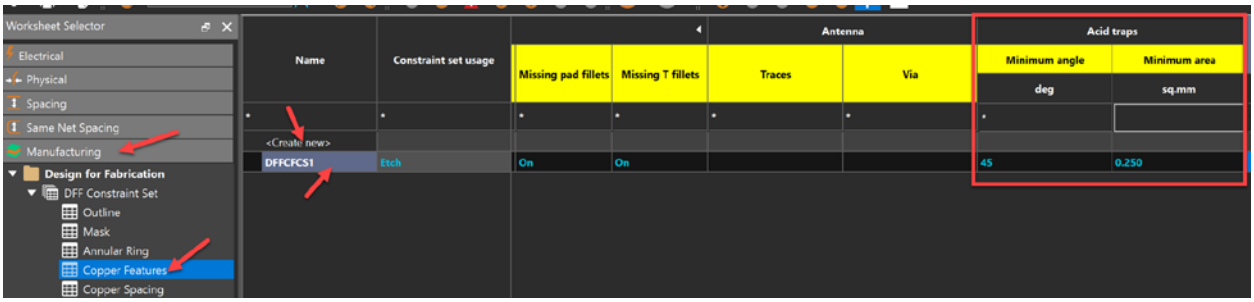


Minimum Copper Area: Smallest Allowable Area of Isolated Copper Features

Purpose: Avoid unintended copper slivers. Slivers are hairline shavings of copper that can cause unintended shorts on the PCB and are very challenging to detect without full testing of the board and can often be intermittent.

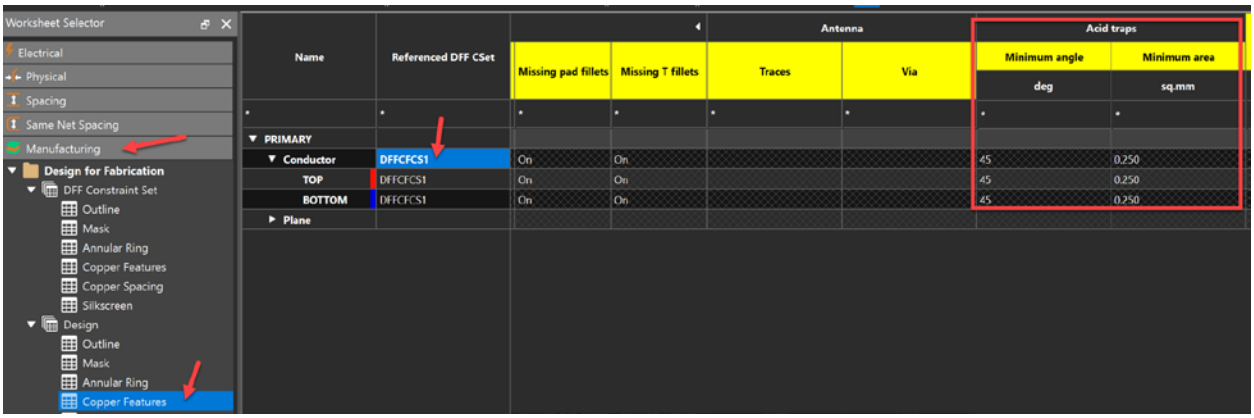
Where to Find:

Similar to the steps in the Acid traps section, minimum copper area can be set as well. Please refer to that section for Acid traps.



How to Apply

Check the Acid Traps section and follow the same steps, but apply to the Minimum area instead.



Assembly Constraints: Rules for Component Placement, Orientation, and Soldering

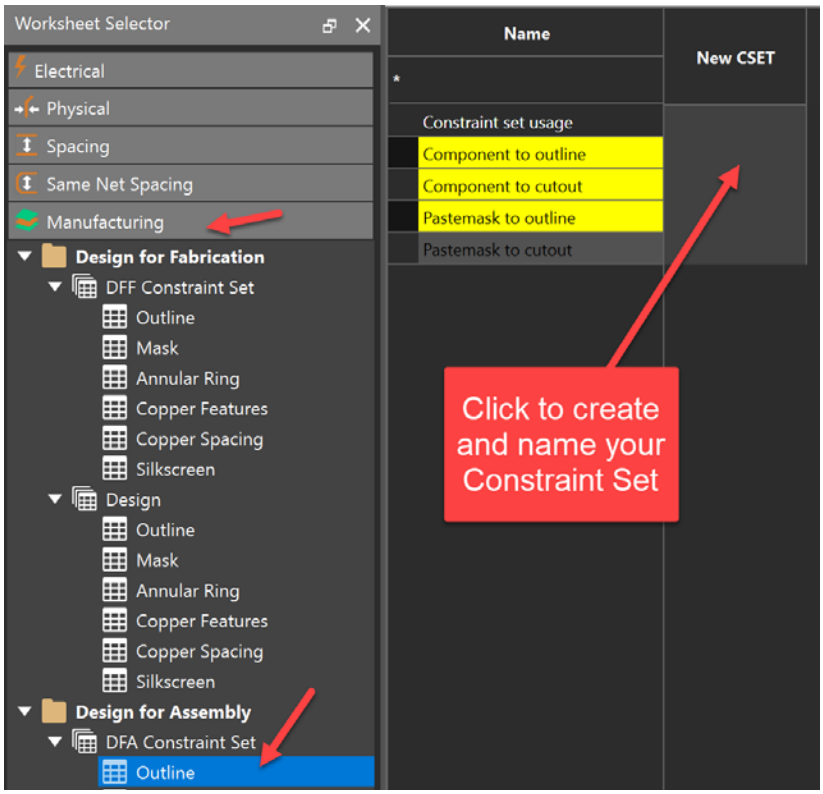
Outlines and Cut Outs

Component to Outline constraints can be set and applied in the following sections shown below.

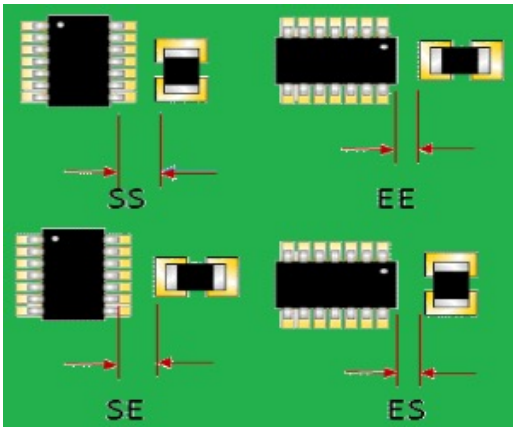
You can set rules for:

- Component to Cut Out
- Pastemask to outline
- Paste Mask to cut out

Where to Find and Create the Constraint Set



Where to Apply the Constraint Set



Component to Component Spacing (Edge and Side Spacing)

Package to Package Spacing

Use the constraint manager to establish Package to Package Spacing for all your components. For more information, please refer to the Component to Component Spacing Class section earlier in this document.

Component Spacing to PCB Features

Use the constraint manager to create and apply the following constraints.

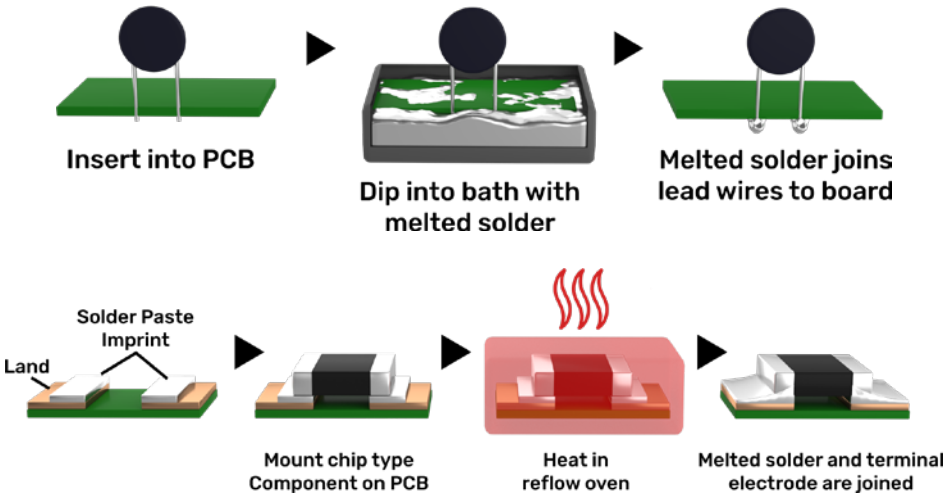
- Component Body to
  - All pin pads
  - All holes
  - Edge fingers

Purpose: The purpose of these constraints is to avoid shorts and challenges in automatic and manual assembly, which can significantly drive up costs (especially for manual testing and assembly).

Impact: You also can hurt yield if the boards are too challenging or costly to assemble, even if they are easy to fabricate.

Pastemask

Use the constraint manager to establish Package to Package Spacing for all your components.



Typical solder paste to soldered component flow for surface mount and through-hole devices on a PCB

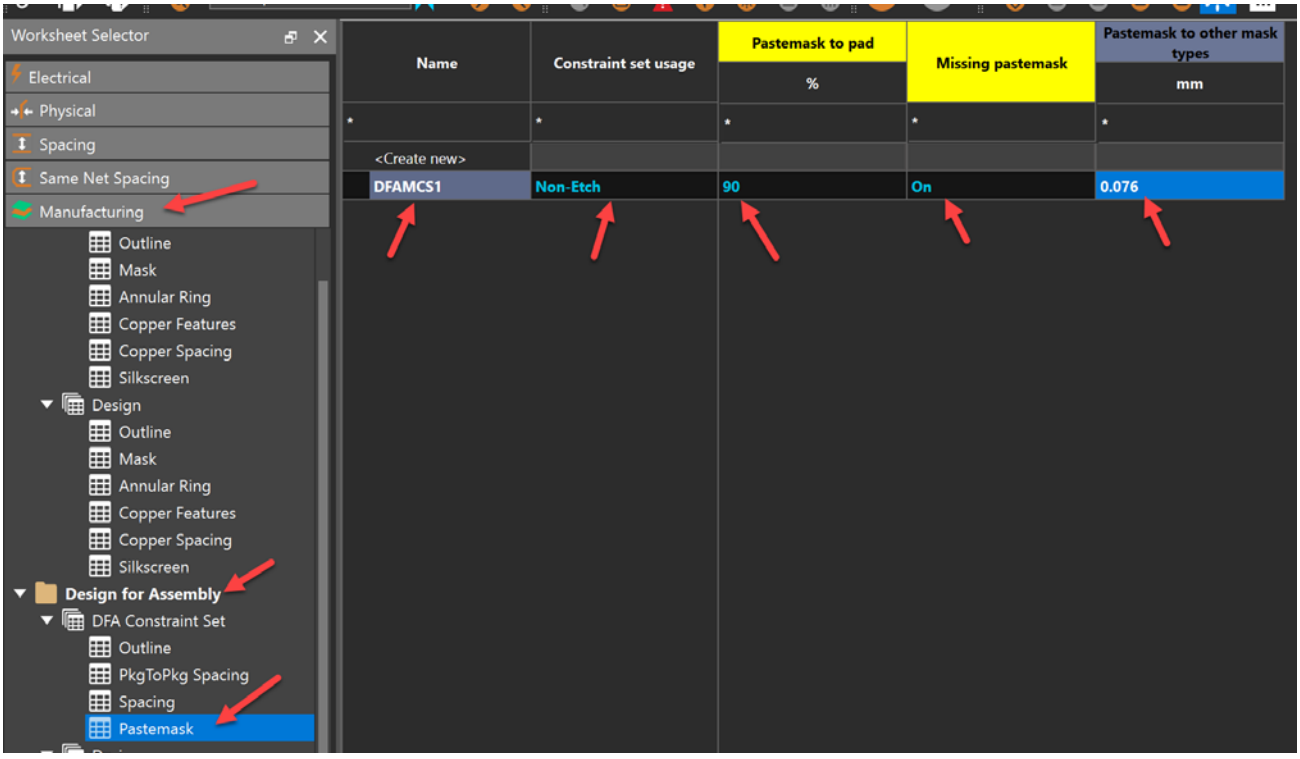
Purpose: Pastemask is extremely important for automatic assembly of components onto your PCB. Solder paste is metallic material with a moderately high melting point used to adhere the components to a PCB copper pad surface using wave soldering or an oven. The paste mask is a film manufactured to create a negative image to squeegee the solder paste onto your PCB (for surface mount soldering preparation).

You can set constraints for various paste mask options including:

- Pastemask to pad
- Missing pastemask
- Pastemask to other mask types
- Pastemask to
  - Pastemask
  - Via pad
  - Other Mask
  - Component Body

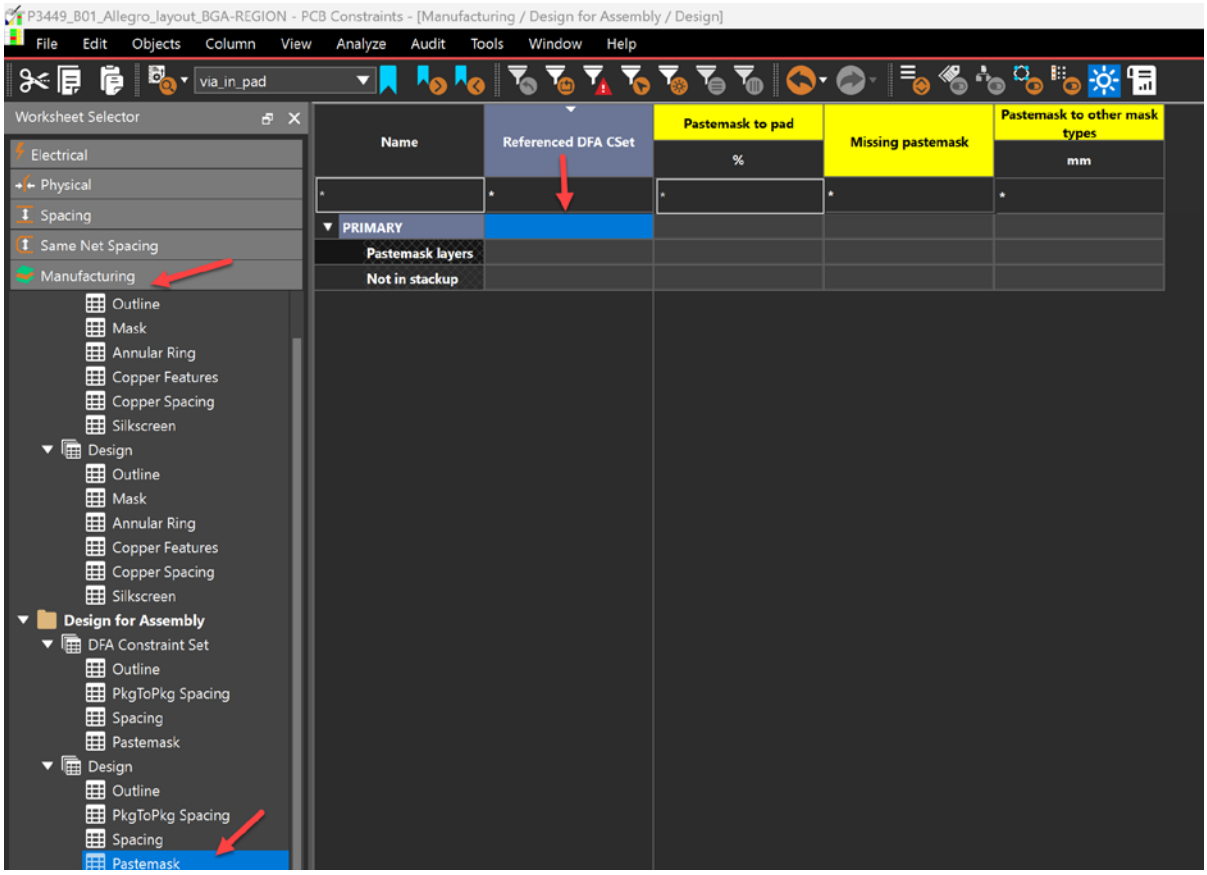
To access, create, and apply paste mask rules onto your design:

1. Open the constraint manager and you'll find your constraint creation options under Manufacturing > Design for Assembly > Pastemask.
2. You can click <Create new> to make your DFAMCS1 constraint, set your required values as per your manufacturing requirements and tolerances (see below).



3. Once that constraint has been created, apply it to your design that has paste mask layers. For example, the section below: Manufacturing > Design for Assembly > Design > Pastemask.

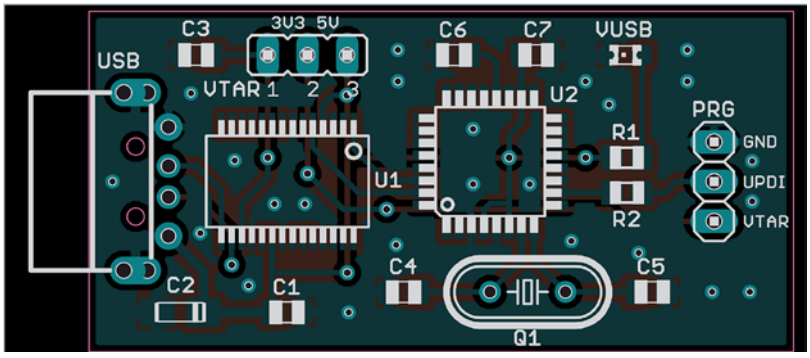
4. Then, choose **Referenced DFA CSet** and then rules from the CSet get applied.



Impact: You also can hurt yield if the boards are too challenging or costly to assemble due to unreliable paste, missing paste or paste that is too close to other objects on the PCB.

Silkscreen and Solder Mask: Specifications for Text and Mask Application on The PCB.

Purpose: Silkscreen is used to write notes on the PCB for easier assembly.



Silkscreen reference designators on a PCB layout

- All pin pads
- All via pads
- All non plated holes
- Min width (line, arc, shape)
- Min length (line, arc)

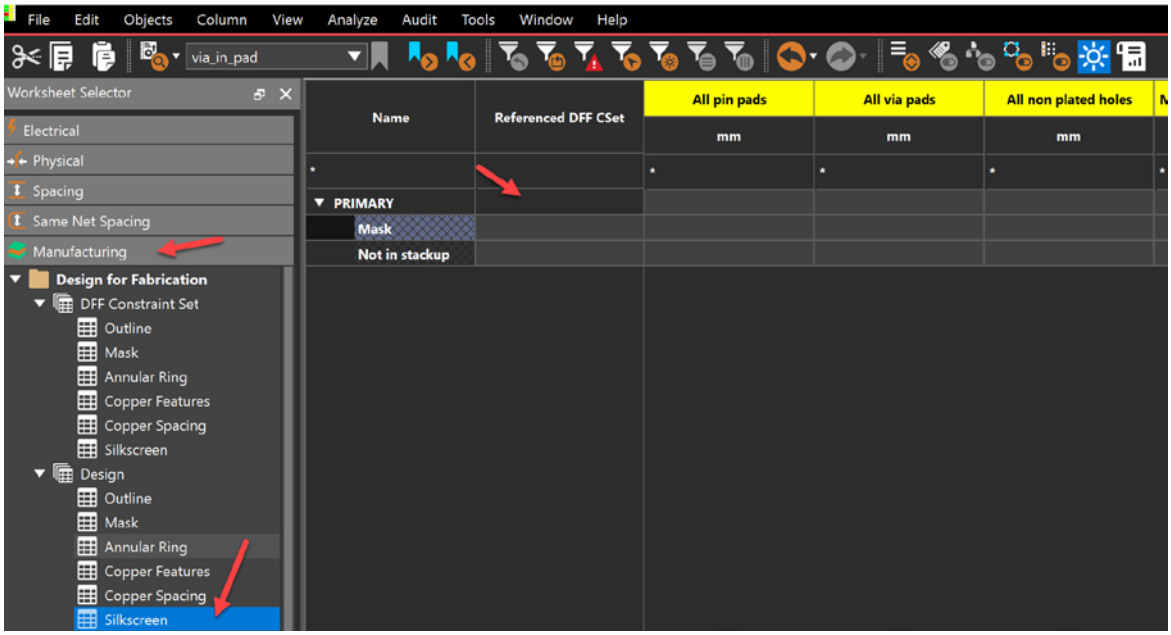
- Text overlap
- Text under component
- Text to line
- Text to shape
- Text to text

Impact: There is risk with having silkscreen in the wrong areas, though, like close to or under pads. There can be slivers and fabrication and manufacturing defects created by misplaced silkscreen. In addition, if the silk screen is missing in critical areas, it can significantly or gradually add on more cost for assembly.

Where to Find:

1. In the constraint manager, navigate to the Manufacturing > Design for Fabrication > Silkscreen worksheet.
2. Then hit the <Create new> button to create a new constraint set. That gets created.
3. Then populate the values based on what your design and manufacturer need (see image below).

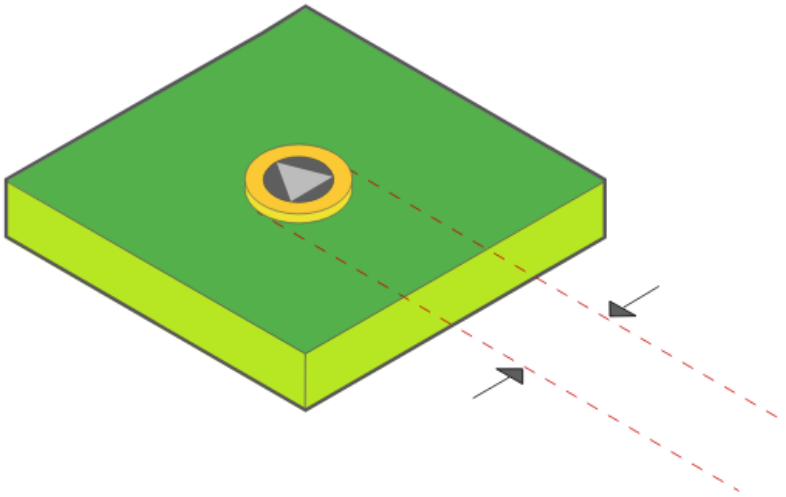
4. Once the constraints are set, you are ready to apply them.
5. Go to Manufacturing > Design for Fabrication > Design > Silkscreen.
6. Click and apply your constraint set onto the cell next to your **PRIMARY** design.



While we have constraints for all fabrication and assembly concerns, we need another for testing and test points. This is addressed in the next section.

Design for Test (DFT) Constraints

Test Points: Placement and Minimum Distances From Other Test Points and Components

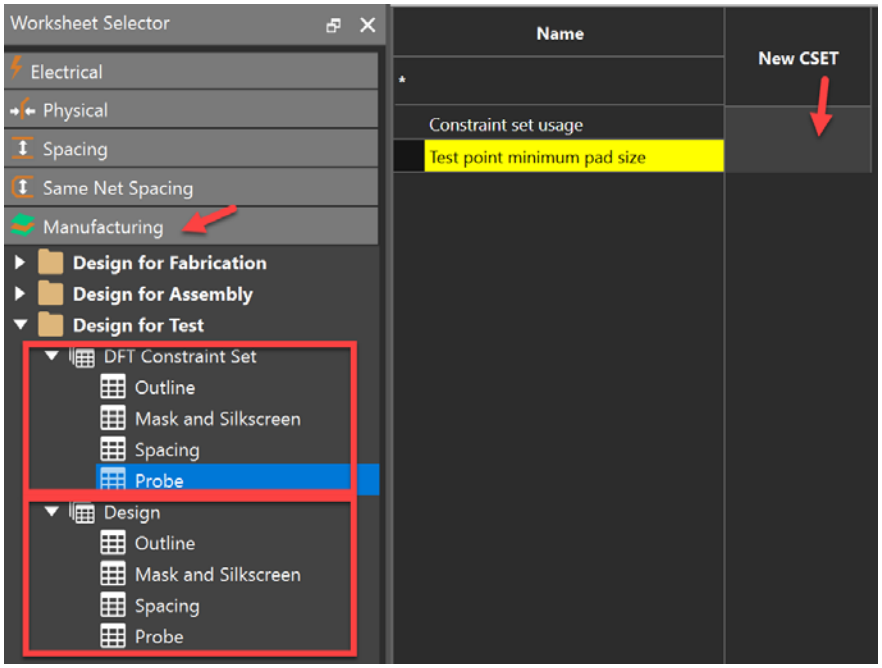


Visual Aid: Test point on pad.

Purpose: Defines the placement and spacing requirements for test points to ensure proper testing and debugging of the PCB.

Steps:

1. Open the Constraint Manager.
2. Navigate to the Design for Test (DFT) section.
3. You would create the constraint set for your design (upper red box in image below).
4. Then apply that constraint set to appropriate objects within the design (lower red box in image below). Set a minimum distance between test points.



In the constraint manager you can set constraints for various parameters such as:

- Outline
  - Test point to outline
  - Test point to cut out
- Mask and Silkscreen
  - Test point on solder mask
  - Test point to silkscreen
- Spacing
  - Test point to test point
  - Test point to component
  - Test point to pin pad
  - Test point to via pad
  - Test point to non plated hole
  - Test point under component
- Probe
  - Test point minimum pad size

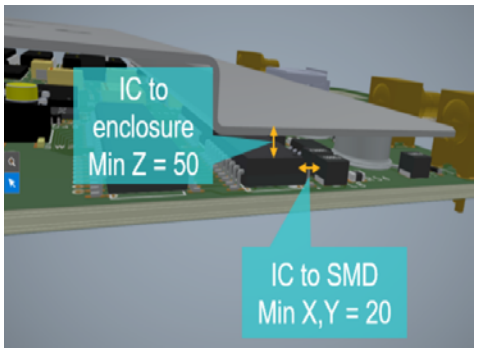
Reason: Proper test point placement ensures accessibility for automated testing equipment and manual probing, facilitating efficient testing and troubleshooting processes.

Impact: Improves testability, reduces testing time, and enhances the overall quality assurance process for the PCB. Well-placed test points can significantly reduce debugging time and improve manufacturing yield.

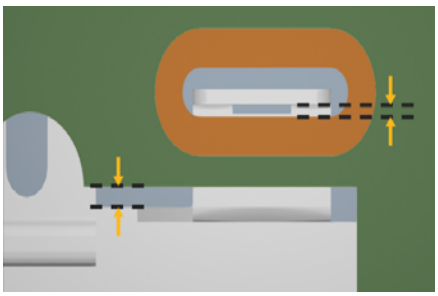
3D Constraints

Purpose: 3D constraints have become a mandatory requirement in the modern PCB design and assembly process.

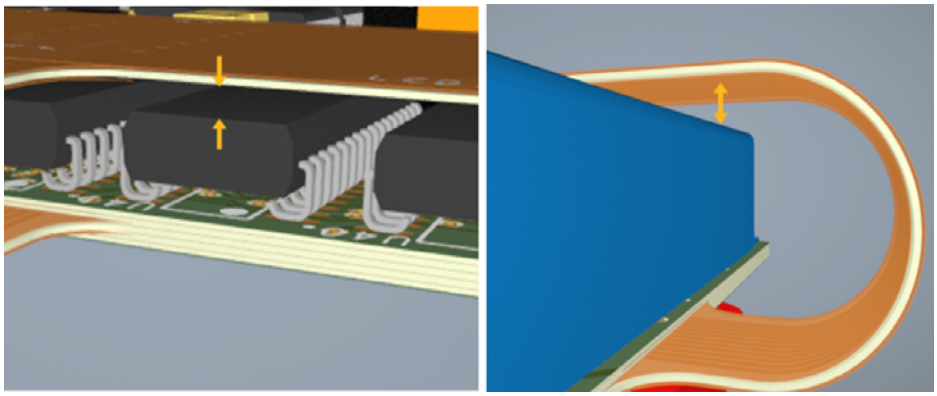
Component to Component



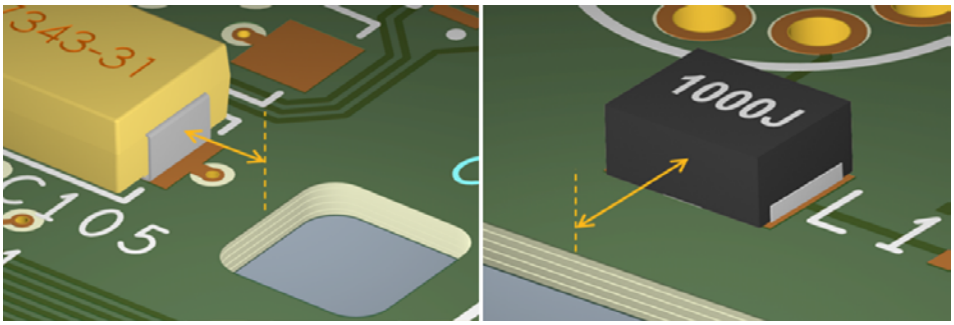
Component to Board



Component to Rigid Flex

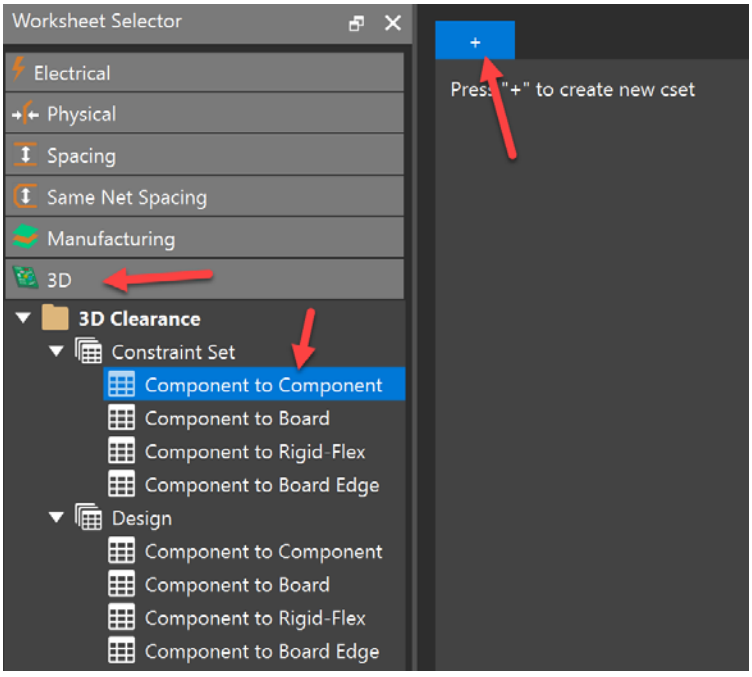


Component to Board Edge

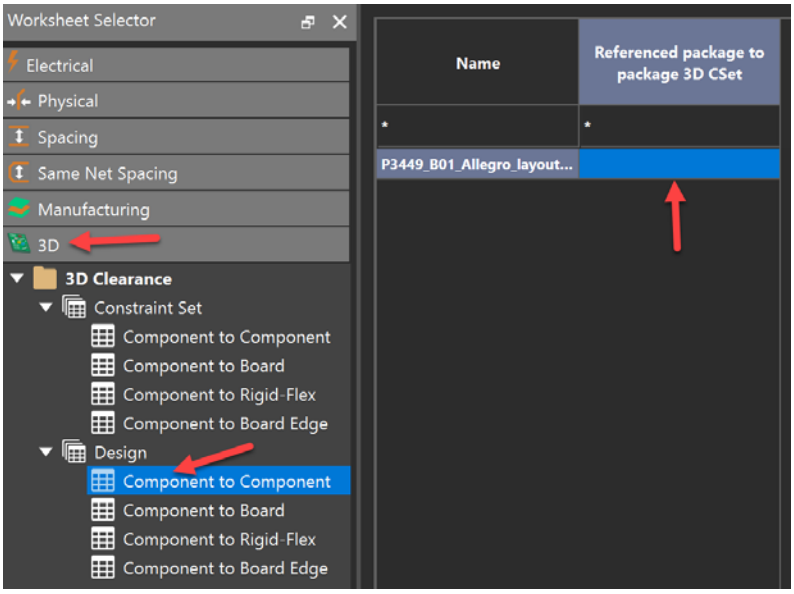


Steps: To access 3D constraints

1. Open the Constraint manager and navigate to the '3D' section > 3D Clearance > Constraint Set.
2. Choose the category within the constraint set that applies to your situation (e.g. Component to Component, Component to Board, Component to Rigid-Flex, Component to Board Edge).
3. Click the + Button to create a new cset and apply your constraint values.



4. Once you're happy with your constraints, go to the 3D Clearance > Design section and apply the appropriate constraint to the relevant objects (e.g. Component to Component, Component to Board, etc.)



Impact: Components, cables and connectors can cause an otherwise functional PCB to not be viable for product use because of lack of ability to fit into a larger system. You may also have components that, due to their spacing, make it difficult or impossible to place them on the PCB without going in a certain order. Poorly 3D constrained boards are also at risk of components and your design enclosures colliding.

Rigid Flex PCB Constraints

Teardrops (Fillets)

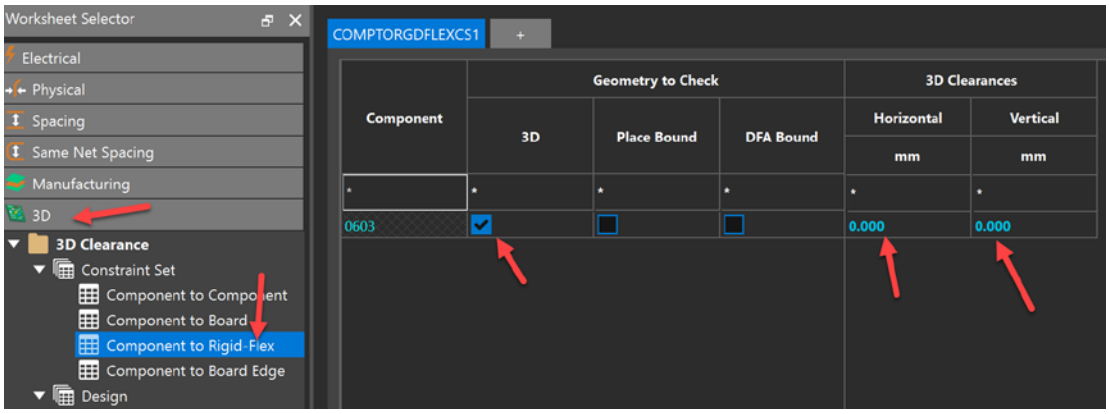
Please see the Teardrops (Fillets) section in the Manufacturing Section.

Component to Flex PCB

Purpose: Components need to maintain a certain distance from the flexible parts of a PCB.

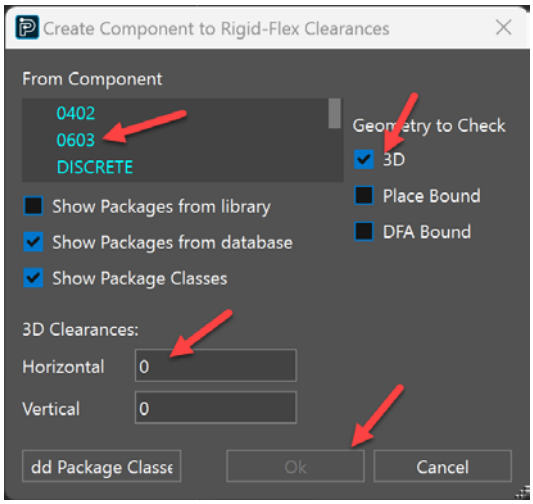
The Constraint manager gives you granular control over components to rigid-flex placement and positioning. To explore that:

1. Open the constraint manager.
2. Go to the worksheet found in 3D > 3D Clearance > Constraint Set > Component to Rigid-Flex.

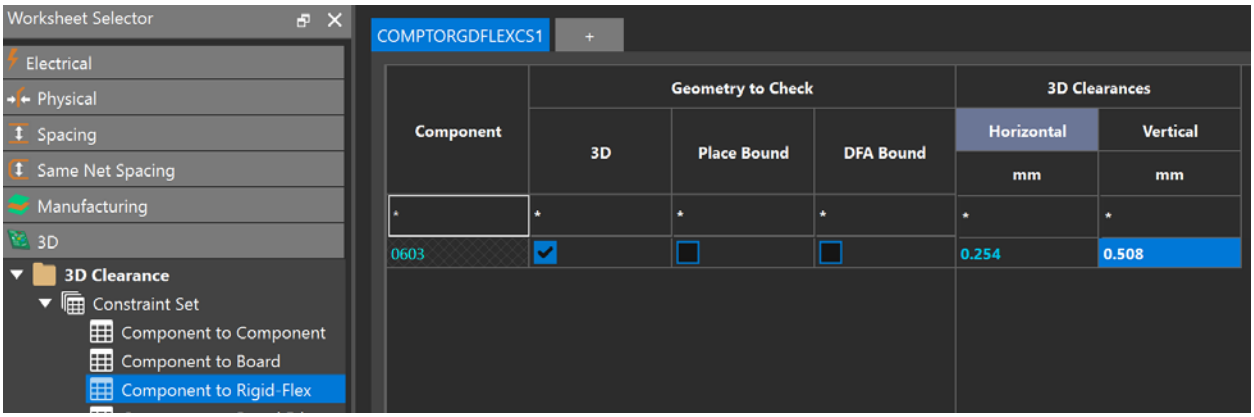


3. In this worksheet, you can choose Add Row at the bottom of the window to open the Create Component to Rigid-Flex Clearances window.

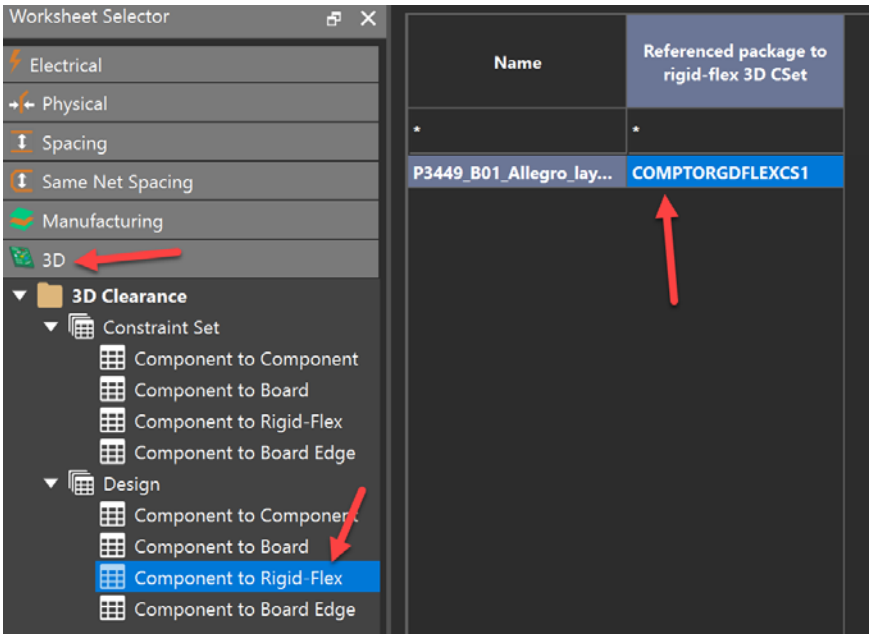
4. Set your 3D clearances and other parameters as shown below, then click Ok.



5. You can set your values even after placing the constraints.



6. Now you can apply the constraint set by choosing the 3D > 3D Clearance > Design > Component to Rigid-Flex worksheet.



Impact: Similar to component 3D assembly constraints, your component to Rigid Flex constraints can cause product issues if they collide, even if the fabrication and assembly go well. This is especially true when it comes to the folding behavior of flexing and folding on a PCB.

Modern hardware and PCB layout require a more holistic approach than traditional methods, and only the most robust set of constraint management tools enable today's top technology.

Conclusion

In Part 2 of the OrCAD X Constraint Manager Guide, we explored the essential standard constraints and rules that form the backbone of PCB design. These constraints, ranging from physical and spacing rules to manufacturing considerations, ensure a reliable and high-quality PCB layout.

By understanding and applying these constraints, designers can effectively manage component placement, electrical integrity, and manufacturing processes, ultimately leading to a robust design that meets industry standards.

As we transition into Part 3, Advanced Constraints, we will delve deeper into more complex design considerations that accommodate cutting-edge technologies and intricate layouts.

This next section will empower you with the knowledge to tackle challenging design environments and push the boundaries of PCB design innovation.