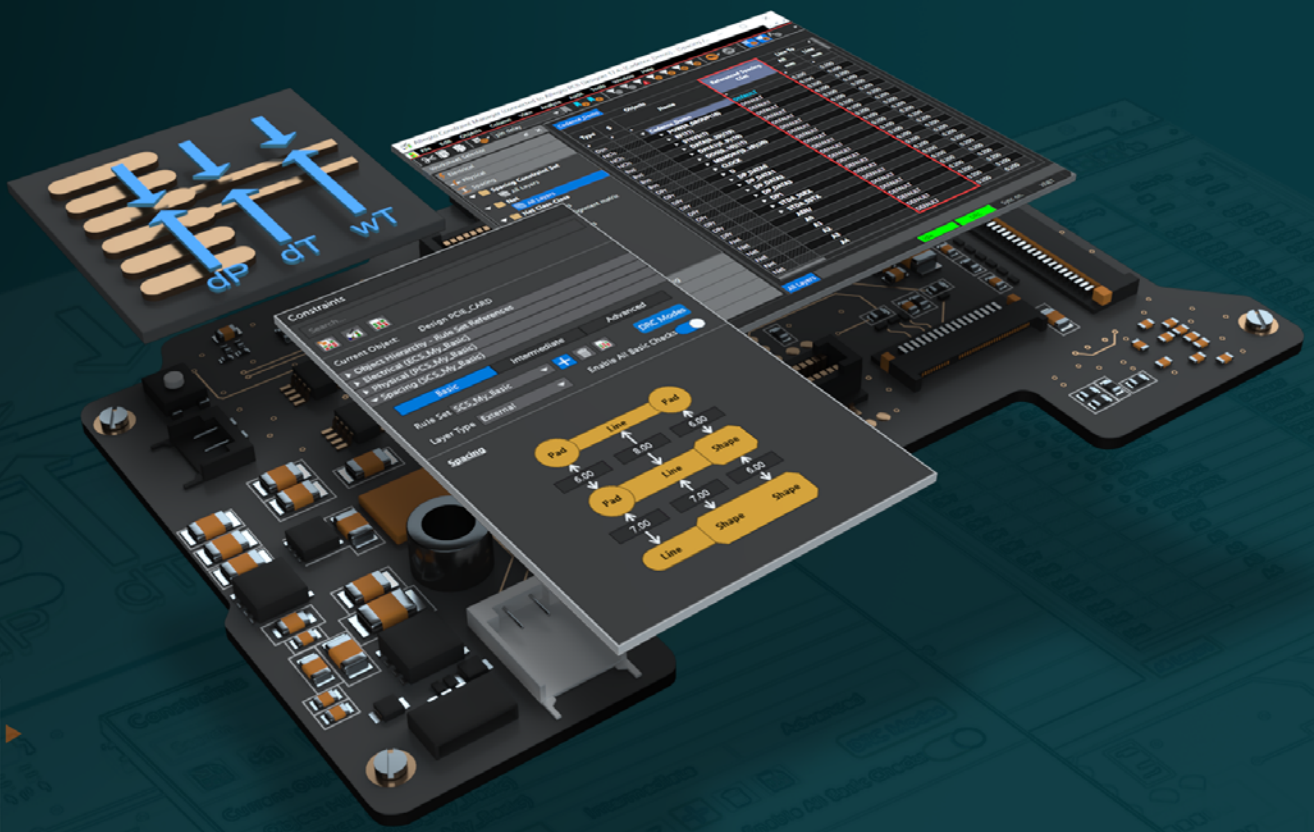
DESIGN **GUIDE**

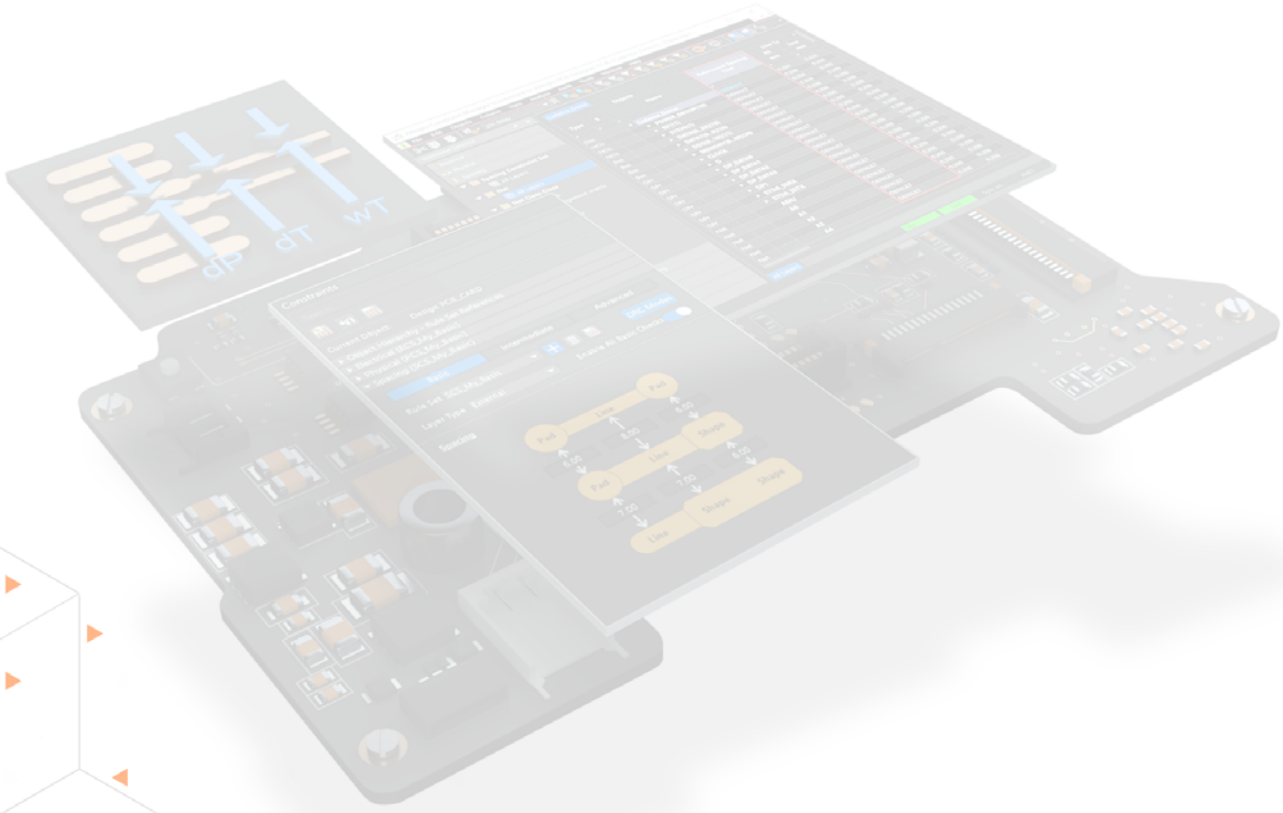
cadence®

OrCAD X Constraint Management Guide

Part 3 of 5



Contents



Part 3 - Advanced Constraints

Advanced constraints include rules for high-speed complex printed circuit boards. Standard PCBs are usually 300 components or fewer, where the primary concern is designing for manufacturing, fabrication, assembly, and testing, then maybe differential pairs and single-ended impedances depending on the protocols in your design.

Complex high-speed PCBs however need considerations for impedance control, differential pairs, inter-pair and intra-pair skew, a limit on the number of vias and other such factors that manage signal integrity and electromagnetic interference.

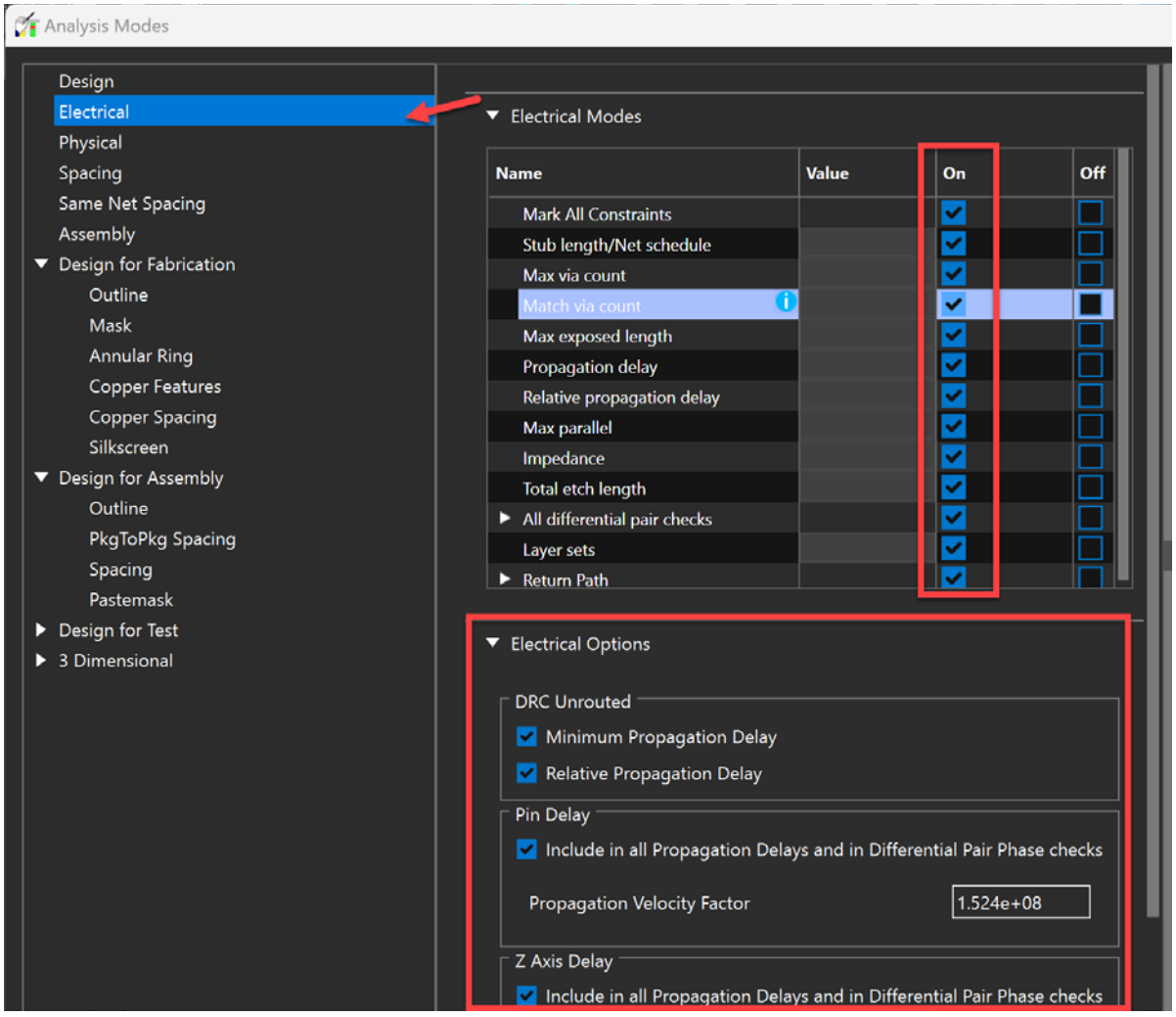
Advanced Constraints also account for typical high-density interconnect boards, military grade PCBs, and rigid-flex or flex PCBs. Anything outside the normal DFM considerations would be considered advanced constraints for a printed circuit board.

Now that we understand the difference between regular and advanced constraints let's look at ways to turn on or off the kinds of constraints we should enforce in the Constraint Modes section.

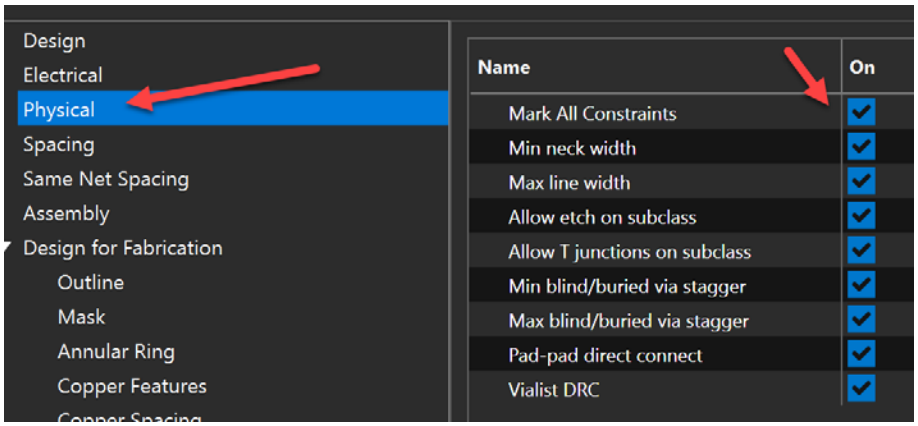
Constraint Modes

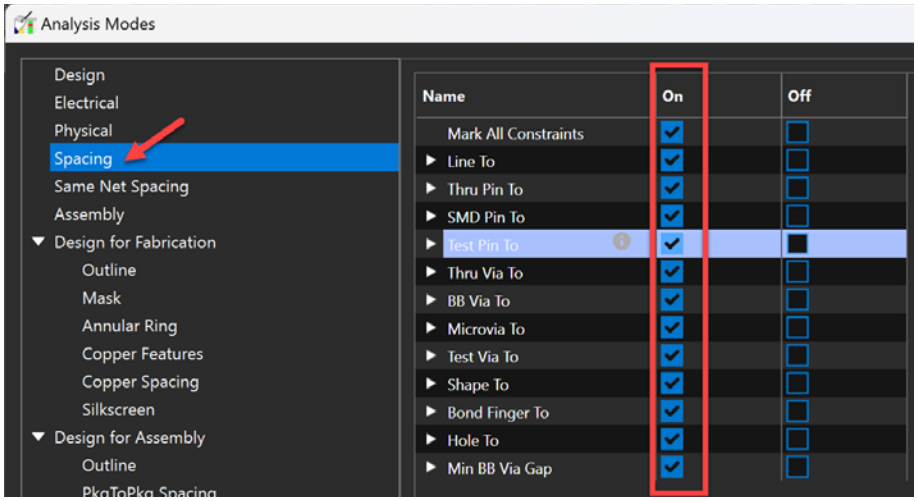
Implementing USB constraints in Cadence OrCAD X.

1. Open Constraint Manager.
2. Go to Analyze - Analysis Mode – Electrical.
3. Enable all the options under Electrical Modes and Electrical Options as seen in the image below.



4. Also, enable all checks in the Physical and Spacing Categories as well.





In general, you want to enable all Electrical, Physical, and Spacing Constraints when working with high-speed constraints.

Signal Integrity

Impedance Control: Specification for controlled impedance traces for high-speed signals

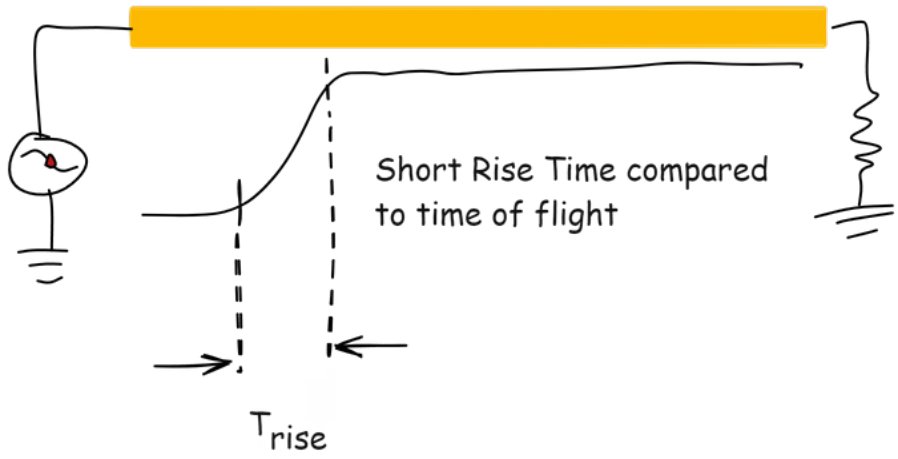
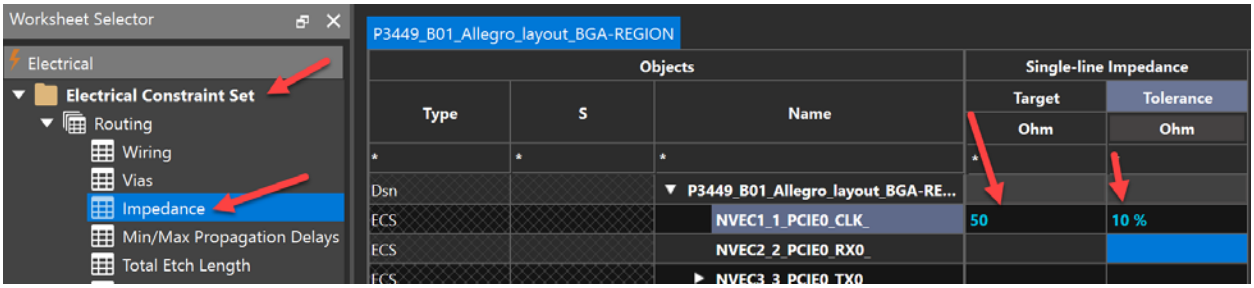


Diagram showing a PCB copper wire with signal propagation

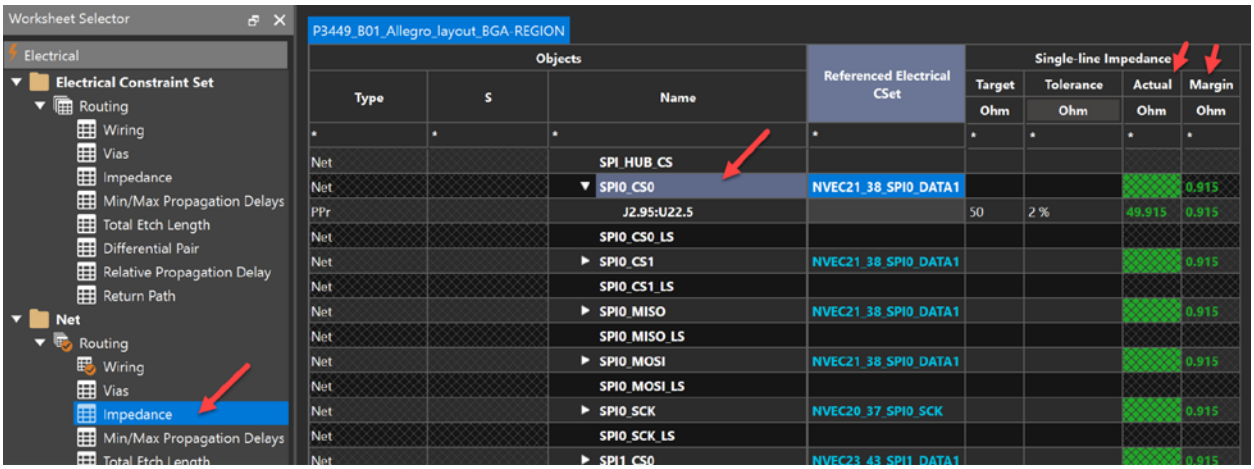
Purpose: Impedance control is used to specify and maintain consistent characteristic impedance for high-speed signal traces throughout the PCB.

Steps to Execute Constraint for Impedance Control:

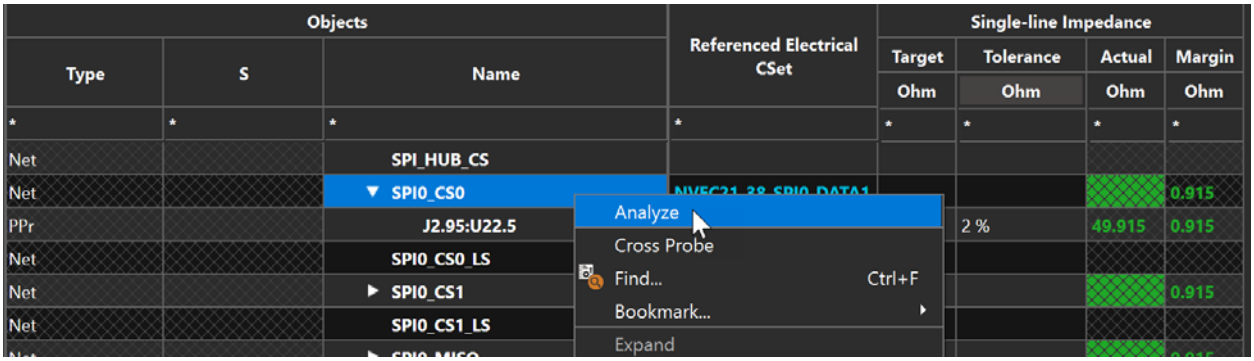
1. Open the Constraint Manager.
2. Navigate to the Electrical Constraint Set > Impedance.
3. Define target impedance values for different trace types (e.g., single-ended).



4. You can then go to the Electrical > Net > Routing > Impedance worksheet and apply the constraint to any net, net class, or net group.



5. Then, you can determine whether the nets are adhering to the rules inside the constraint set by right-clicking a net name and then clicking Analyze.



6. The analysis will show red, yellow or green for whether your net complies with the Single line impedance constraint.
7. It lets you know the target impedance, the tolerance, the actual impedance of the trace, and the margin (how much you are in terms of impedance).

Note: The behavior of the trace will be such that when you're routing it, the trace thickness will change to maintain the impedance, or at least a DRC error will appear if your trace falls outside the target impedance range.

Reason: Controlled impedance is crucial for maintaining signal integrity in high-speed circuits. It helps minimize signal reflections, reduce crosstalk, and ensure proper signal transmission. Specify target impedance values (e.g., 50Ω for single-ended traces, 100Ω for differential pairs) to minimize reflections and ensure compatibility with specific communication protocols. This involves controlling trace width, spacing, and dielectric properties.

Impact on the Board:

- Improves signal quality and reduces distortion in high-speed signals (by reducing reflections)
- Enhances overall system performance and reliability
- It may require specific PCB materials and manufacturing processes to achieve the desired impedance values
- Can influence trace routing and layer stack-up decisions

By implementing proper impedance control constraints, designers can ensure that high-speed signals maintain their integrity throughout the PCB, leading to more reliable and higher-performing electronic products.

Crosstalk Mitigation: Maximum parallel trace length

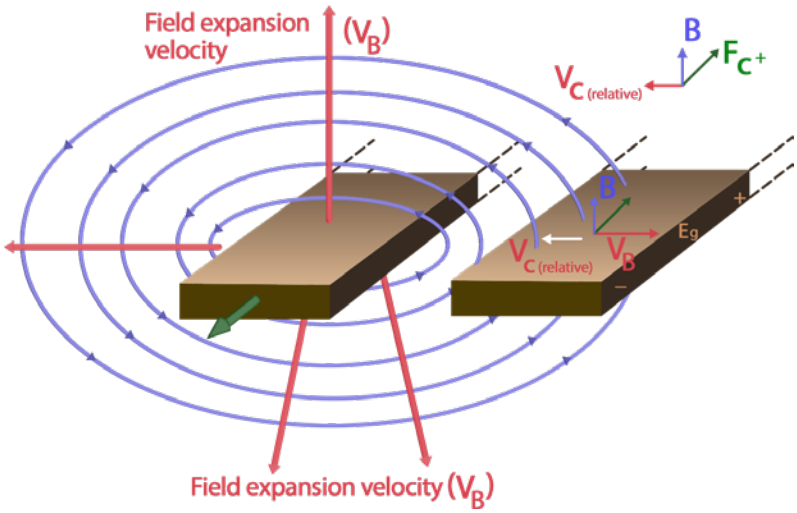


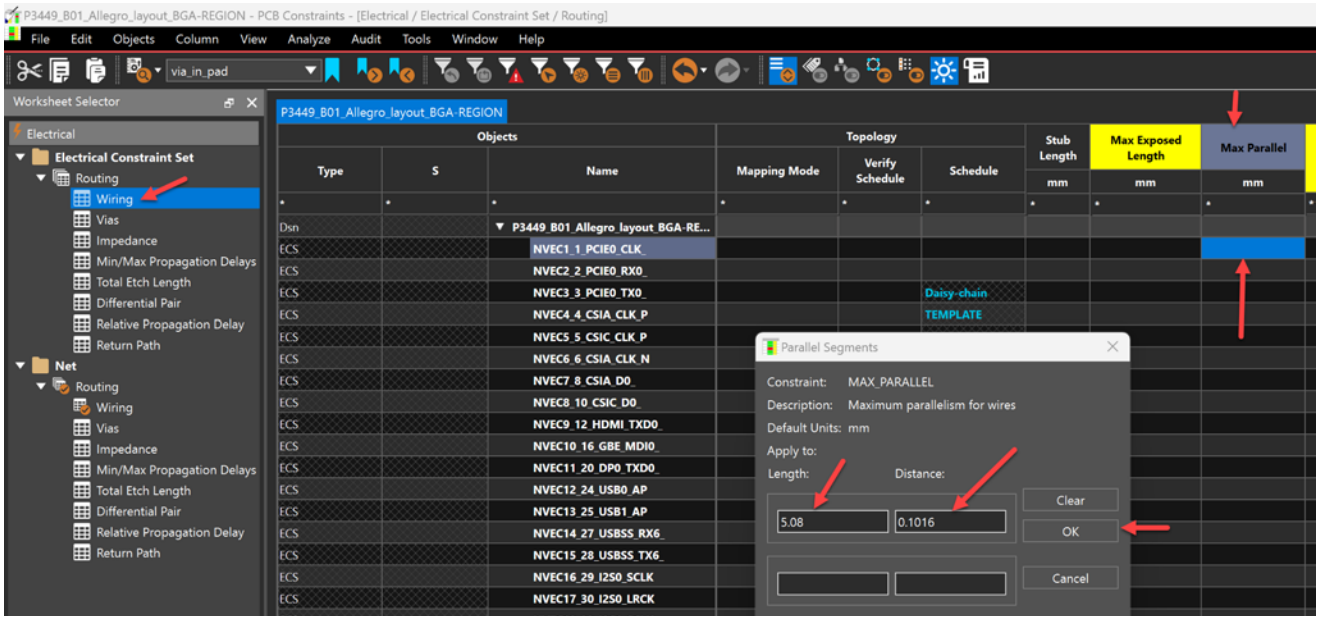
Diagram illustrating crosstalk between two traces running parallel to each other. (source: Sierra Circuits)

Purpose: Limit the length that signal traces run parallel to each other to reduce coupling and crosstalk. This is especially crucial for high-speed differential pairs. The acceptable length depends on factors like trace spacing, layer stack-up, and signal frequency.

In this example, you will learn how the Constraint Manager prevents excessive coupling among traces.

Steps to Execute Constraints:

1. Open the Constraint Manager.
2. Navigate to the **Electrical > Electrical Constraint Set > Routing > Wiring** worksheet.
3. Scroll horizontally to the Max Parallel column, then in that same column, select the cell for any of the Electrical Constraint sets shown below. Then a Parallel Segments window will appear.



4. Enter some values that would work for your design calculations (e.g., not allowing traces that are 0.1016 mm / 4 mils apart to traverse more than 5.08 mm / 200 mils together). Click OK.
5. With the constraint set values set, apply the constraint set by going to the **Electrical > Net > Routing > Wiring** worksheet.
6. Click one of the applicable nets (e.g., **PCIE0_CLKREQ**), then apply the constraint set (in this case **NVEC1_1_PCIE0_CLK_**)

Reason: Signal Integrity constraints are crucial for maintaining data integrity, especially in high-speed designs where signals are more susceptible to degradation and interference.

Impact on the Board:

- Reduces signal distortion and data errors
- Improves overall system reliability and performance
- May influence trace routing, layer stack-up, and component placement decisions
- This can lead to more complex design rules and potentially increased PCB manufacturing costs

By implementing proper Signal Integrity constraints, designers can ensure that their PCBs maintain signal quality and minimize interference, resulting in more reliable and higher-performing electronic products.

EMC and EMI

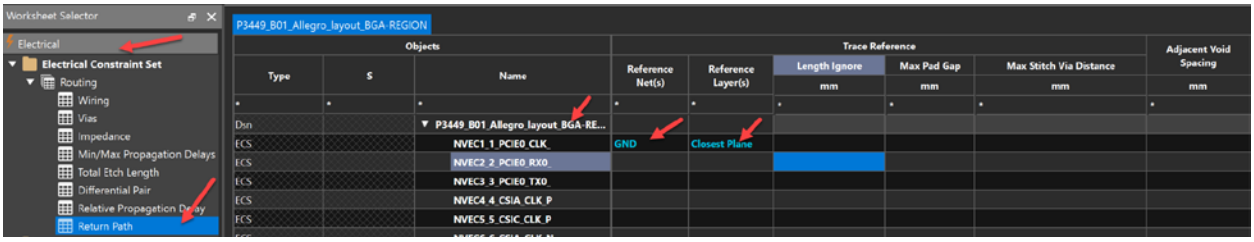
Return Path

Purpose: Reduce electromagnetic interference by checking that signals are following a proper return path.

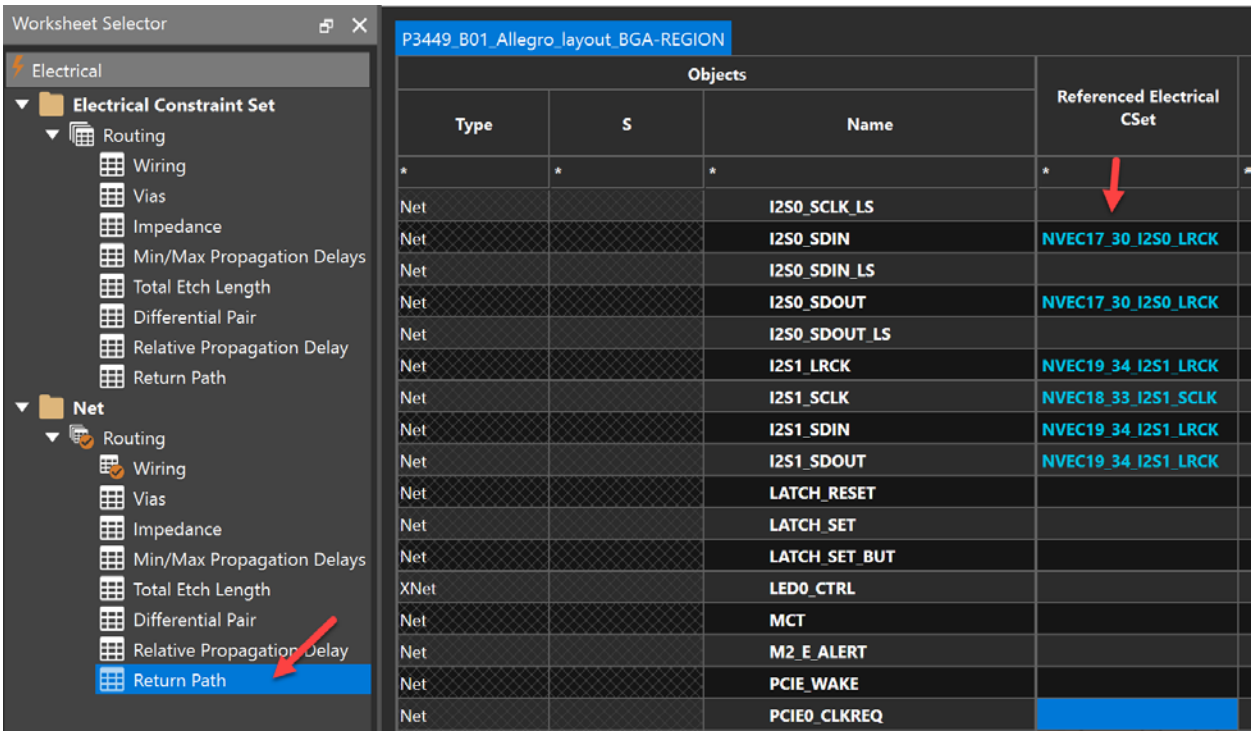
OrCAD X Constraints support return path checking for Impedance and EMI.

Steps to implement return path checks:

1. Open the constraint manager.
2. Go to the worksheet found in **Electrical > Electrical Constraint Set > Routing > Return Path.**
3. Right-click on the DSN cell name (P3449_B01…), create an Electrical CSet, give it a name, and then it will add itself to your list of ECSets (see below).
4. Whether you create an ECSet or use an existing one, you have multiple options available for return path checks.



5. You can set the right reference Nets and layers for your signals.
6. After such, to apply the rules, go to **Electrical > Net > Routing > Return Path**, choose the net to which you want to apply your ECSet, and that's it.



Impact on the Board:

- Improves overall reliability and performance of the PCB in various electromagnetic environments
- Ensures compliance with regulatory standards, which is essential for product certification and market entry
- May influence component placement, routing strategies, and layer stack-up decisions
- This can lead to the inclusion of additional shielding or filtering components
- It might require changes in trace routing to minimize crosstalk and emissions

By implementing proper EMC and EMI constraints like return path checking, designers can create PCBs that not only function well but also meet the stringent electromagnetic compatibility requirements of modern electronic devices.

High-speed constraints/electrical design rules:

Min/max relative propagation delay: Controlling signal timing

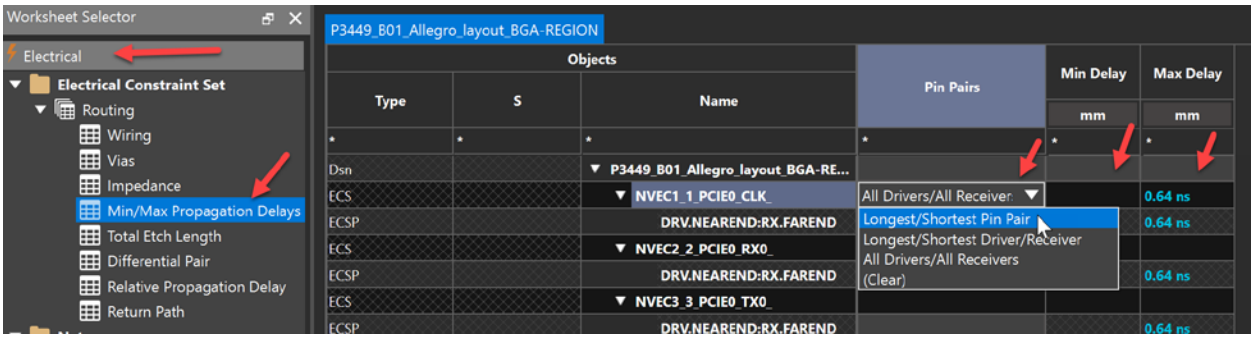
Definition: Managing the propagation delay of signals to ensure they arrive at their destination at the correct time.

Example: Ensuring that critical signals have minimal delay to synchronize with other signals.

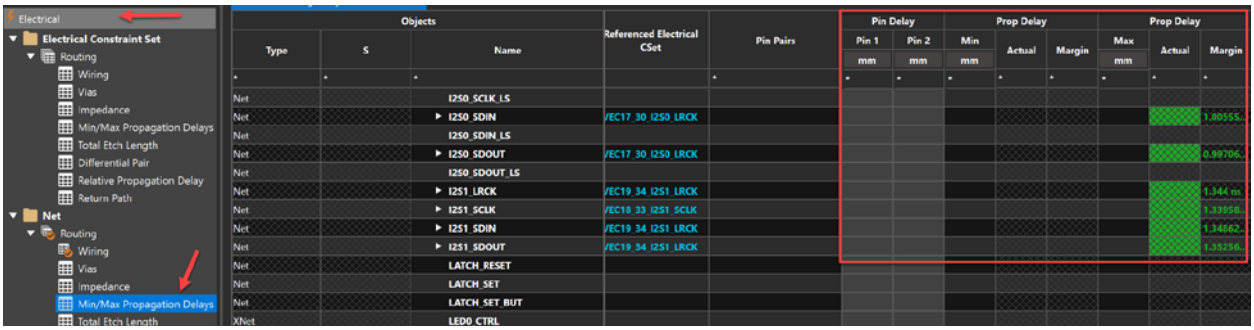
Steps:

To set the signal propagation delay:

1. Go to the following worksheet: **Electrical > Routing > Min/Max Propagation Delays**.
2. You can create your desired constraint set, but let's look at the existing ones shown below.

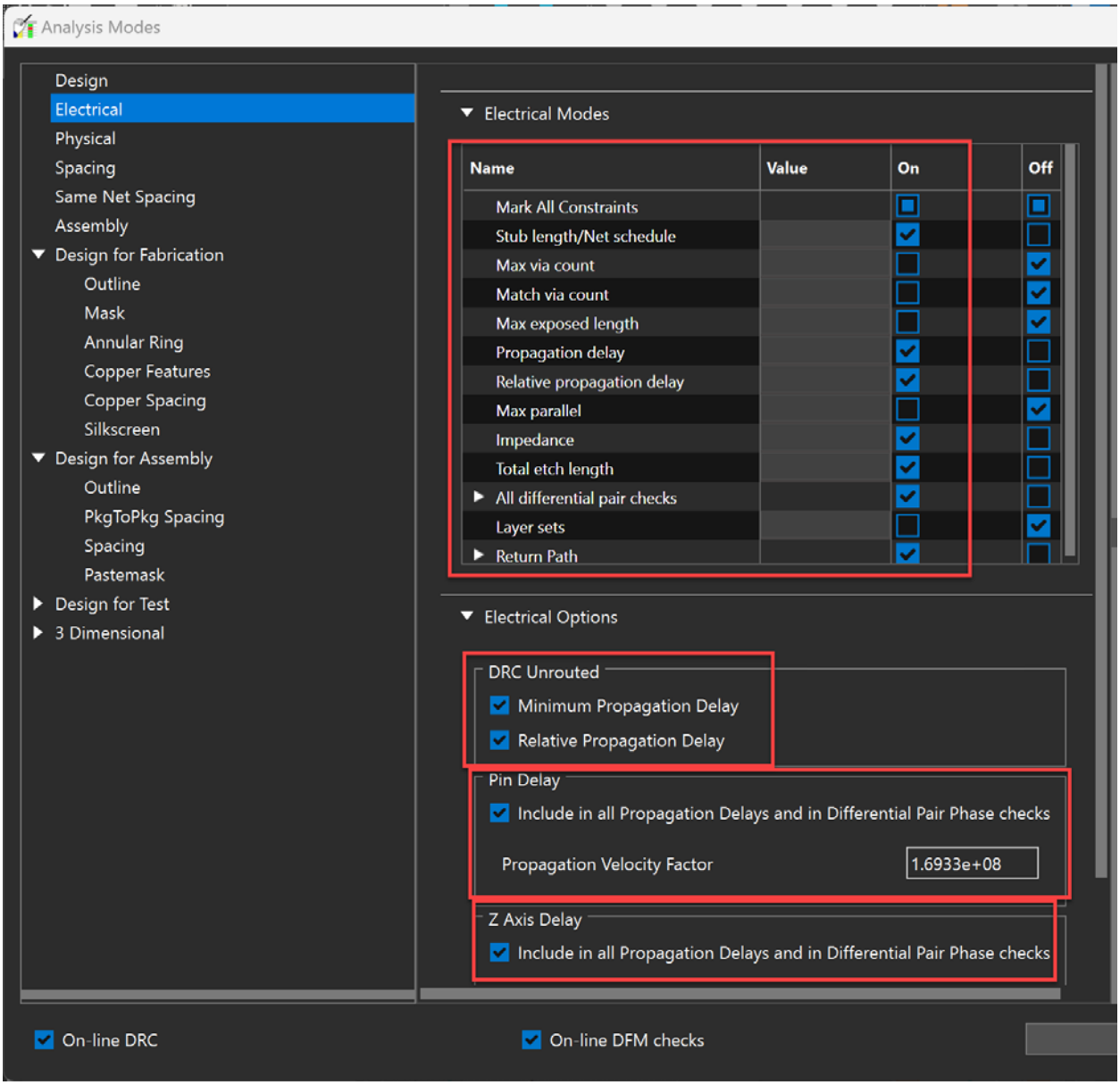


3. You can choose the pin pairs (transmitter and receiver) that will be on either side of the signal being propagated through the respective trace.
4. Choose the Pin Pairs based on your design criteria.
5. Next you can apply the constraint in the worksheet called **Net > Routing > Min/Max Propagation Delays**



6. Notice that once you apply your constraint set, you can right click on the nets of interest, then choose Analyze, then the constraint manager will let you know in the Prop Delay columns whether those nets have the actual propagation delays you need in the board.

IMPORTANT: Please note that you must enable this analysis mode in Constraint Manager. To ensure this, go to the menu at the top, Analyze - Analysis Modes. The Analysis Modes window will appear.



Check all the electrical modes you want analyzed and include the checked items shown in the image above.

Click OK, then the Constraint Manager will be able to analyze the relevant constraints.

Benefit of Propagation Delay: Improves timing accuracy and reduces the risk of data errors. Assess this pre- and post-routing layout. This built-in high-speed analysis feature greatly reduces risk of errors in the PCB design. It is still recommended to analyze the signal integrity and timing analysis using post layout software, but these features are extremely powerful within OrCAD X Presto PCB Editor.

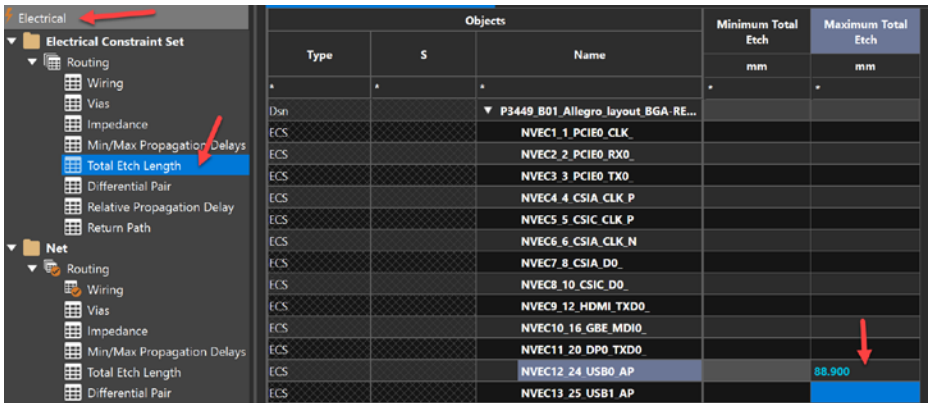
Create accurate models of signal propagation delays to account for potential signal degradation during operation. This helps in timing analysis and ensuring proper synchronization in high-speed designs.

Critical Trace Length

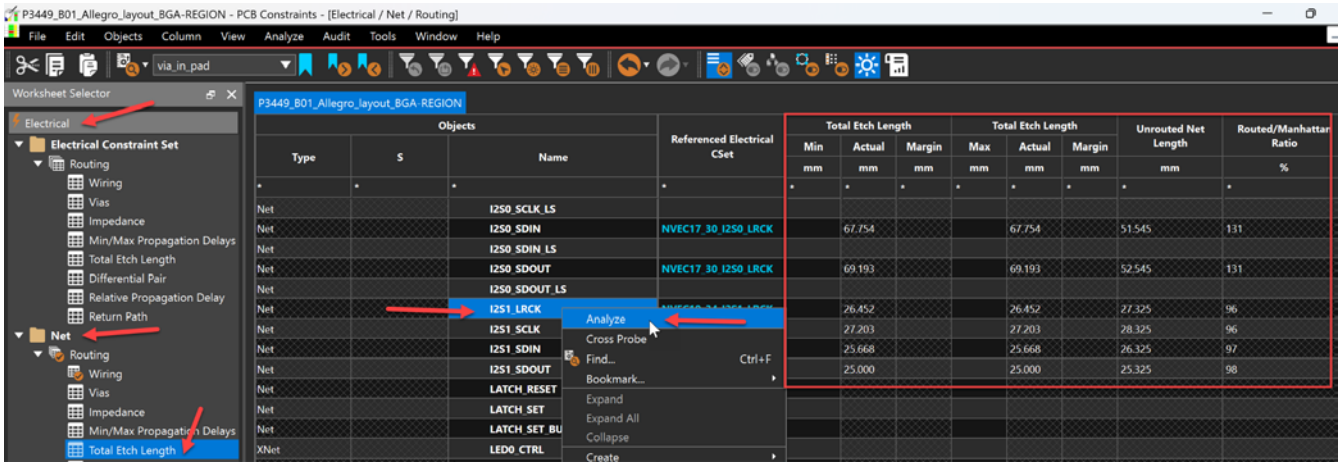
Definition: Critical trace length is the length of a trace or transmission line that would cause the signal to reflect if it's too long electrically.

Steps:

1. Open Constraint Manager.
2. Navigate to the worksheet Electrical > Routing > Total Etch Length.
3. We have existing Constraint Sets but feel free to make a new one.
4. For an electrical constraint set in the list, set the Maximum Total Etch. For example, USB 2.0 operating at 480 Mbps may see any traces longer than 3500 mils (88.90 mm) electrically long. So we set the max total etch to that value (shown below).



5. Recall that this is just the constraint set. It must be applied to nets in the design. Navigate to the **Electrical > Net > Routing > Total Etch Length** worksheet.
6. Next right click on the nets you want to analyze then choose **Analyze**. You will see the results below.



7. The Constraint Manager shows what the total etch length of the traces are, the length of the unrouted parts and even the percent of the routed net over the Manhattan distance (orthogonal position and distance if only routing at 90 degree angles).

Impact: Manufacturers have significantly reduced the rise times of chip signal transmissions, and we may not always have enough space on a PCB to slow these signals down. Fortunately, we can shorten trace lengths, which helps create a more compact PCB layout. This reduction minimizes the chances of signal reflections, preserving signal integrity and ensuring effective communication between devices for optimal PCB functionality. It's essential to set maximum trace lengths to avoid critical timing issues and signal degradation, especially for high-speed signals, as longer traces can lead to increased attenuation and skew.

Length Matching

Purpose: Ensuring that traces carrying related signals are of equal length. Matching the lengths of data lines in a memory interface to ensure synchronized data transfer.

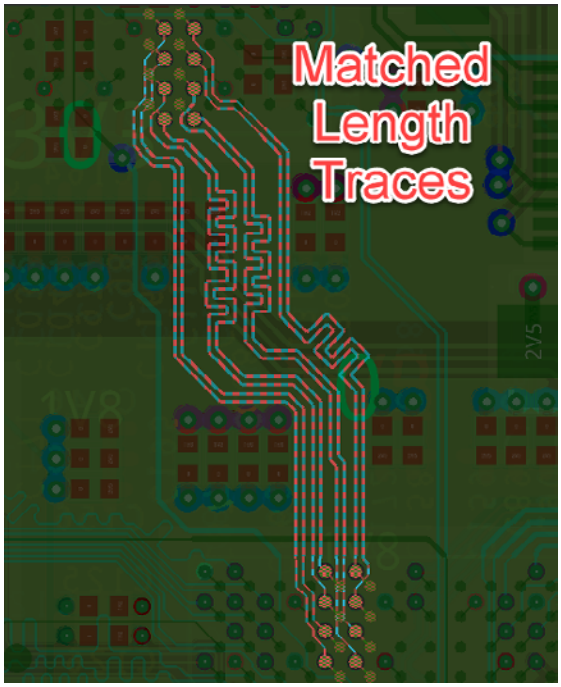
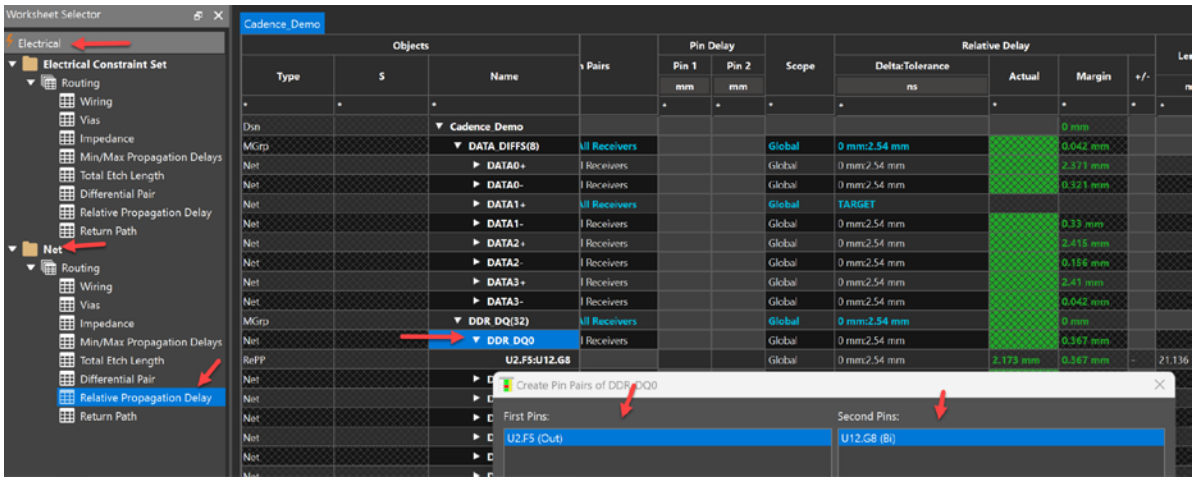


Diagram showing matched-length traces on a PCB.

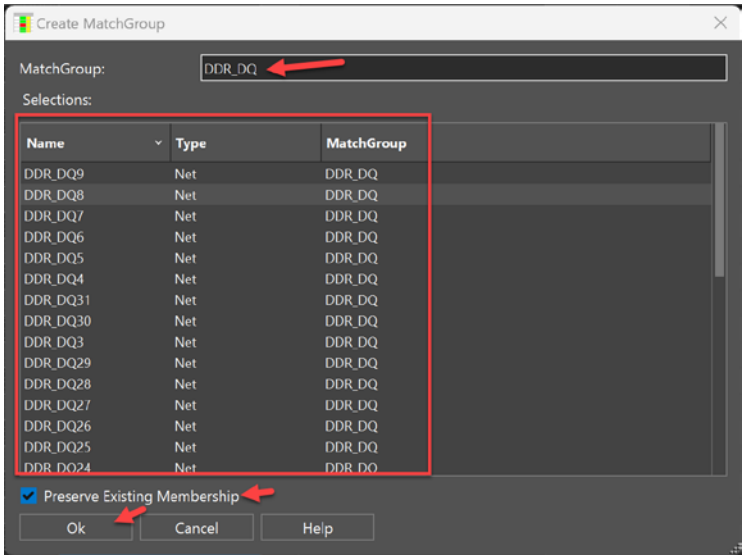
Steps/Example:

1. Open the Constraint Manager.
2. First, ensure that the constraint manager is analyzing all the electrical constraints, pin delays, etc. in the Analysis Mode (from the menu select Analyze - Analysis Mode, choose all options in Electrical then click Apply then Okay).
3. Then navigate to this worksheet: Electrical > Net > Relative Propagation Delay.
4. In your design you will need to create a matched group for nets that are carrying parallel signals, like in the image below where we have DDR_DQ(32) having 32 nets.
5. But first, make a pin pair for all the nets you want to put into a matched group. For example, let's say you didn't have the DDR_DQ# signals in a match group yet. You would select something like the DDR_DQ0, right click it - Create - Pin Pair..., click OK when presented with the pin options.

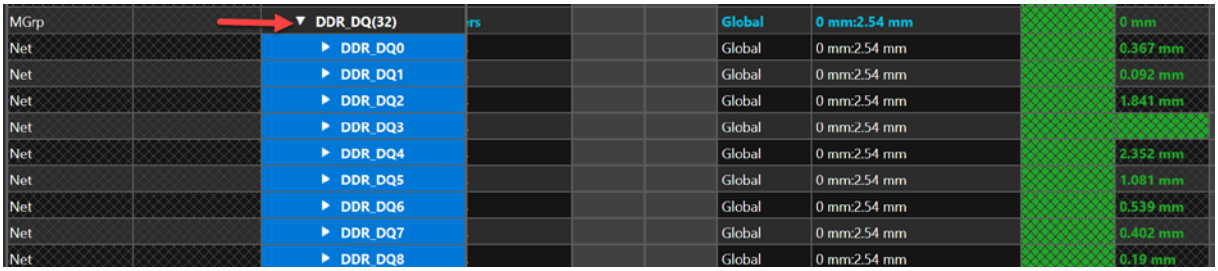


6. Once done, that will create the pin pair underneath the signal in the worksheet (shown below).

7. Where it says All Driver/All Receivers, you can change the pin pair relationships to other options such as:
   a. Longest Pin Pair
   b. Longest Driver/Receiver
   c. All Drivers/All Receivers
   d. (Clear)
8. For this example, we selected **All Drivers/All Receivers**. After that, you repeat the previous steps to create more pin paired nets, then to put your nets into a matched group.
9. To put nets into a matched group, click hold and drag the mouse to highlight all the nets of interest (DDR_DQ0 through DDR_DQ31 in this case), then right click any of them, choose **Create - Match Group**. A new window would appear.



10. Give the match group a name, like DDR_DQ, then click OK (Ensure that the **Preserve Existing Membership** checkbox is enabled).
11. The group gets created and is shown in the worksheet.

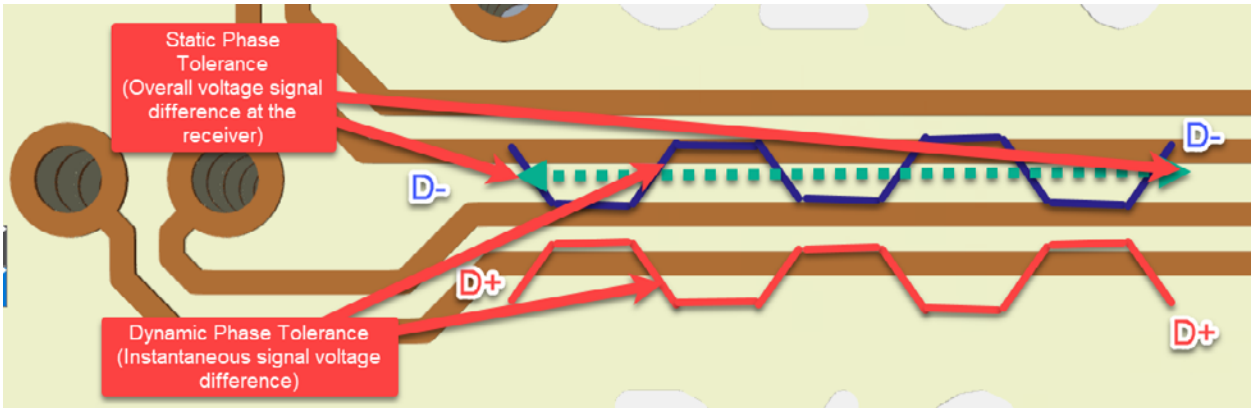


12. To see the analysis of the routed traces with respect to their pin delays and Relative Delays, right click on the Match Group just created (DDR_DQ(32)), then choose Analyze.
13. There will be color codes (yellow if not in range, green if fully in range, red if problematic) to show you which traces are within tolerance of the longest Driver Receiver pair.

Impact: Prevents timing issues and ensures reliable data transmission for parallel signal communication (e.g. DDR3).

Differential pairs (High-Speed)

Definition: Rules for routing differential pairs, which are pairs of traces that carry equal and opposite signals.



Differential pairs showing signal propagation with Static Phase vs. Dynamic phase.

This blog on our website explains two important concepts for differential pairs, inter pair skew, and intra pair skew:

"Ideally, synchronized signals need to arrive at their destination simultaneously to ensure there is no loss of data arising from timing issues. In reality, however, differences (even minute) in the propagation paths mean no two signals will ever arrive at the same time. For greater ease of use, components are forgiving and allow for some timing mismatch – known as clock skew – within tolerable limits.

Timing mismatches are most heavily reliant on the length of the traces, resulting in two variations:

- Intra pair skew between two lines of a differential pair, which indicates the timing difference between the positive and negative signal lines. Keeping the mismatch low between the two differential signals allows for more headroom and better noise protection in balanced lines.
- Inter pair skew indicates the timing difference between signals used in data formats that do not have an embedded clock signal. Inter-pair skew can cover both single-ended and differential pairs within a data format, making some signals doubly constrained by skew.

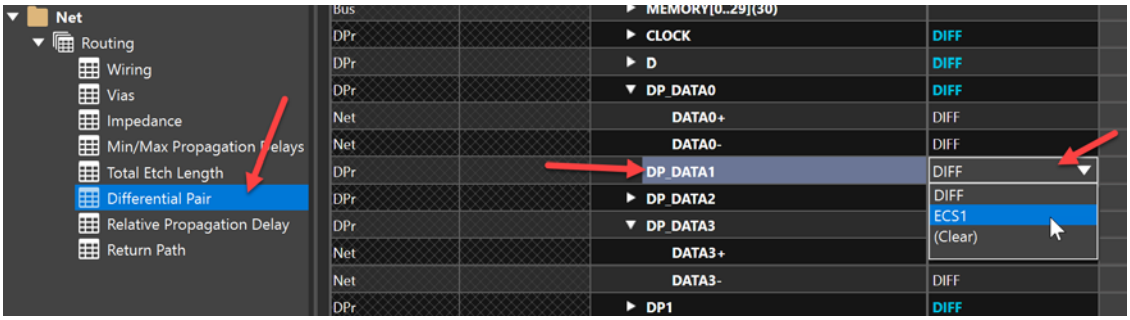
Example: For this example, we will use Constraint manager to ensure differential pairs are routed together with consistent spacing to maintain signal integrity for dynamic signals and for overall length matching.

1. Open the Constraint Manager
2. Go to the worksheet Electrical > Electrical Constraint Set > Routing > Differential Pair.
3. Create a constraint set (e.g. ECS1).
4. Fill in values for Static Phase Tolerance and Dynamic Phase Tolerance as shown below.

Name	Uncoupled Length		Static Phase Tolerance	Dynamic Phase	
	r Control	Max		Max Length	Tolerance
		mm	mm	mm	mm
		*	*	*	*
Cadence_Demo					
DIFF		2.000	6 mm		
ECS1		2.000	2.54 mm	0.508	0.254 mm

5. You should already have values populated for the other parameters. Now apply the constraint set to any relevant diff pairs by going to the worksheet **Electrical > Net > Differential Pair**.

6. Choose the ECS1 Constraint Set we recently made and apply it to any differential pair, say to the DP_DATA1 diff pair.



7. Then the values will appear on the relevant columns (see below).

Objects	Static Phase			Dynamic Phase				Min L Spaci
Name	lerance	Actual	Margin	Max Length	Tolerance	Actual	Margin	
	mm			mm	mm			mm
*		*	*	*	*	*	*	
Cadence_Demo			0.33 mm					0.000
ADDRESS(24)								0.000
DATA(15)	mm			0.508	0.254 mm			0.000
DATA[0..20](19)								
DATA1[0..9](10)								
DDS[0..10](11)								
MEMORY[0..29](30)								
CLOCK								0.107
D								0.107
DP_DATA0								0.107
DATA0+								0.107
DATA0-								0.107
DP_DATA1	mm		0.33 mm	0.508	0.254 mm			0.099
DATA1+	mm		0.33 mm	0.508	0.254 mm			0.099
U1.D6:U2.D5	mm	2.21 mm	0.33 mm	0.508	0.254 mm			
DATA1-	mm			0.508	0.254 mm			0.099
U1.C6:U2.C5	mm			0.508	0.254 mm			

8. Notice that from the analysis (you can right click the DP_DATA1 field then choose Analyze) that our traces are within target tolerances.

Meaning of the Parameters:

Implement specific rules for differential pairs to ensure optimal signal propagation. This includes:

- **Dynamic phase tolerance:** Allow for slight variations in differential pair length matching to account for manufacturing tolerances. Ensuring that this remains as close to 0 as possible, reduces the common mode voltage that can be created by slightly mismatched signals - intra pair skew.
- **Static phase control:** Set strict length matching requirements to minimize skew between the positive and negative signals. Some signals do not have to be matched instantaneously, but their data must arrive at the receiver at the same time.
- **Maximum uncoupled length:** Specify the maximum length that differential pair traces can be routed separately before recoupling. Being uncoupled allows for the introduction of unevenly distributed noise among diff pair traces, which can cause the differential receiver to have a harder time canceling the signal noise.

Impact:

The signals propagating through the differential pairs are in sync in real time and at the receiver. Proper control over the traces for in sync signal behavior reduces noise created from common mode voltages and improves signal timing for high-speed data transmission.

Other High-Speed Constraints

Wiring topology

Set specific routing paths for technologies like DDR3 and T-branch to minimize signal attenuation due to PCB material properties. Or Daisy Chain or star topologies.

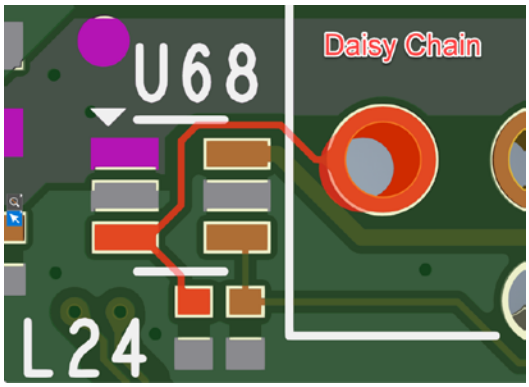


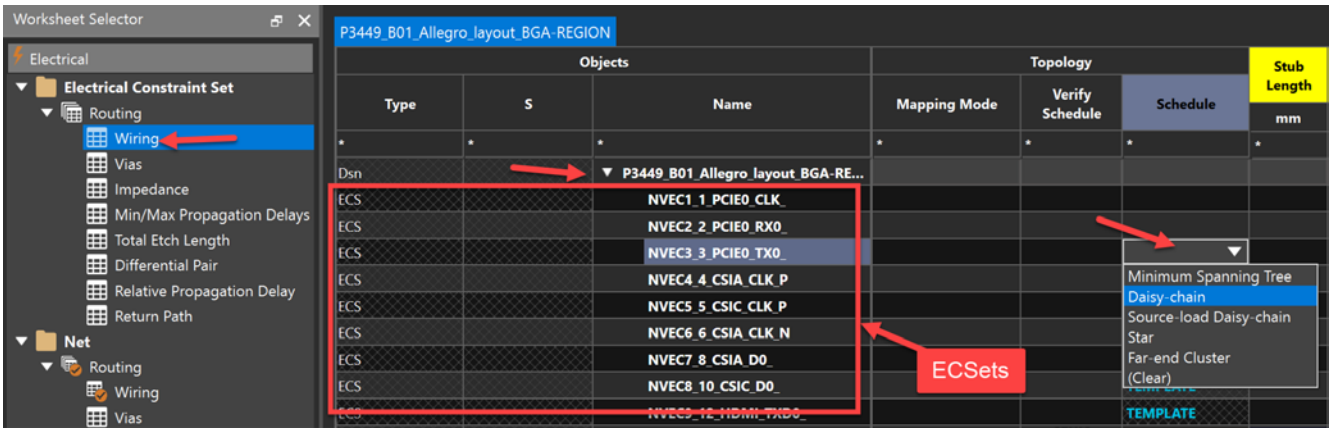
Diagram showing the prioritized routing of critical nets on a PCB

Definition: Wiring topology involves organizing the connections between different nets on a PCB to achieve a certain outcome, such as minimizing signal reflections, signal attenuation or voltage drops.

Example: Let's ensure that a pulse-width modulated net follows a daisy-chain topology.

Steps:

1. Open the Constraint Manager, then go to the Electrical > Electrical Constraint Set > Routing > Wiring spreadsheet.
2. In the Schedule column, you can right click your DSN cell, create a new Electrical Constraint Set (ECS). Notice in the image below, we have multiple ECSets already declared.
3. Select the drop-down in one of the cells in the **Schedule** column and you can choose your net topology.

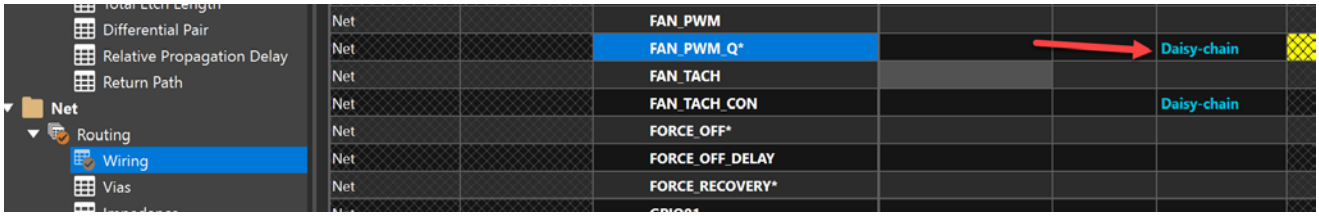


You have options such as:

- Minimum Spanning Tree
- Daisy-chain
- Source-load Daisy-chain
- Star
- Far-end Cluster
- (Clear)

Each topology has its own benefits, depending on the application.

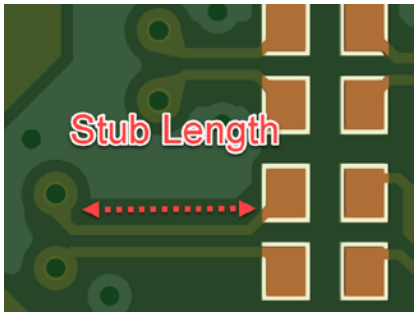
4. Once you have set the topology for that ECSet, you can apply it to the appropriate nets found in the spreadsheet under **Electrical** > **Net** > **Routing** > **Wiring**.
5. In this example, however, you can also directly apply a net schedule directly (see below).



Note: Depending on your use case, you can use either constraint sets or a specific rule application as needed, like in this example. However, please use constraint sets as much as possible to catch the majority of cases first before applying net-specific one-off rules. Using constraint sets modularizes and streamlines your PCB design constraint process and makes you more efficient. The constraint set method also reduces the likelihood of errors and forgotten constraints.

Benefit: Improves signal integrity and timing by ensuring critical connections are made efficiently.

Stub limits (Max Stub Length)



Top view of PCB displaying trace stub length

Maximum Stub Length

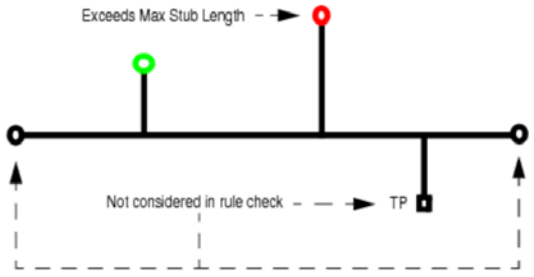
Checks the maximum stub length in design units for daisy chain routing.

Note: When a pin is routed to a connect line, the stub is the line of etch between the pin and the connect line.

The stub length constraint is validated only if NET_SCHEDULE is enabled and RATSNEST_SCHEDULE is set to either MIN_DAISY_CHAIN or MIN_SOURCE_LOAD_DAISY.

>

This check ignores pins at the end of clines, dangling clines, and test points. The chosen net schedule impacts the rule check.



Legal Values: Design Units
DRC Code: ES
Applicable Objects: Xnet, Net, ElectricalCSet, NetClass, DiffPair, Bus, NetGroup
Attribute Name: STUB_LENGTH

A stub as defined in OrCAD X Presto PCB Editor

Purpose: To restrict the number of stubs on a trace's vias or on a net wiring topology to reduce signal reflections and maintain signal integrity. For high-speed designs, aim for zero or minimal stubs. When stubs are unavoidable, keep them as short as possible.

Applies to: USB, HDMI, and any other high-speed interfaces that need minimal fanouts or stubs to operate efficiently.

Importance: Affects current-carrying capacity and signal integrity

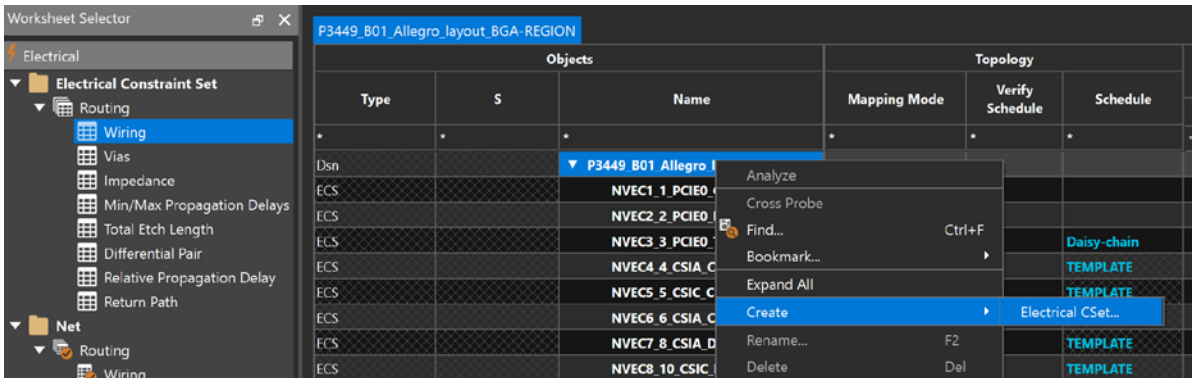
Application: Power distribution, high-speed signals

Steps:

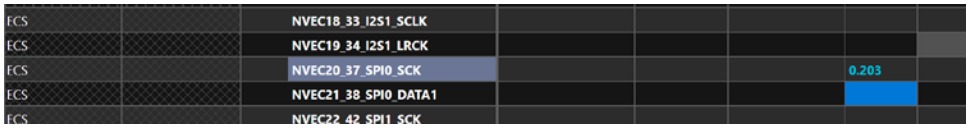
1. Open the Constraint Manager (CM).

Tip: As usual we will make a constraint set that holds the rules/constraints, then we apply that constraint set to a net, class, group or region.

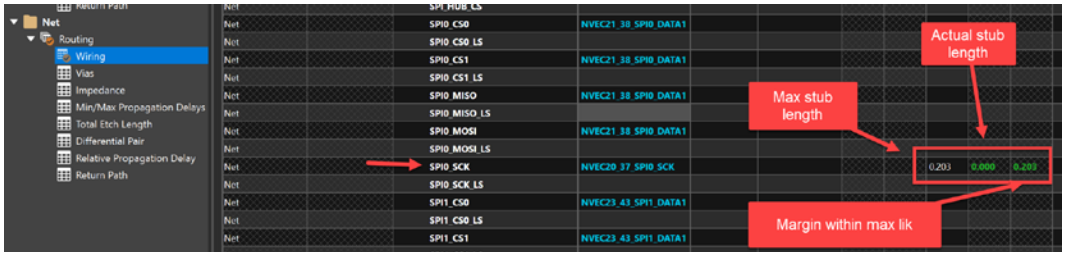
2. Create an electrical constraint set under Electrical > Electrical Constraint Set > Routing > Wiring > Right click the DSN.
3. Choose **Create - Electrical CSet…**



4. Give the ECSet a name and it will be added to the spreadsheet.
5. Once added, enter a desired maximum stub length for the ECSet.
6. For example, let's say you want your stubs to be no more than 8 mils (0.203 mm), so you enter '8 mils' in the rule shown below for the SPI0_SCK signal constraint set.



7. Now you go to the following location to apply that constraint and stub rule it has:
8. In the CM, go to Net > Routing > Wiring.
9. Choose from the **Referenced Electrical CSet** column to set it to your desired net.
10. Notice how the stub length rule applies to the net, with added details like Max, Actual and Margin.



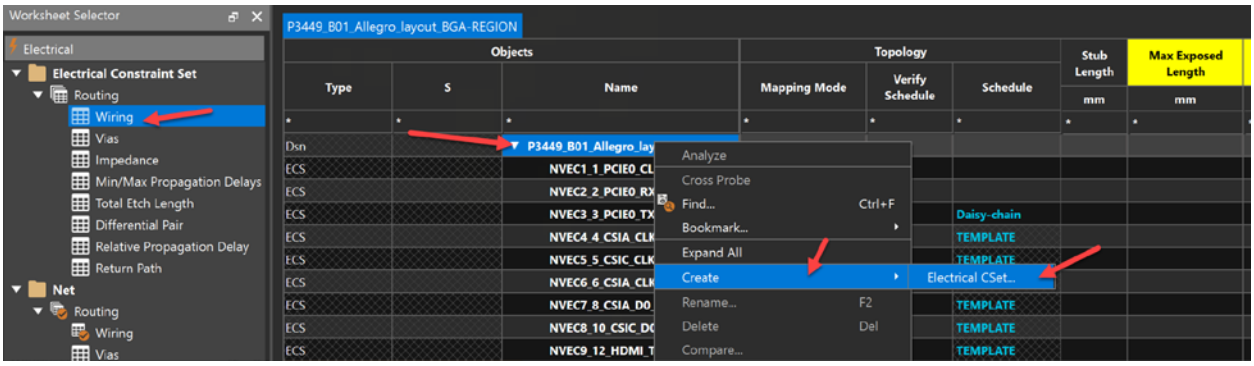
Tip: Use to ensure tight signal integrity, and minimal reflections and antennas.

Maximum stub exposed length

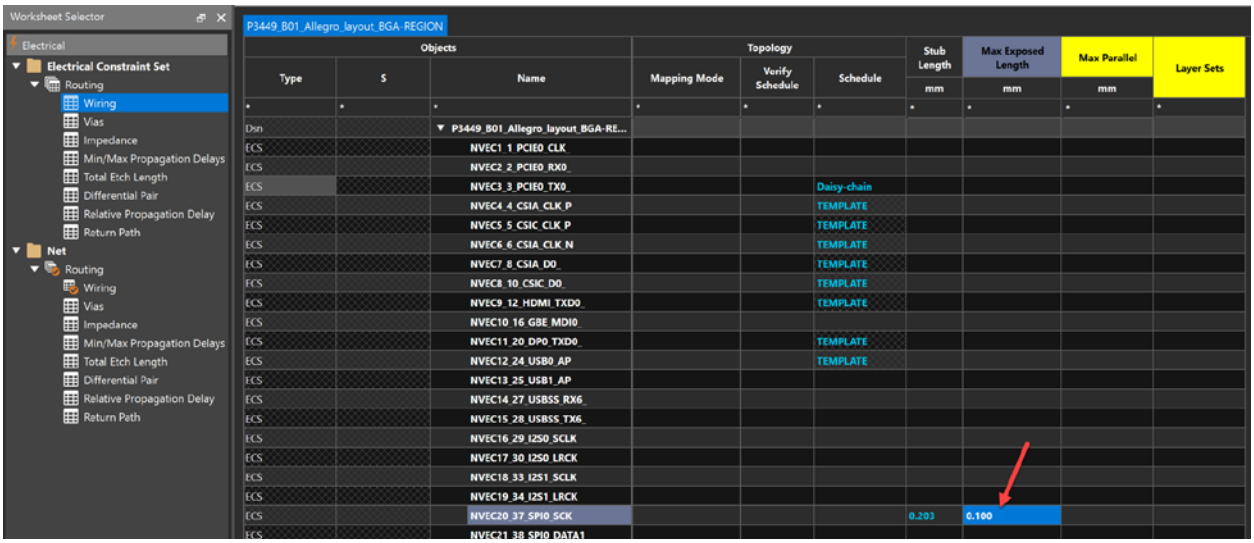
Set a maximum length for exposed stubs to prevent unintentional antenna effects. This is particularly important for high-frequency signals where wavelengths are shorter. A general rule of thumb is to keep stub lengths below 1/20th of the signal's wavelength.

Steps:

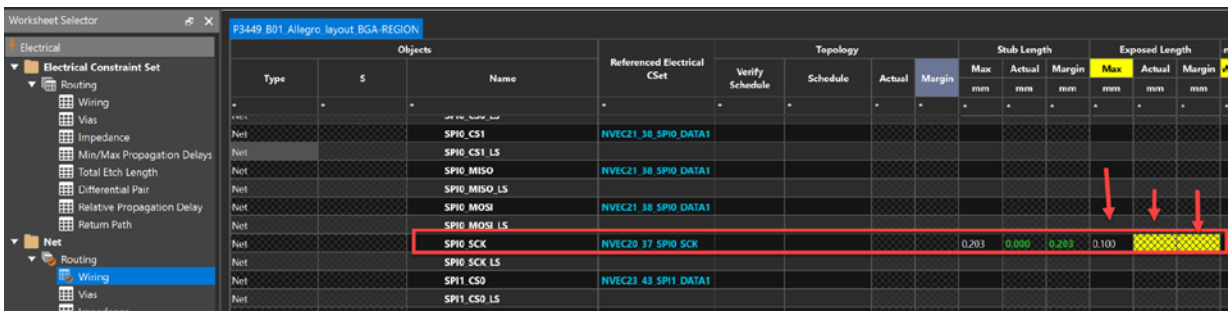
1. Similar to the stub length rule application, open the CM.
2. Create an electrical CSet in the Electrical Constraint Set > Routing > Wiring worksheet.



3. Once created, scroll horizontally and fill in a max exposed trace length (ideally below 1/20th of signal wavelength) in the **Max Exposed Length** field in the row of your desired ECSet.



4. Finally, go to Electrical > Net > Routing > Wiring.
5. Click and apply the appropriate ECSet onto the desired net by selecting the ECSet from the Referenced Electrical CSet column. The rule is automatically applied to that net.

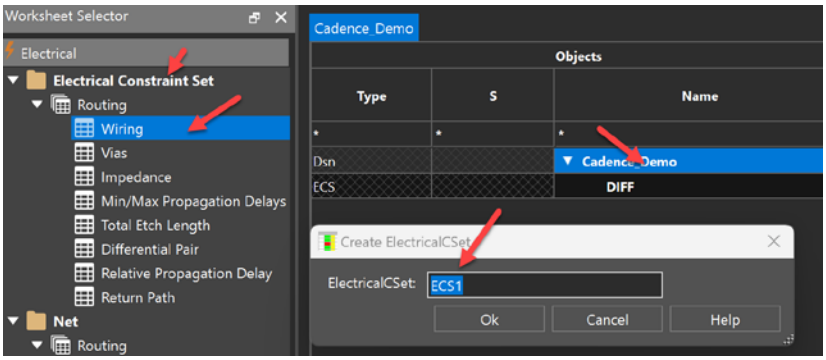


Layer restrictions

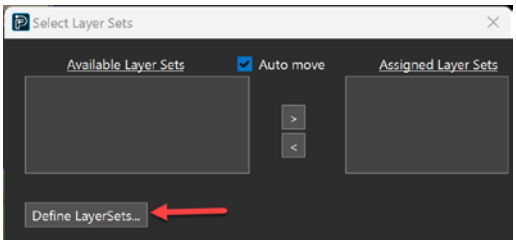
Purpose: Control EMI by limiting the layers through which a trace can be routed. For example, keep high-speed signals on internal layers sandwiched between ground planes for better shielding.

Example:

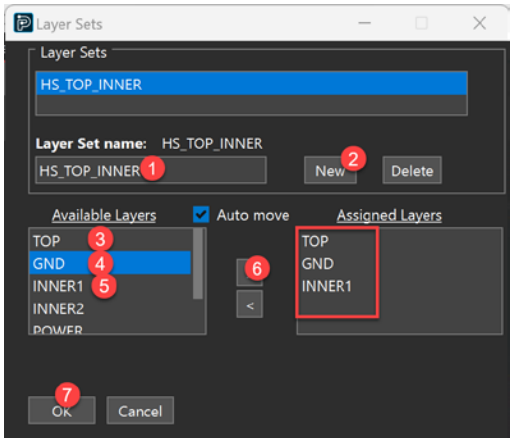
1. Open the Constraint Manager.
2. Go to the worksheet **Electrical Constraint Set > Routing > Wiring**.
3. Create an electrical constraint set and give it a name (e.g. ECS1) shown below.



4. Click the cell under the Layer Sets column that is in the same row as your ECS1 row. The Select Layer Sets window pulls up.

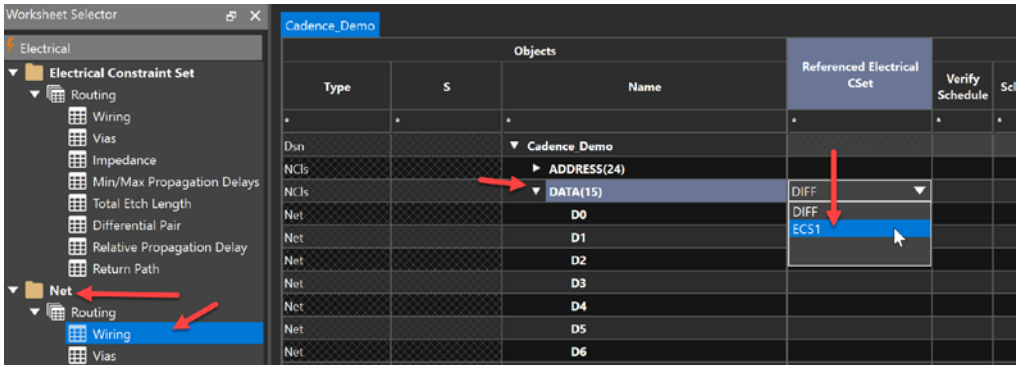


5. We don't have any layer sets defined, so click the Define LayerSets… button.
6. Enter a name for the Layer Set: HS_TOP_INNER, then hit New. That creates the layer set.
7. Next, depending on your application, choose which layers you want this rule to apply to. For example, we would prefer high-speed signals to be routed on the top of the PCB and the inner layer and in some cases the GND layer, but no traces are allowed on the bottom half of the PCB (to control for Capacitive plane couple, controlling the EM signals in the Z-axis, etc.).



8. Click OK. Then you're taken back to the Select Layer Sets window.

9. Click the HS_TOP_INNER from the Available Layer Sets list. It will move over to the Assigned Layer Sets section. Click OK.
10. Finally we will apply this ECSet (ECS1) to the DATA(15) Net Class as an example, as shown below.



11. Scroll horizontally to the final column named Layer Sets.
12. Some nets in the Net Class will pass or fail the Name within the layer set, because not all the nets are routed on the TOP, GND or INNER1 layers. So it is working as intended.

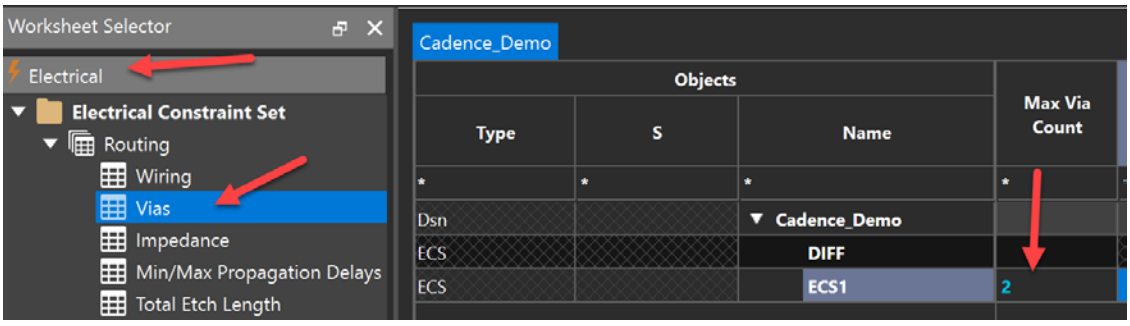
Impact: The layers a signal goes through vertically affect how much coupling and EMI is passed through the PCB. Utilize the constraint manager to avoid unnecessary EMC issues in PCB Design.

Maximum Via Count

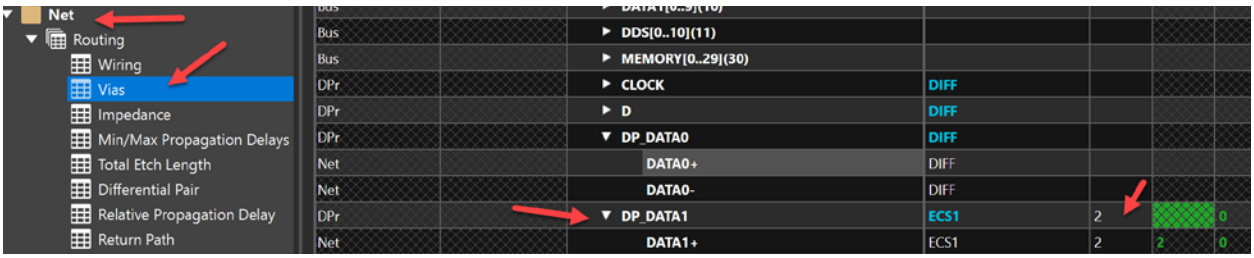
Purpose: Set the maximum number of vias for a trace or net to maintain impedance control and minimize parasitic capacitance. Each via introduces discontinuities and can degrade signal integrity, especially at high frequencies.

Steps:

1. Open the Constraint Manager.
2. Navigate to the Electrical > Electrical Constraint Set > Routing > Vias worksheet.
3. Then either by creating a constraint set or using an existing one (like the ECS1 below), set the Max Via Count to 2.



4. Now you can apply this constraint set to specific differential pairs or nets by going to the Electrical > Net > Routing > Vias worksheet.



5. In our case, the DP_DATA1 has the ECS1 Constraint set and the via limits applied. Notice how the actual number of vias on the DP_DATA1 differential pair are within the acceptable limit of vias established in the Electrical Constraint Set (ECS1).

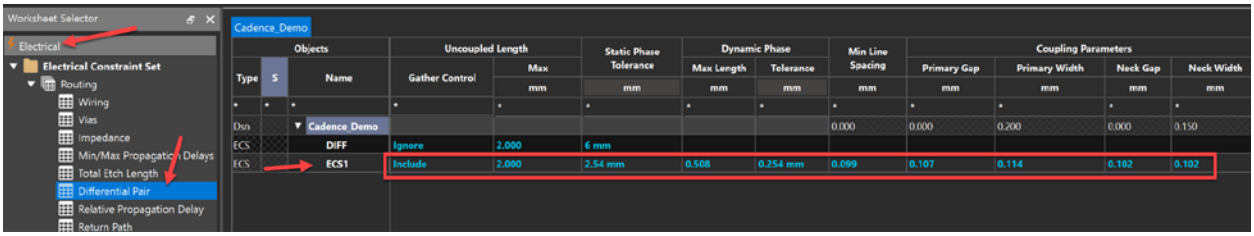
Impact: It is easy to forget so many important factors in PCB design that are all crucial for high-speed designs. For instance, for USB 3.2, it's strongly recommended to use no vias or layer transitions. However, if transitions (vias) are needed, to use no more than two. Constraining the number of vias ensures that we do not inadvertently introduce errors into our board because of forgetting the via limits. Let the constraint manager do the remembering for you as a designer.

Example Constraints for Common Applications

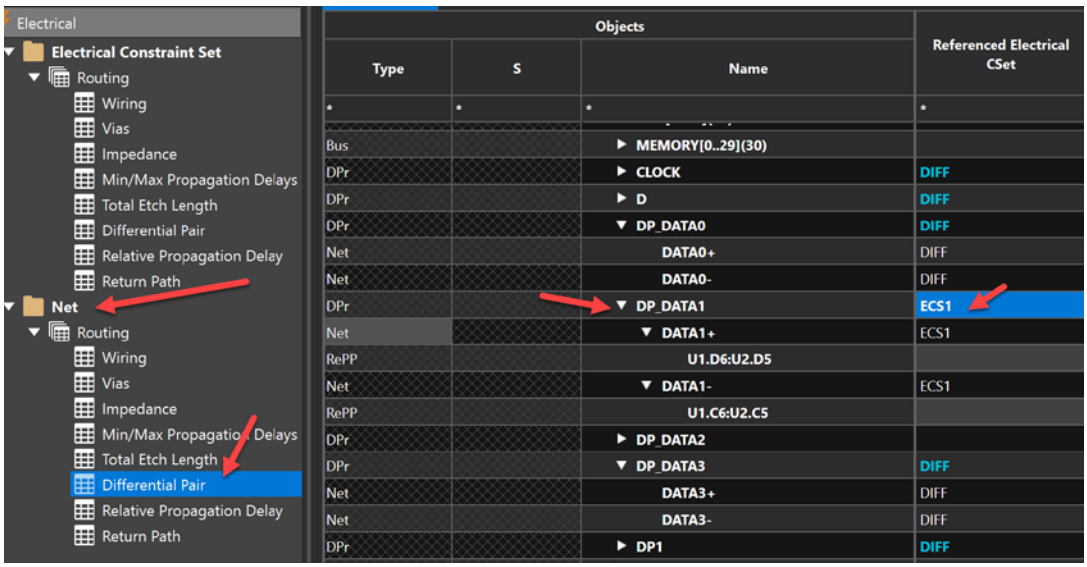
USB (Universal Serial Bus) Constraints

1. Define differential pair routing rules:

   a. Set your constraint set and rules in the Electrical > Electrical Constraint Set > Routing > Differential Pair worksheet.



   b. Then apply that constraint set to the relevant differential pair in the **Electrical > Net Routing > Differential Pair** worksheet (e.g. ECS1).



2. Next, set impedance control for high-speed signals so they automatically adjust their widths during layer transitions (sometimes our calculations for physical constraints on the differential pair don't always hold when stackup changes are made, but the field solver in the OrCAD X PCB software calculates the widths for us in real-time to fix this).

   a. Set the constraint and values for impedance in the Electrical Constraint Set > Routing > Impedance worksheet.

   b. For USB 2.0 and 3.2 you can set them at 50 Ohms with 2-10% tolerance (to be in the 100 Ohm differential impedance range) for single ended impedance (check with your manufacturer for tolerances they can provide for impedance).

   c. Follow the instructions on impedance constraints and application.

3. Establish length matching for data lines:

a. For USB Data+ and Data- signal traces, follow the Differential Pairs setup sections for Basic setup, Spacing setup and high-speed constraint setup.

4. Configure EMC rules:

a. For EMC, the differential pairs on USB 3.0 and higher usually need to be restricted to specific layers on the PCB.

b. Refer to the Layer restrictions section of this document for instructions on how to set up the right layers for your USB signals.

Double Data Rate (DDR) Constraints

- Differential pair skew control
  - Set your differential pair rules according to the basic, spacing and high-speed instructions for differential pairs in this document guide
- Differential pair common-mode voltage constraints
  - Refer to the dynamic and Static Phase control parameters in the high-speed differential pair sections
- Set up length matching for address and control signals
  - Please refer to the Length matching section of this document (utilizing relative propagation delays and driver pin settings)
- Define timing constraints for setup and hold times
  - Outside the scope of this document. Please refer to Cadence signal integrity guides and courses
- Establish impedance control for data lines
  - Please see the Impedance Control section of this document
- Configure termination requirements
  - Outside the scope of this document
- Routing topology depending on the DDR protocol (DDR2, 3, 4, etc. like minimum spanning tree, T-topology, fly-by topology, etc.)
  - Instructions found in the Wiring Topology section of this document

Rigid-Flex PCB Constraints

- Define bend radius limitations for flex areas
  - Not applicable to the Constraint Manager guide
- Set up layer stack rules for transition areas
  - Found in the Layer restrictions section of this document
- Establish component placement restrictions on flex sections (keep out)
  - Found in the Component Spacing constraints section of this document
- Establish routing areas (bend-only, non-bend, etc.)
  - Not applicable to the constraint document - please see Rigid Flex guide
- Configure VIA usage rules in flex regions
  - Via Limits can be found in the Maximum via count section of this document
  - Via rules for flex regions can be found in the Manufacturing Constraints section under DFF Constraint Set and Design sections. Please see the Manufacturing section for more step by step information on how to implement those constraints.

RF (Radio Frequency) Circuit Constraints

- Define impedance control for RF transmission lines
  - You may use the standard Impedance control instructions in the Impedance Control section
- Set up rules for RF shielding and isolation
  - Not directly supported in OrCAD X Presto PCB Editor
- Establish guidelines for component placement to minimize interference
  - Please see the component spacing sections in this document
- Configure constraints for antenna design and placement
  - Outside the scope of this document

Conclusion of Part 3 - Advanced Constraints

In Part 3 of the OrCAD X Constraint Manager Guide, we delved into advanced constraints critical for managing complex PCB designs. By mastering high-speed constraints and electrical design rules such as net scheduling, impedance control, and differential pairs routing, designers can ensure optimal performance and reliability in cutting-edge technologies. These constraints are essential for high-speed interfaces like USB, DDR, PCIe, and RF circuits, where precise control over signal integrity and timing is paramount.

As we transition into Part 4, Constraints Optimization, we will explore techniques to enhance design efficiency and flexibility. This section will guide power users through the effective use of EC Sets, schematic-to-PCB constraints, and modular approaches, offering tools to refine design processes and achieve superior results. Prepare to elevate your constraint management skills to a new level of sophistication and efficiency.