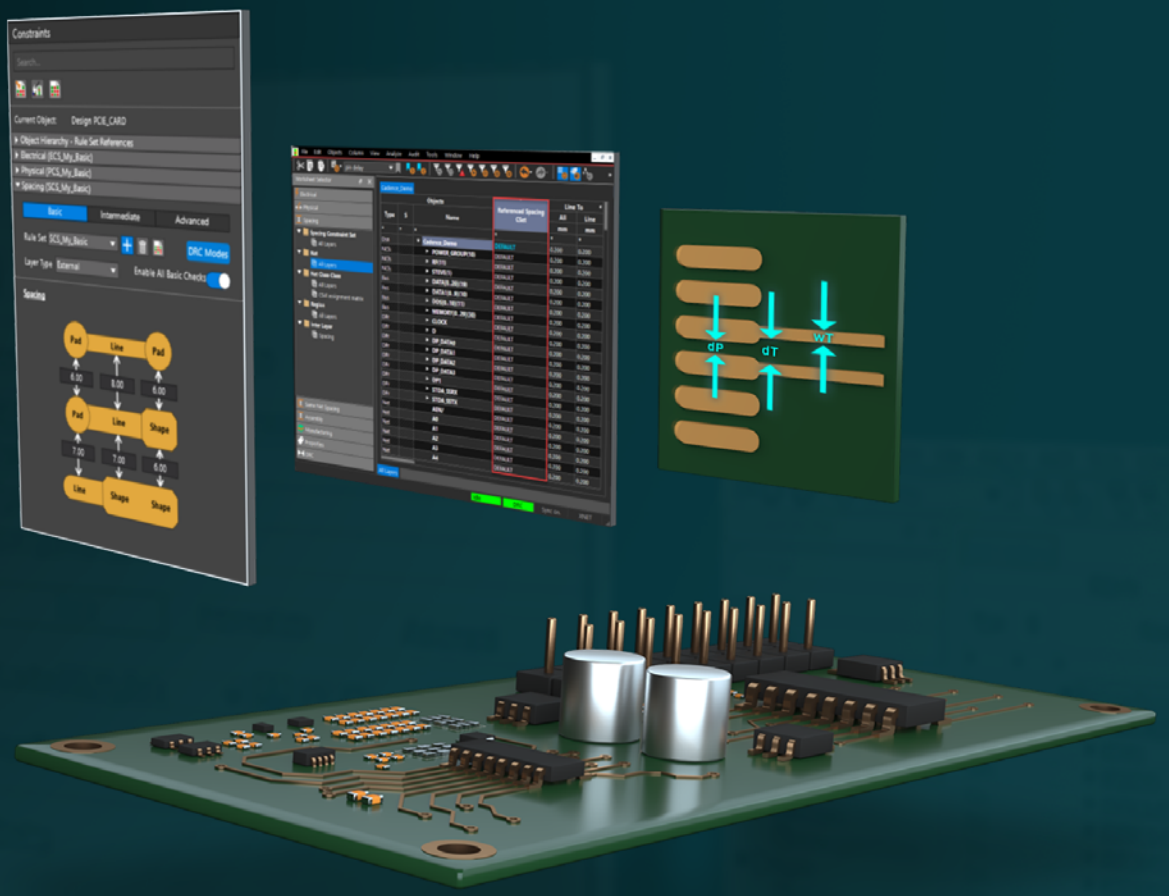
DESIGN **GUIDE**

cadence®

OrCAD X Constraint Management Guide

Part 5 of 5



Contents

Part 5 – Project Example in OrCAD X

In this part of the document, instead of walking you through the steps to execute each constraint set, we simply show you the constraints applied in the design and why. Let's look at the FPGA project that uses DDR2 and DDR3 memory.

Now that you know about constraint management in OrCAD X, the question remains, how do we implement constraints optimally from start to finish on a real design? In Part 5 we will guide you through utilizing the Constraint Manager from OrCAD X Capture to Presto PCB Editor to ensure you have a properly constrained design.

Hardware Design Project

Here is a picture of the project schematic shown below:

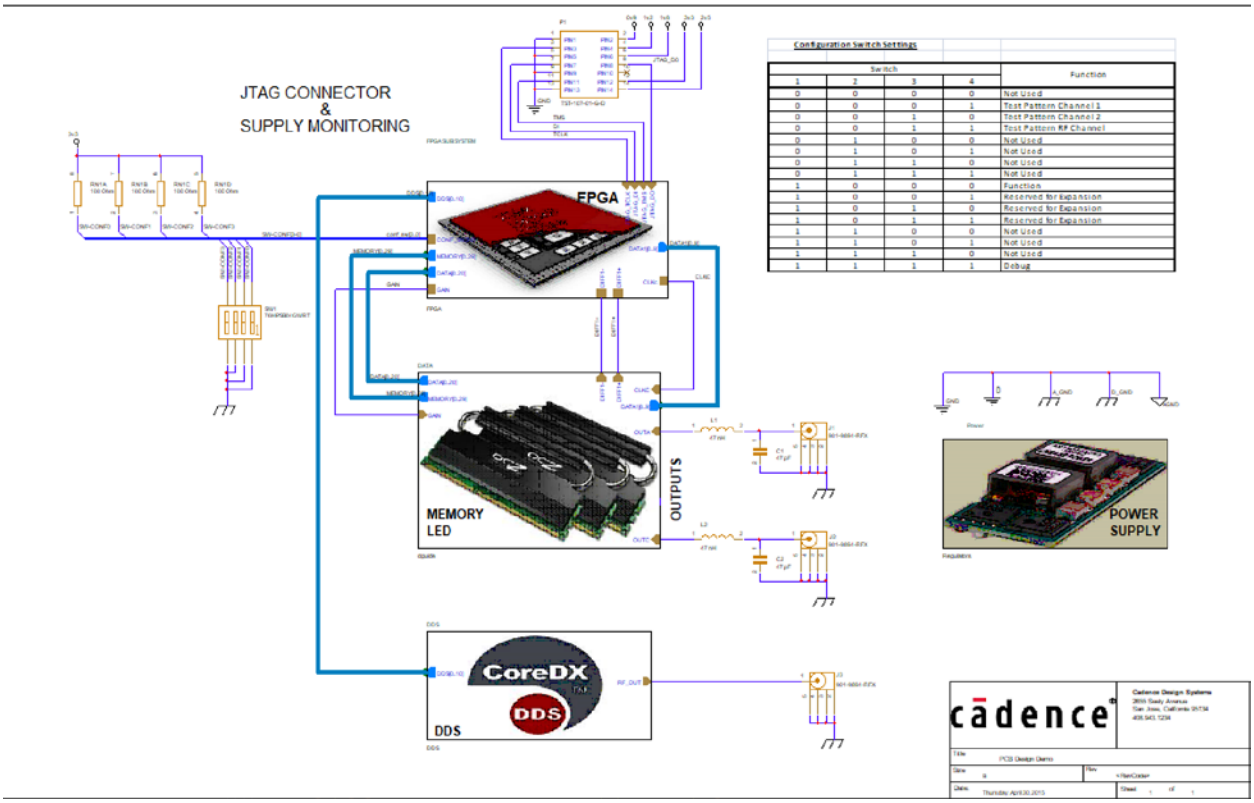


Figure 1. Project Schematic

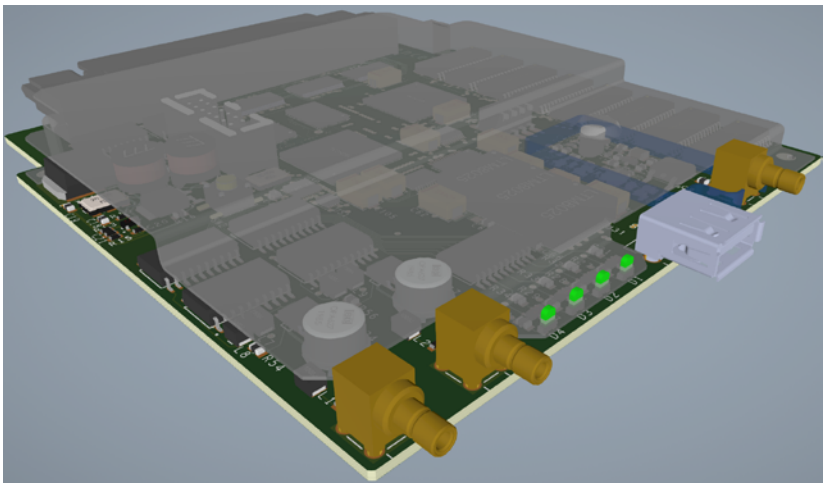


Figure 2. 3D View of High-speed PCB assembly for Constraint Management Demo

Modern Hardware Design Process

1. Planning
2. Electronics Design
3. Components (selection, models, etc.)
4. Schematic Capture and Simulation
5. Constraint Management, Netlisting, and Bill of Materials
6. PCB Stackup and Signal Integrity Analysis
7. Constraints Management for PCB and Pre-routing
8. Component Placement
9. Wiring
10. Design Rule Checks and final touches

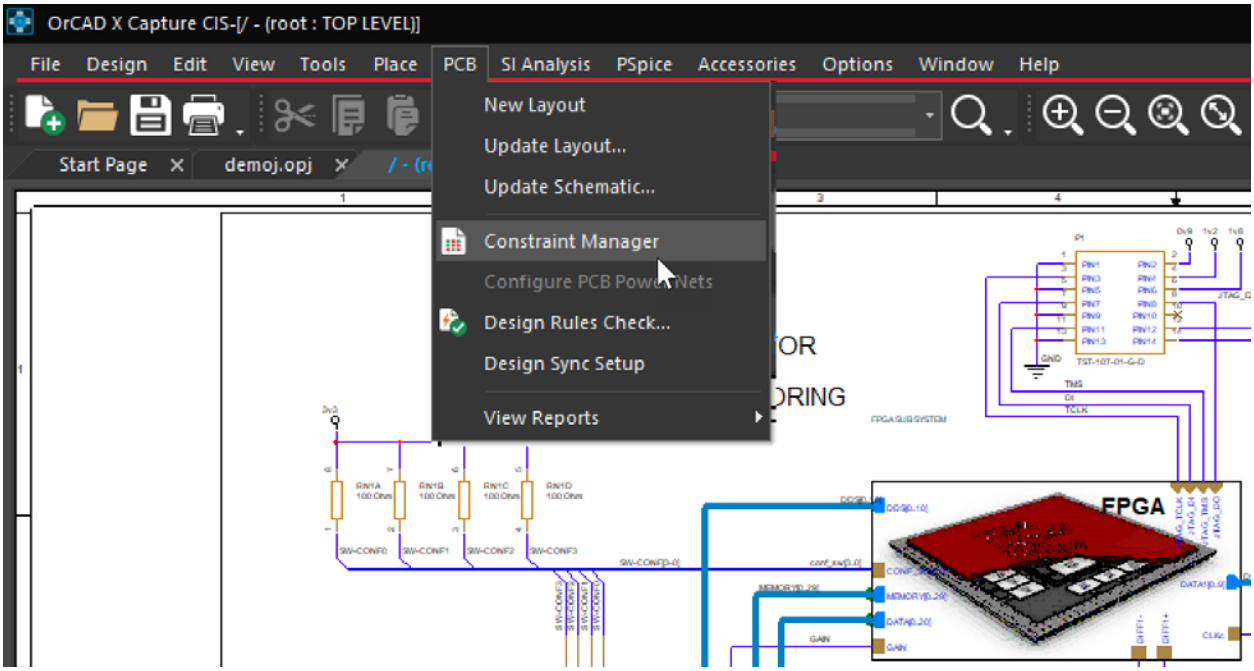
Organize the Nets

Identify nets that are suitable for net classes, net groups, and constraint regions.

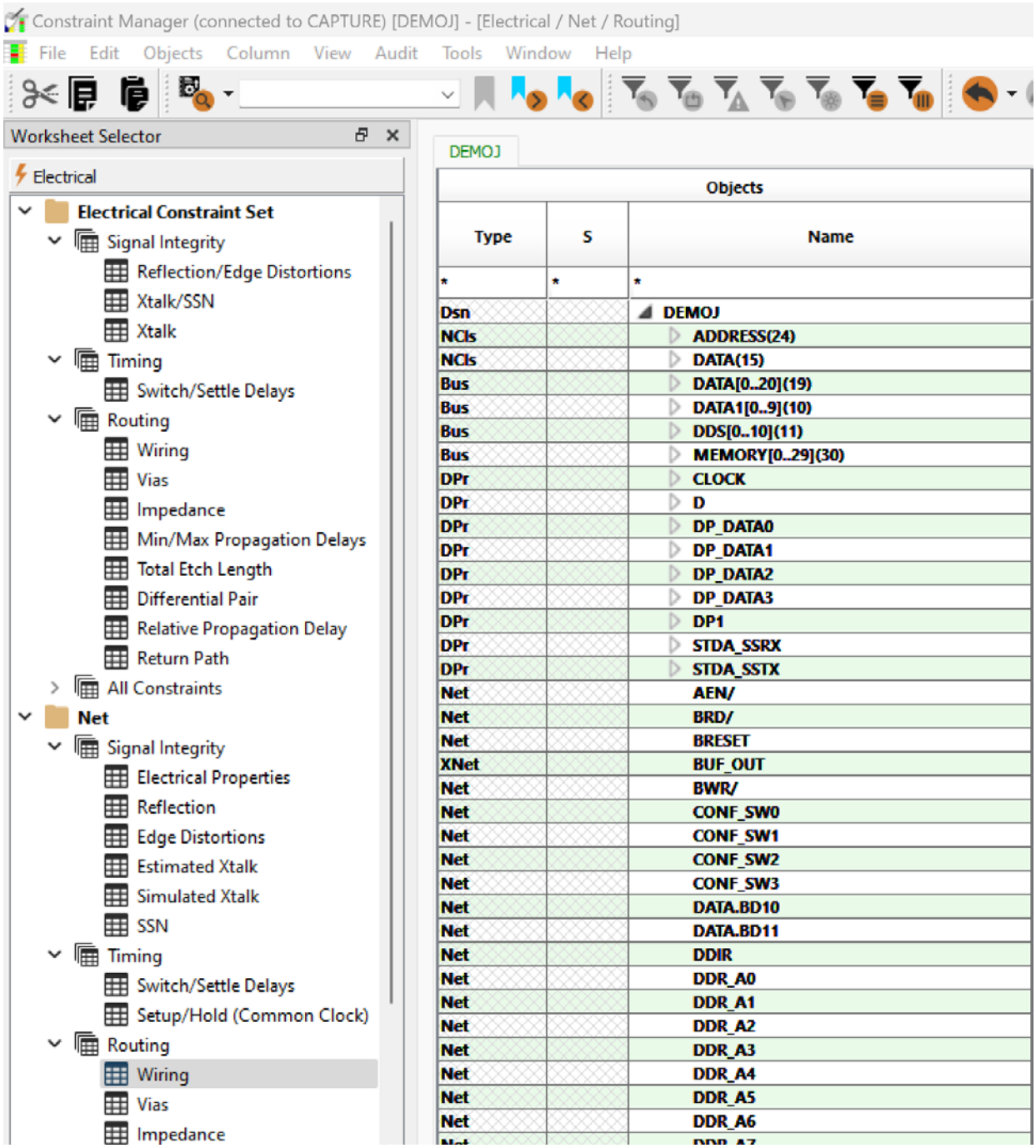
Define Net Classes

At this stage the engineers have defined the net classes. To do that in OrCAD X Capture you would:

1. Open Constraint Manager from the main toolbar menu: PCB > Constraint Manager.



2. Navigate to the **Electrical > Net > Routing > Wiring** worksheet.



3. You will see all the nets listed in alphabetical order. Notice the name of the project **DEMOJ** and its row is labeled **Dsn (DSN refers to the OrCAD X project file extension)**. Also notice the other rows are labeled as:

   a. NCls = Net Class

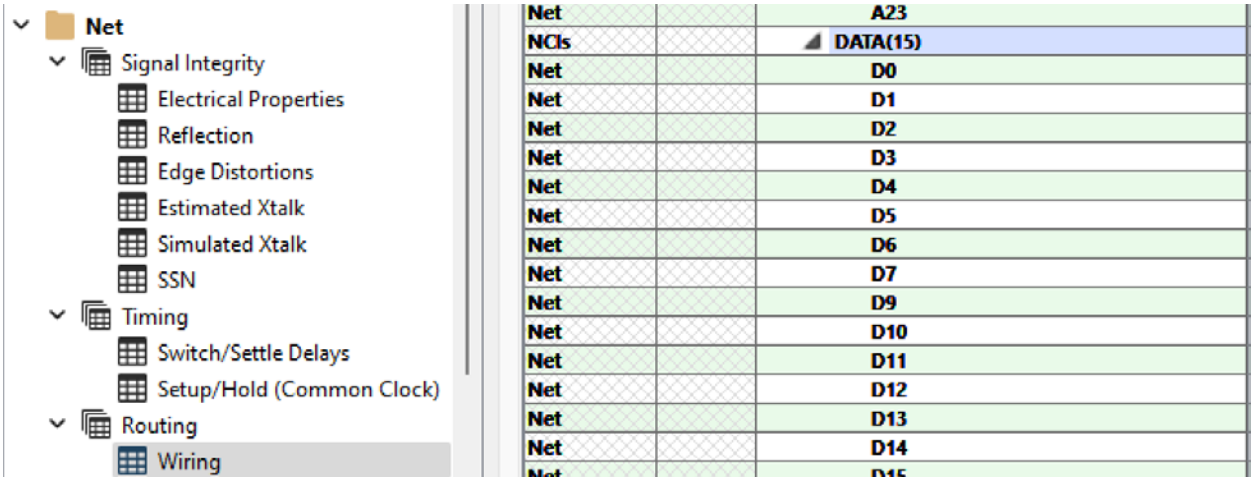
   b. Bus = Bus

   c. DPr = Differential Pair

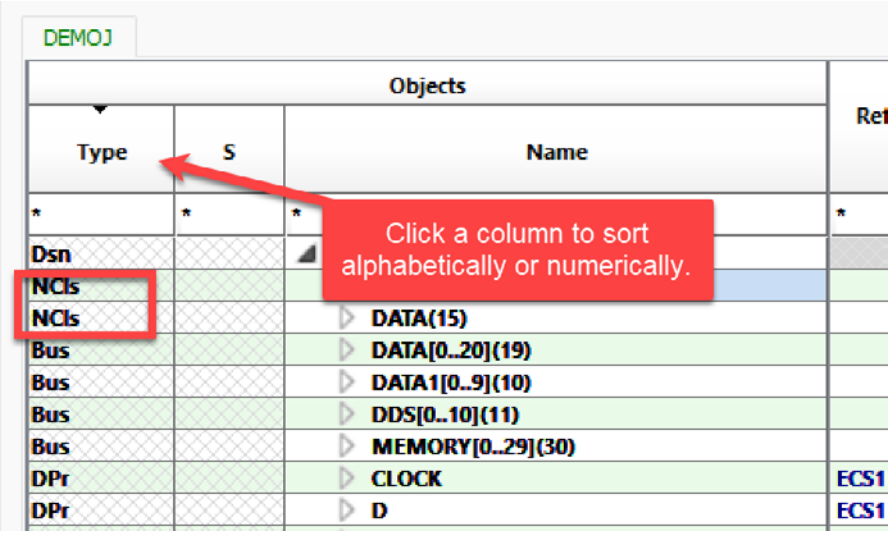
   d. XNet = Extended Net

   e. NGr = Net Group

4. These labels will help you to quickly identify the type of group or organization the nets are placed into.
5. Notice we have a net class named **DATA**(15) (it's named DATA but it has 15 members)



6. As shown in previous parts of the guide, you can create a net class by highlighting the nets you want in that class, then right clicking any of the highlighted nets, then choosing **Create – Net Class**, naming that class then clicking OK.
7. That has been repeated to create the net classes shown below.



As shown in the first part of this document, Net Classes are often not enough to organize all our nets. Net Classes organize nets by physical and electrical properties, but oftentimes we also need to organize nets by function, regardless of their properties. Let's look at the Net Groups defined in this project.

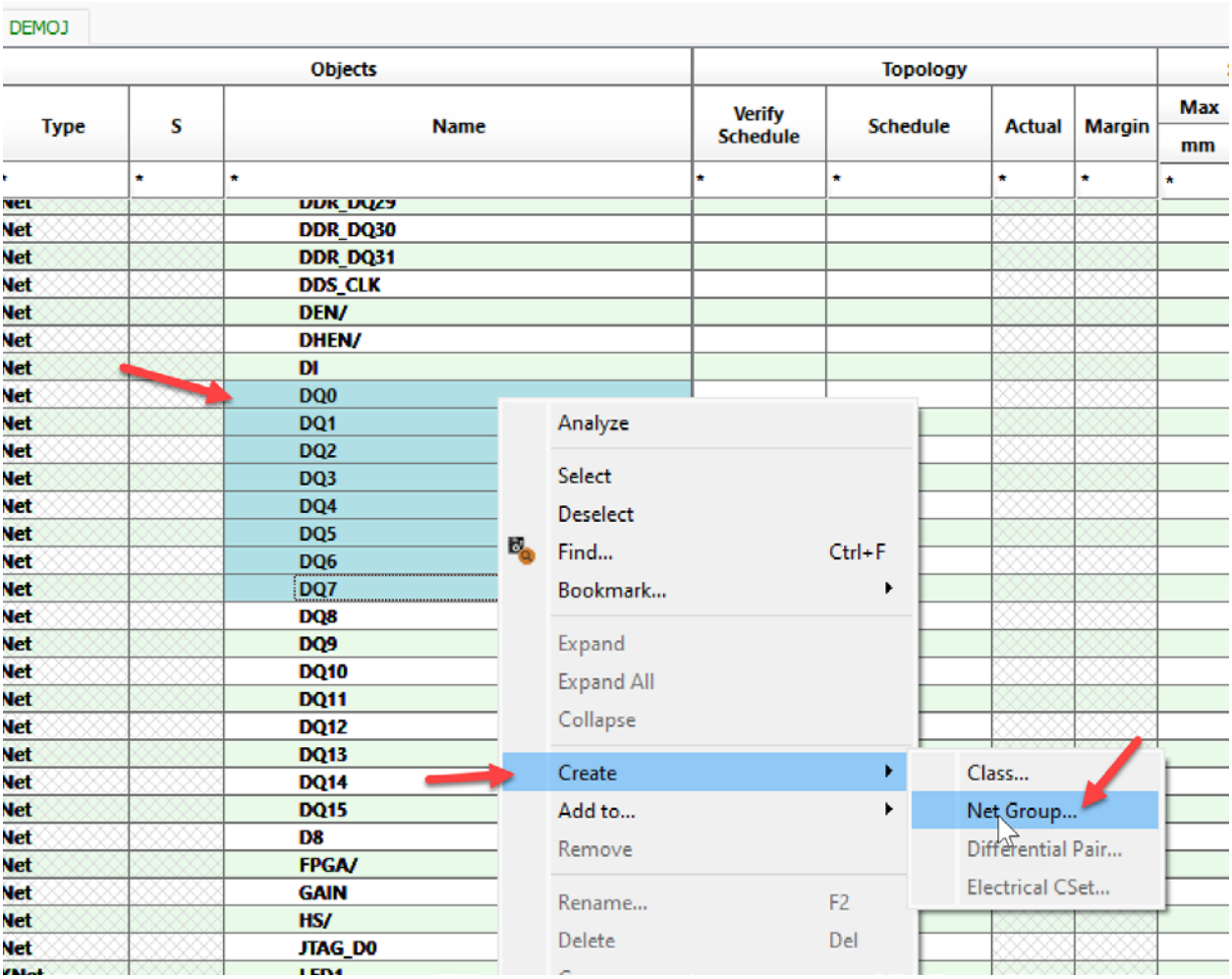
Define Net Groups

We also need to define our net groups for the following (e.g. for HDMI, USB, DDR2, DDR3, or any important functional groups etc.)

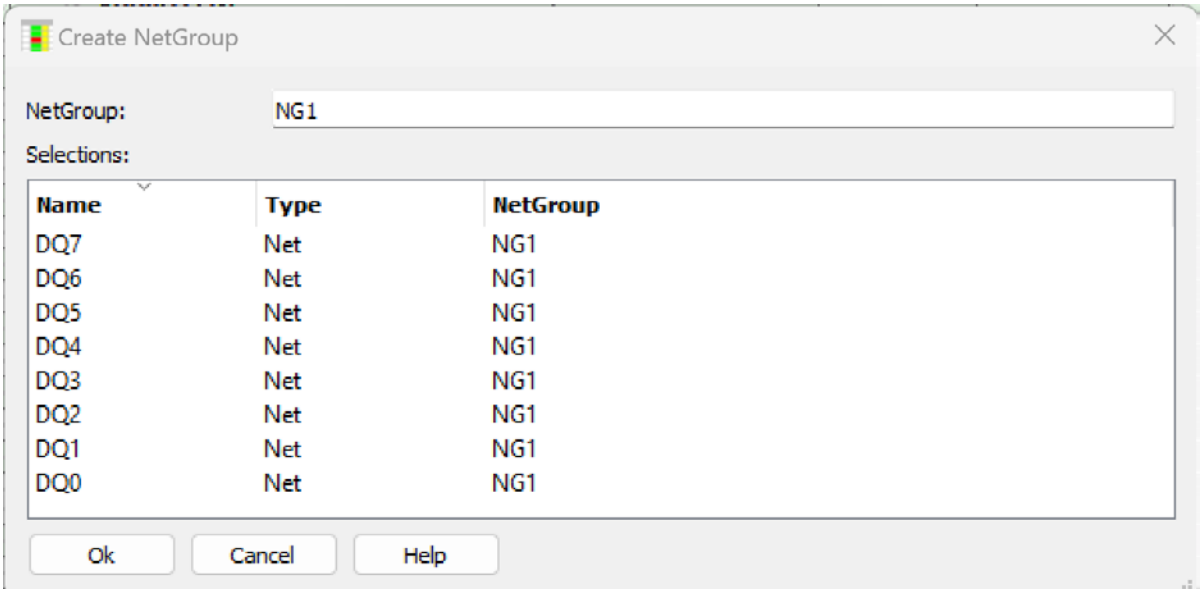
Within the Constraint Manager in OrCAD X Capture:

8. Go back to the **Electrical > Routing > Wiring** worksheet.
9. You will see all the nets in your design, along with their organizational labels (NCls, DPr, etc.)

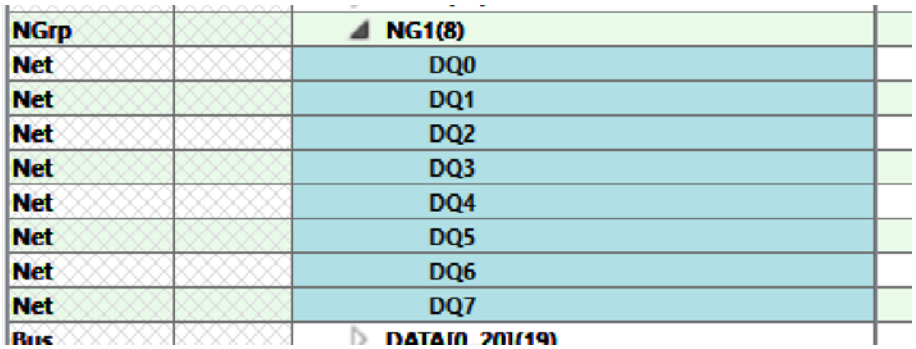
10. Let's create some net groups by right clicking a selection of nets, for example DQ0 – DQ7, then right click, choose **Create – Net Group…**



11. Then choose a name like NG1, then click **OK**. Typically, the default names work well for groups and classes.



12. Now you have a net group you can further create constraints (see below).



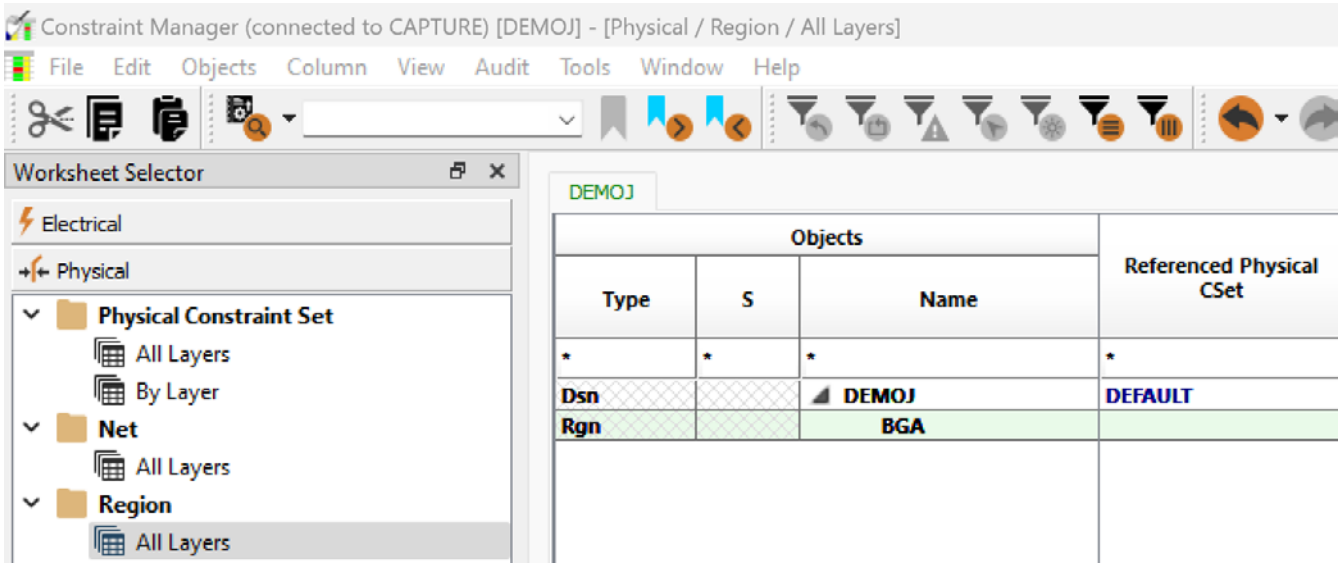
We will not create constraints here, but they will come in handy after all our groups, net classes and regions are set up.

Next consider making a constraint region for the DDR2 and DDR3 devices.

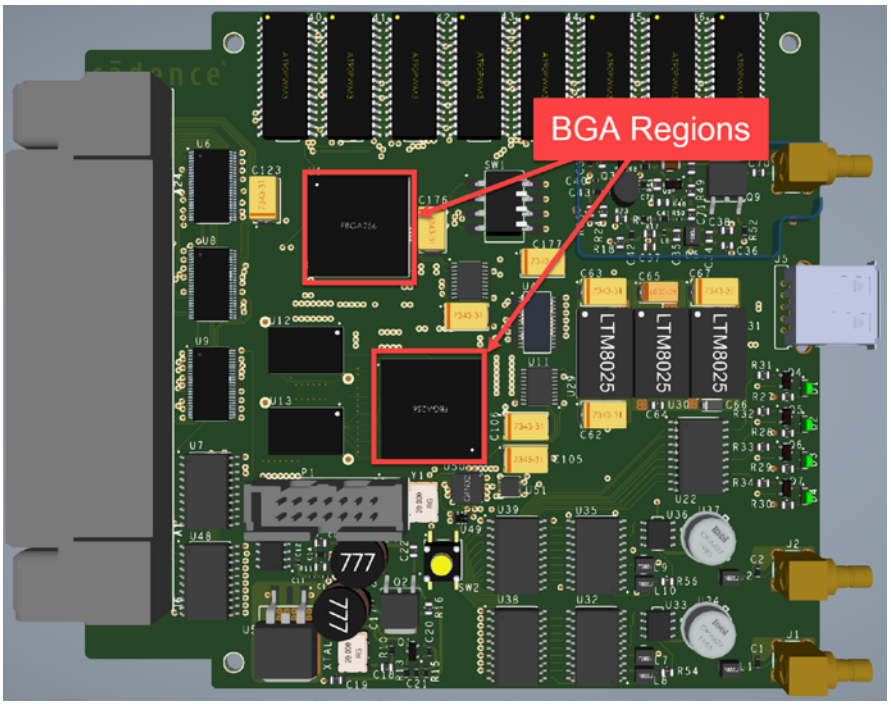
Decide On Constraint Regions

In this schematic, we have memory modules and devices that will likely need special routing spacing. So let us make two constraint regions in preparation for that, even if we do not have to use them later.

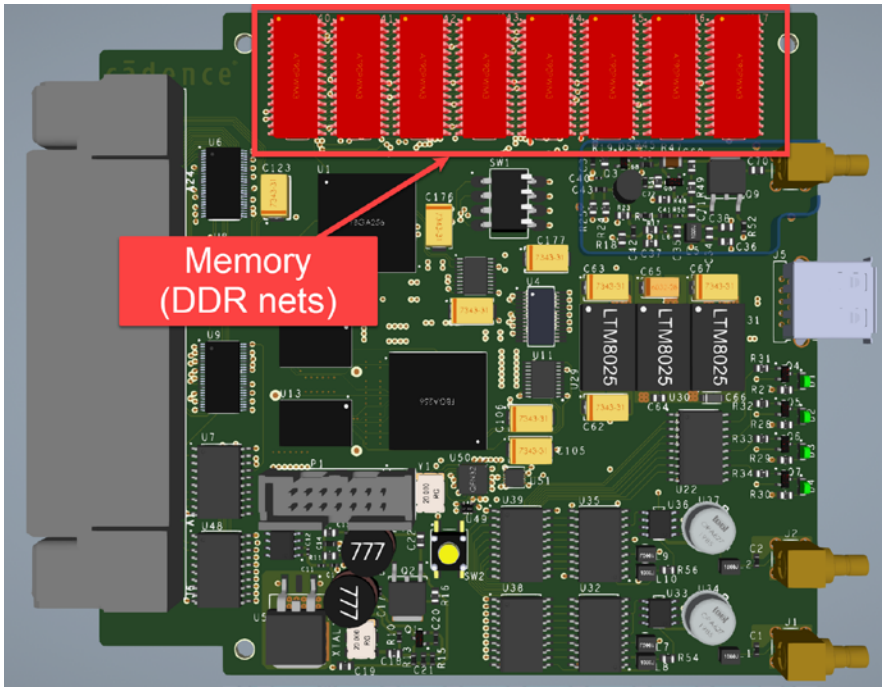
1. Open the Constraint Manager in OrCAD X Capture.
2. In the constraint manager, go to **Physical > Region > All Layers**.



We already have a region defined named BGA, but let's add DDR2 and DDR3 just in case we need special rules for those trace widths in that area of the PCB. In the image below, you can see the areas and chips where the BGA region would apply on the PCB.



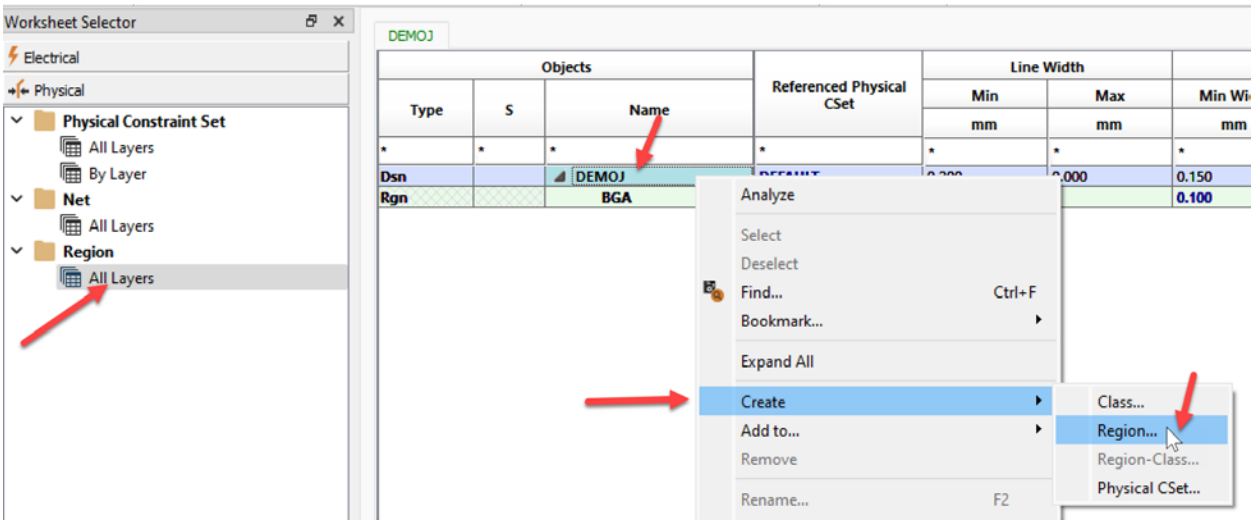
Also, below you can see where the DDR regions we create will apply to the design.



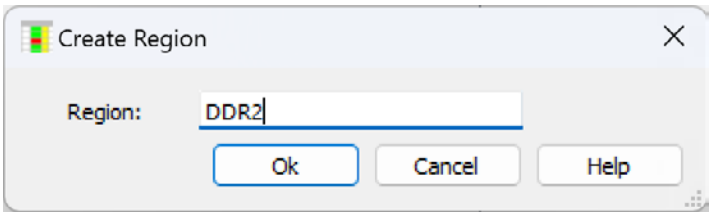
Note: Physical region definition is for physical attributes only. We would need to create a region for spacing rules as well.

TIP: Recall that even though we have net classes and groups, we still need specific rules in certain parts of the PCB across different layers (or all) for that area sometimes so we can deviate from the default, class, and group net routing and spacing rules. Please refer to our complete section on Constraint Regions in a previous part of this guide.

3. To create a new **Physical** region, right click the cell named **DEMOJ, Create – Region**.

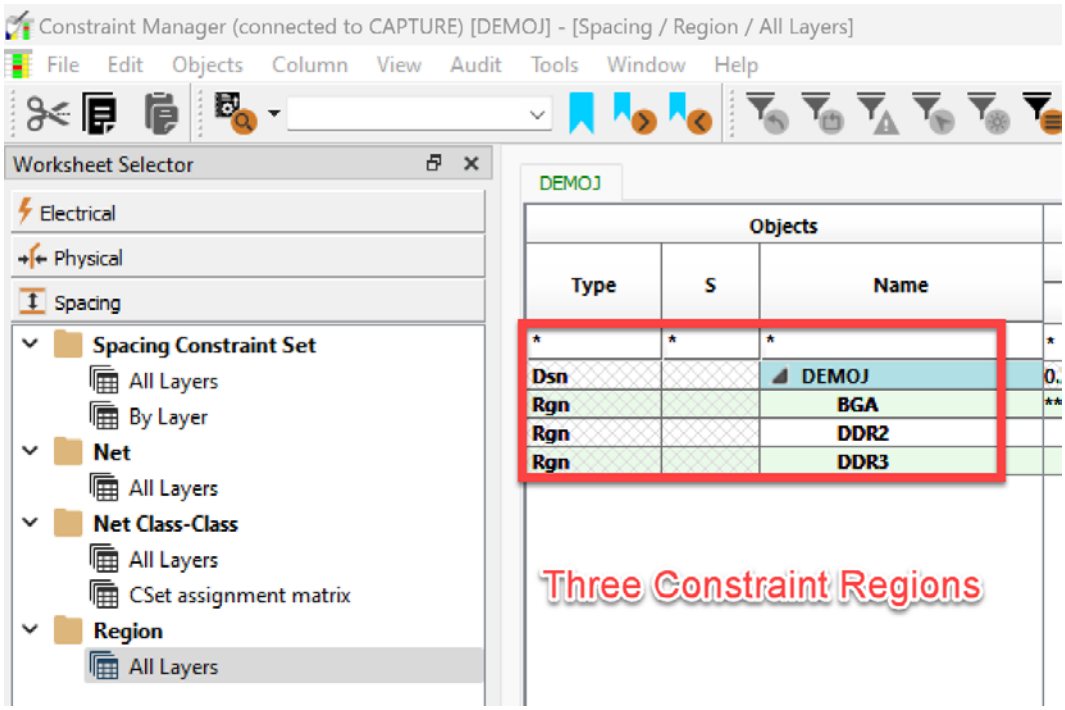


4. A Create Region window appears. Name the Region a relevant name, like DDR2 for example. Click OK.



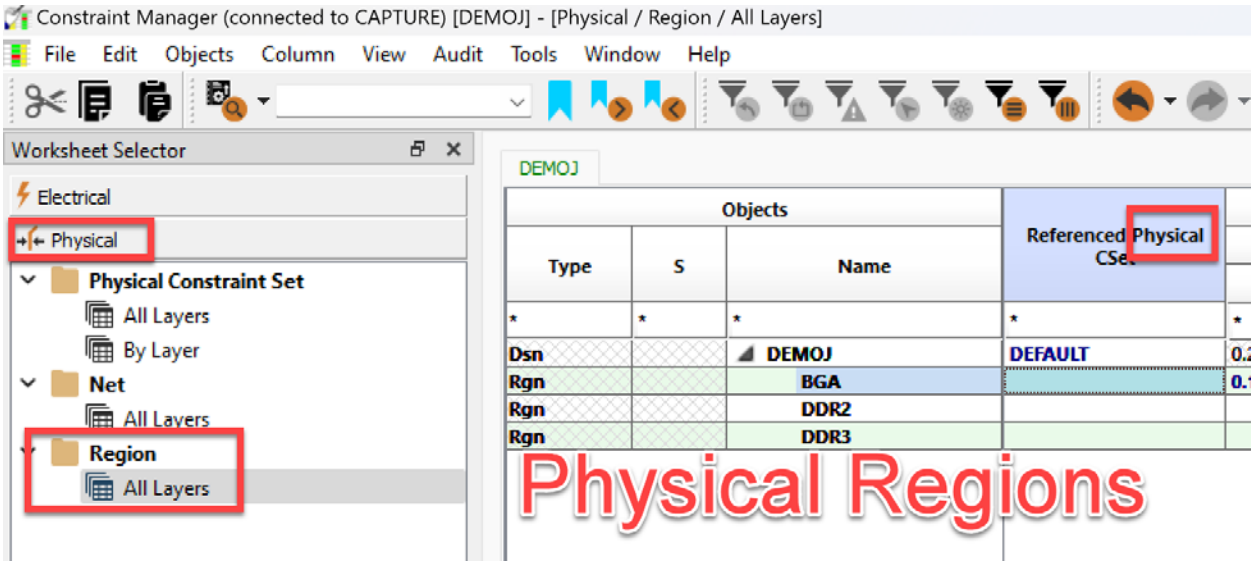
Once that's done, your region will appear in alphabetical order with the other regions in the worksheet.

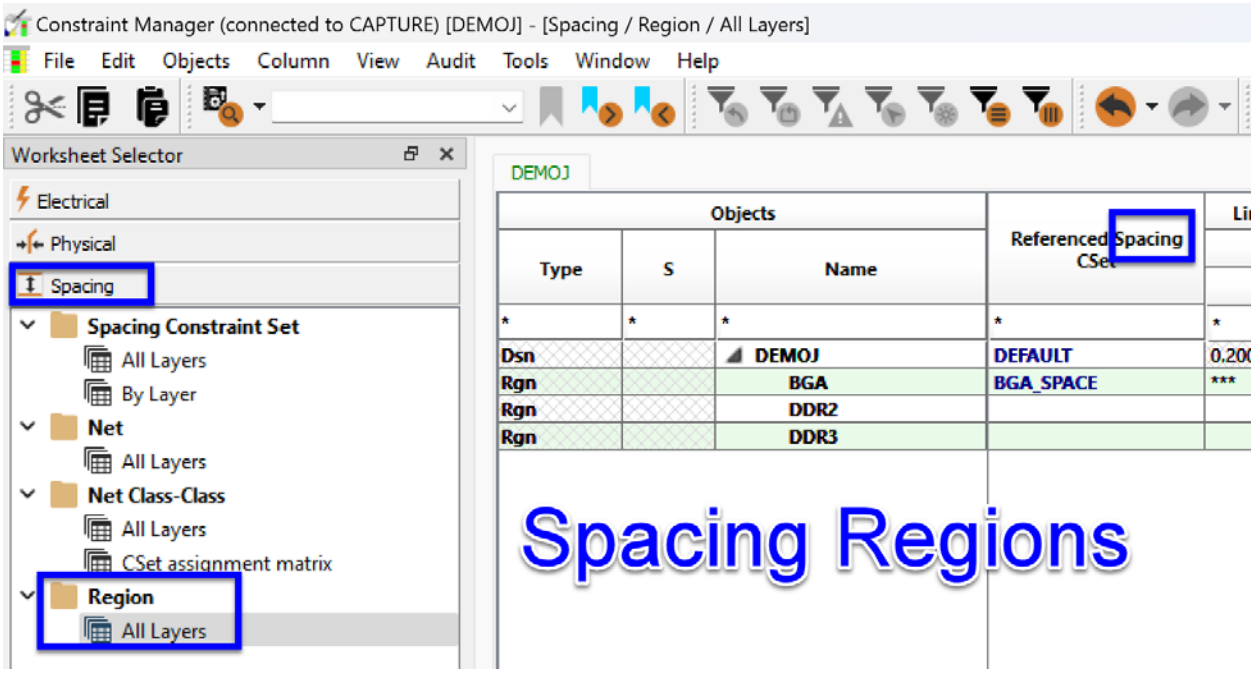
5. Repeat steps 3 through 4 to create a physical region named DDR3. You will then see the list of regions you created as shown below.



Setting Spacing Regions

Notice how the **Spacing** regions were automatically created in the Constraint Manager **Spacing – Region – All Layers** worksheet, like the Constraint Manager **Physical – Region – All Layers** worksheet.





This region distinction is here to remind us that we need to define Physical constraint sets and Spacing constraint sets separately and add them as separate constraints onto physical and spacing net classes, groups and regions.

The overlapping constraint sets create a beautiful matrix of rules that make everything adhere to your requirements reliably, robustly and effortlessly.

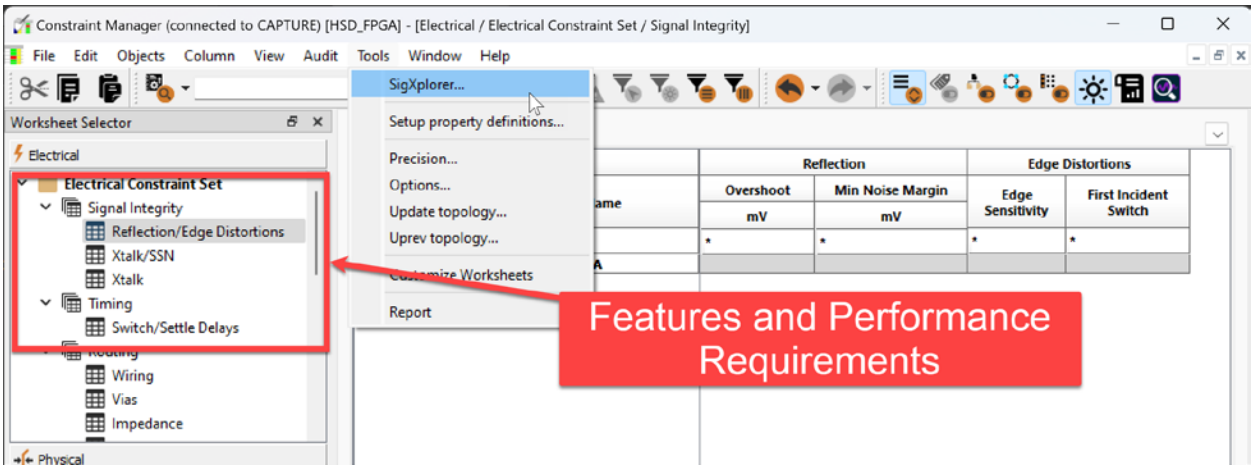
Now that our groups, net classes and regions are set up, it is time to apply constraints to those objects.

Schematic Constraints Overview

In the modern hardware design process, constraint management must follow the design requirements, goals, features, and expectations for the product.

The constraints fallout from the signal integrity, power integrity, electrical, mechanical and electromagnetic requirements necessary for the product to be considered a success.

Notice on the schematic capture side, our Constraint Manager has some options for signal integrity requirements (such as signal reflections, edge distortions, etc.), crosstalk (Xtalk) performance, allowed simultaneous switching noise (SSN), and so on, while on the PCB side it does not.



In the modern hardware design process, the performance requirements are set at the design and schematic, not the PCB implementation phase, as that phase it is too late to think about signal integrity and performance.

In the following sections we create and apply as many of the rules (constraints) needed for the design to meet said requirements.

The main performance categories that we can constrain are electrical (e.g. impedance), physical (copper features like trace width), and spacing (e.g. distance from other objects to avoid EMC issues).

After that we will want to set some net properties as well.

These steps are all to facilitate the efficient execution of PCB layout for the PCB designer.

Counterintuitively, the more rules and restrictions we have, the easier it is to create and route a printed circuit board.

So, let's start with electrical constraints.

Electrical Constraints

In OrCAD X Capture let's set the electrical constraints to meet design needs.

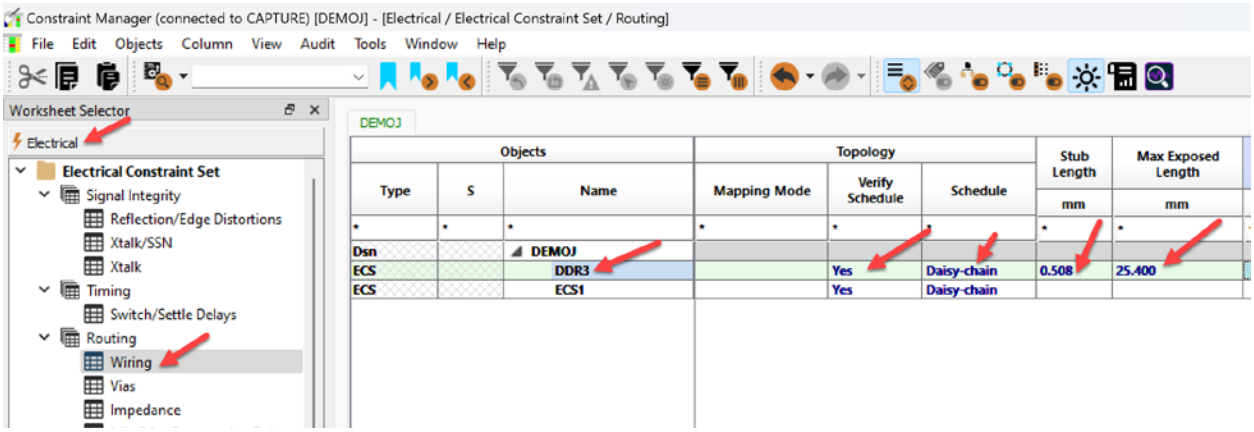
Notice the Signal Integrity and Timing sections.

1. Skip these sections and go to the **Electrical - Routing – Wiring** worksheet.
2. Right click on the Dsn named **DEMOJ – Create - Electrical CSet…**
3. Give your constraint set a descriptive name like 'DDR3', then click OK.

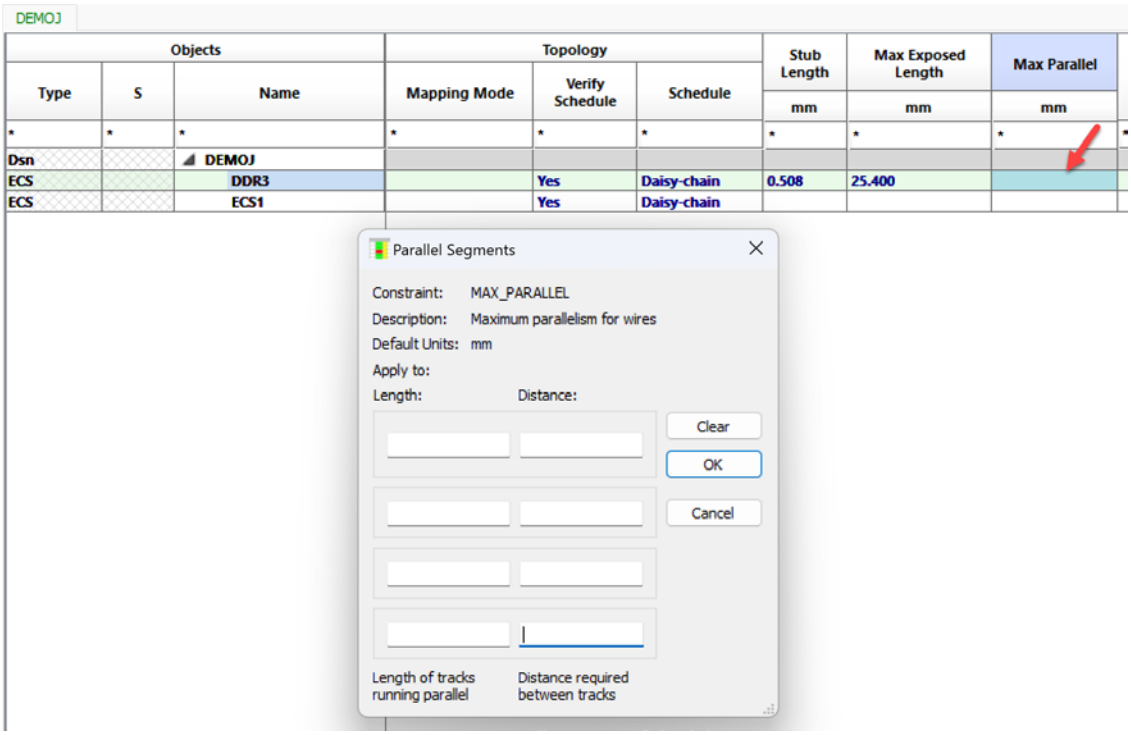
The Constraint Manager lets you assign multiple electrical rules like the routing style, stubs lengths, parallel traces and layer sets. Set the following values as shown in the image below.

4. Once the DDR3 constraint set is created, click the cell under the Verify Schedule column and set it to Yes. This ensures that the constraints are checked during the routing process, which helps maintain signal integrity.
5. Set the Schedule to Daisy-chain. This routing pattern reduces the chances of signal reflections in the DDR3 topology by ensuring the signal terminates at the last DDR3 chip in the memory bank.

6. Set Stub Length to 20 mils (0.508 mm). A shorter stub length reduces signal reflections, which is critical for maintaining signal integrity in high-speed designs. Depending on your design's signal propagation and rise times, stub lengths of 10, 20, or 30 mils may be acceptable.
7. Set the Max Exposed Length to 1000 mils (25.400 mm). This value helps control the amount of potential electromagnetic interference (EMI) onto or emitted from the exposed traces. Adjust the Max Exposed Length based on specific design requirements to ensure optimal performance.



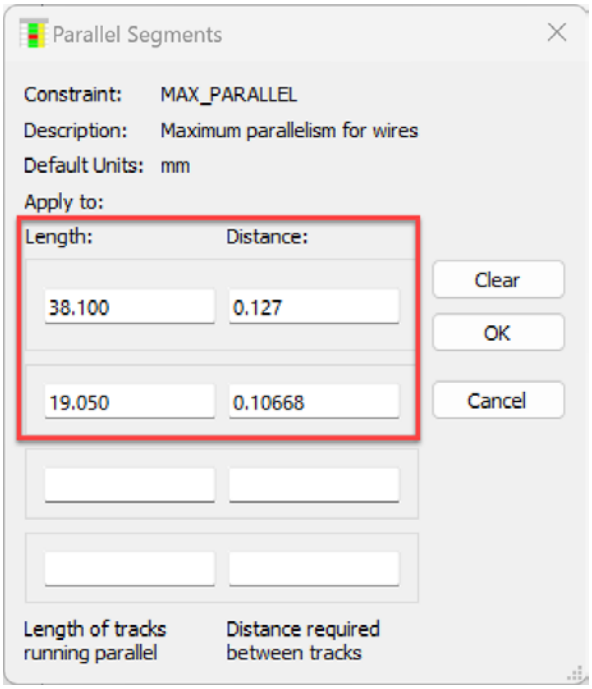
8. Set the Max Parallel value by clicking the cell. This will open up a new window.



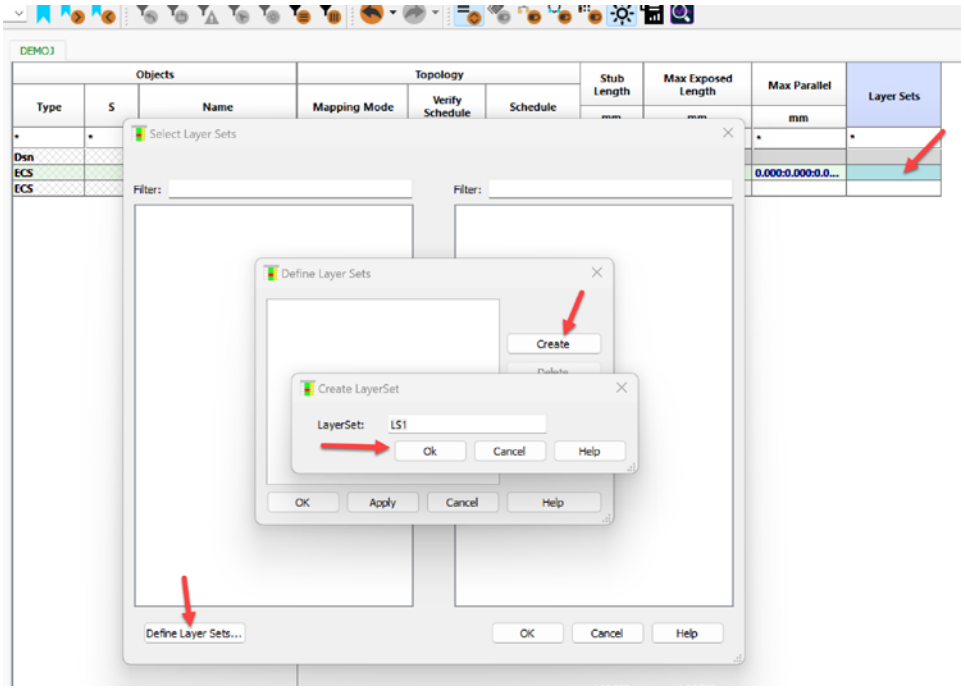
9. Set the Length value in row 1 to 1500 mils (38.100 mm) and the Distance value in row 1 to say, 5 mils (0.127 mm), then click OK. Setting a limit to the distance that traces can run closely in parallel to each other limits crosstalk.

TIP: Crosstalk occurs when electromagnetic interference from one trace (the aggressor) affects a nearby trace (the victim), leading to unwanted noise and potential signal integrity issues in high-speed PCB designs. The amount of crosstalk increases with the parallel length of the traces, the distance between them, and the signal frequency, making it crucial to minimize parallel runs and maintain adequate spacing between traces to reduce this effect.

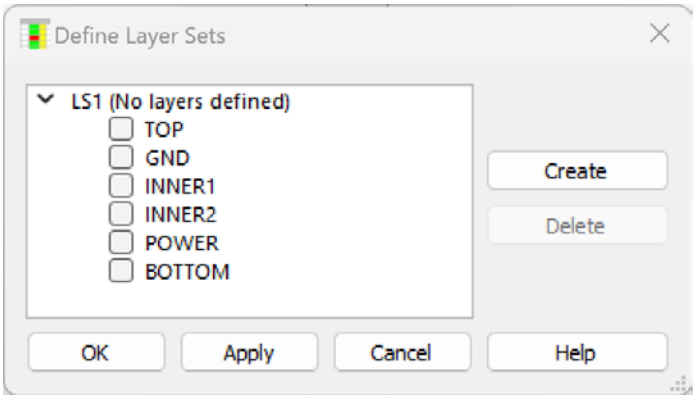
10. In the second row, let's consider traces that are closer together 4.2 mils (0.10668 mm). Those traces should not be allowed to run in parallel with each other as long as traces are 5 mils apart, because the coupling will be stronger from the smaller gap. Therefore, reduce the parallel length to 750 mils (19.050 mm). Please use the settings in the image below.



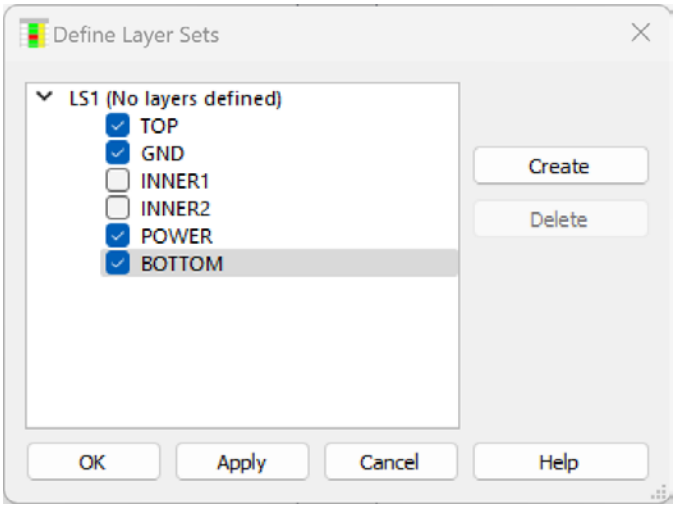
11. Our last constraint is Layer Sets. Maybe we want to limit the DDR3 traces to only the top and bottom layers of the PCB for example (or TOP and INNER1 or BOTTOM and INNER2) to manage EMC and board capacitance. Click the Layer Sets cell, the Select Layer Sets window appears.
12. Click **Define Layer Sets…** The Define Layer Sets window appears. Then click **Create**.
13. Now name the layer set. For example, choose 'LS1'.



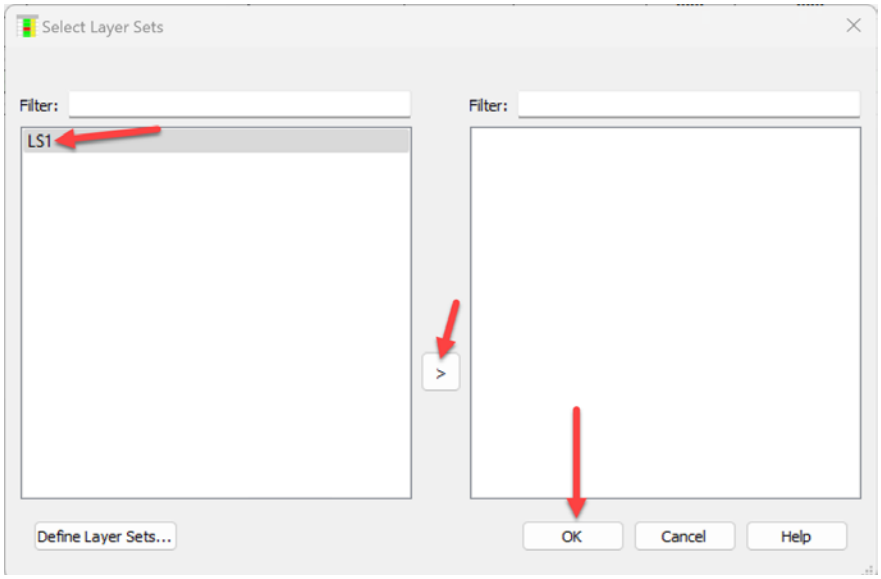
14. Then the LS1 (No layers defined) list will appear, and you can click the arrow to expand the list.



15. Select the checkboxes for the **TOP, GND, POWER,** and **BOTTOM** layers (see below). Click **Apply** then **OK**.



16. You'll be taken back to the Select Layer Sets window. Choose the LS1 item, then click the **>** arrow to move it to the right column, then click OK.

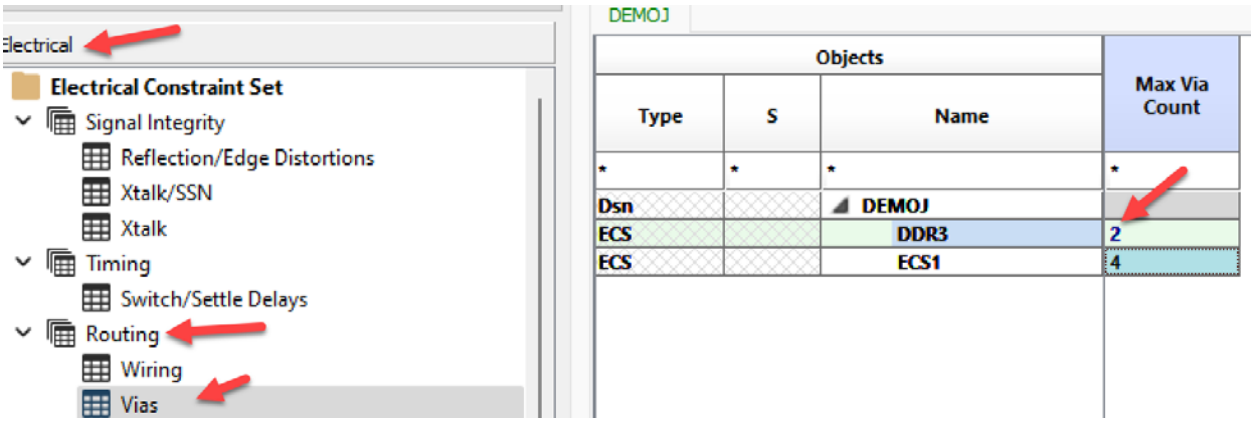


Now the DDR3 signals will not be allowed onto the layers INNER1 or INNER2. You may change these layer sets at any time.

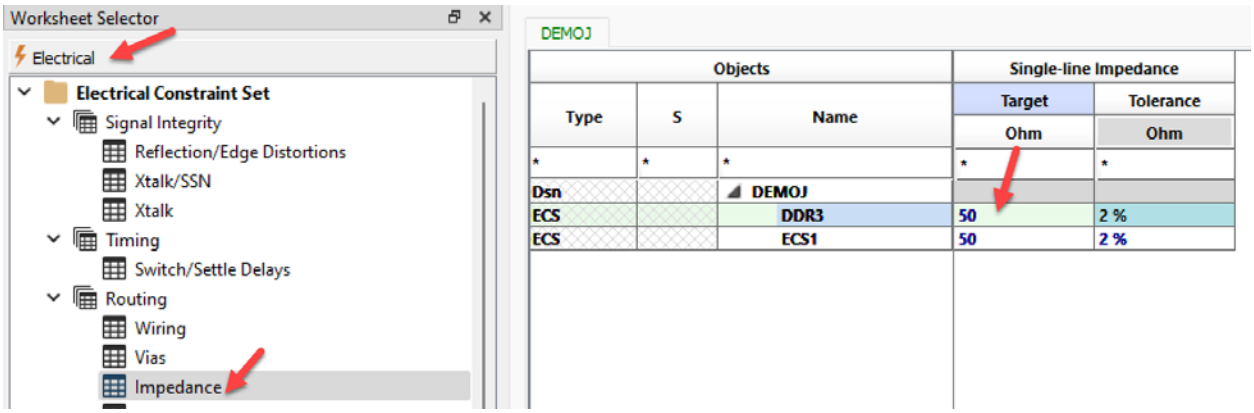
17. Let's add more constraints to this DDR3 ECSet, like Vias – Max Via Count = 2, Impedance, Propagation delays, Total Etch Length, Differential Pair parameters, Relative propagation delay and Return Path.

Please see the images below for those values in the constraint set.

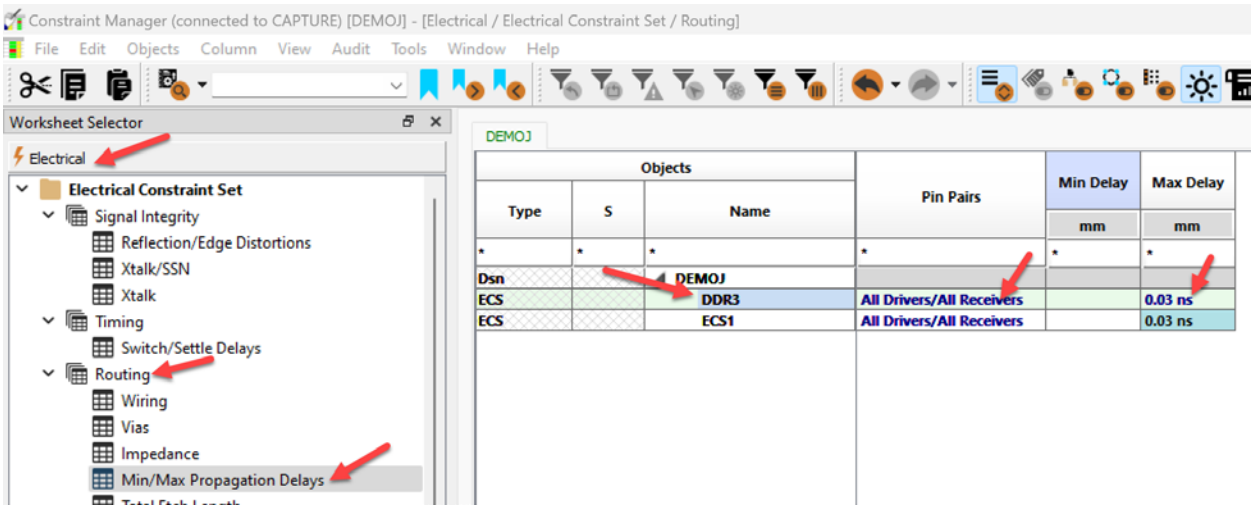
Max Via Count



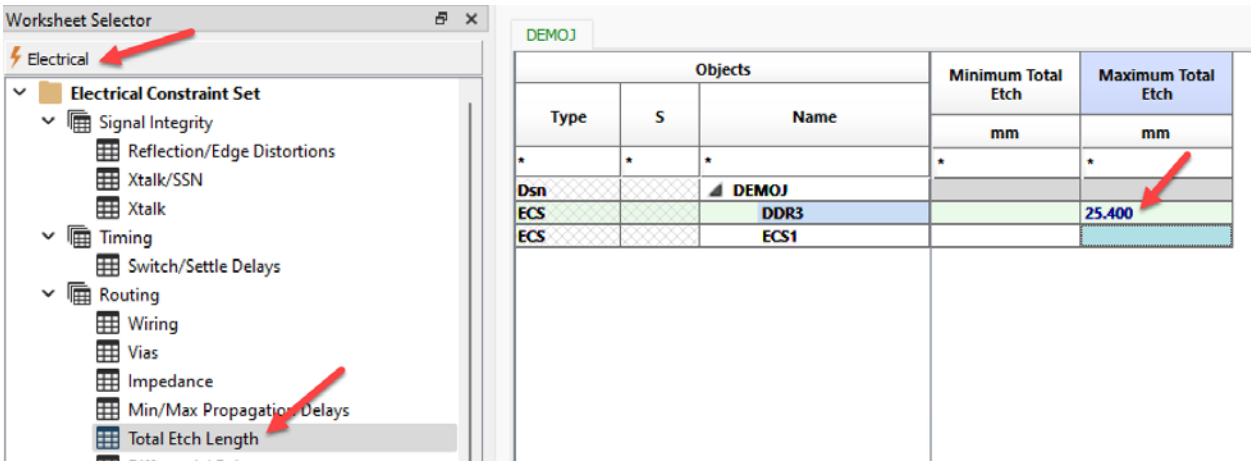
Impedance



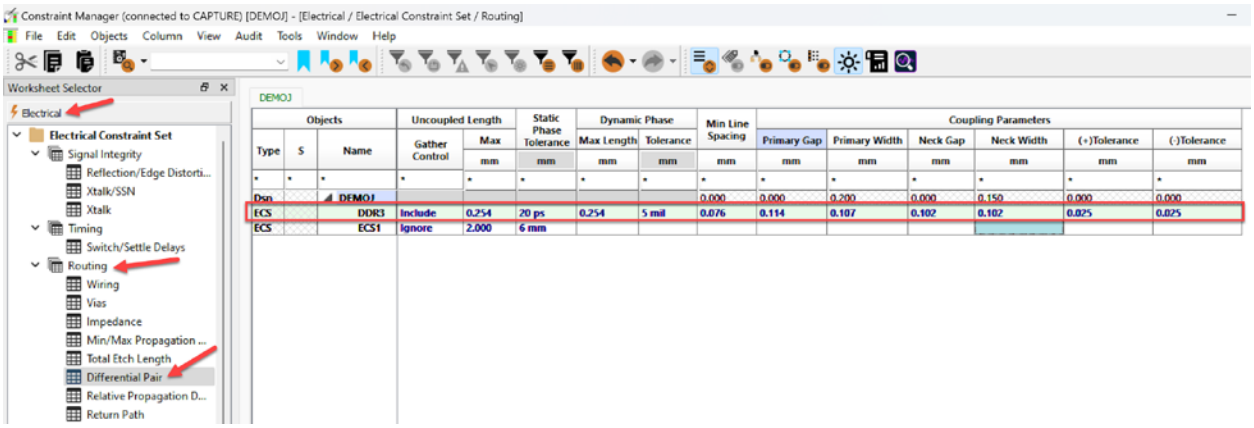
Min/Max Propagation Delays



Total Etch Length

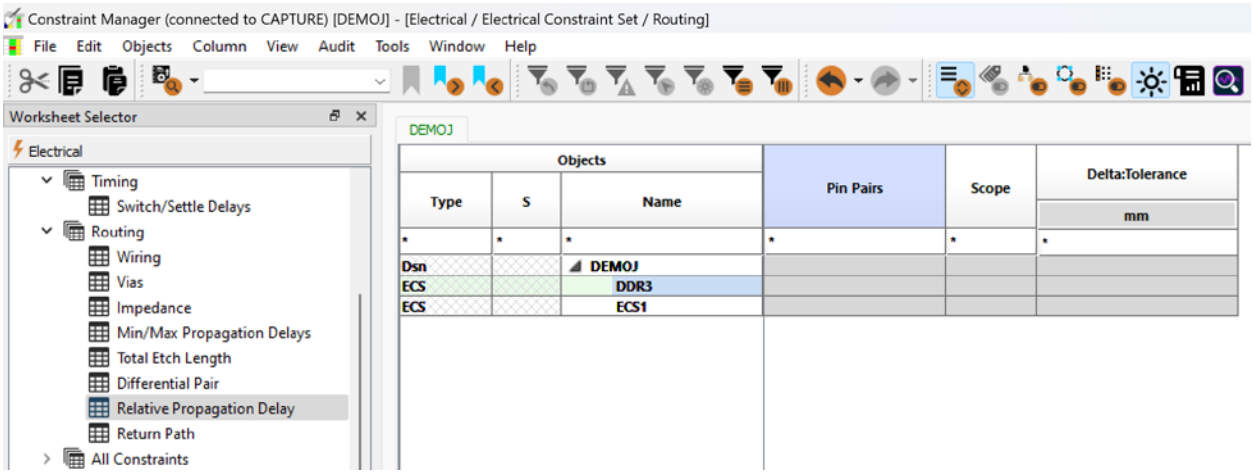


Differential Pair Parameters



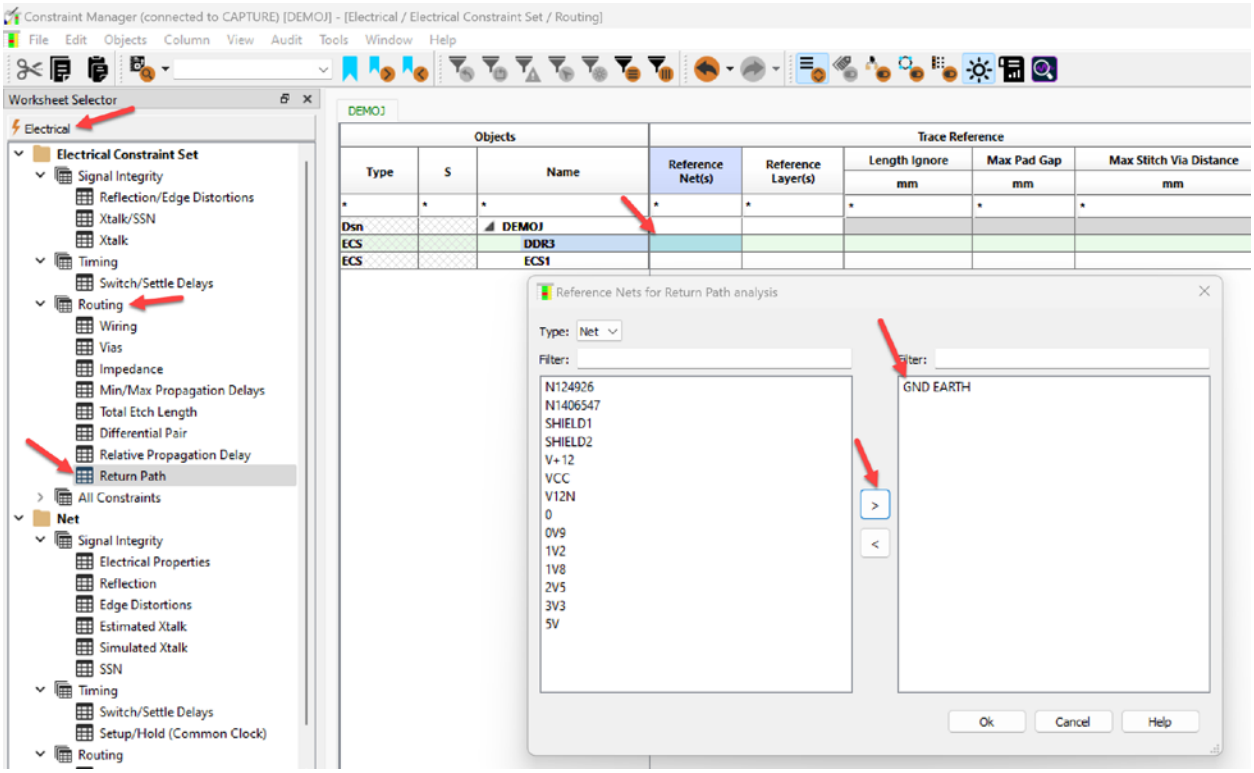
Relative Propagation Delay

No entries are possible in the **Electrical Constraint Set > Routing > Relative Propagation Delay** worksheet.



Return Path

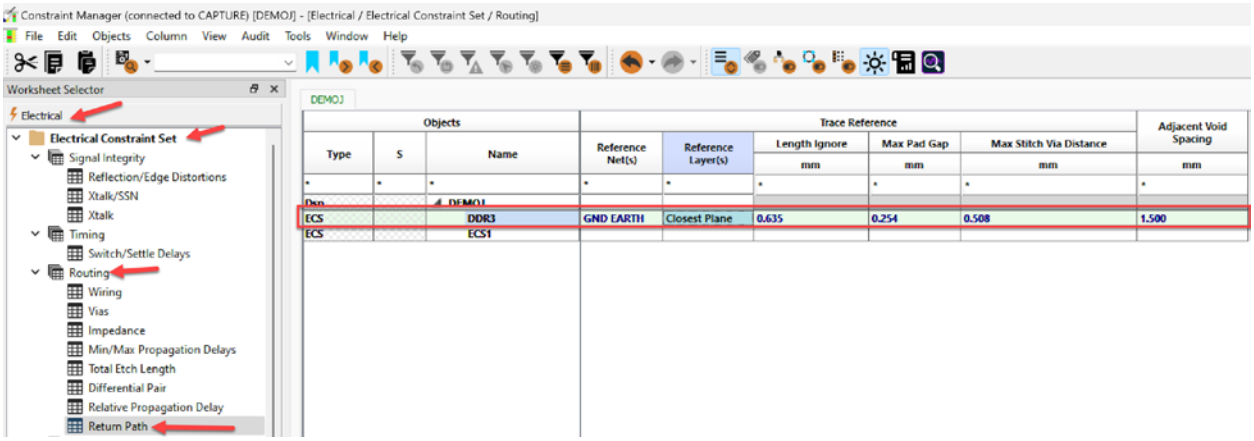
By clicking the options shown below, you can set the GND EARTH net as the return path for your DDR3 **Electrical Constraint Set** and clicking Ok.



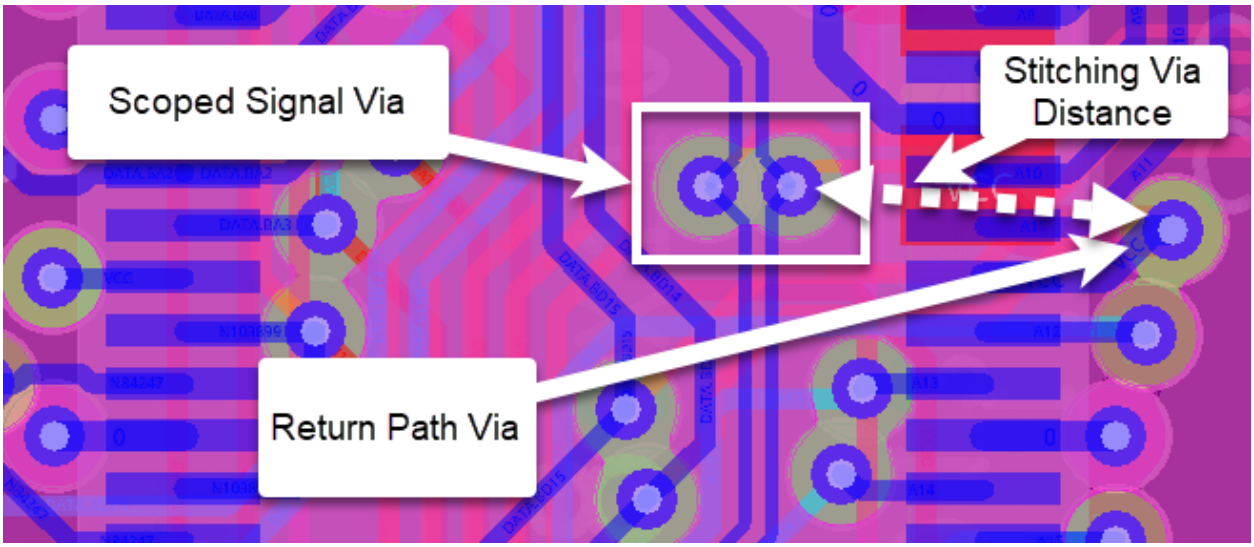
Then fill in the rest of the details shown below:

- **Reference Net(s)** – GND EARTH
- **Reference Layer(s)** – Closest Plane
- **Length Ignore** – 25 mils (0.635 mm)
- **Max Pad Gap** – 10 mils (0.254 mm)
- **Max Stitch Via Distance** – 20 mils (0.508 mm)
- **Adjacent Void Spacing** – 60 mils (1.5 mm)

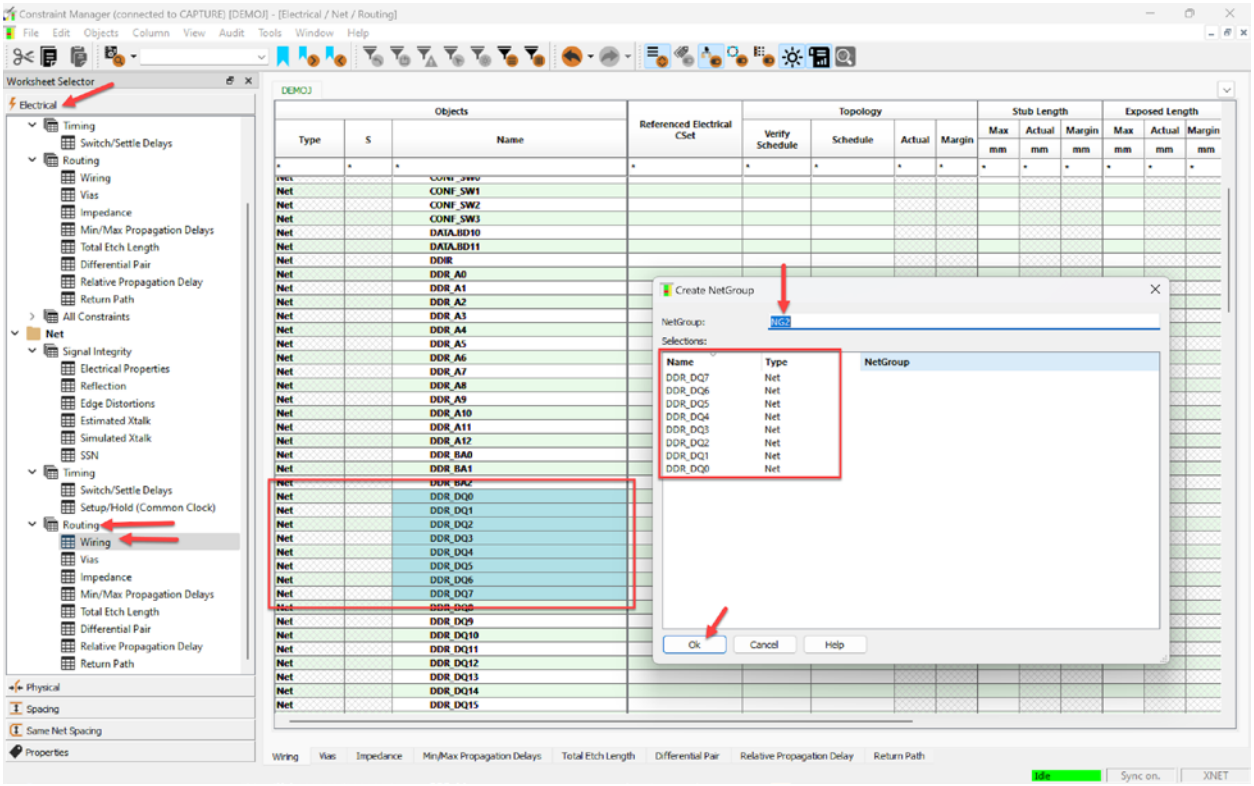
These values assume transfer rates in the 3.5 GHz to 5 GHz ranges and 10 picoseconds to 30 picosecond signal rise times.



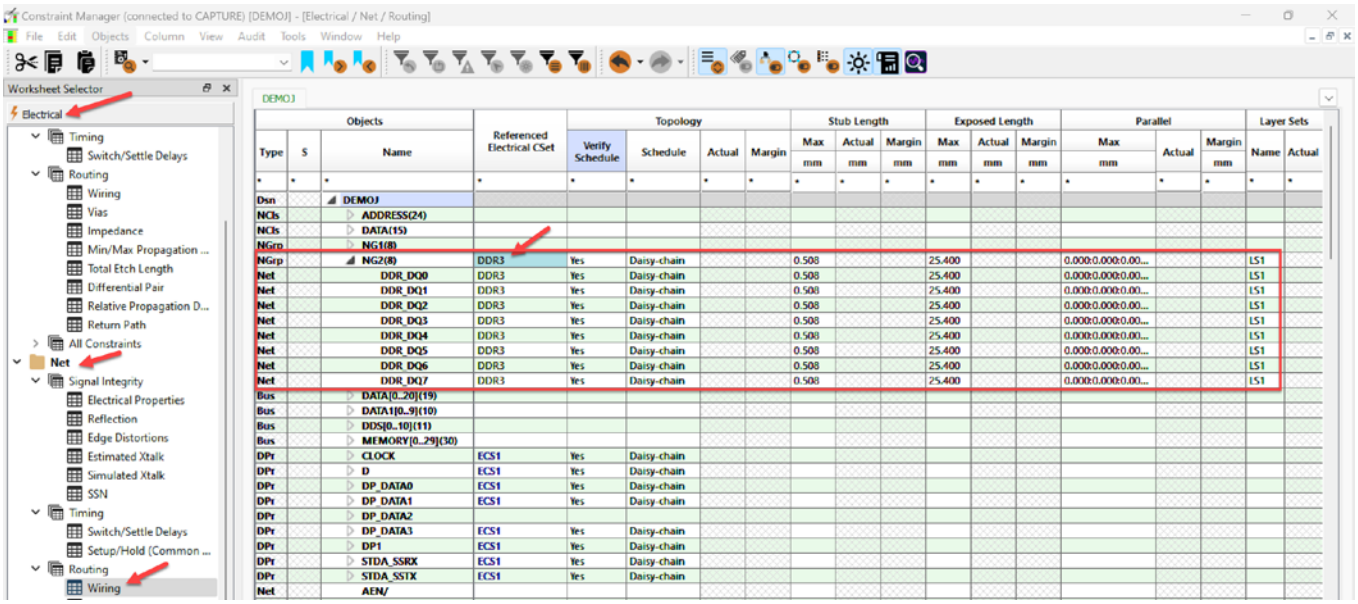
Note: The **Max Stitch Via Distance** is a rule that defines the distance at which a return path via should be present from a via of the scoped signal (see image below).



18. Apply these rules into your constraint set DDR3, then apply the constraint set to your nets by opening the **Electrical** > **Net** > **Routing** > **Wiring** worksheet.
19. Now let's apply the **Electrical Constraint Set** (**ECSet**) **DDR3** to the nets **DDR_DQ0** through **DDR_DQ7**. Click, drag, and highlight those nets. Right click on any of the highlighted net row names, then **Create - Net Group**. Select the net name, then Click Ok.



20. Now you have a net group (named NG2(8)) where you can apply any constraint set you want. Apply the DDR3 constraint set by clicking on the **Referenced Electrical CSet** cell for the NG2(8) group (see below).



Now that you know how to create constraint sets and apply them to your nets, we will only show the constraint sets that can be created.

We'll show how to apply the constraints to your nets in the Physical and Spacing and Same Net Spacing sections of the OrCAD X Capture Constraint Manager tool.

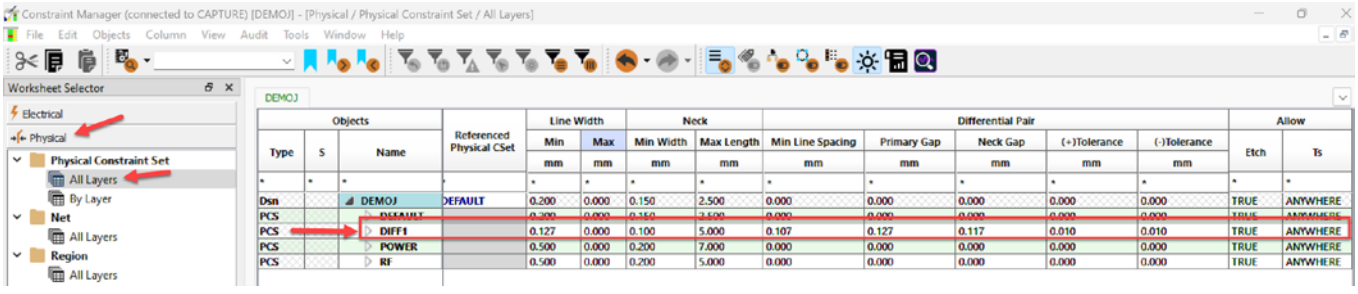
We'll also show the Properties section of the Constraint Manager tool.

After that, we will look at the Constraint Manager on the PCB Editor side in OrCAD X.

Physical Constraints

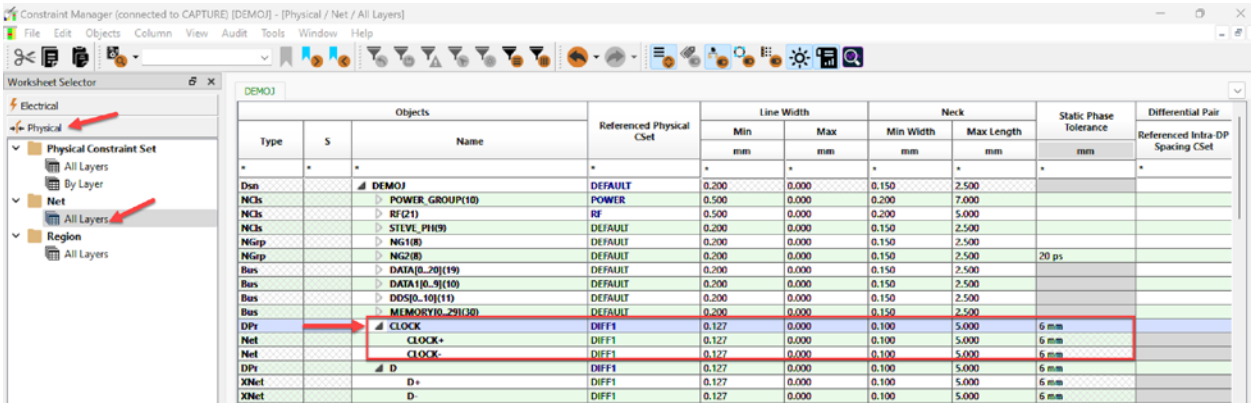
Here is an example of the physical constraint sets created within Constraint Manager.

Physical Constraint Set



Applied Constraint Set

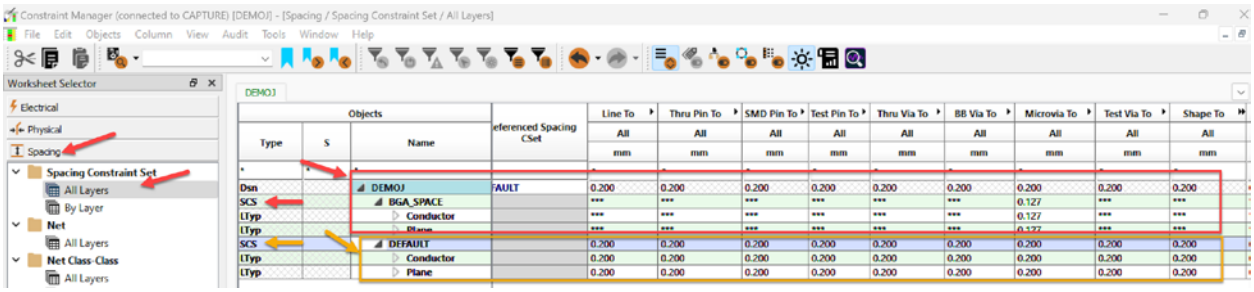
Here is where you apply the constraints (see image below).



Spacing Constraints

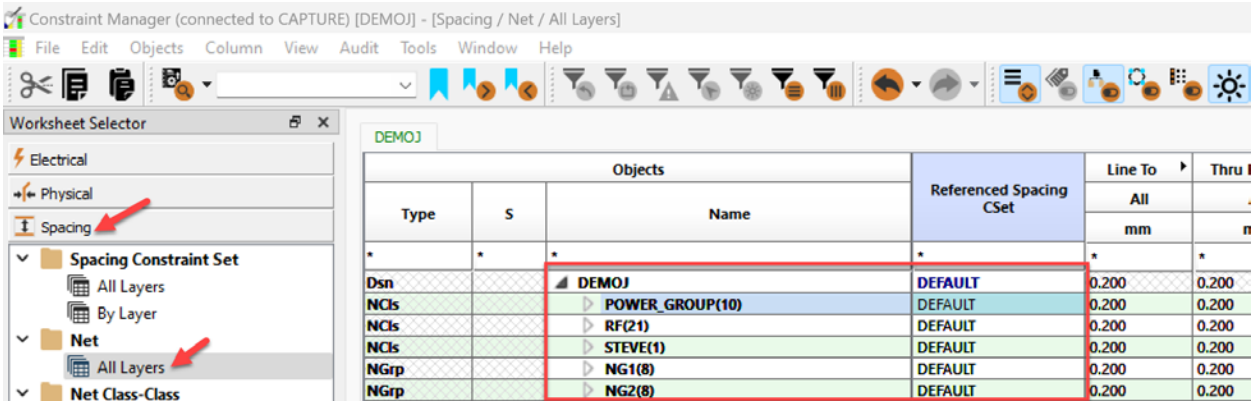
Here are the spacing constraint sets created for the design (shown below). There is a spacing constraint set for the BGAs in the design, called BGA_SPACE. Then there is the DEFAULT constraint set for the entire design in general.

Spacing Constraint Set

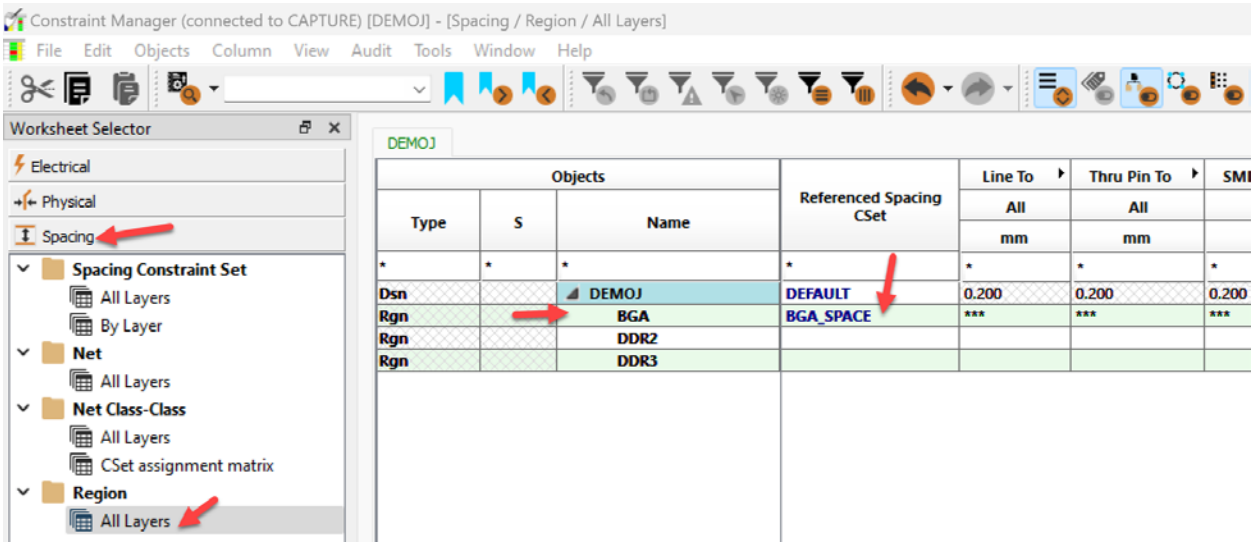


Applied Constraint Set

As expected, the default constraint set is applied to most of the nets in the design.



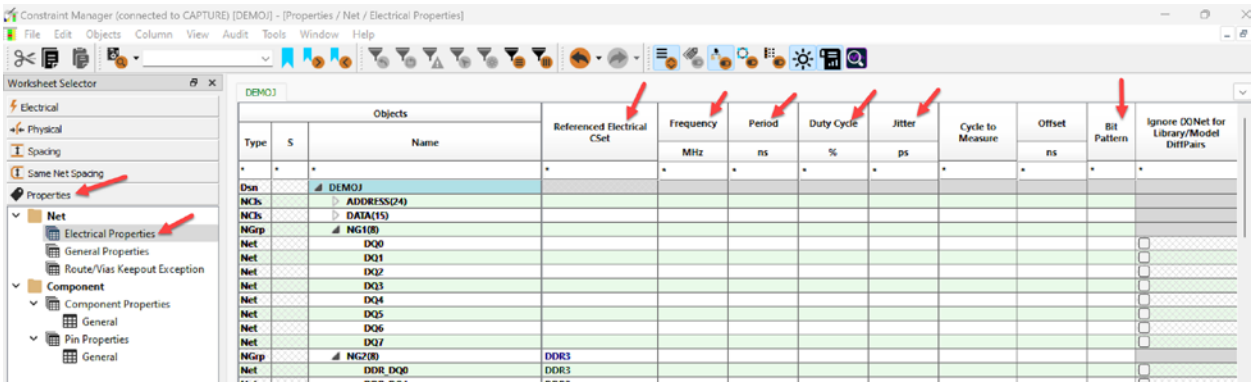
Notice that our region-based constraint set is applied to the Regions worksheet in a specific BGA region instead of being applied to various nets.



Note: There are spacing regions for the DDR2 and DDR3 devices, but we have not created spacing constraints for either of these devices since they're using SOIC packaging instead of BGA packaging. Upon inspecting the pin sizes for the SOIC packaging, we don't need to adjust the default spacing or physical settings for our traces.

Electrical Properties

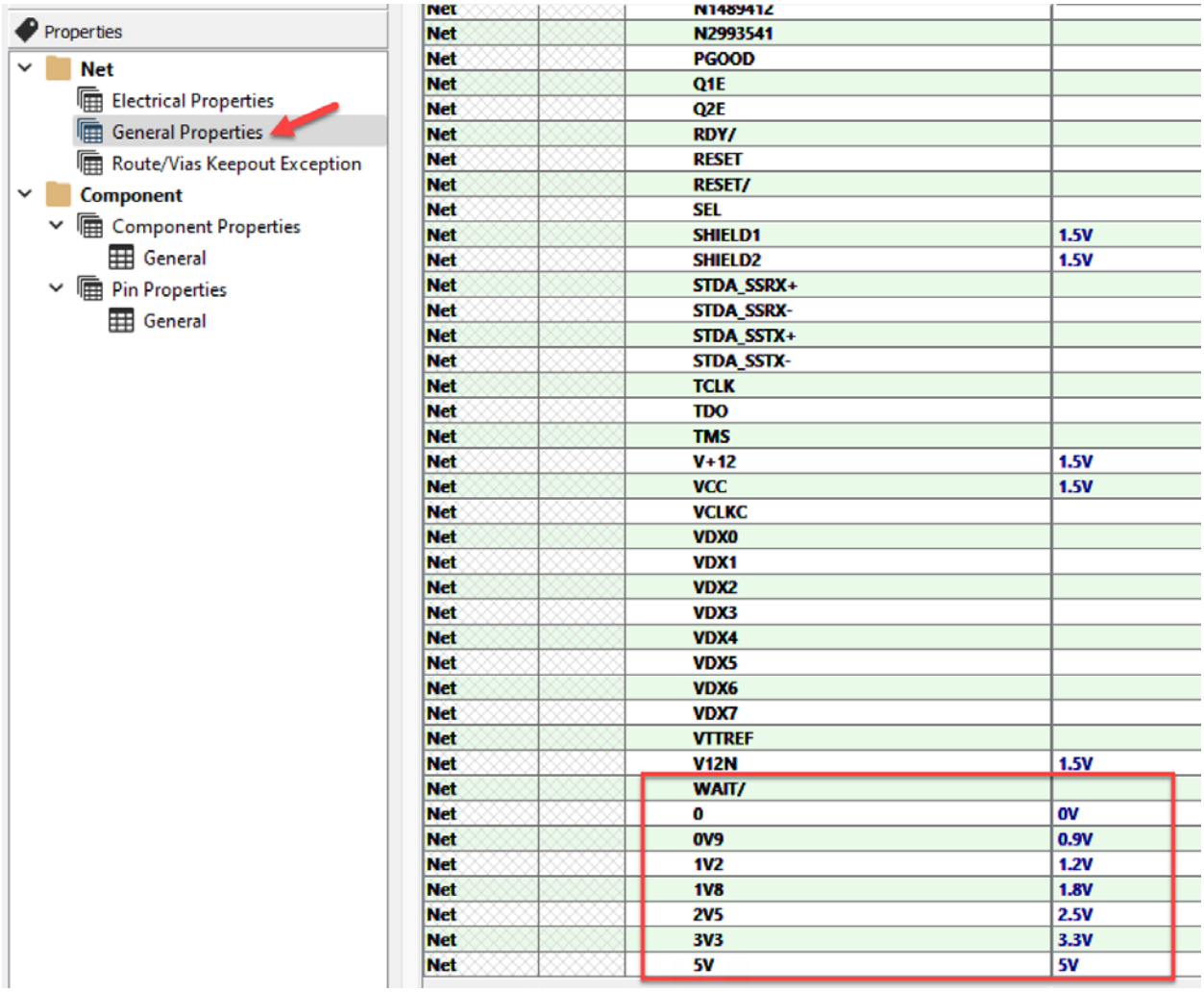
Within the Constraint Manager, we can assign properties and values to specific nets. This feature is extremely useful for doing PCB layout simulations (e.g. power IR drop analysis, signal integrity transmission line simulation). See the image below to find the electrical properties section.



Notice that in the **Properties > Net > Electrical Properties** worksheet, you can set so many parameters:

- Frequency (the rate of pulses per second on a net. Also, the inverse of the Period)
- Period (the time between when a signal repeats itself. e.g. the time from the beginning of one pulse to the beginning of the next pulse)
- Duty Cycle (the length of time a pulse on the net will be high within the signal period)
- Jitter (the amount of jitter expected on the trace for that net)
- Bit Pattern (this is the signal pulses that are expected on a net, such as 01011001)

Then, in the **General Properties** section, we already have voltages set for some of the nets (see image below). Setting voltages helps assist circuit simulation for impedance drops and signal integrity analysis.



Net		N1489412	
Net		N2993541	
Net		PGOOD	
Net		Q1E	
Net		Q2E	
Net		RDY/	
Net		RESET	
Net		RESET/	
Net		SEL	
Net		SHIELD1	1.5V
Net		SHIELD2	1.5V
Net		STDA_SSRX+	
Net		STDA_SSRX-	
Net		STDA_SSTX+	
Net		STDA_SSTX-	
Net		TCLK	
Net		TDO	
Net		TMS	
Net		V+12	1.5V
Net		VCC	1.5V
Net		VCLKC	
Net		VDX0	
Net		VDX1	
Net		VDX2	
Net		VDX3	
Net		VDX4	
Net		VDX5	
Net		VDX6	
Net		VDX7	
Net		VTTREF	
Net		V12N	1.5V
Net		WAIT/	
Net		0	0V
Net		0V9	0.9V
Net		1V2	1.2V
Net		1V8	1.8V
Net		2V5	2.5V
Net		3V3	3.3V
Net		5V	5V

The remaining worksheets, such as Component > Component Properties > General and Component > Pin Properties > General, are not set.

This concludes the schematic side of the constraint manager and its use. Now we will push these constraints to the PCB layout side to maintain project integrity.

After that, we will simply review the constraints found in the PCB layout for our demo board.

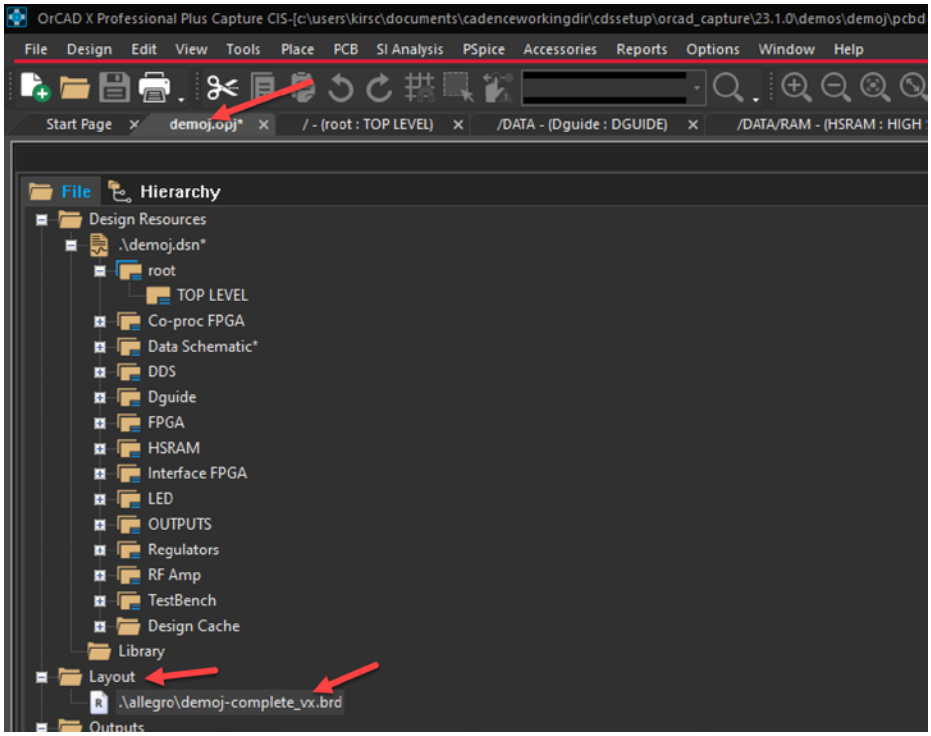
- Within the Constraint Manager worksheet, Create a Constraint Set that you will apply later.
- Apply that Constraint Set to a class, group or region in your design.
- Repeat similar steps for all kinds of constraints (Physical, Electrical, Spacing, Manufacturing and so on).

PCB Constraints Overview

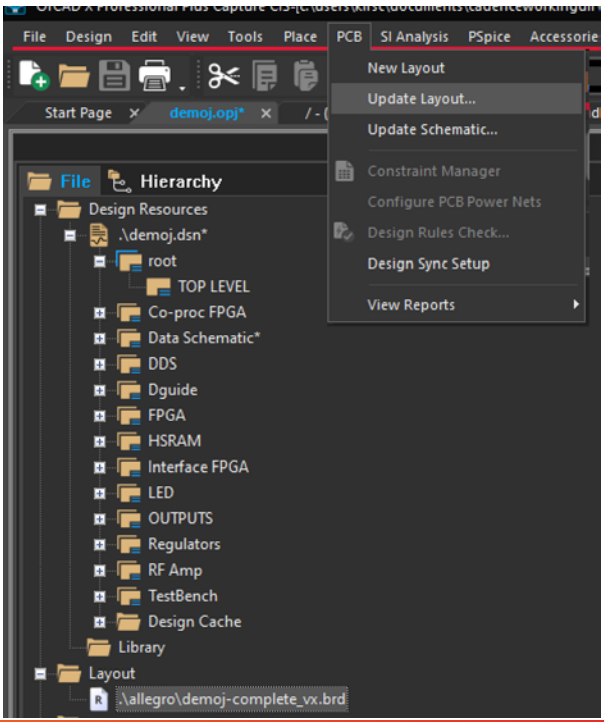
The same constraint manager that is available within OrCAD X Capture also exists within OrCAD X Presto PCB Editor.

To find it:

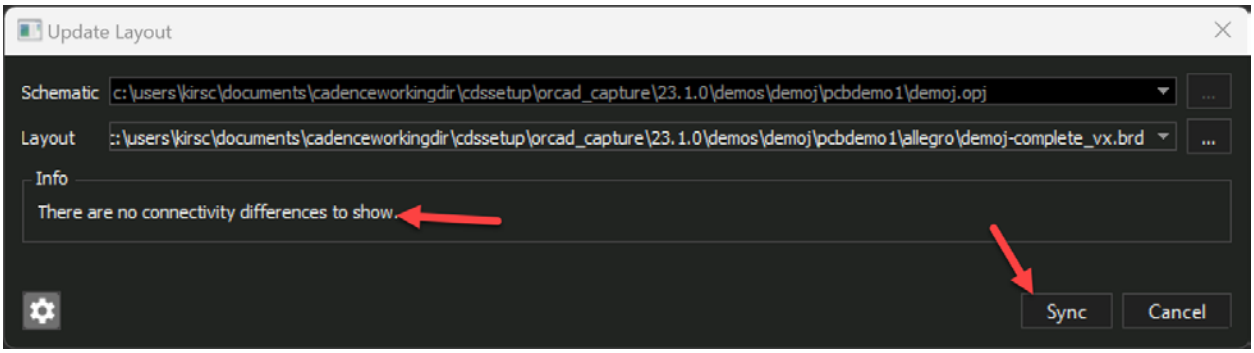
1. Close the current Constraint Manager in Capture. Constraints are saved instantly so there is no need to save it.
2. Navigate to the Capture project file hierarchy and you should have your board design file as part of your project (see image below).



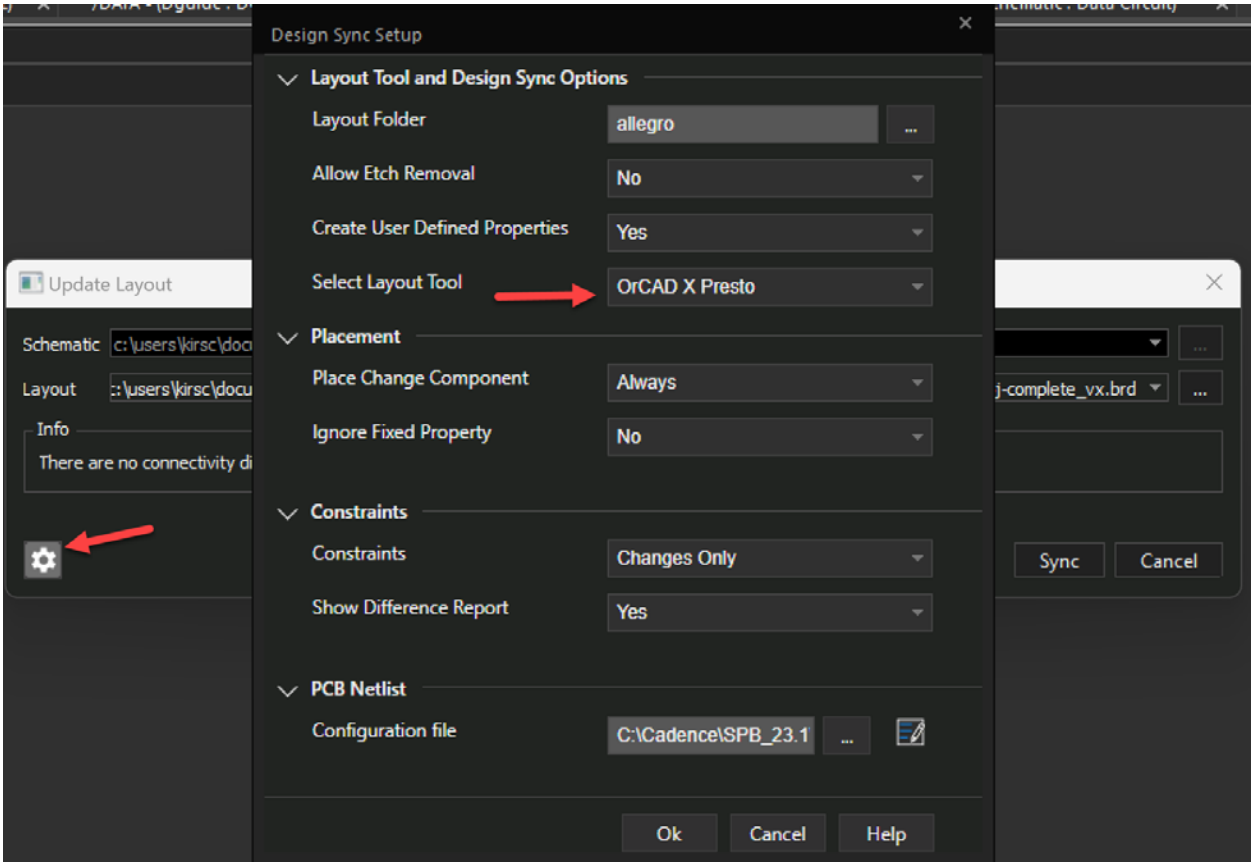
3. Select the board file, then update the board by clicking Menu **PCB – Update Layout**.



4. The Update Layout window will appear.

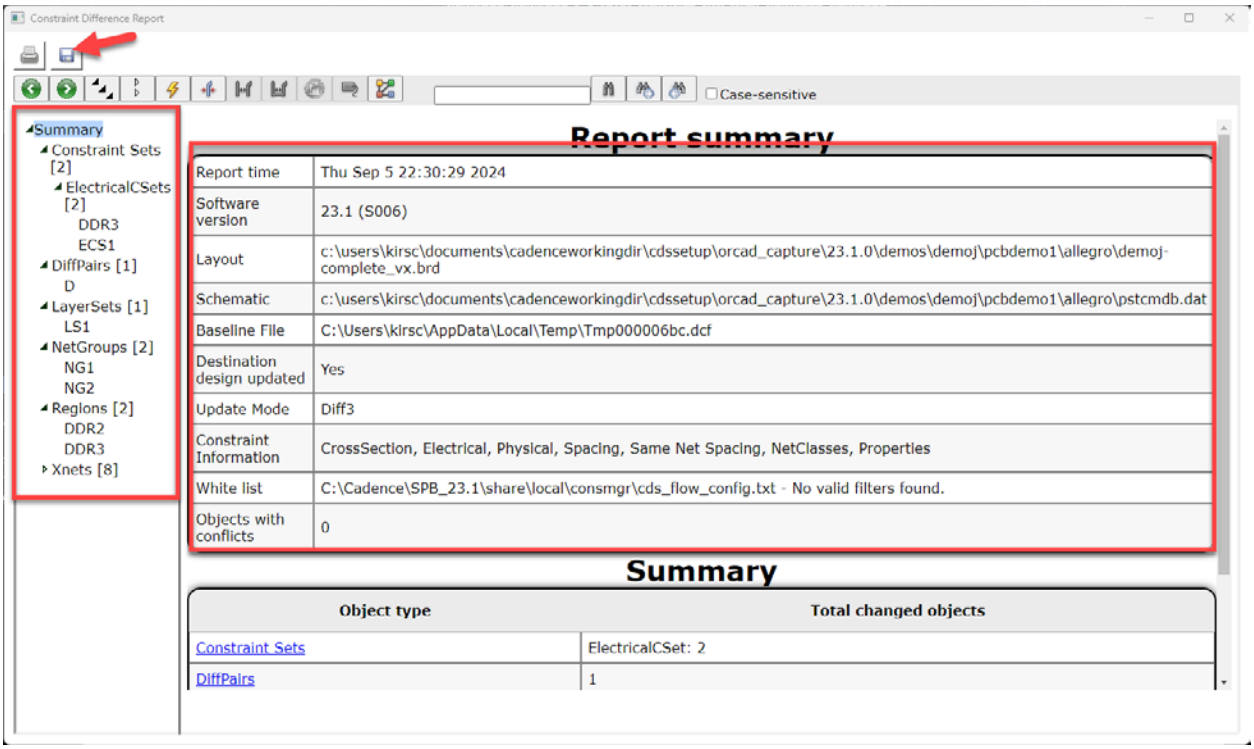


5. Click the gear icon and ensure you set **Select Layout Tool** to **OrCAD X Presto**.



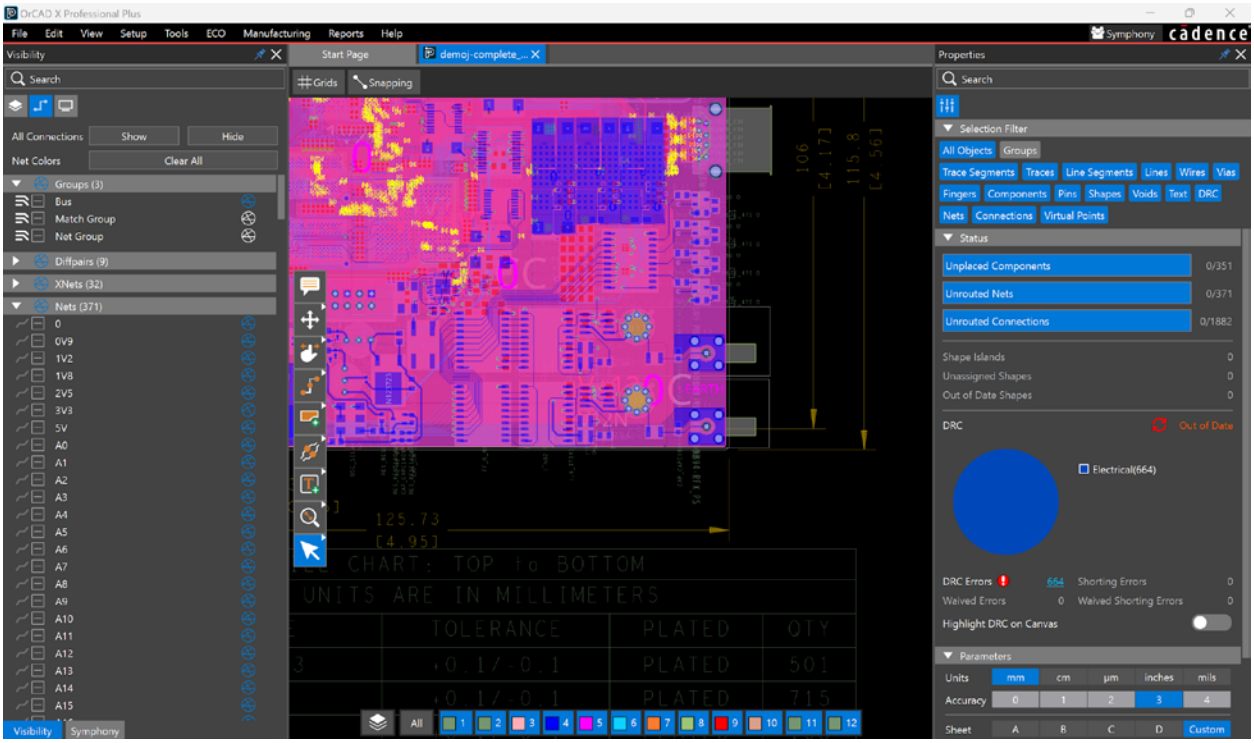
6. Click Ok.
7. Then in the previous window, Click Sync.

This will open OrCAD X Presto PCB Editor and also generate a summary report of all changes found in the Capture Constraint Manager that might have been pushed to the PCB layout.



You can even save the constraints report summary for future team use and notes, just in case something goes wrong with the transferred constraints. We can track why.

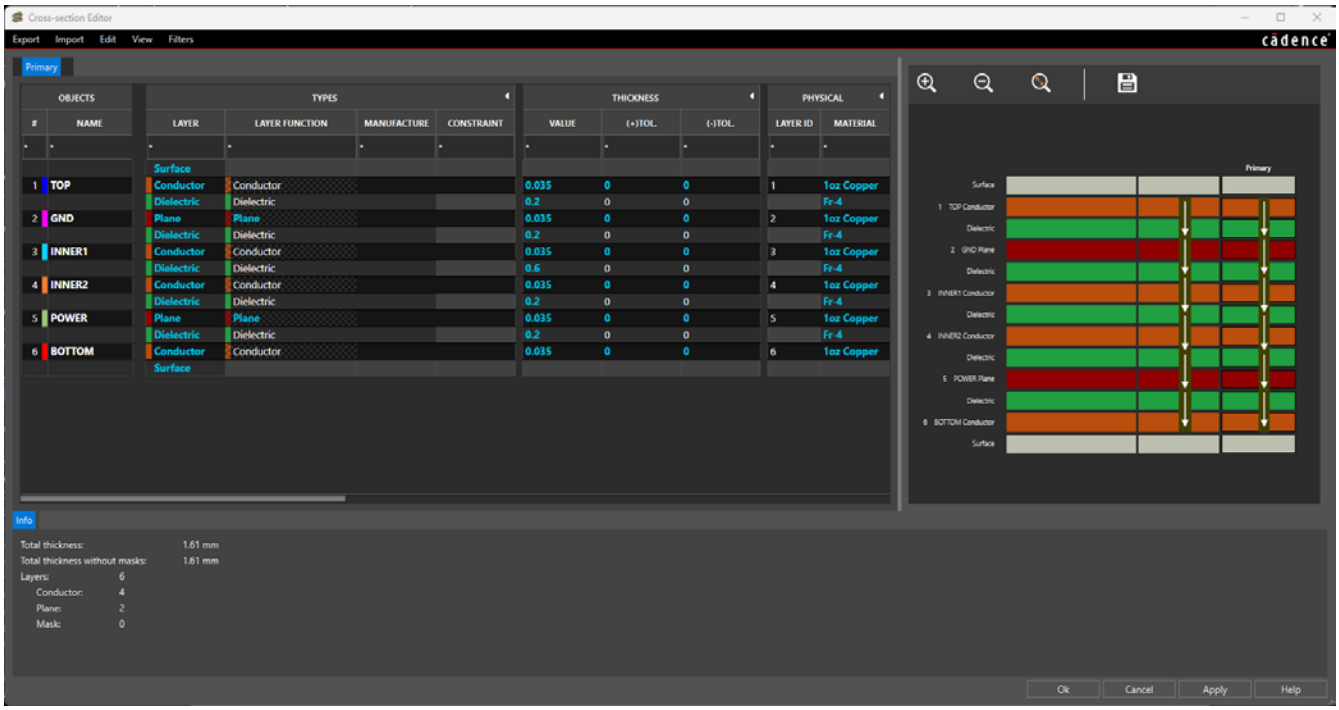
In your new environment, OrCAD X Presto PCB Editor, you can now use the Constraint Manager here.



PCB Stack up

In OrCAD X Presto PCB Editor, note the PCB stack up for this board. To do that:

1. Go to the menu at the top, then select **Tools – Cross Section**.



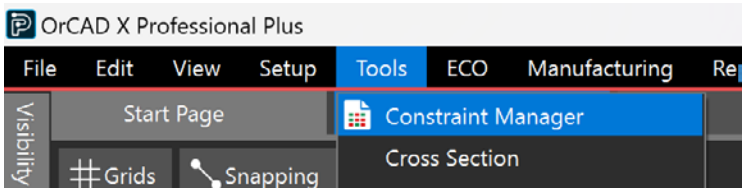
2. Click Ok to close the stack up.

In the next section we will cover the main constraints you will want to apply for any simple to complex printed circuit board. In this case for our project, we are applying simple constraints to this complex board first, then the advanced constraints.

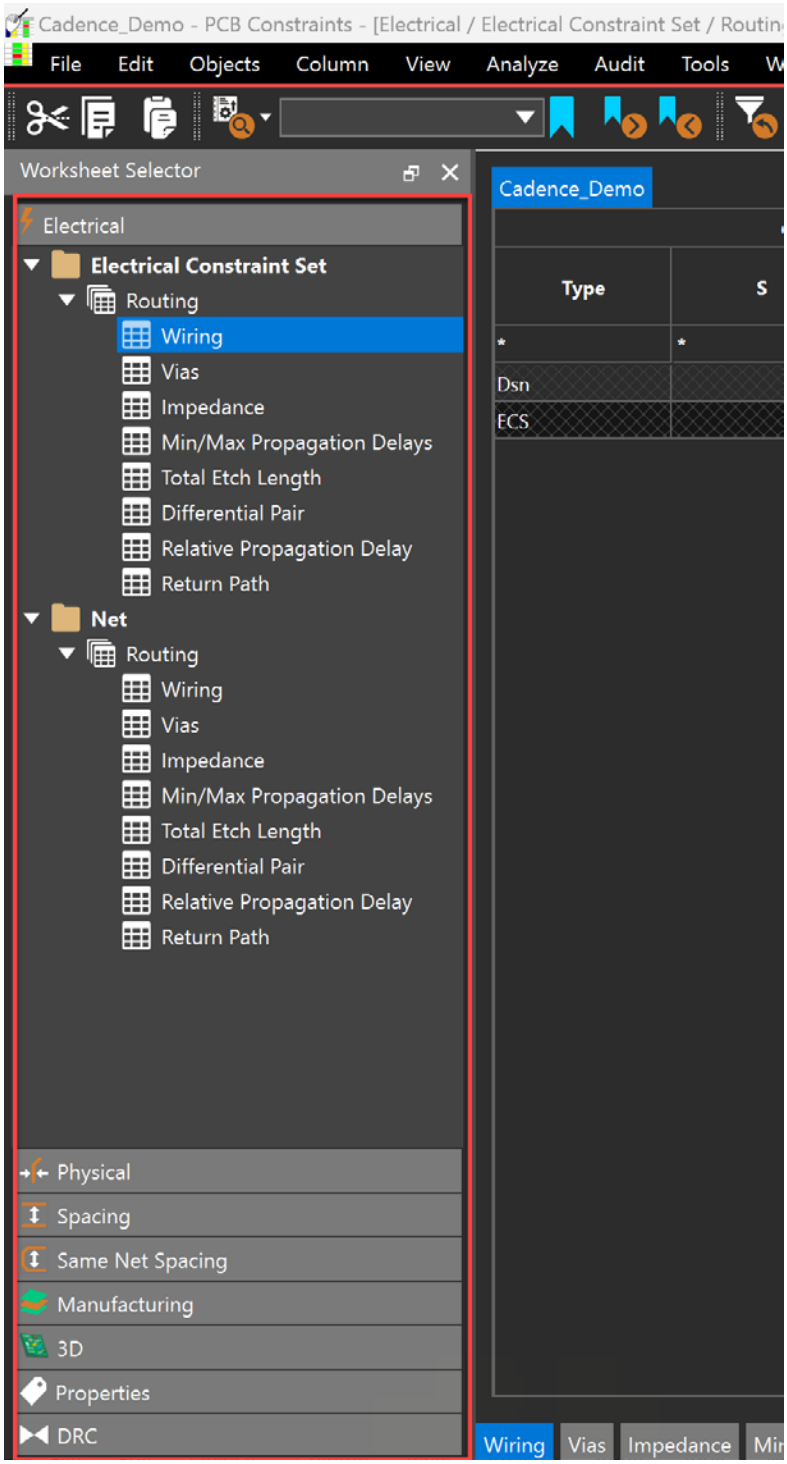
Opening The Constraint Manager (PCB Side)

The following constraints can be applied to standard PCBs (please refer to the previous sections of this document to learn how to implement these constraints).

Open Constraint Manager in OrCAD X Presto PCB Editor by clicking on the main menu and choosing **Tools – Constraint Manager**.



The Constraint Manager opens, and the worksheet categories are visible on the left of the window.

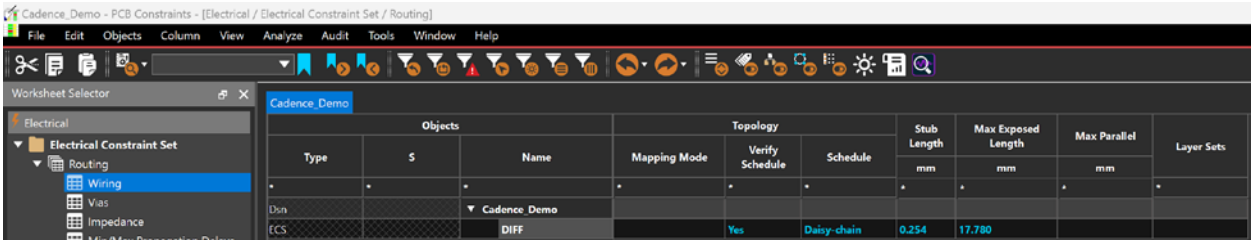


All Constraints for Analysis

The Constraint Manager can analyze most potential bottlenecks for a printed circuit board and apply constraints accordingly. To find out the kinds of constraints we can enforce on our PCB, have the Constraint Manager open.

Standard Electrical Constraints
In this section we can control the following:

- Wiring
- Vias
- Impedance
- Min/Max propagation delays
- Total Etch Length
- Differential Pair
- Relative Propagation Delay
- Return Path



Standard Physical Constraints
In this section we control the following:

- Referenced Physical CSet
- Line Width (Min, Max)
- Neck (Min Width, Max Length)
- Differential Pair (Min Line Spacing, Primary Gap, Neck Gap, (+)Tolerance, (-)Tolerance
- Vias
- BB Via Stagger (Min, Max)
- Allow (Pad-Pad Connect, Etch, Ts)

Then under the Net workbook folder named All Layers we have even more options:

- Line Width (Min Max)
- Neck (Min Width, Max Length)
- Uncoupled Length (Gather Control Max)
- Static Phase Tolerance
- Dynamic Phase (Max Length, Tolerance)
- Differential Pair (Referenced Intra-DP Spacing CSet, Min Line Spacing, Primary Gap, Neck Gap, (+)Tolerance, (-)Tolerance)
- Vias
- BB Via Stagger (Min, Max)
- Allow (Pad-Pad Connect, Etch, Ts)

Standard Spacing Constraints

Then we have spacing necessary to maintain signal integrity for cross talk, and avoid manufacturing defects in general.

Under the **Spacing Constraint Set** > **All Layers** worksheet:

- Line To…
- Thru Pin To…
- SMD Pin To…
- Test Pin To…
- Thru Via To…
- BB Via To…
- Microvia To…
- Test Via To…
- Bond Finger To…
- Hole To…
- Min BB Via Gap

Then there is the **Net Class-Class** > **All Layers** worksheet which contains the same constraints as above but allows you to set constraints between Net Classes instead of only single nets one by one.

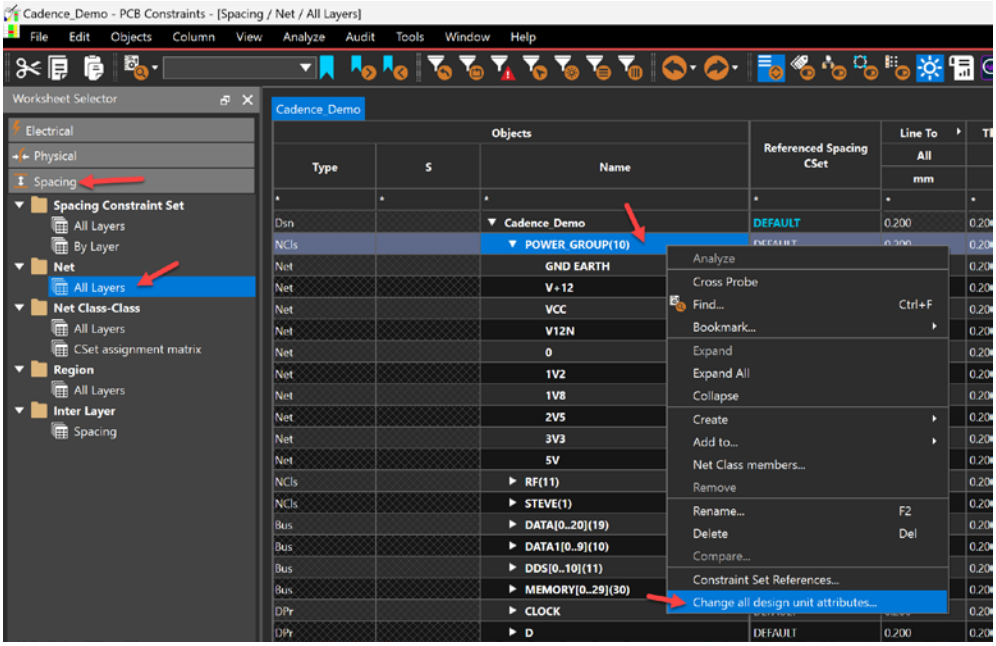
Standard Same Net Spacing Constraints

For the most part, Same Net Spacing can be left as is, unless you need to change the thermal relief on the layer. But even then, that can be changed in your design properties.

TIP: If you end up having shorting errors between traces and planes, then this constraints area might be the culprit. You'll want to adjust your **Shape to…** spacing setting such that shapes have some distance away from all other objects for isolation purposes.

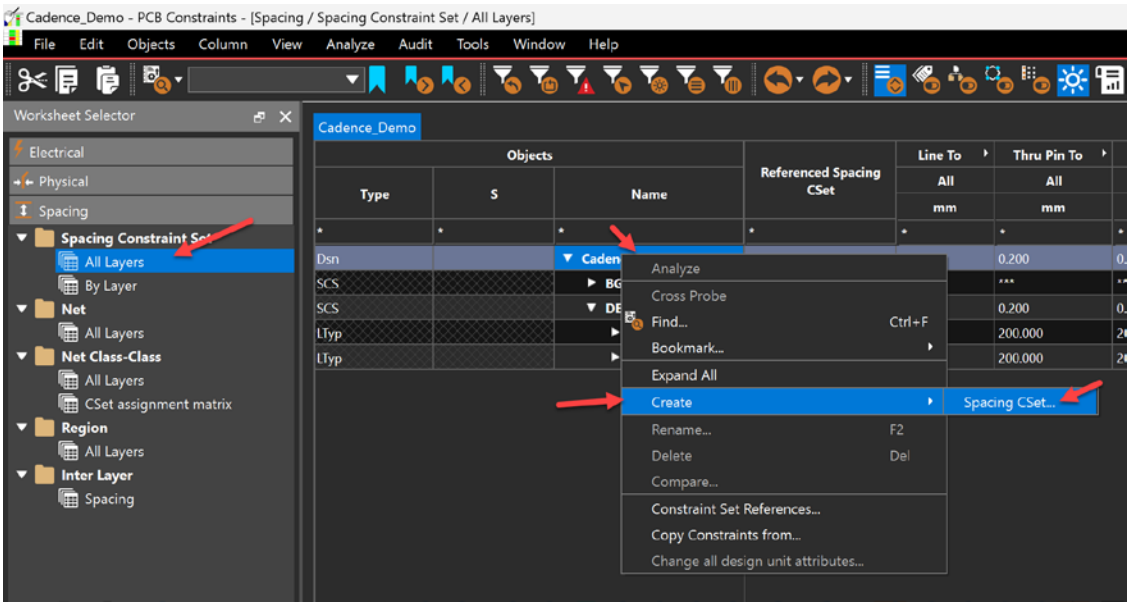
For example, let's say you wanted all power planes and shapes (members of the POWER_GROUP) at least ~7.87 mils (0.2 mm) away from copper pads, even if the through-hole or surface mount pad is part of the same net (you may want to do this to provide thermal relief spacing).

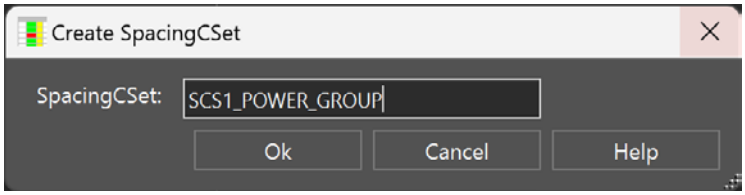
You would go to the **Spacing > Net > All Layers** worksheet, then in the POWER_GROUP(10) cell, right click the cell, choose **Change all design unit attributes…**

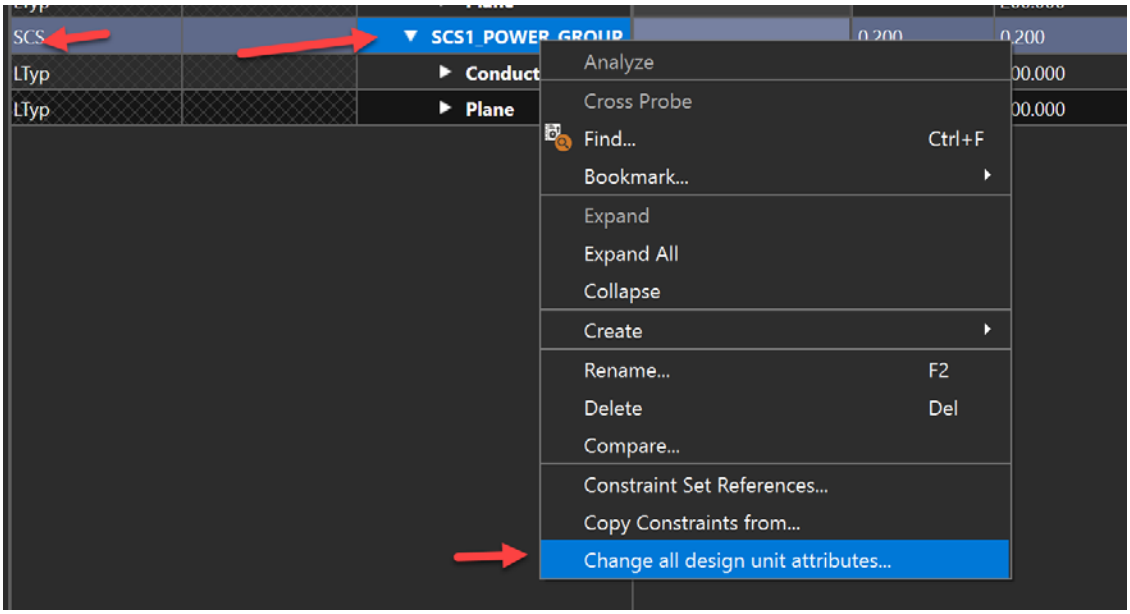


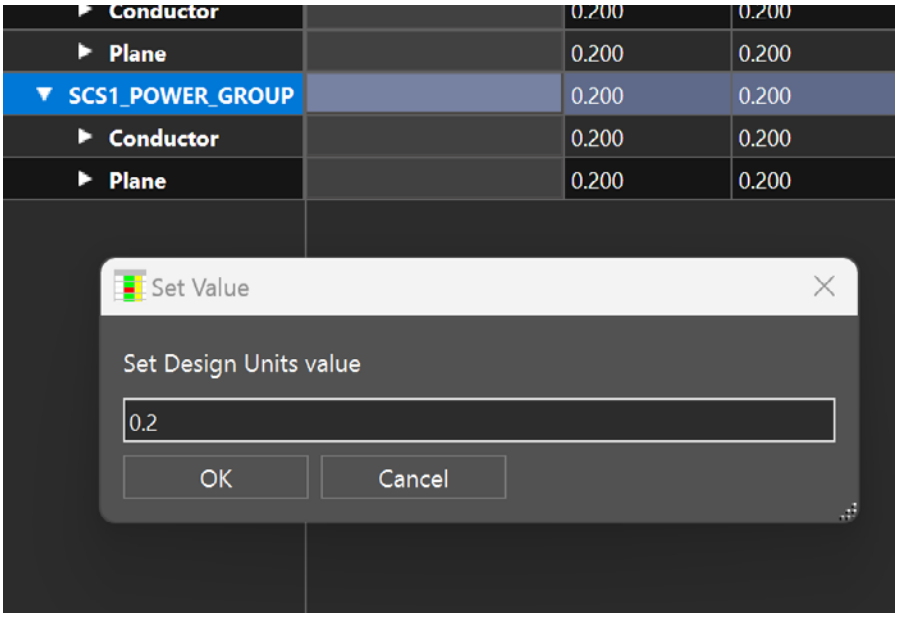
In the new window, set the value to 0.20 (since we're in millimeters and this field doesn't automatically convert the units), then click Ok.

Note that this will override the DEFAULT constraint set that's being applied to all the nets in that POWER_GROUP(10). So it is recommended to create a Constraint set for POWER nets first, then apply that to the **Spacing > Net > All Layers** worksheet (see below).



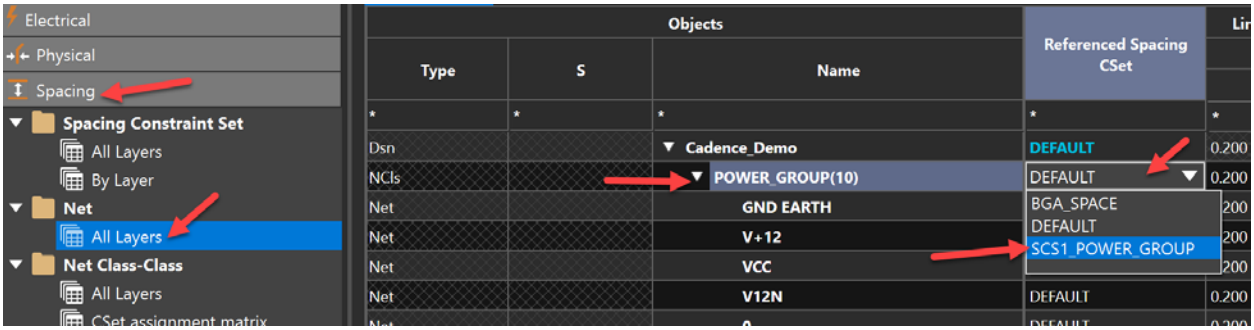






Click OK, then all the rows for that constraint set (SCS1_POWER_GROUP) get set to 0.2 mm.

Now we can apply the constraint set to the **Spacing >Net > All Layers** worksheet by selecting it from the dropdown options shown below and applying it to the **POWER_GROUP**.



Standard Manufacturing Constraints

Now in the Manufacturing section we have many checks to consider:

Design for Fabrication

- Outline
- Mask
- Annular Ring
- Copper Features
- Copper Spacing
- Silkscreen

Design for Assembly

- Outline
- PkgToPkg Spacing
- Spacing
- Pastemask

Design for Test

- Outline
- Mask and Silkscreen
- Spacing
- Probe

 Standard 3D Constraints

Now it's not enough to just do 2D constraints. 3D is considered.

- Component to Component
- Component to Board
- Component to Rigid-Flex
- Component to Board Edge

 Properties

We also have properties being held inside Constraint Manager that came over from the schematic, such as:

Net

- Electrical Properties
  - Frequency
  - Period
  - Duty Cycle
  - Jitter
  - Cycle to Measure
  - Offset
  - Bit Pattern
  - Enable highspeed adjacent layer Keep-outs
- General Properties
  - Voltage
  - Weight
  - Route (Priority vs. to Shape)
- Route/Vias Keepout Exception

Component

- Component Properties
  - General
  - Thermal
  - Swapping
  - Reuse
- Pin Properties
  - General (Pinuse, Pin Delay, Shorting Net, Voltage Source Pin)
  - Shapes
  - Manufacturing

Standard DRCs

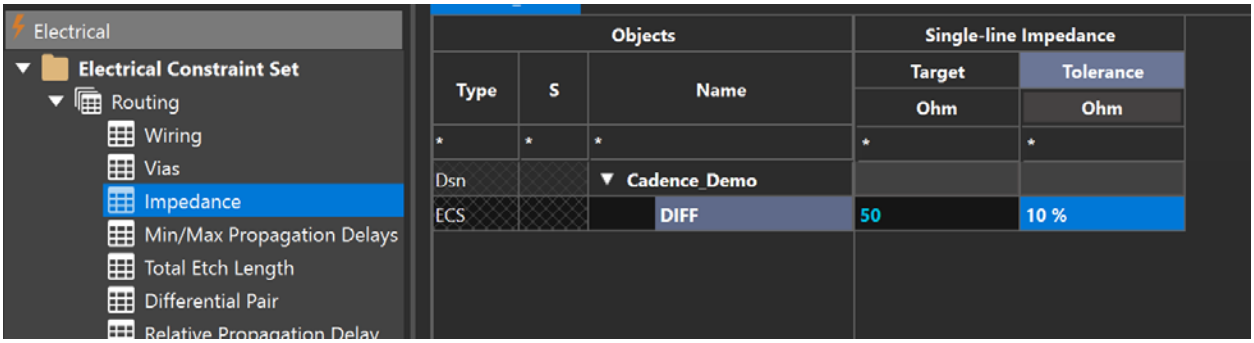
In the following sections we will show you the constraint sets that are created and then the nets (and objects) those constraint sets apply to.

Applying Standard PCB Constraints

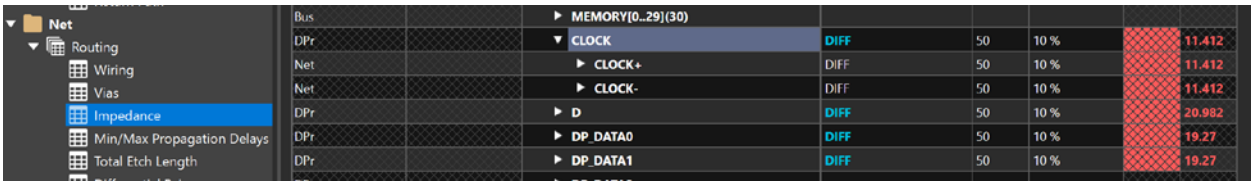
With the Constraint Manager open, we need to set various constraints for the PCB.

Standard Electrical Constraints

Even in some low-speed boards, we need 50 Ohms of Impedance. So we set the impedance to 50 ohms for single-ended PCBs at 10% tolerance, since that is what most manufacturers can handle.



Then that impedance gets applied to whichever net it applies to. Like the CLOCK+ and CLOCK- signals below:



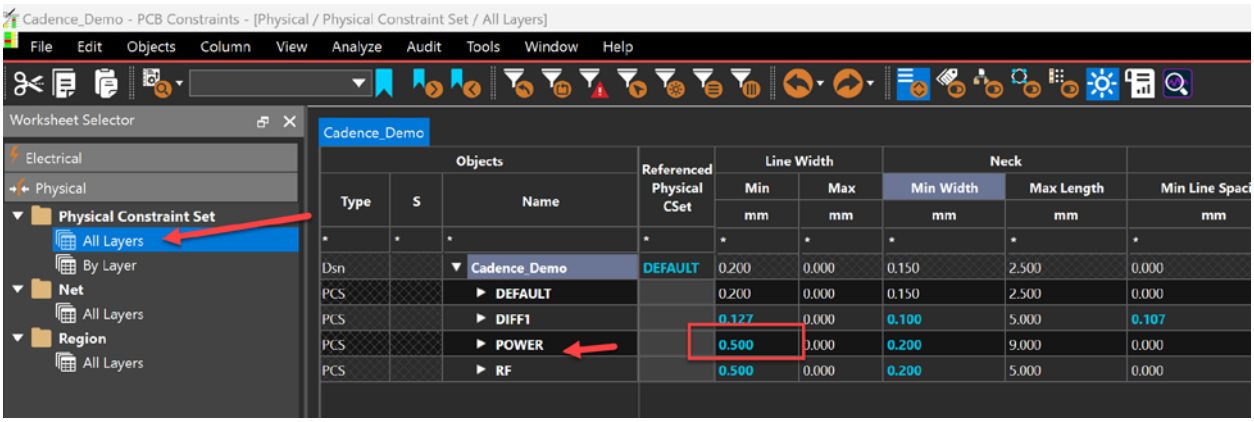
The rest of the constraints are in the high-speed applications section later in this guide.

Standard Physical Constraints

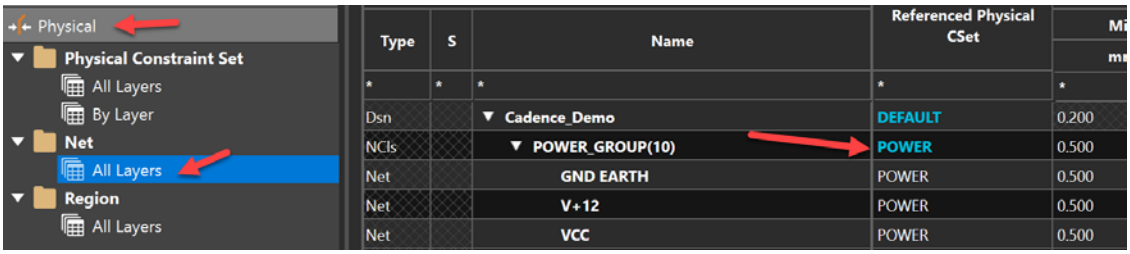
For physical constraints we have the following:

Trace Width

Trace Width (**Line Width**) is set in the Physical CSet to 0.500 mm (19.685 mils) for power traces.

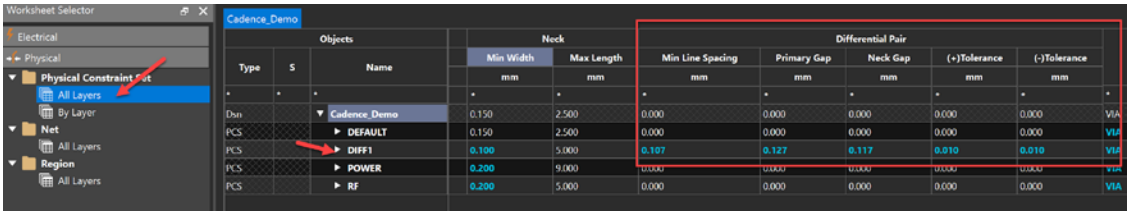


Assign Constraint set to the **POWER_GROUP** nets.



Differential Pairs

In most boards you will have differential pairs, so notice the differential pairs set below.

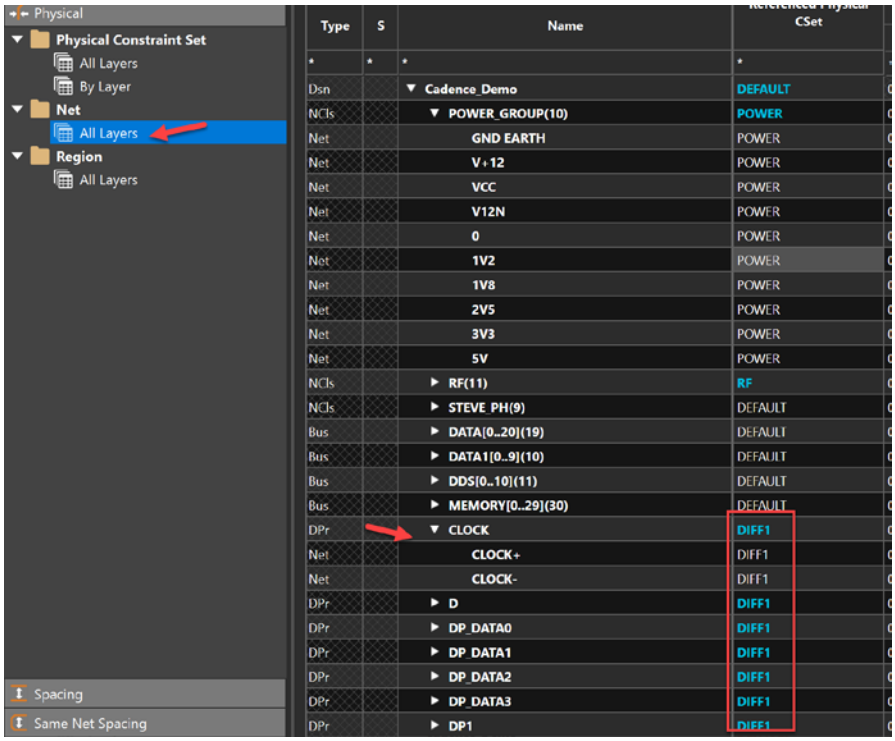


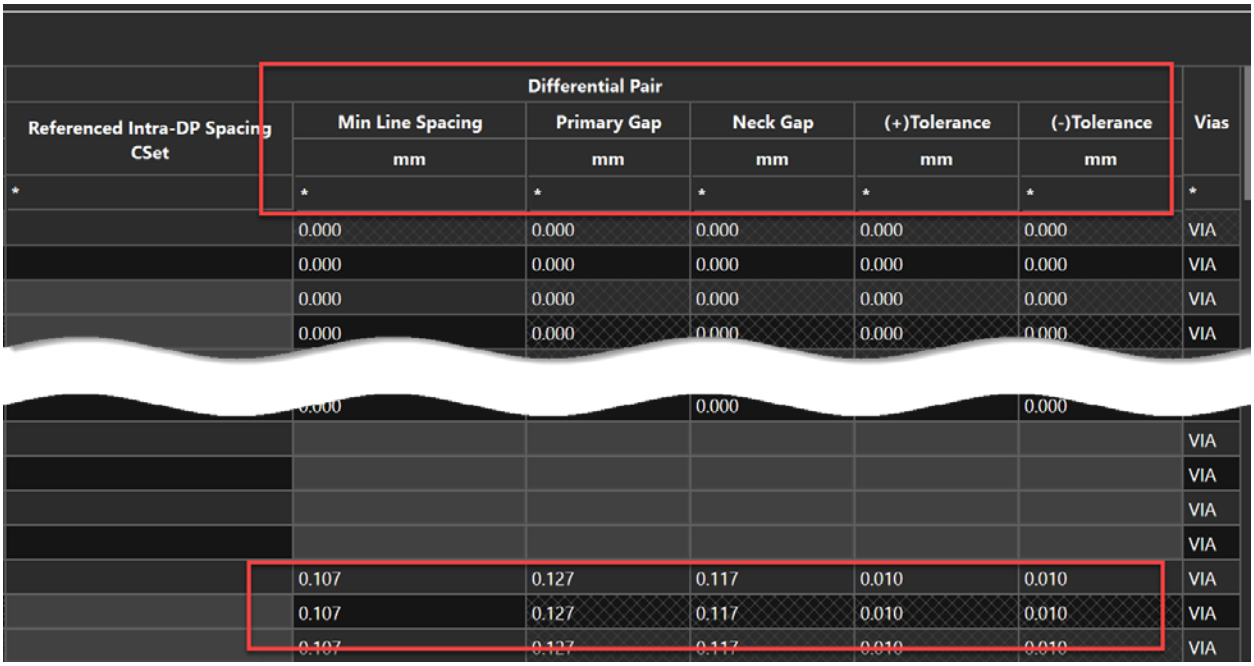
Constraint Set Values

The values from the image are:

- Min Line Spacing = 0.107 mm
- Primary Gap = 0.127 mm
- Neck Gap = 0.117 mm
- (+)Tolerance = 0.010 mm
- (-)Tolerance = 0.010 mm

Applied Constraint Set to diffpairs in the design

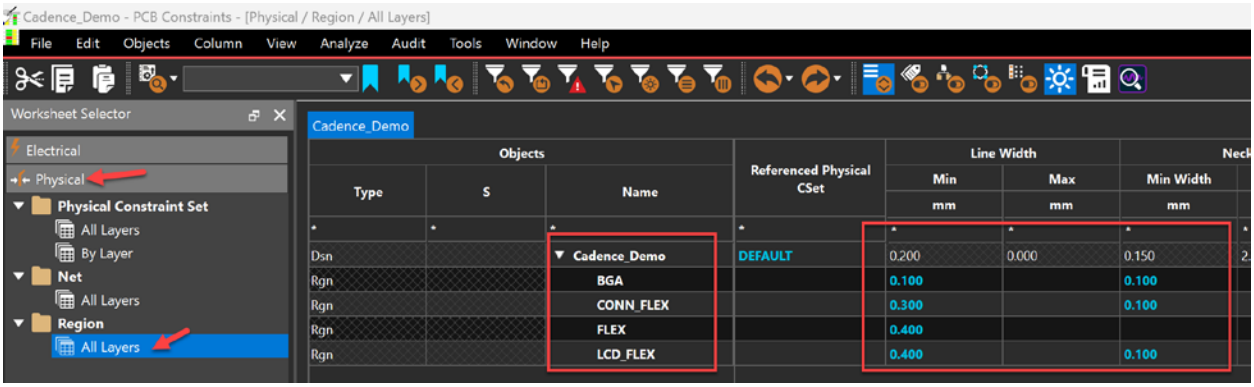




Referenced Intra-DP Spacing CSet	Differential Pair					Vias
	Min Line Spacing	Primary Gap	Neck Gap	(+)Tolerance	(-)Tolerance	
	mm	mm	mm	mm	mm	
*	*	*	*	*	*	*
	0.000	0.000	0.000	0.000	0.000	VIA
	0.000	0.000	0.000	0.000	0.000	VIA
	0.000	0.000	0.000	0.000	0.000	VIA
	0.000	0.000	0.000	0.000	0.000	VIA
	0.000		0.000		0.000	
						VIA
						VIA
						VIA
						VIA
	0.107	0.127	0.117	0.010	0.010	VIA
	0.107	0.127	0.117	0.010	0.010	VIA
	0.107	0.127	0.117	0.010	0.010	VIA

Physical Region

We have BGA and Flex areas where we use a different set of rules for minimum **Line Width**. We can also set **Differential Pair** values, **Minimum Neck** width and so on. In these cases, we simply apply any existing constraint sets we want to use to manage those regions of the board. You can also directly enter the values you want for these regions (shown in blue text).



However, the best method is to create a Physical Constraint Set (see below),

Then assign it to the appropriate region.

Standard Spacing Constraints

Standard Same Net Spacing Constraints

Standard Manufacturing Constraints

Standard 3D Constraints

Standard Properties

Standard DRCs

Applying High-Speed and Advanced Constraints

The following constraints can be applied to complex and/or high-speed PCBs (please refer to the previous sections of this document to learn more about implementing those constraints).

Advanced Constraints Application

Advanced Electrical Constraints

Wiring topology

Set specific routing paths for technologies like DDR3 and T-branch to minimize signal attenuation due to PCB material properties. Or Daisy Chain or star topologies.

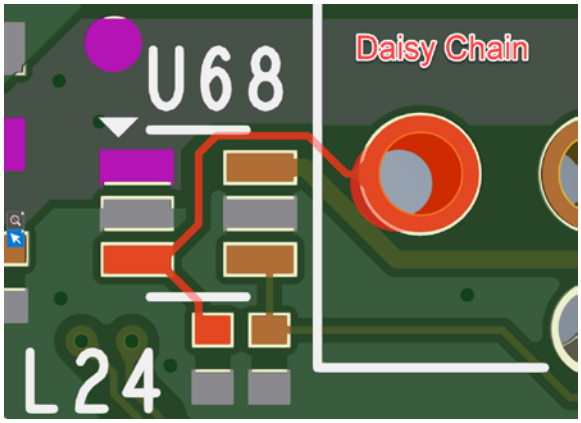


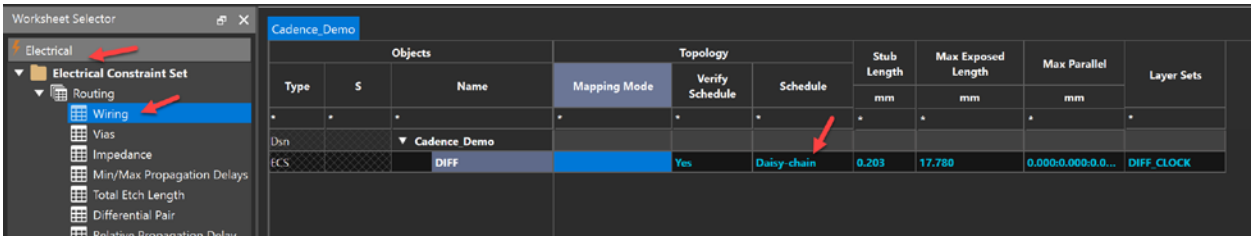
Image: Diagram showing the prioritized routing of critical nets on a PCB.

Definition: Wiring topology involves organizing the connections between different nets on a PCB to achieve a certain outcome, such as minimizing signal reflections, signal attenuation or voltage drops.

Example: Let's ensure that a pulse-width modulated net follows a daisy-chain topology.

Steps:

1. Open the Constraint Manager, then go to the **Electrical > Routing > Wiring** worksheet.
2. In the Type column, you can right click your **Dsn** cell, create a new Electrical Constraint Set (ECS). Notice in the image below, an ECSet has already been created.
3. Select the drop-down in the **Schedule** column and choose your net topology.

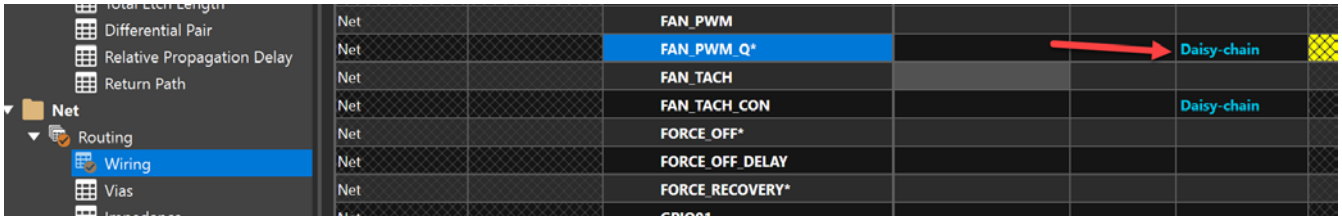


You have options such as:

- Minimum Spanning Tree
- Daisy-chain
- Source-load Daisy-chain
- Star
- Far-end Cluster
- (Clear)

Each topology has its own benefits, depending on the application.

4. Once you have set the topology for that ECSet, you can apply it to the appropriate nets found in the spreadsheet under **Electrical** > **Net** > **Routing** > **Wiring**.
5. In this example, however, you can also directly apply a net schedule (see below).

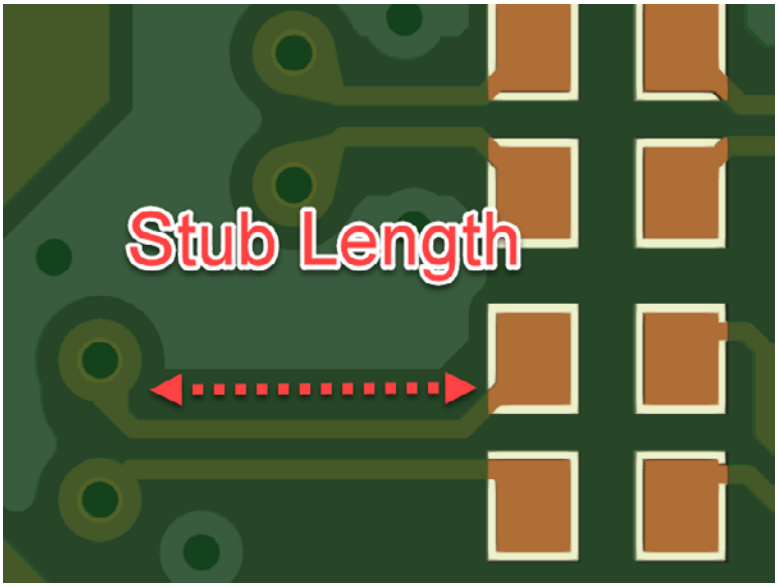


Note: Depending on your use case, you can use either constraint sets, or a specific rule application as needed, like in this example. However, please use constraint sets as often as possible to catch most cases first before applying net-specific one-off rules. Using constraint sets modularizes and streamlines your PCB design constraint process and makes you more efficient. The constraint set method also reduces the likelihood of errors and forgotten constraints. You can also import, and export constraint sets across your team so that everyone adheres to similar standards. The less you do unique constraint values that are outside (or override) the constraint sets, the fewer problems you will have.

Benefit of a good Wiring Topology: Improves signal integrity and timing by ensuring critical connections are made efficiently.

Stub Length (Max Stub Length)

Stubs that lead off traces and pads can act as antennas. Those antennas are problematic for electromagnetic field compatibility and electromagnetic interference (EMC and EMI).



PCB trace stub on top view of PCB

In the image below, we show exactly what gets checked in the software for stub length.

Maximum Stub Length

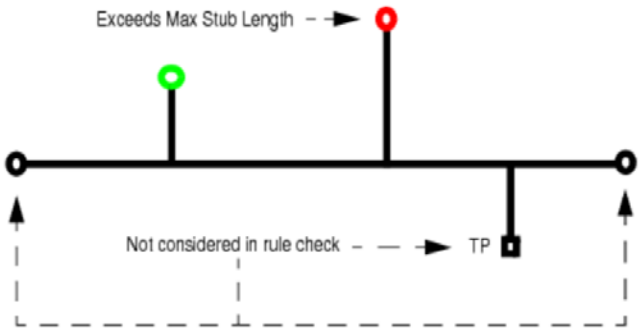
Checks the maximum stub length in design units for daisy chain routing.

Note: When a pin is routed to a connect line, the stub is the line of etch between the pin and the connect line.

The stub length constraint is validated only if NET_SCHEDULE is enabled and RATSNEST_SCHEDULE is set to either MIN_DAISY_CHAIN or MIN_SOURCE_LOAD_DAISY.

>

This check ignores pins at the end of clines, dangling clines, and test points. The chosen net schedule impacts the rule check.



Legal Values: Design Units
DRC Code: ES
Applicable Objects: Xnet, Net, ElectricalCSet, NetClass, DiffPair, Bus, NetGroup
Attribute Name: STUB_LENGTH

Image: A stub as defined in OrCAD X Presto PCB Editor.

Purpose: To restrict the number of stubs on a trace's vias or on a net wiring topology to reduce signal reflections and maintain signal integrity. For high-speed designs, aim for zero or minimal stubs. When stubs are unavoidable, keep them as short as possible.

Applies to: USB, HDMI and any other high-speed interfaces that need minimal fanouts or stubs to operate efficiently.

Importance: Affects current-carrying capacity and signal integrity.

Application: Power distribution, high-speed signals.

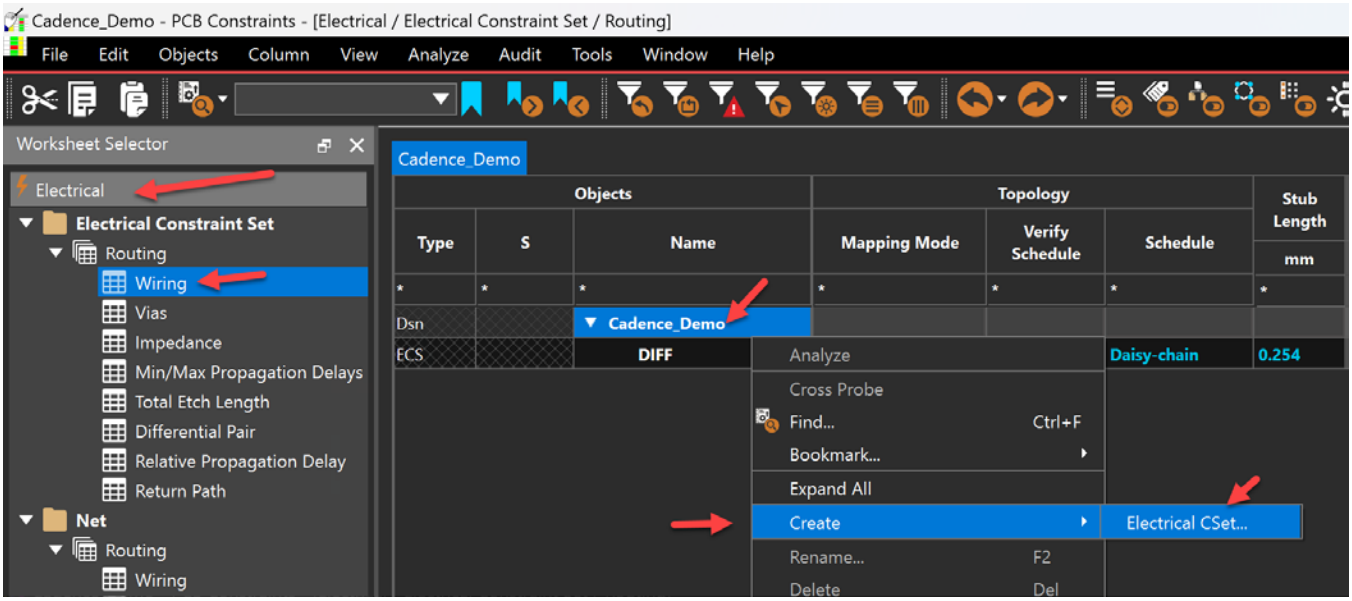
Steps:

1. Open the Constraint Manager using **Tools** - **Constraint Manager**.

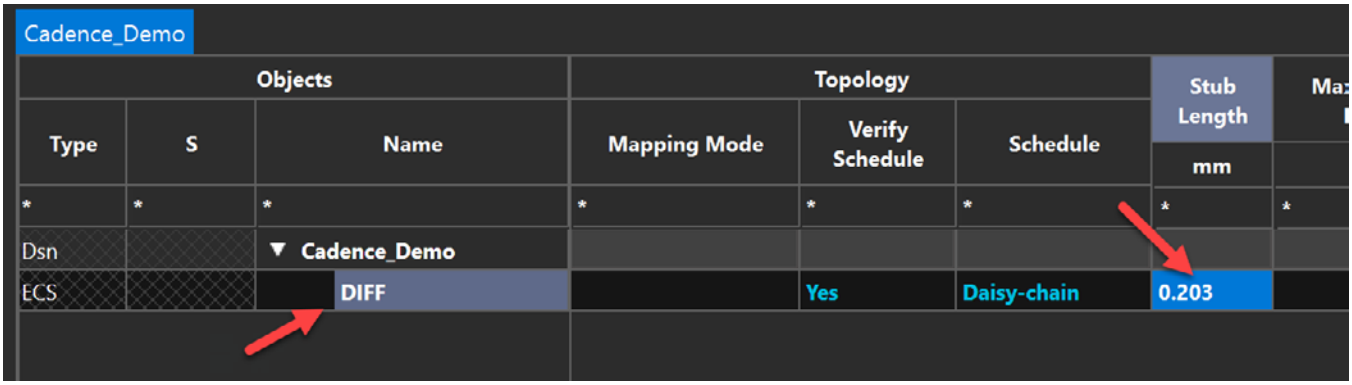
TIP: As usual we will make a constraint set that holds the rules/constraints, then we apply that constraint set to a net, class, group or region.

2. Create an electrical constraint set under **Electrical > Electrical Constraint Set > Routing > Wiring**. Right click the **Dsn** cell's name.

3. Choose **Create - Electrical CSet…**

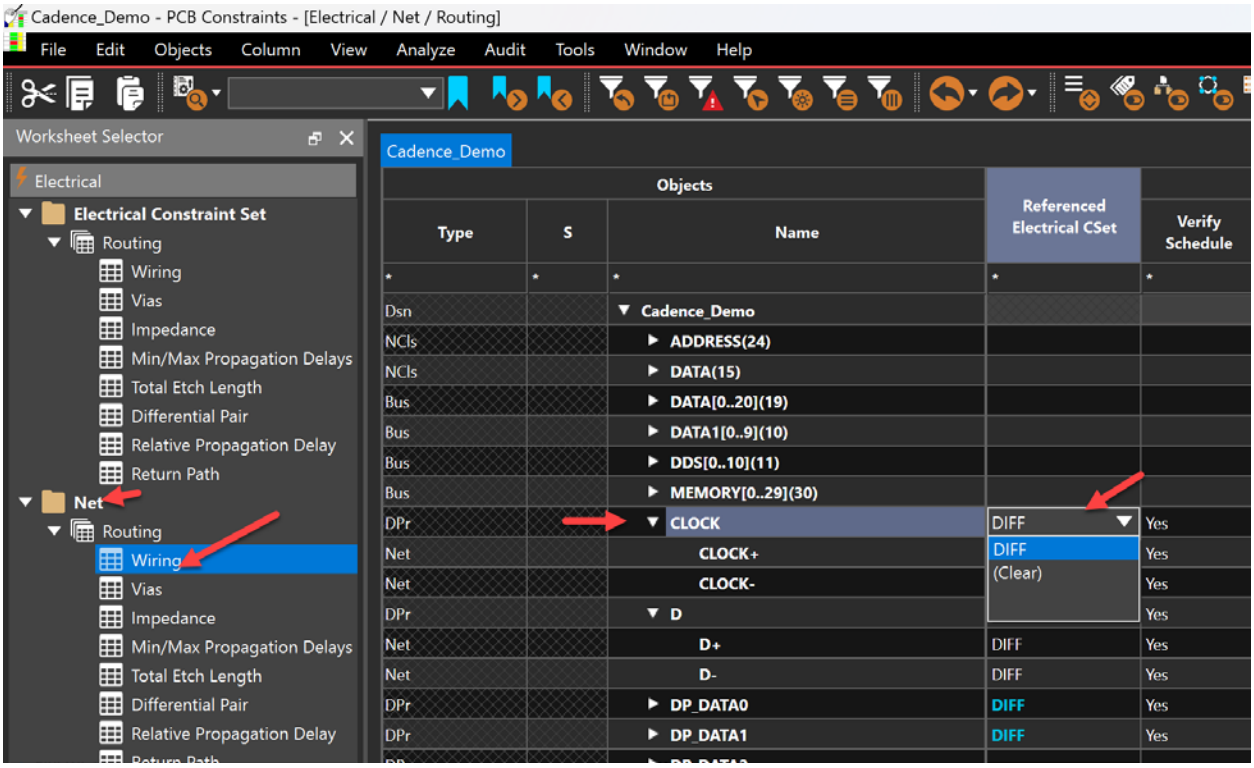


4. Give the ECSet a name and it will be added to the spreadsheet.
5. Once added, enter a desired maximum stub length for the ECSet.
6. For example, let's say you want your stubs to be no more than 8 mils (0.0203 mm), so you enter '8 mils' in the rule shown below for the **DIFF** signal constraint set.

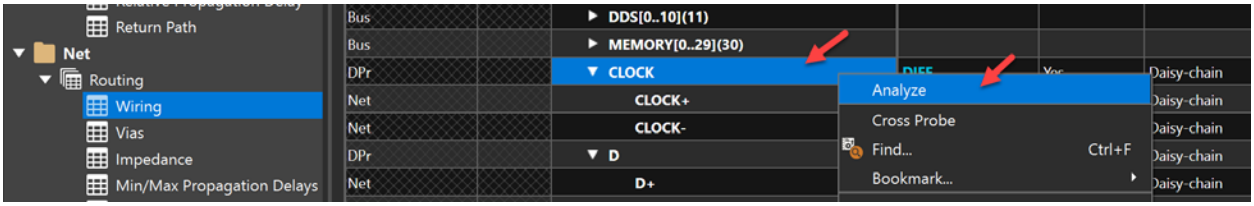


7. Now let's apply that constraint and the stub rule it has.
8. In the Constraint Manager go to **Electrical > Net > Routing > Wiring**.

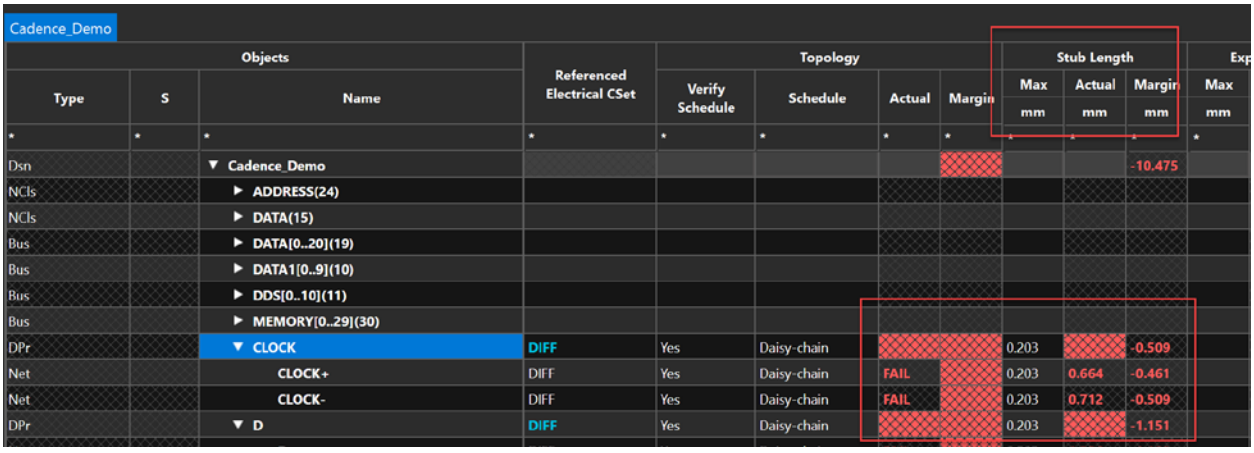
9. Choose from the **Referenced Electrical CSet** column and set it to your desired net.



10. In the Constraint Manager, analyze whether the rules are being adhered to by a particular net class, group, or differential pair, by right clicking that Object name and choosing **Analyze** (as shown below).



11. You will then see results on whether Stub Length limits are being adhered to for any traces that need that constraint set applied.



Reminder: Stub Length Limits are used to ensure tight signal integrity and minimal reflections and antennas, namely for nets that carry signals with extremely short rise times (30 picoseconds or less, 5 GHz or higher frequencies).

Similar to stub length limits, we need to limit total trace length on the outer layers of the PCB to avoid EMI that are picked up by or transmitted from said traces.

Maximum Exposed Length

Set a maximum length for exposed stubs to prevent unintentional antenna effects. This is particularly important for high-frequency signals where wavelengths are shorter. A general rule of thumb is to keep stub lengths below 1/20th of the signal's wavelength, but please note that each situation depends on **simulating** the conditions for your specific stack-up, your dielectric and conductor materials, signals being transmitted and preliminary signal integrity analysis. Rules of thumb, while can often be a good enough solution sooner, can still lead to re-spun boards later without proper simulation.

TIP: You can perform signal integrity analysis and simulations pre-layout, during layout and post-layout using TopXplorer.

To ensure that you're on track with your signal integrity goals, use information on signals propagating through your design and are using IBIS models for your transmitting ICs and simulate them in TopXplorer.

For example, this differential pair, CLOCK (CLOCK+ and CLOCK-) from the images in the Stub Length section of this part can be analyzed as it is right now. You want to simulate the circuit topology, test some conditions to find out what will make it compliant with your Stub Length requirements.

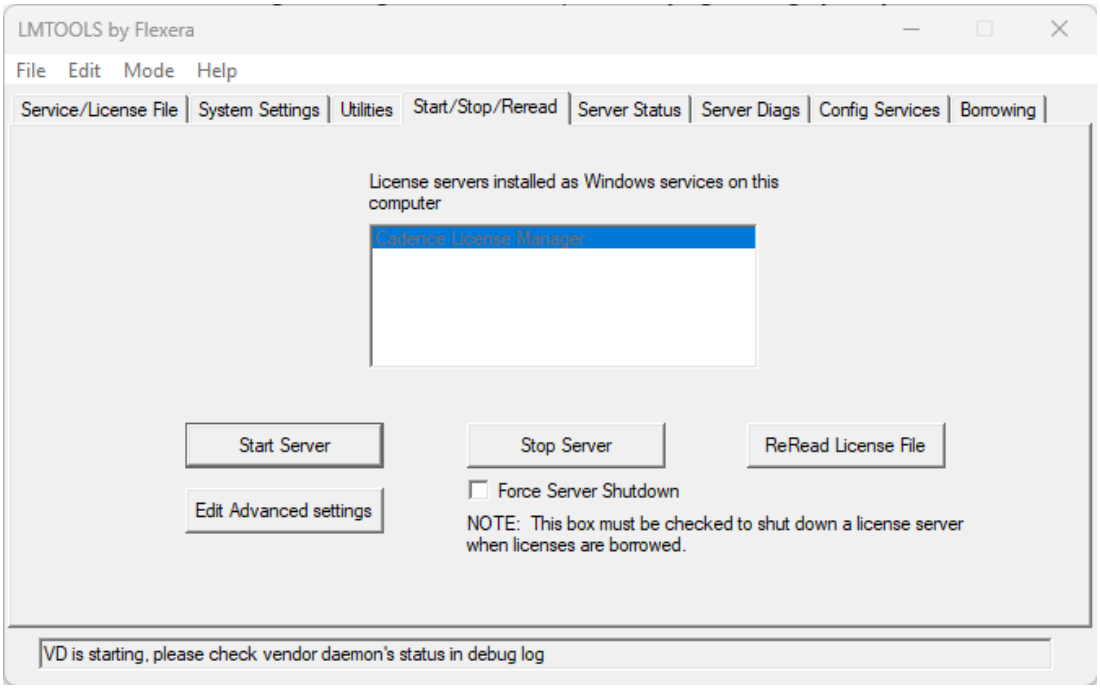
To do such analyses on any net, right click the Net Class/Group/Diff Pair object name, select Explore Topology.

IMPORTANT NOTE: If you get an error message regarding licenses not being available, you first need to download and install the correct version of Cadence Sigrity X Aurora software (for example if using OrCAD X 24.1, then install Sigrity 24.1 and its subsequent updates for that base version 24).

After that, even when installed, you may need to create and set the Environment variable (SIGRITY_EDA_DIR = C:\Cadence\Sigrity2024.1) in both the local and system environment variables in Windows.

Finally, open LMTools (would be installed from the License Manager software from Cadence) from the Windows Start menu. Then go to the Start/Stop/Reread tab, click the ReRead License File button, then after waiting for 10-20 seconds, click the Stop Server button, then wait another 5-10 seconds, then click Start Server.

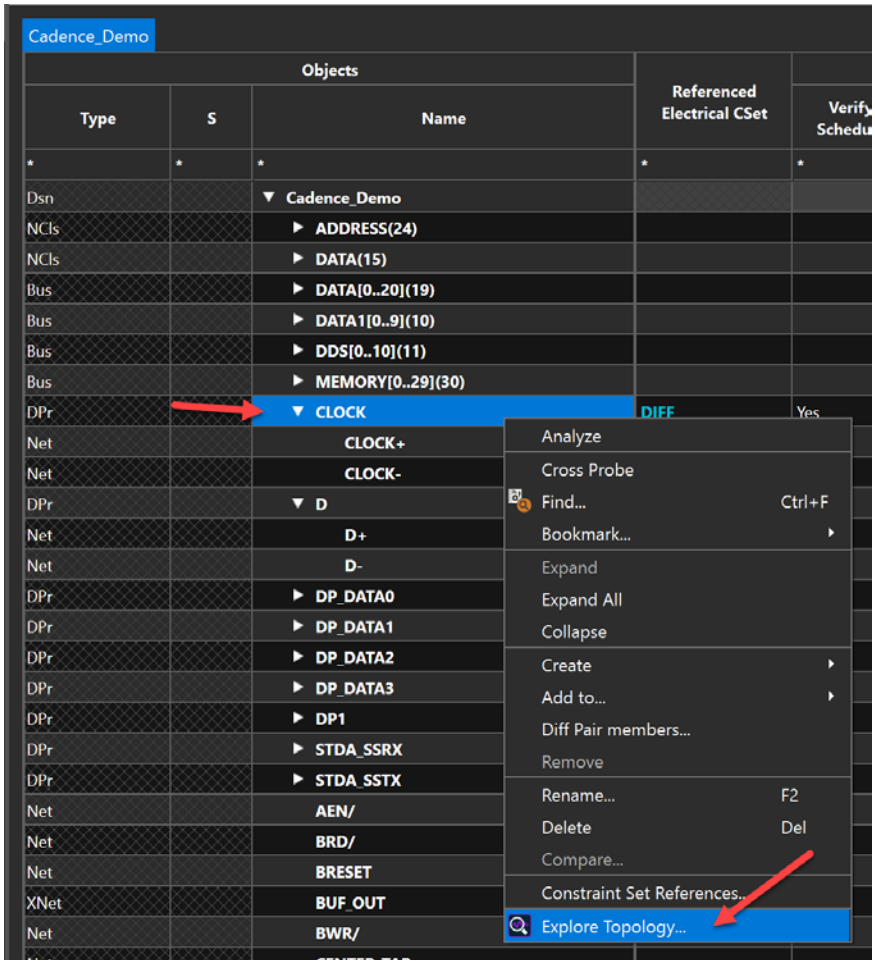
After another 5-20 seconds (the LMTOOLS by Flexera window might stop responding during this time, but it will respond eventually), you can run TopXplorer from the Constraint Manager.



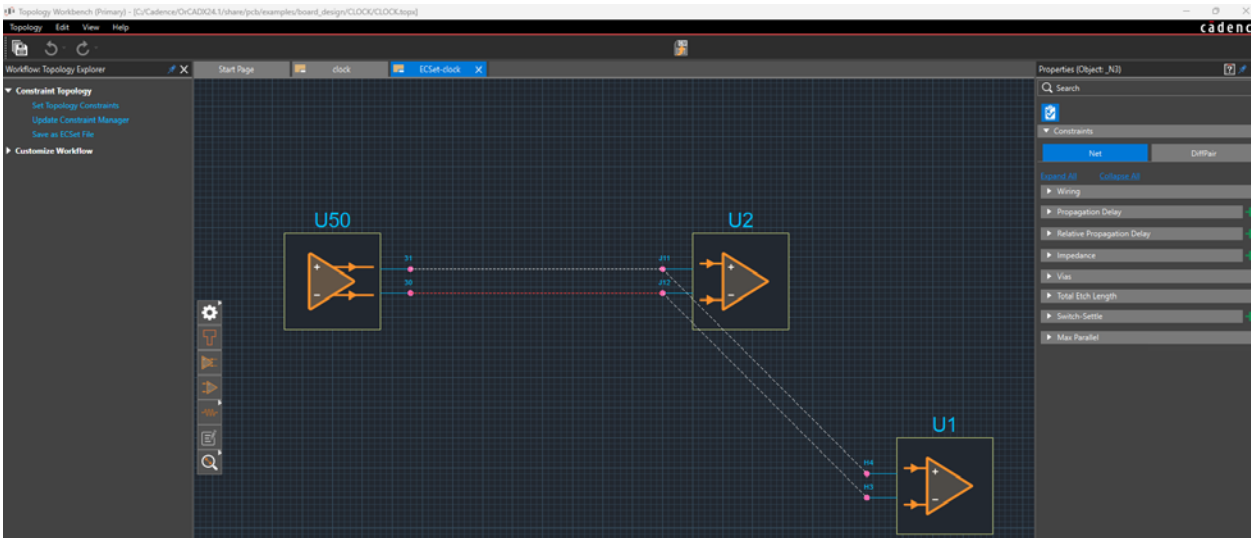
We will not show how to use TopXplorer, but only how to access it, since using TopXplorer is outside the scope of this document.

Steps to find a trace(s)' topologies in TopXplorer for signal integrity and transmission line analysis:

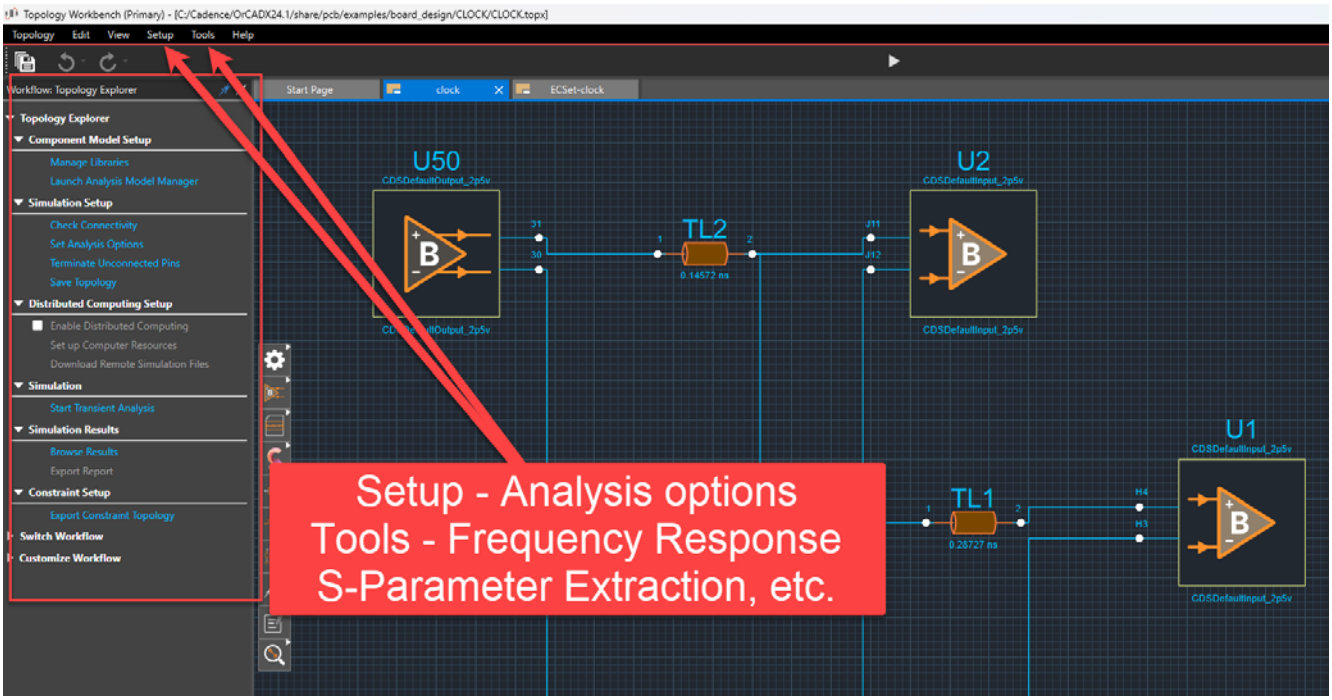
1. Within Constraint Manager, right click an object (like a differential pair like CLOCK), then select **Explore Topology.**



2. A window like the one below opens and you can explore various features and tools to analyze your signals, considering the actual board they are on, in real-time.



We will stop there for now, but know that you can do all sorts of things like different analysis types and options, frequency response and even S-parameter extraction. The findings from such analysis methods can be back-propagated as desirable constraints back into the Constraint Manager. Then the PCB designer can use those new constraints as the rule of law to finish laying out the PCB to meet requirements.

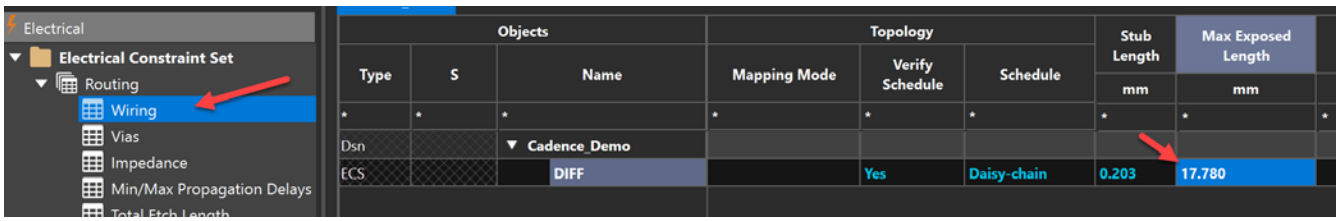


Results-driven design (i.e. from simulation findings and requirements) is a mandatory part of the process to support first-time right design and fewer design iterations and re-spins. TopXplorer is a signal integrity tool that adheres to the results driven design standard for modern PCB designers and hardware engineers.

Let us switch gears back to maximum exposed length. In the next set of steps, we will show how to set the maximum exposed length of conductive material that is allowed on the outer layers of the PCB (top and/or bottom).

Steps on how to change maximum exposed length outside the PCB:

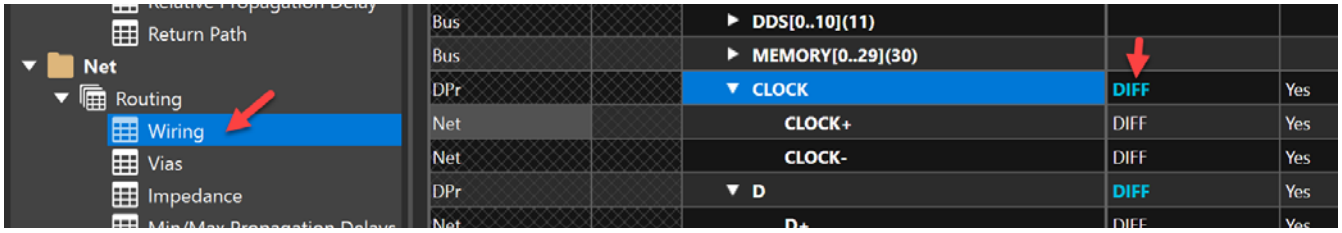
1. Similar to the stub length rule application, open the Constraint Manager.
2. Create an electrical CSet in the **Electrical Constraint Set > Routing > Wiring** worksheet OR use an **existing** CSET (e.g. DIFF).
3. Set the **Max Exposed Length** to say, 750 mils (17.780 mm).



Design Note: This value was chosen arbitrarily as half the 1500 mil critical trace length for a USB 3.2 differential pair signal operating at 5 GHz Nyquist frequency (i.e. 10 Gbps) from a Texas Instruments controller from their datasheet recommendations. The reason being that the rise time for that chip and a 10 Gbps per second signal hovers typically around 20-30 picoseconds and the speed of travel to avoid reflection is around the 1500 mil mark. Then, we decide to cut that in half to be more on the cautious side, since we want at most, both outer top layer and outer bottom layer traces to result in that 1500 mil limit. However, you **must** verify with the chip manufacturer and/or designers the expected signal speed and acceptable

critical length to know what a 'safe' outer layer trace length should be. For instance, if your signals are pushing 40 Gbps (20 GHz Nyquist) and quadruple the MT/s of USB 3.2 then cut 1500 mils down to a quarter of what we put for USB 3.2. (i.e. 1500 mils / 4 = 375 mils). But that's a rule of thumb. Verify with TopXplorer. The real-world requirements can vary significantly depending on dielectric and conductive materials of the PCB, coating, environment, etc. If you do need to use a rule of thumb and don't have access to simulation, then a very conservative value is 1/20th the signal wavelength. Verify with simulation later.

4. Finally, go to **Electrical > Net > Routing > Wiring**.
5. Click and apply the appropriate ECSet onto the desired net by selecting the ECSet from the **Referenced Electrical CSet** column. The rule is automatically applied to that net.



Objects		Referenced Electrical CSet	Topology				Stub Length			Exposed Length		
	Name		Verify Schedule	Schedule	Actual	Margin	Max	Actual	Margin	Max	Actual	Margin
							mm	mm	mm	mm	mm	mm
	*	*	*	*	*	*	*	*	*	*	*	*
▼	Cadence_Demo								-10.475			-55.190
▶	ADDRESS(24)											
▶	DATA(15)											
▶	DATA[0..20](19)											
▶	DATA1[0..9](10)											
▶	DDS[0..10](11)											
▶	MEMORY[0..29](30)											
▼	CLOCK	DIFF	Yes	Daisy-chain			0.203		-0.509	17.780		12.089
	CLOCK+	DIFF	Yes	Daisy-chain	FAIL		0.203	0.664	-0.461	17.780	5.222	12.558
	CLOCK-	DIFF	Yes	Daisy-chain	FAIL		0.203	0.712	-0.509	17.780	5.691	12.089

Notice how the CLOCK signal adheres to the Exposed Length restriction (green color means it adheres/is good), with margin to spare (12.089 mm to work with).

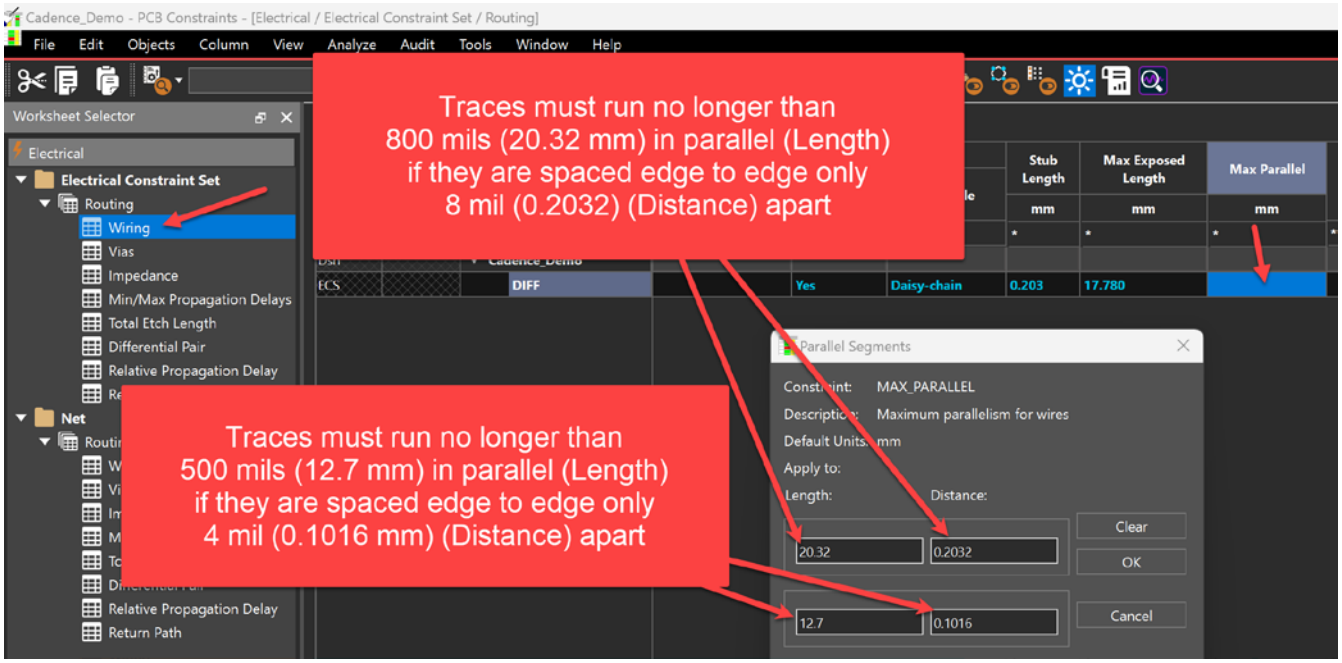
As an experiment, adjust the margin to something like 1 mil and see what happens to the same row being analyzed. It will turn red immediately, since the Constraint Manager is always active.

Key Note:

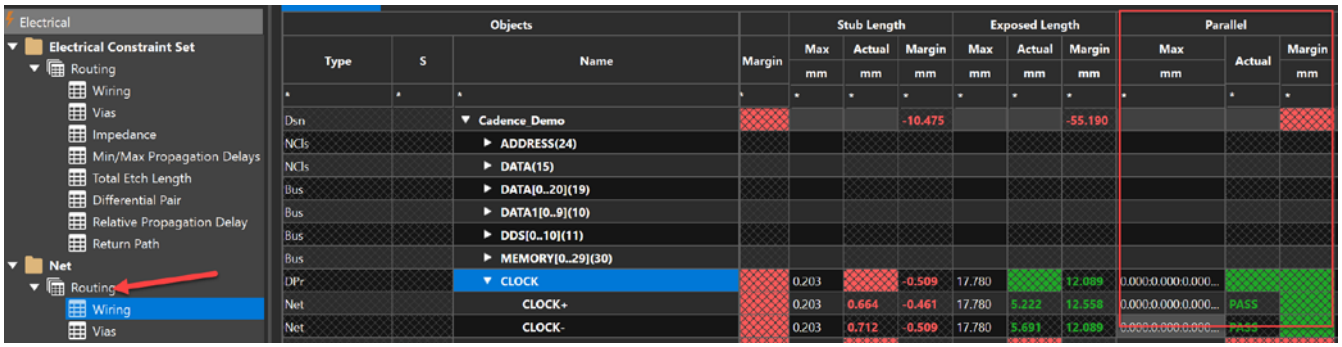
For the rest of this project application, follow the instructions from previous parts of the guide as the steps are the same. We will show images of our implementation for this design.

Maximum parallel trace length

Limit the length that signal traces run parallel to each other to reduce coupling and crosstalk. This is especially crucial for high-speed differential pairs. The acceptable length depends on factors like trace spacing, layer stack-up, and signal frequency. So the values below are just examples. We set the allowed Max parallel traces for two situations for this Constraint Set.



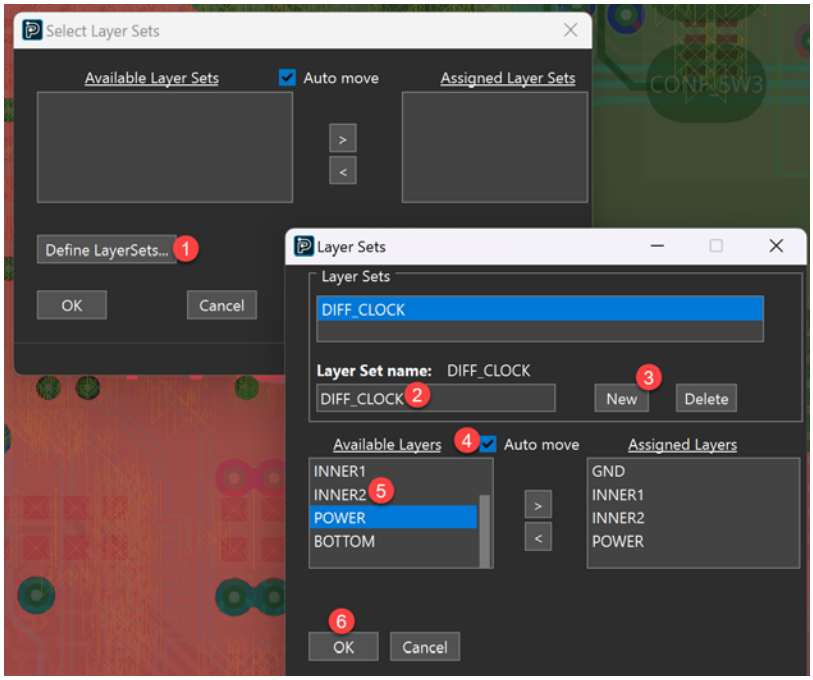
The Rule immediately applies in the Constraint Manager and the design adheres to the rule.

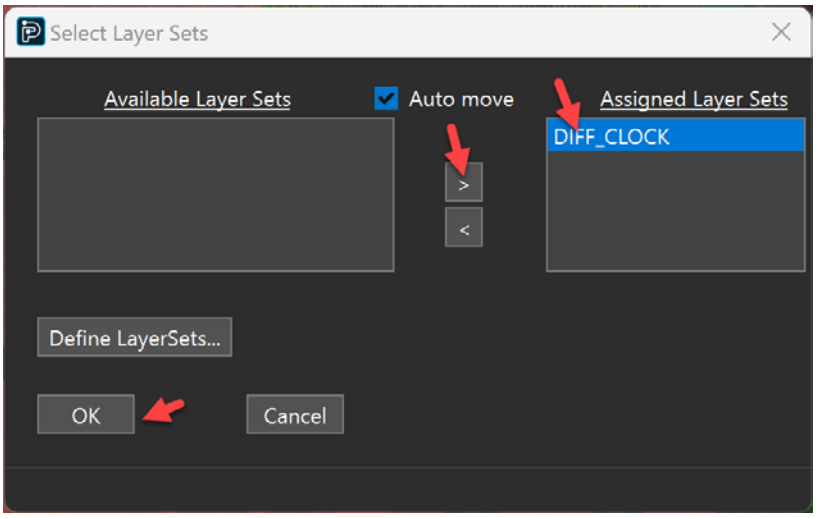


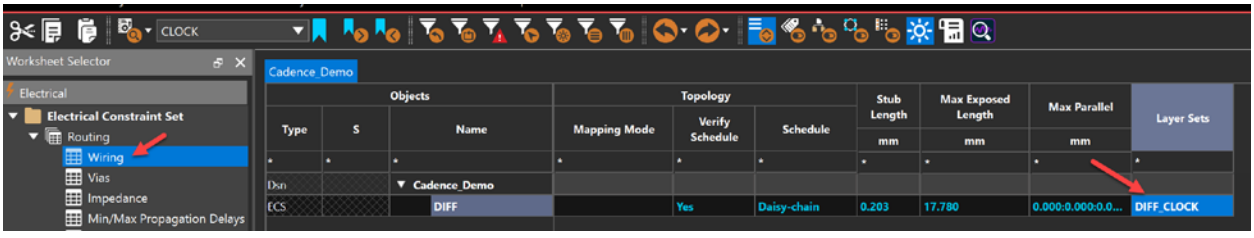
Layer restrictions

Control EMI by limiting the layers through which a trace can be routed. For example, keep high-speed signals on internal layers sandwiched between ground planes for better shielding.

In our design, we want the CLOCK+ and CLOCK- signals to **not** be routed on the PCB surface. It is sensitive to noise and controls the timing for important devices in the design. So, we set the allowed routed layers to the internal layers (as seen below).

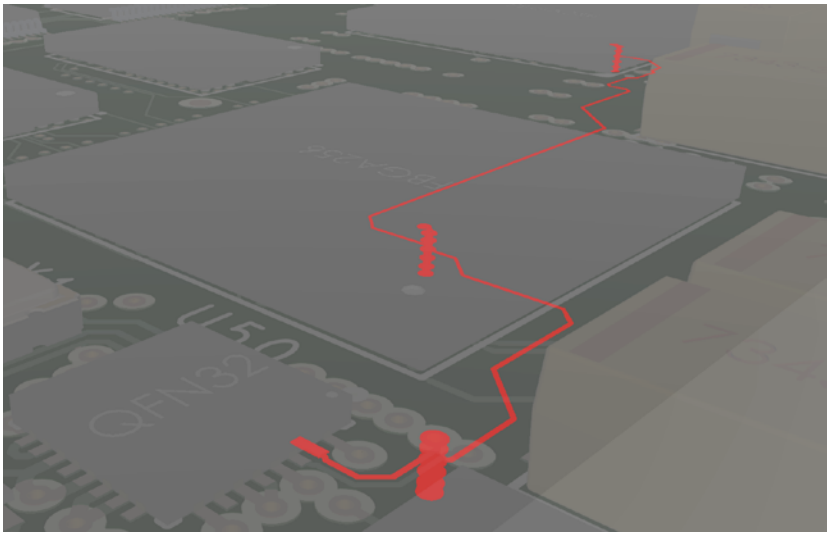






The routing adheres to this layer set rule (at least for CLOCK+ and CLOCK-) but does give some indication/warning about the lengths of trace material that were ignored in the process. Strictly speaking, it is not realistic for **no** amount of trace to fall outside a layer restriction. So, some is acceptable/ignored.

To visualize this, here is the CLOCK+ signal trace shown below.



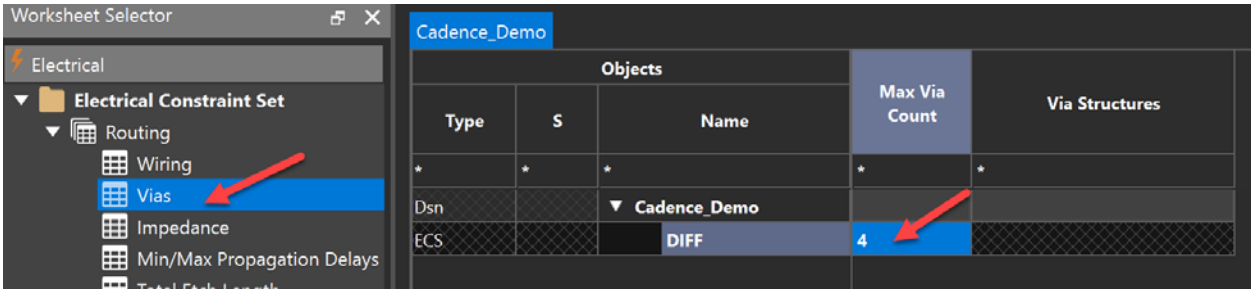
Now that this is finished, let's move to Vias.

Maximum via count

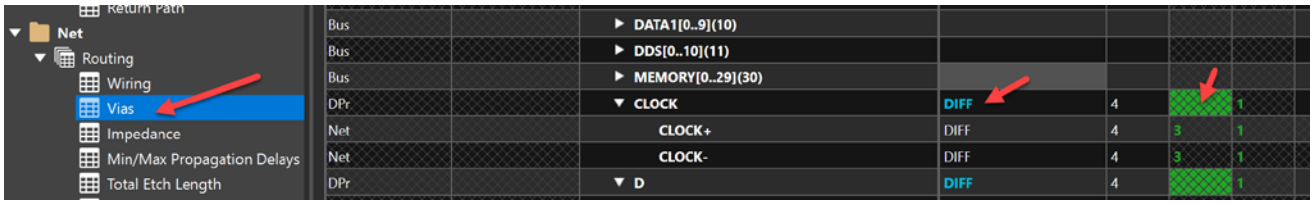
Set the maximum number of vias for a trace or net to maintain impedance control and minimize parasitic capacitance. Each via introduces discontinuities and can degrade signal integrity, especially at high frequencies.

The maximum number of vias we will allow on traces that take on the DIFF Constraint set is 4 Vias (ideally it should be 2-3, but 4 can work in our case).

Here is the Constraint set being modified:



And here is how the design holds up to that constraint:



The actual count is green, meaning we are within our 4-via limit. The margin is 1, so we can add one via and still be within the limit.

Characteristic impedance

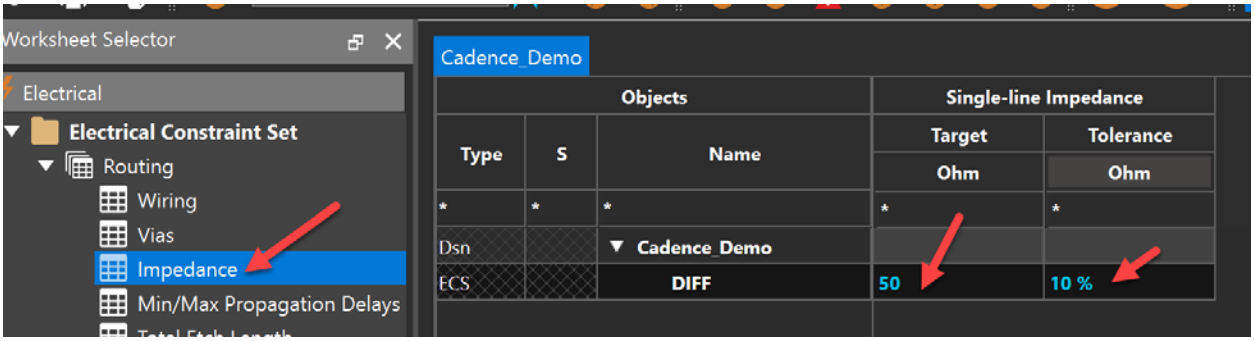
Specify target impedance values (e.g., 50Ω for single-ended traces, 100Ω for differential pairs) to minimize reflections and ensure compatibility with specific communication protocols. This involves controlling trace width, spacing, and dielectric properties.

Our manufacturer said they can do 50 Ohm single ended impedance on traces but within a 10% tolerance without charging significantly more money. So, we'll go with that option below.

Note: The differential impedance can be calculated from the Cross Section Editor for the PCB Stackup. It is found in the OrCAD X Presto PCB Editor menu item **Tools – Cross Section**. How to use the tool to do the calculations is outside the scope of this guide. For now, assume that a 50-ohm single-line impedance is roughly an 85 to 130 Ohm differential impedance.

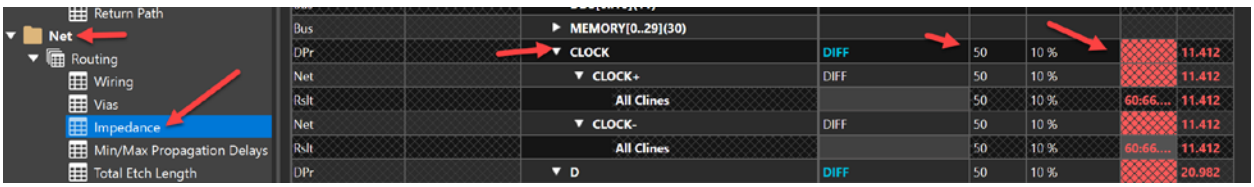
But use the calculated values for differential impedance from the Cross Section tool, then input those values into the Differential Pair part of the Constraint Set.

The single-ended impedance range could end up being violated for differential traces, depending on the situation, and still be okay for the design to perform.



TIP: For Tolerance, you can simply type a value, then the software will assume you mean Ohms. For example, type in 10, then hit Enter. Your software will set it to 10 Ohm. You can type in 10 % instead, however, and it will adjust the Ohm accordingly without you having to calculate it.

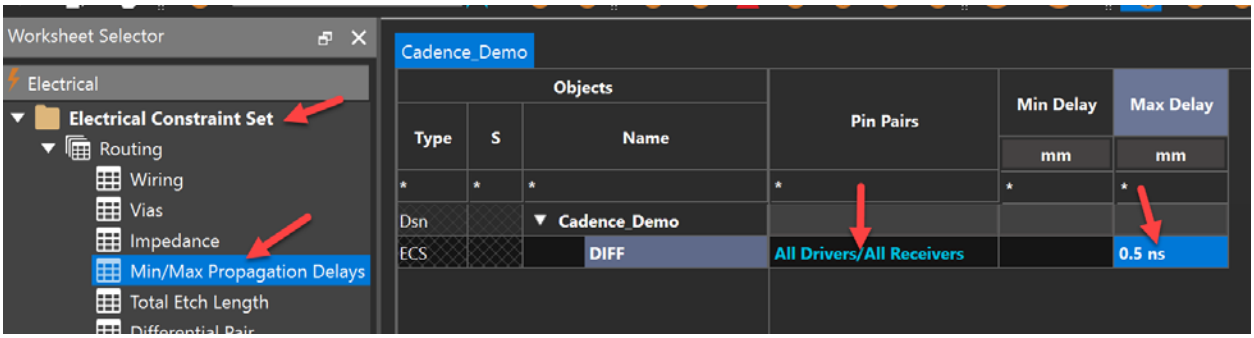
The PCB designer routed the traces and they fall outside the single ended impedance range, but that's fine. For traces that need single-ended to be 50 Ohms, it works out fine.



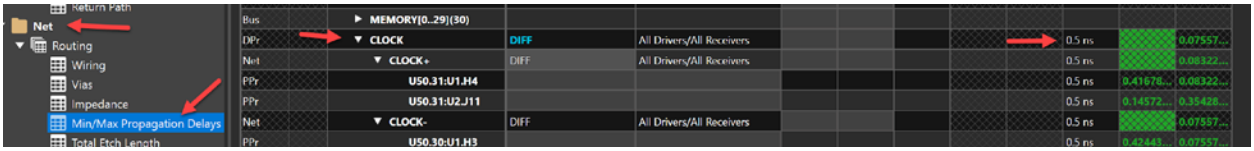
Propagation delay modeling

Create accurate models of signal propagation delays to account for potential signal degradation during operation. This helps with timing analysis and ensuring proper synchronization in high-speed designs.

We set the Constraint Set values to the ones shown below (**All Drivers/All Receivers** at a **Maximum Delay** of 500 picoseconds = 0.5 nanoseconds).



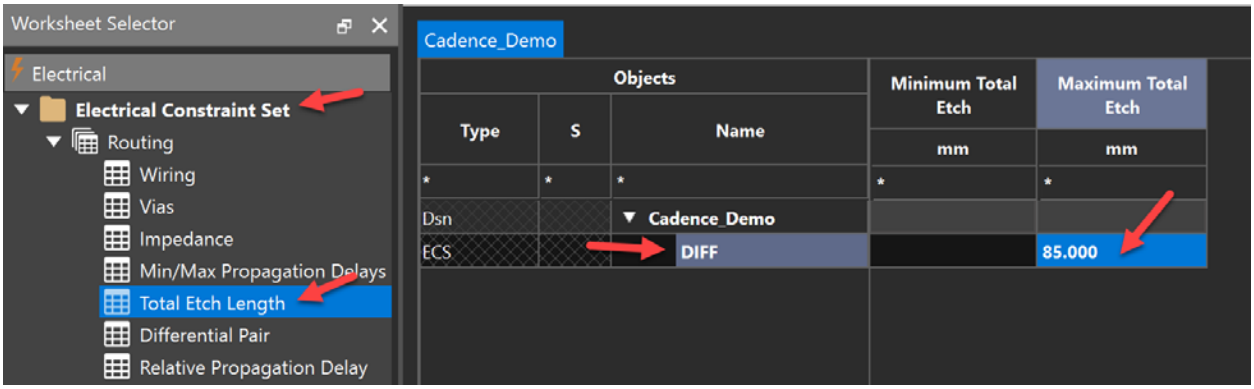
Then when we check our design (which takes pin delay into consideration) we see that we're within our constraints (we are still within the DIFF Constraint ECSet, as a reminder).



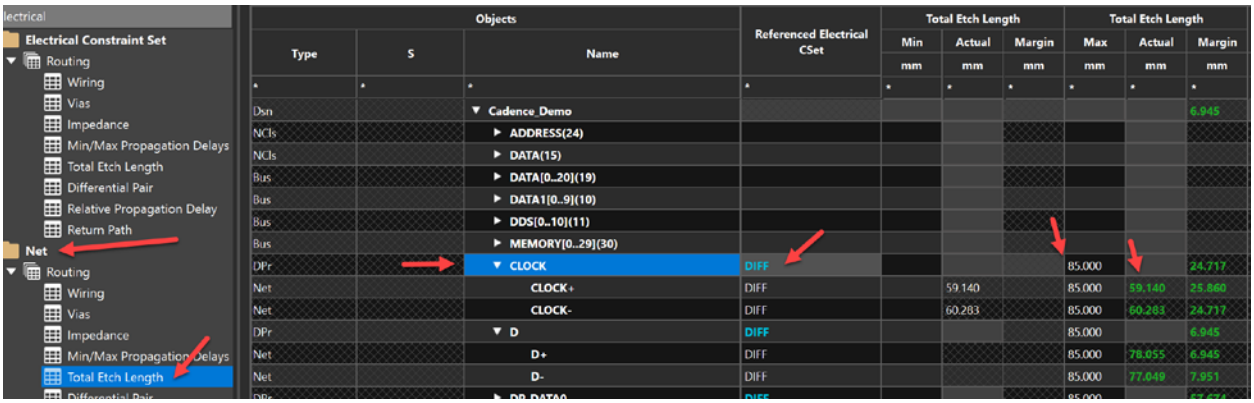
Total etch length limits

Set maximum trace lengths to avoid critical timing issues and signal degradation. This is particularly important for high-speed signals where longer traces can lead to increased attenuation and skew.

Let's say our total etch must not exceed 85 mm based on calculations from the materials, dissipation factor of the dielectric, conductive material type, etc. That rule gets applied to the Constraint Set under **Maximum Total Etch**, as shown below.



Then we check if we're within spec, it shows that we are well within range.



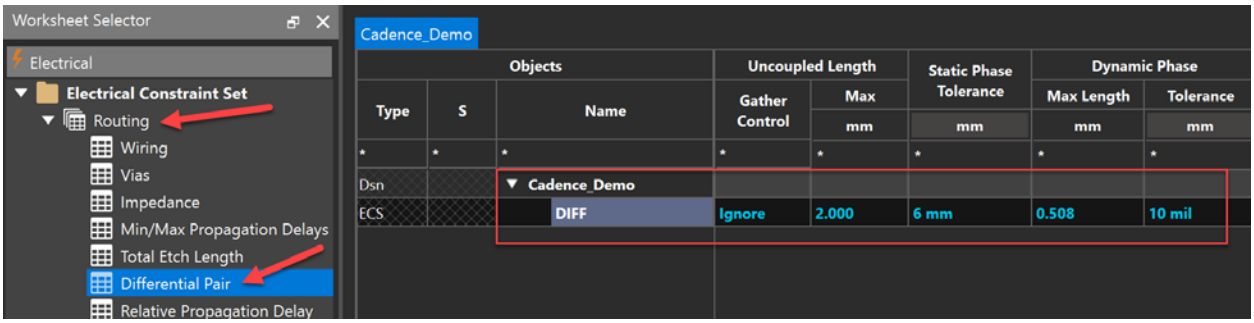
Differential pair rules

Implement specific rules for differential pairs to ensure optimal signal propagation. This includes:

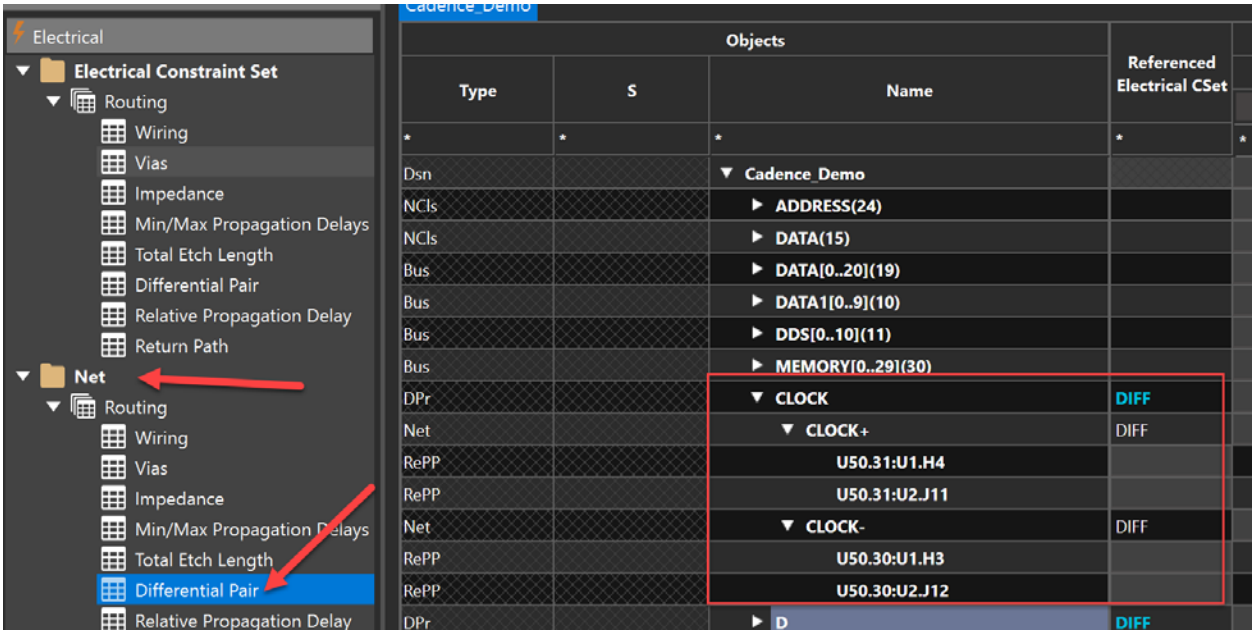
- **Dynamic phase tolerance:** Allow for slight variations in differential pair length matching to account for manufacturing tolerances.
- **Static phase control:** Set strict length matching requirements to minimize skew between the positive and negative signals.
- **Maximum uncoupled length:** Specify the maximum length that differential pair traces can be routed separately before recoupling.

Interestingly, the differential pair rules are split in which sheet we can use to constrain that differential pair (i.e. we can use Electrical Constraints or Physical Constraints). We recommend using the Electrical Constraint Set rules for Differential Pairs for Uncoupled Length, Static Phase Tolerance and Dynamic Phase, then use Physical Constraint sets for the other parameters on that Differential Pair.

As shown below, we set some differential pair rules in our Electrical Constraint set.



Then in the Net section we can apply them.



We see the routing is within range for our signal integrity related constraints we made in the **Electrical Constraint Set** named DIFF.

Objects	Pin Delay		Uncoupled Length					Static Phase			Dynamic Phase	
Name	Pin 1	Pin 2	Gather Control	Length Ignored	Max	Actual	Margin	Tolerance	Actual	Margin	Max Length	Tolerance
	mm	mm		mm	mm	mm	mm	mm			mm	mm
Cadence_Demo							0.035			2.571 mm		
ADDRESS(24)												
DATA(15)												
DATA[0..20](19)												
DATA1[0..9](10)												
DDS[0..10](11)												
MEMORY[0..29](30)												
CLOCK			Ignore		2.000		0.168	6 mm		4.905 mm	0.508	10 mil
CLOCK+			Ignore		2.000		0.417	6 mm			0.508	10 mil
U50.31:U1.H4			Ignore	1.472	2.000	1.583	0.417	6 mm			0.508	10 mil
U50.31:U2.J11			Ignore	1.660	2.000	0.828	1.172	6 mm			0.508	10 mil
CLOCK-			Ignore		2.000		0.168	6 mm		4.905 mm	0.508	10 mil
U50.30:U1.H3			Ignore	1.516	2.000	1.832	0.168	6 mm	1.095 mm	4.905 mm	0.508	10 mil
U50.30:U2.J12			Ignore	1.906	2.000	0.828	1.172	6 mm	1.052 mm	4.948 mm	0.508	10 mil

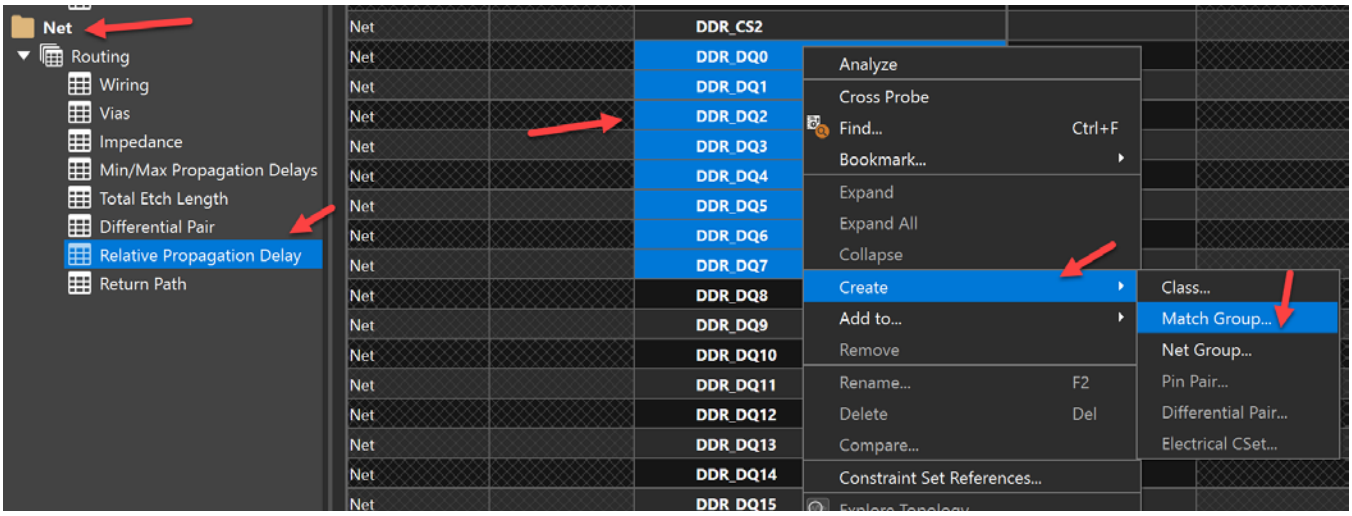
Relative signal velocity

Understand and account for the relative speed at which signals travel through different PCB materials and trace geometries. This knowledge is crucial for accurate timing calculations and can help prevent board re-spins due to signal integrity issues.

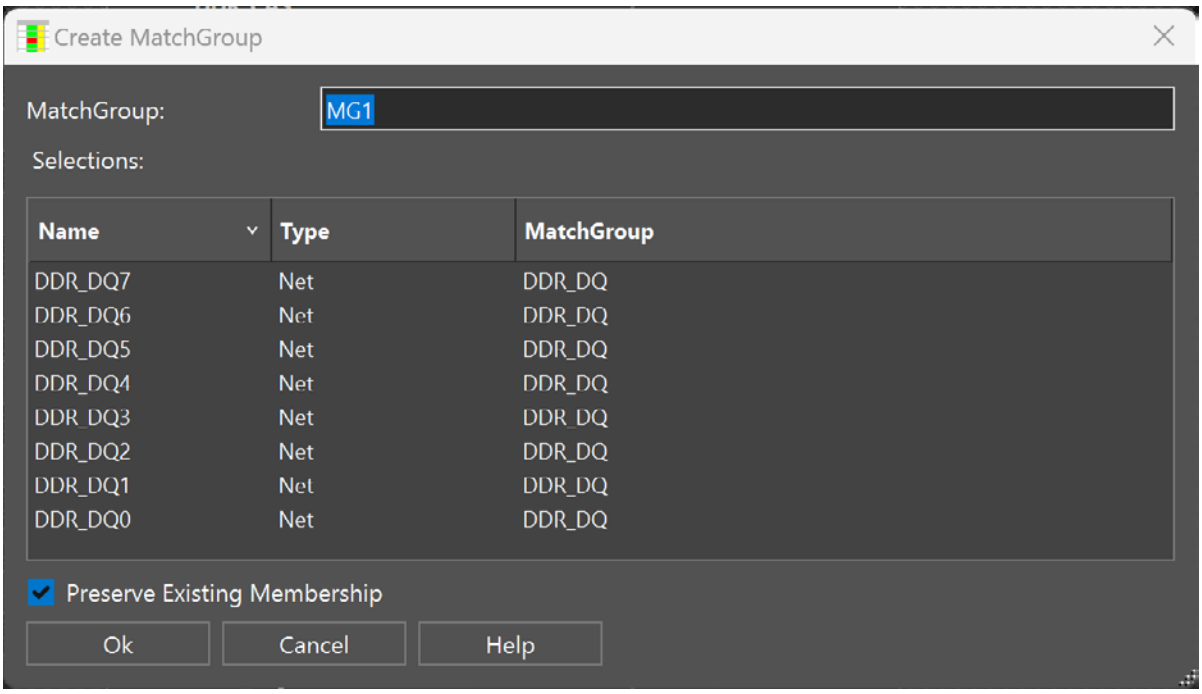
Relative propagation delay applies for Match Groups that need to be length matched within their local group of signals. For instance, if we have signals for DDR like DDR_DQ0-DDR_DQ7 and they all need to have their signals arrive within 15 picoseconds of one another or less. There is a way to let the Constraint Manager know this.

In Constraint Manager, in the Electrical category, go to your **Net > Relative Propagation Delay** worksheet.

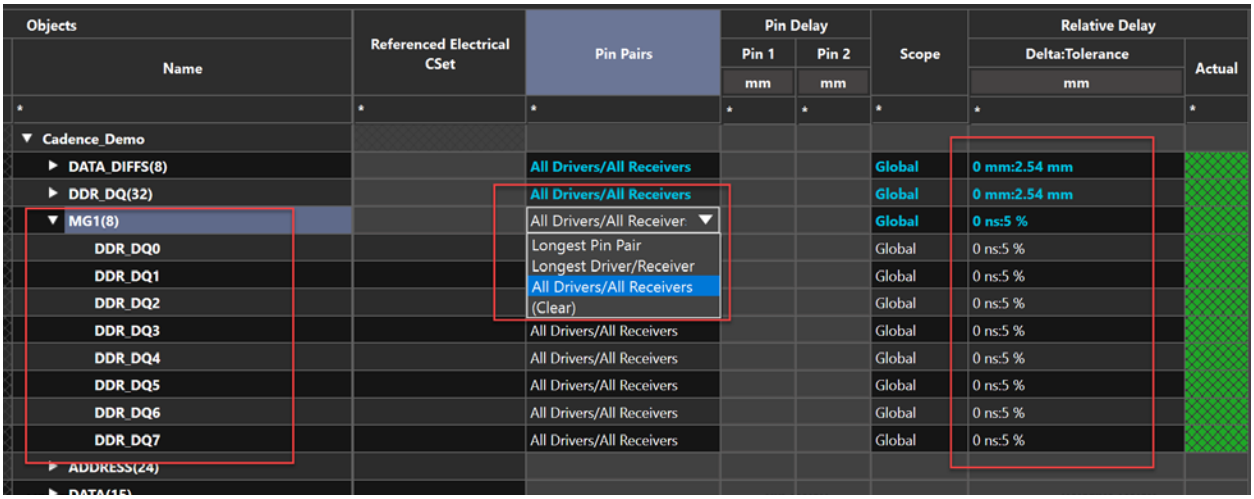
Highlight the nets you want to add to a matching group (i.e. DDR_DQ0 through DDR_DQ7, for 8 bit), then right click, **Create – Match Group…**



Give the match group a name.



Then click Ok. You will get the following image below and the option to change what Constraint Manager cares to constrain.



The largest benefit for this constraint type at all is to minimize skew. Skew occurs when two or more signal traces are carrying signals that need to arrive at the receiver at a similar time, but they do not. Instead one signal arrives so early or late, that the information they are supposed to share (using parallel communication) gets out of sync or 'skewed', then the data becomes corrupt. If that happens often enough, you may get a blue screen of death (BSOD) on a computer, as an example of a system that is not unfamiliar with skew.

Note that you can force the trace lengths within a match group to always match their lengths with the Longest Pin Pair found in that group. For example, let's say the longest trace you routed was DDR_DQ5 at 1600 mils (40.64 mm).

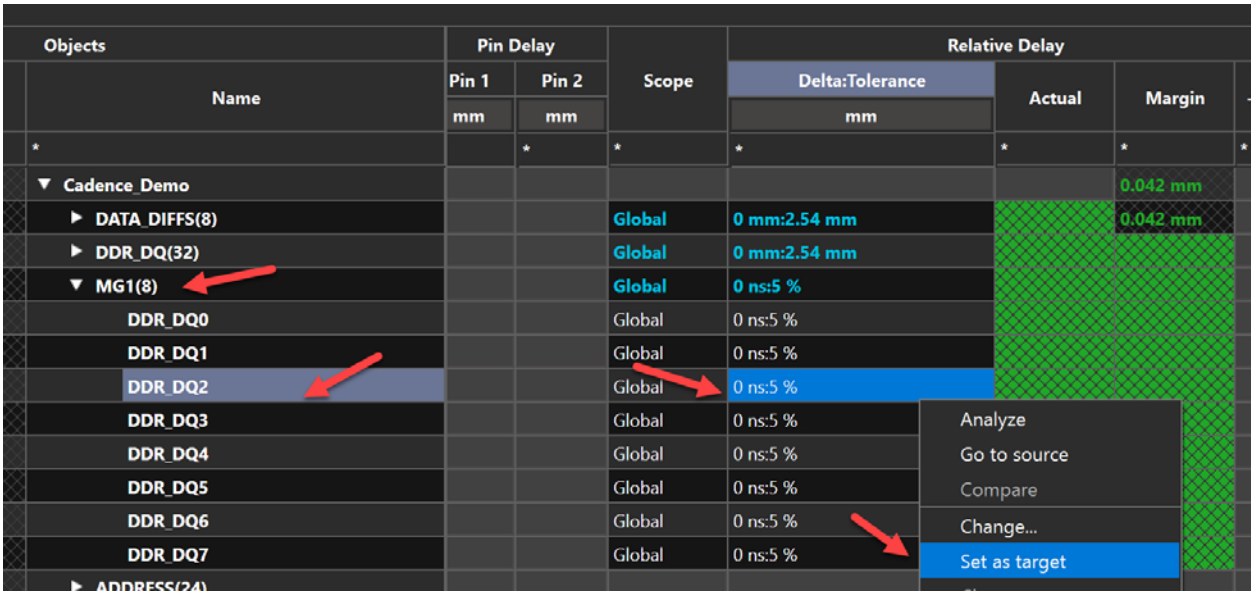
That means any trace in that Match Group DDR_DQ0 - DDR_DQ7 must also be 1600 mils (40.64 mm) with some tolerance (but not too much). So the longer we make the longest trace, the longer we must make the other traces to match it. Otherwise, the signals would have skew.

Match by Longest Driver/Receiver

This is similar to matching by longest pin pair, but the pins just need to be a driver from an IC and a receiver from an IC.

Match Length to All Driver/All Receivers

This applies the rules to all traces at the same time, but you must specify a target net for the other nets to try and match their lengths with. To do that, go back to the Constraint Manager. Go to the **Electrical > Net > Routing > Relative Propagation Delay** worksheet. Then right click the **Delta:Tolerance** column for one of the nets (e.g. for DDR_DQ2). Then choose **Set as Target**.



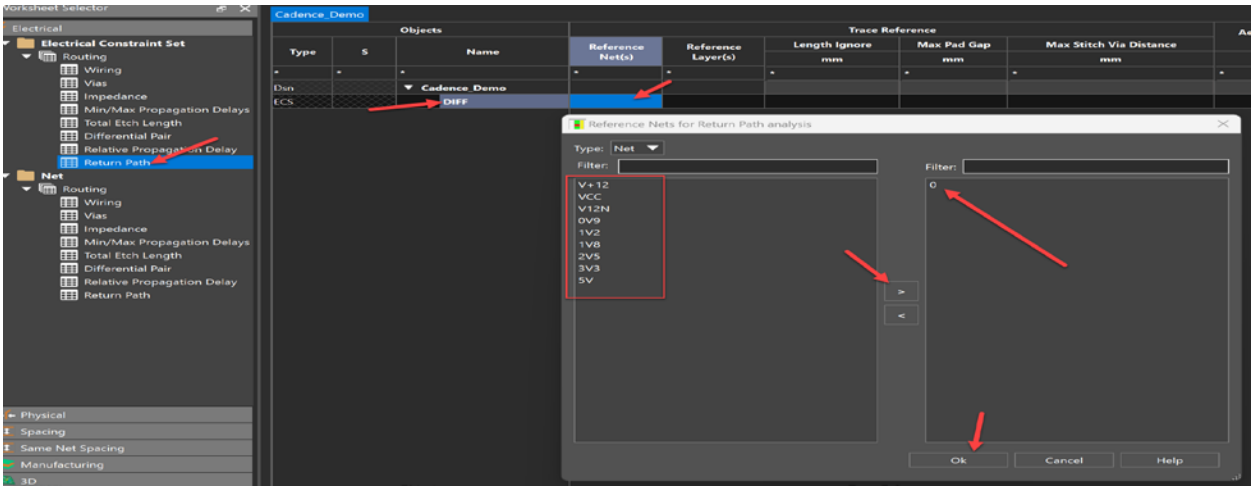
The Constraint Manager will want all other nets within that match group to be within a certain difference (we call it **Delta: Tolerance**) in length from that target net's length. Meaning that if DDR_DQ2 were suddenly 70 mils long, then all other traces from DDR_DQ0 and DDR_DDR3 to DDR_DQ7 must be 70 mils (1.778 mm) long within a 0 mm difference, and a tolerance of arriving 5% within that length is acceptable for skew for our application.

Important Note: Please note that all values are unique to each specific use case.

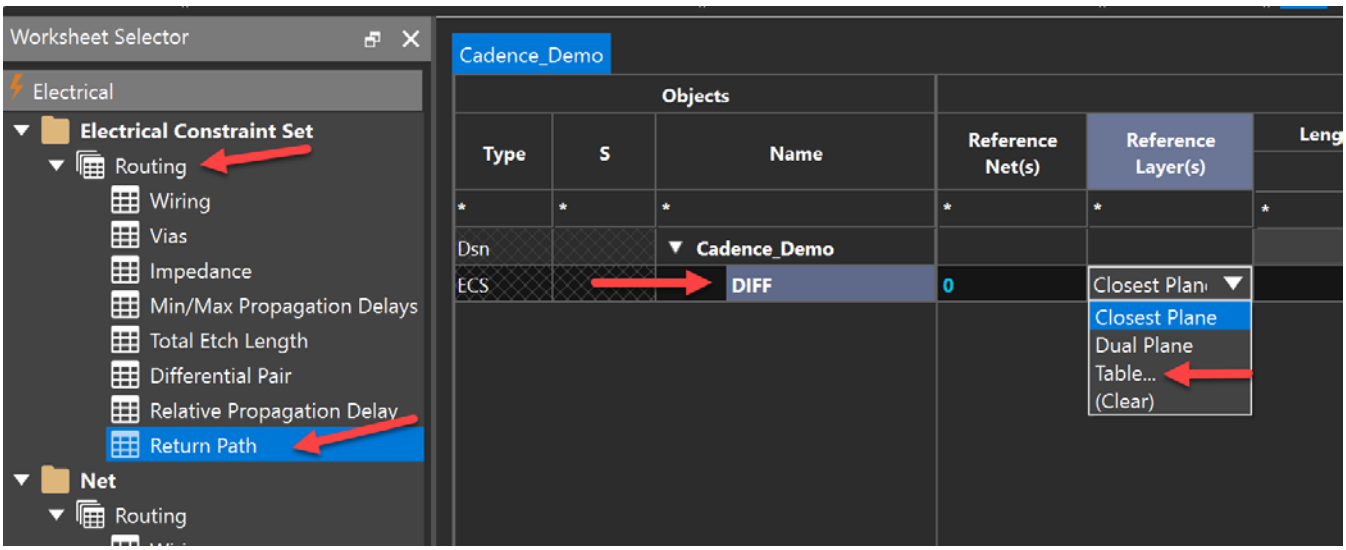
Return path management

Define allowed return paths underneath signal traces to maintain signal integrity and minimize EMI. A continuous, low-impedance return path is crucial for high-frequency signals. Consider using solid ground planes and avoiding splits or gaps in the return path.

For our application, we set the Reference Net to 0, which is our 'Ground' reference (we set layer 2 off as the ground plane).



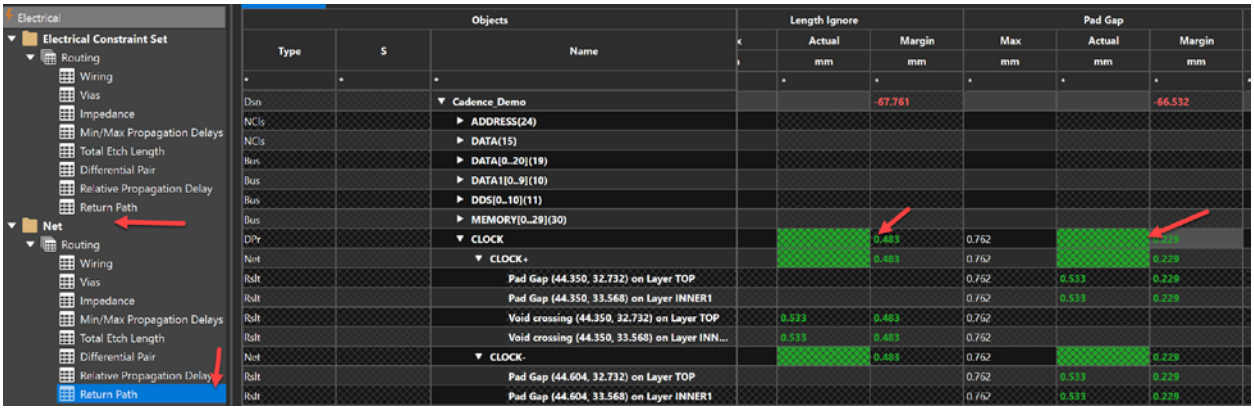
We then set Reference Layer(s) to the plane that aligns with the behavior of the signals and/or routing of said signals. To keep things simple we select Closest Plane. Just note that if you route your traces on say, the bottom layer (layer 6), and the closest plane happens to be layer 5 of 6, then your signal return path may flow along layer 5 instead of layer 2 (the layer that holds the net 0 that we used as the reference net in the previous cell). With that likely being a voltage difference from the 0 net ground plane, then noise and unwanted EMI may occur. If that is not acceptable, consider using the **Table…** option from the dropdown menu shown below to choose specific planes.



We went with **Closest Plane** for this example. In the remaining cells that go to the right, you can specify the amount of acceptable gaps in the return path, the length of copper to ignore, adjacent void spacings and so on. Managing the return path for signals is just as important as managing the signal routes themselves for impedance control, signal integrity (to reduce impedance discontinuity, and therefore discourage signal reflections) and electromagnetic compatibility. Max Pad Gap set to 30 mils (0.762 mm) and the Length Ignore set to 40 mils (1.016 mm).

Objects			Trace Reference	
Name	Reference Net(s)	Reference Layer(s)	Length Ignore mm	Max Pad Gap mm
*	*	*	*	*
▼ Cadence_Demo				
DIFF	0	Closest Plane	1.016	0.762

As usual, any values entered are immediately applied to the nets that use this Electrical Constraint Set as seen below. Looks like the design is constrained nicely!



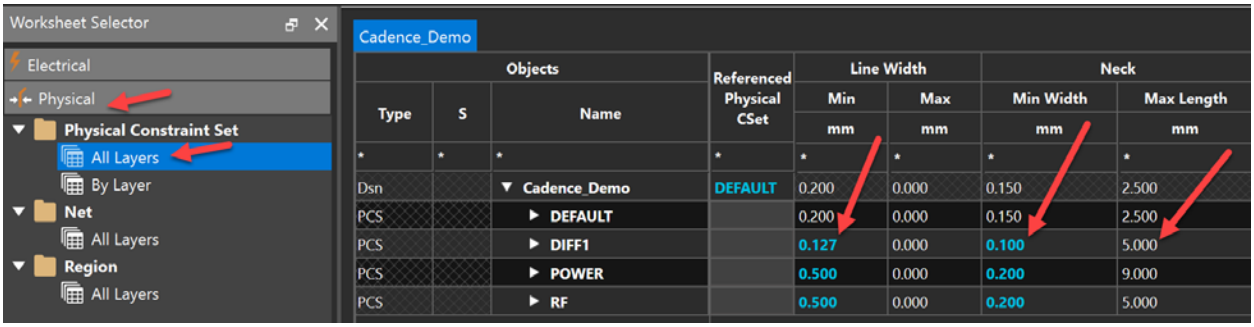
We are at the end of the Electrical Constraints examples that you will need for most high-speed digital designs. Let us continue with Physical Constraints, especially for differential pairs.

Advanced Physical Constraints

In this section we address the physical constraints in an example physical constraint set that you need to apply for practical high-speed or complex designs. It is understood that you already know how to create constraint sets and apply them to net classes, groups and regions. So, we will only show the constraint set, then where they got applied while giving some context to their importance.

Trace Width

For physical constraints we already set the Line Width (trace width), the minimum width (narrows down to 0.100 mm = 3.93 mils) and maximum length we allow a neck to run (about 5 mm = 196 mils, but no longer).



Differential Pair Advanced Physical Constraints

The Differential Pair values are set as shown below.

Cadence_Demo

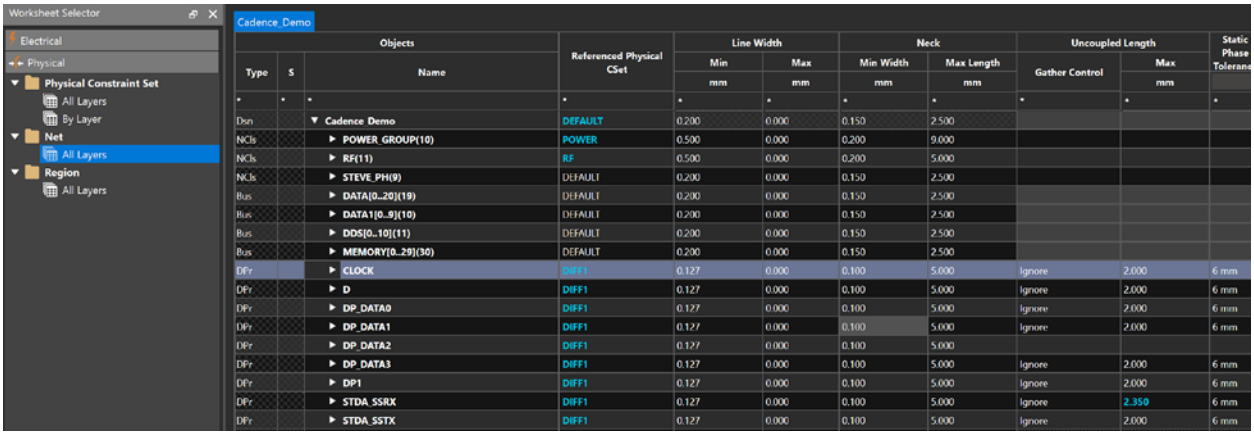
Objects			Differential Pair				
Type	S	Name	Min Line Spacing	Primary Gap	Neck Gap	(+)Tolerance	(-)Tolerance
			mm	mm	mm	mm	mm
*	*	*	*	*	*	*	*
Dsn		▼ Cadence_Demo	0.000	0.000	0.000	0.000	0.000
PCS		▶ DEFAULT	0.000	0.000	0.000	0.000	0.000
PCS		▶ DIFF1	0.107	0.127	0.117	0.010	0.010
PCS		▶ POWER	0.000	0.000	0.000	0.000	0.000
PCS		▶ RF	0.000	0.000	0.000	0.000	0.000

Then finally we have Vias set for all the Physical Constraint Sets as well.

Cadence_Demo

Objects			Vias	BB Via Stagger		Allow		
Type	S	Name		Min	Max	Pad-Pad Connect	Etch	Ts
				mm	mm			
*	*	*	*	*	*	*	*	*
Dsn		▼ Cadence_Demo	VIA	0.127	0.000	ALL_ALLOWED	TRUE	ANYWHERE
PCS		▶ DEFAULT	VIA	0.127	0.000	ALL_ALLOWED	TRUE	ANYWHERE
PCS		▶ DIFF1	VIA	0.127	0.000	ALL_ALLOWED	TRUE	ANYWHERE
PCS		▶ POWER	VIA	0.127	0.000	ALL_ALLOWED	TRUE	ANYWHERE
PCS		▶ RF	VIA	0.127	0.000	ALL_ALLOWED	TRUE	ANYWHERE

Notice how all the rules within the constraint sets are applied accordingly (seen below).

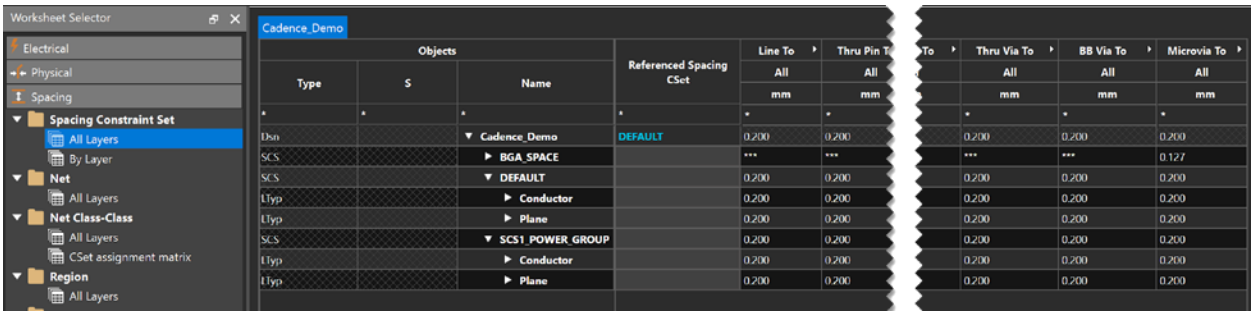


Objects			Referenced Physical CSet	Line Width		Neck		Uncoupled Length		Static Phase Tolerance
Type	S	Name		Min	Max	Min Width	Max Length	Gather Control	Max	
				mm	mm	mm	mm		mm	
*	*	*	*	*	*	*	*	*	*	*
Dsn		▼ Cadence_Demo	DEFAULT	0.200	0.000	0.150	2.500			
NCls		▶ POWER_GROUP(10)	POWER	0.500	0.000	0.200	9.000			
NCls		▶ RF(11)	RF	0.500	0.000	0.200	5.000			
NCls		▶ STEVE_PH(9)	DEFAULT	0.200	0.000	0.150	2.500			
Bus		▶ DATA[0..20](19)	DEFAULT	0.200	0.000	0.150	2.500			
Bus		▶ DATA1[0..9](10)	DEFAULT	0.200	0.000	0.150	2.500			
Bus		▶ DDS[0..10](11)	DEFAULT	0.200	0.000	0.150	2.500			
Bus		▶ MEMORY[0..29](30)	DEFAULT	0.200	0.000	0.150	2.500			
DPr		▶ CLOCK	DIFF1	0.127	0.000	0.100	5.000	Ignore	2.000	6 mm
DPr		▶ D	DIFF1	0.127	0.000	0.100	5.000	Ignore	2.000	6 mm
DPr		▶ DP_DATA0	DIFF1	0.127	0.000	0.100	5.000	Ignore	2.000	6 mm
DPr		▶ DP_DATA1	DIFF1	0.127	0.000	0.100	5.000	Ignore	2.000	6 mm
DPr		▶ DP_DATA2	DIFF1	0.127	0.000	0.100	5.000			
DPr		▶ DP_DATA3	DIFF1	0.127	0.000	0.100	5.000	Ignore	2.000	6 mm
DPr		▶ DP1	DIFF1	0.127	0.000	0.100	5.000	Ignore	2.000	6 mm
DPr		▶ STDA_SSRX	DIFF1	0.127	0.000	0.100	5.000	Ignore	2.350	6 mm
DPr		▶ STDA_SSTX	DIFF1	0.127	0.000	0.100	5.000	Ignore	2.000	6 mm

Setting the physical and electrical rules for your differential pairs almost completes differential pairs for your designs. You need to assign spacing constraints to your differential pairs for them to be considered fully 'ready' for high-speed/complex layouts. We will cover the spacing constraints and space-to-space class constraints required for differential pairs.

Advanced Spacing Constraints

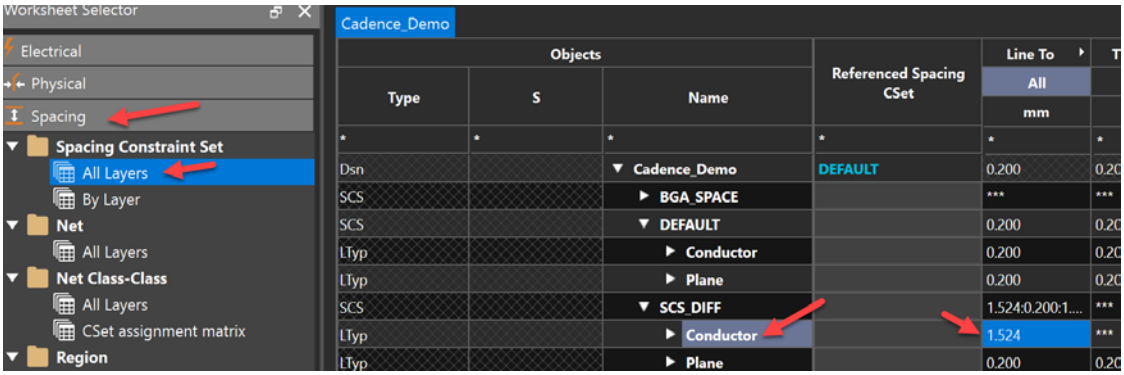
Notice we have standard spacing constraints applied like you would for any standard design, high-speed or not.



Those rules will be applied immediately to any nets using the Constraint Set.

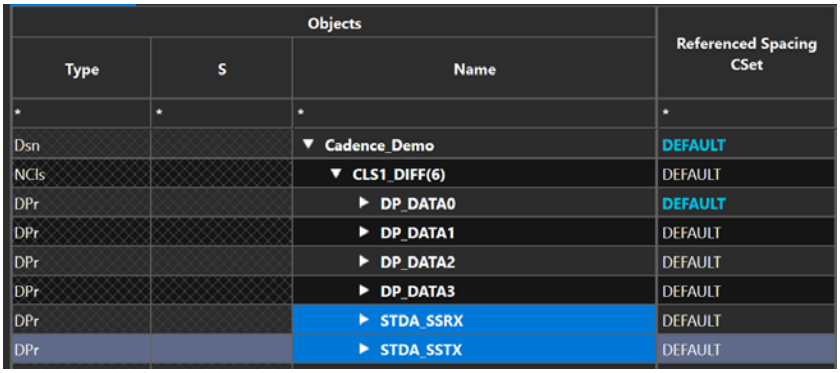
Of keen interest is how to set up spacing for differential pairs. Let's say we want the differential pair traces to be 60 mils (1.524 mm) away from all other objects (except between their own single-ended traces within the diff pairs of course).

In this case, we create a Spacing Constraint Set named SCS_DIFF (shown below) and set its **Line To** value to 60 mils (1.524 mm). You can double-click the Line To column to see what all objects we are requiring the differential pairs to be at least 60 mils away from, in case you need to do some fine-tuning there.

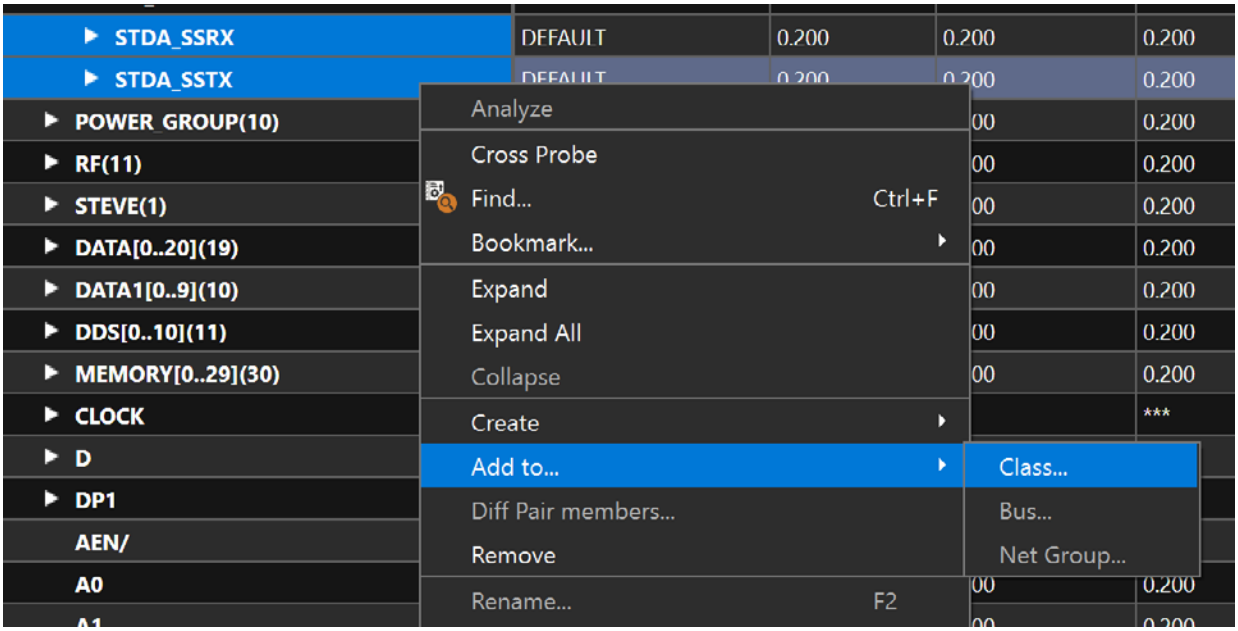


But what about differential pair to differential pair spacing? In our design, we don't need diff pairs (like TX and RX) to be more than 20 mils apart. So we need to tell the Constraint Manager that the SCS_DIFF class members only need to be 20 mils apart from other SCS_DIFF class members. That will require a Net Class-to-Class spacing.

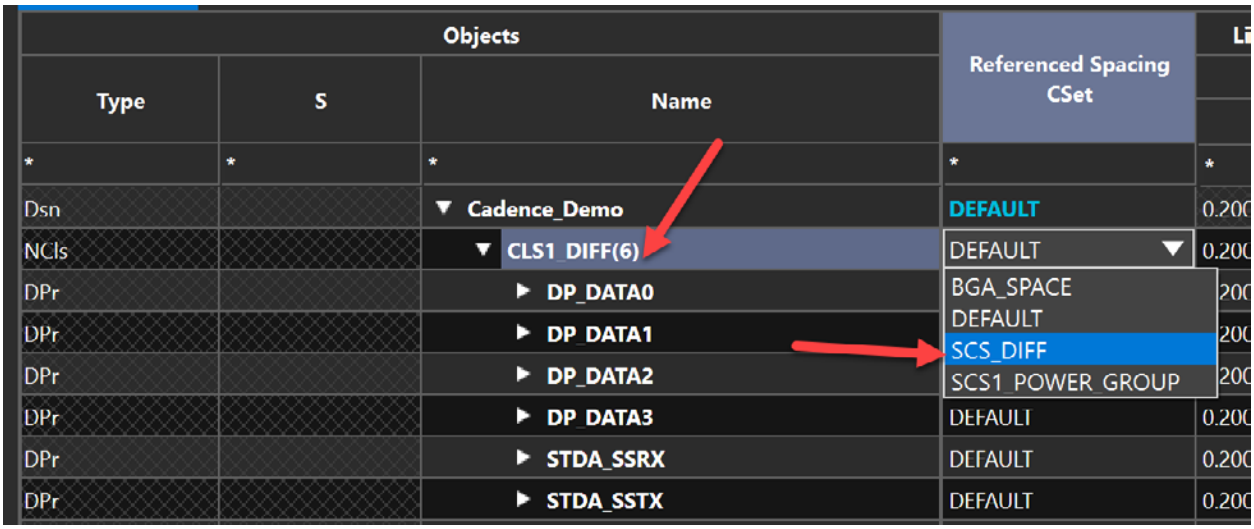
Before Creating a Class-to-Class spacing, we must ensure that we have Net Classes applied where appropriate. Navigate to the **Net > All Layers** worksheet, then highlight all the nets you want inside a differential pair net class that we will call CLS1_DIFF (shown below).



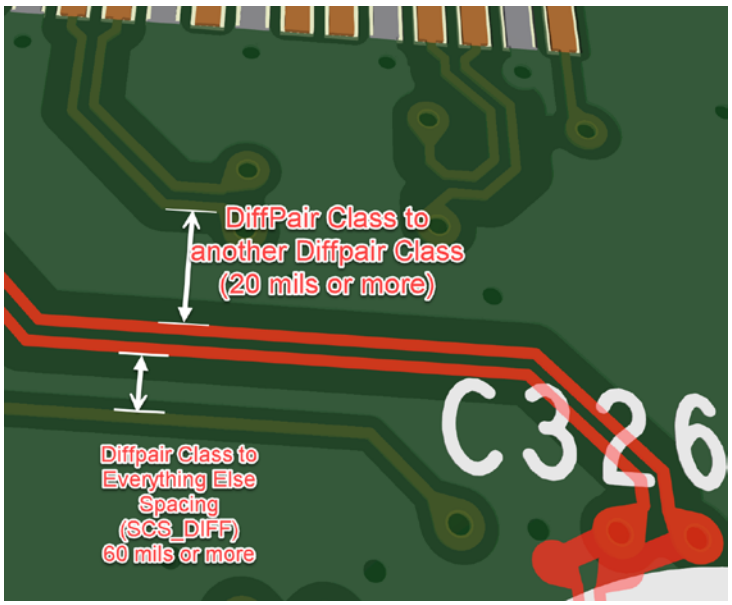
If you forget any nets, you can CTRL select those as well, then right click and choose **Add To** – **Class** to add them to the CLS1_DIFF net class.



Now, currently the members of that Net class have default spacing to other nets. We need to change that to the spacing constraint set we created instead SCS_DIFF.



However, that will only cause the members of that Net Class to be distanced 60 mils away from other nets outside of the class of differential pairs. While that's desirable, we want the differential pairs to only need to be 20 mils apart or more amongst themselves.

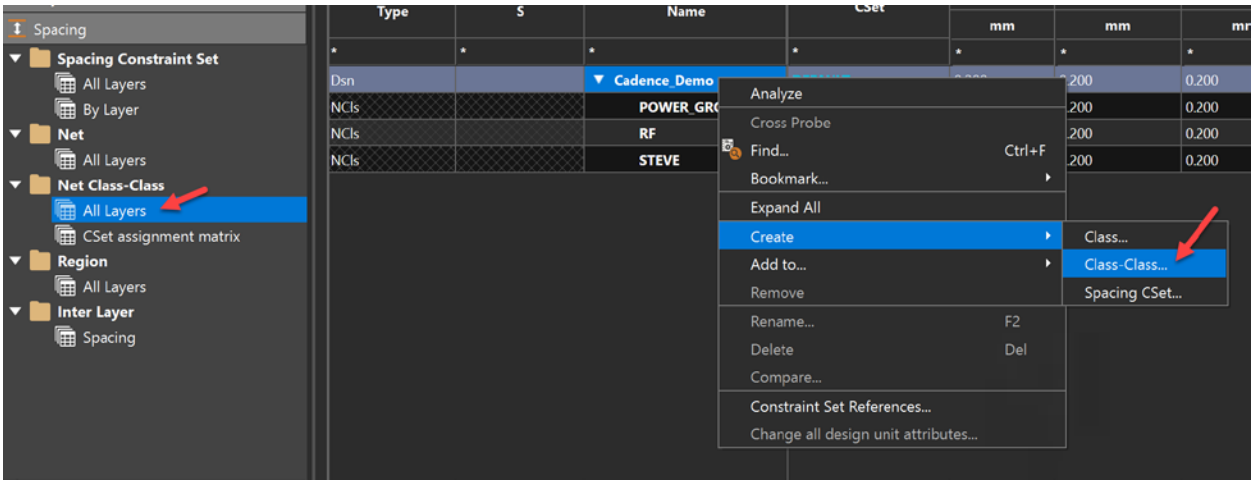


Otherwise, if differential pairs had to be 60 mils away from other diff pairs, it would be near impossible to route differential pairs on a dense PCB. They would be forced to stay 60 mils away from each other, which is not necessary in many cases.

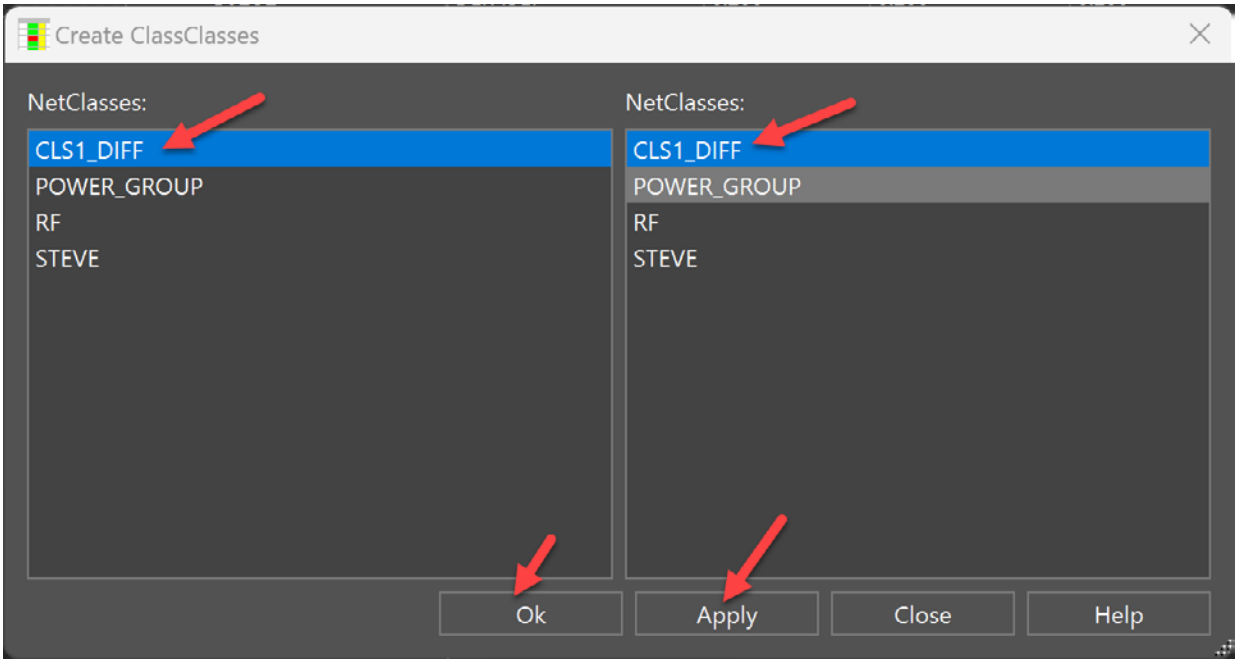
Class-to-Class Spacing for Differential Pairs to Differential Pairs Spacing

So, for this reason, Class-to-Class spacing is introduced, so that any **CLS1_DIFF** class object can be 20 mils from any other **CLS1_DIFF** class object (one differential pair to another).

To implement said class-to-class spacing, click the **Net Class-Class > All Layers** worksheet. Right-click the Cadence_Demo design, choose **Create** – **Class-Class**.

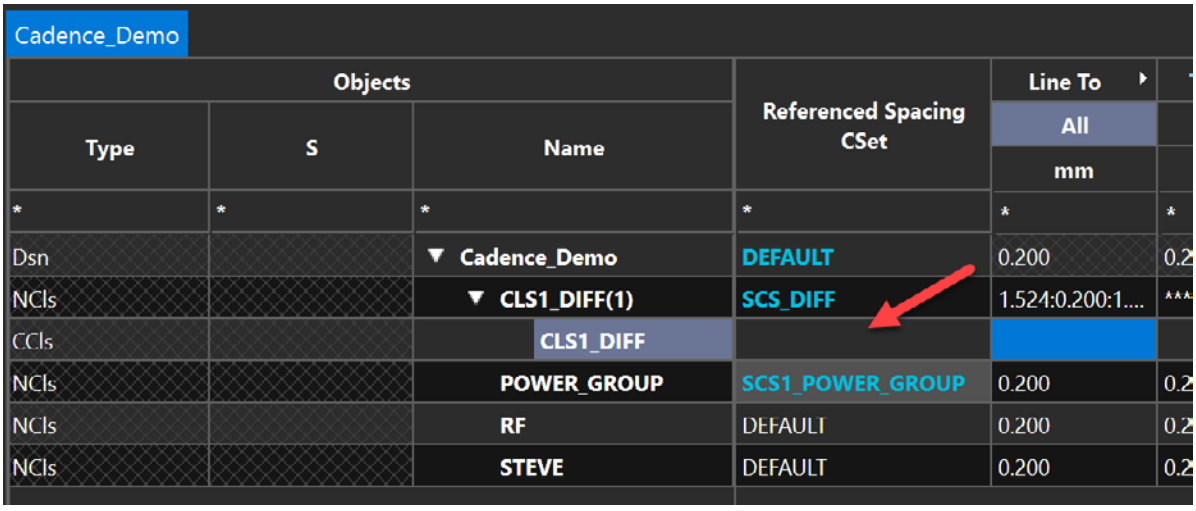


In this new window, we want the net class on the left to be spaced a certain distance from the net class on the right (CLS1_DIFF to itself, basically). Select those classes (CLS1_DIFF on the left and CLS1_DIFF on the right as shown), then click Apply, then Ok.



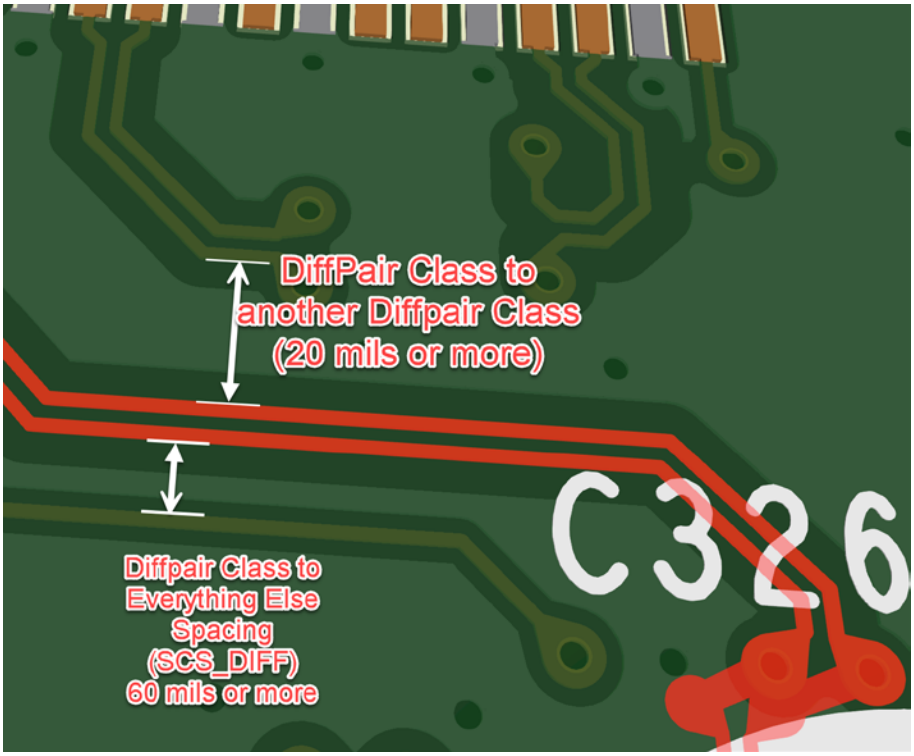
A new row will appear on the worksheet as a CCls object underneath a NCls object…i.e. the CLS1_DIFF Net class nested under itself as a class-to-class spacing row.

It means that any Net Class underneath that class is what the upper-level class is being spaced against (**CLS1_DIFF** to **CLS1_DIFF** spacing). Even if the class is itself like we demonstrate here, that's okay to do.

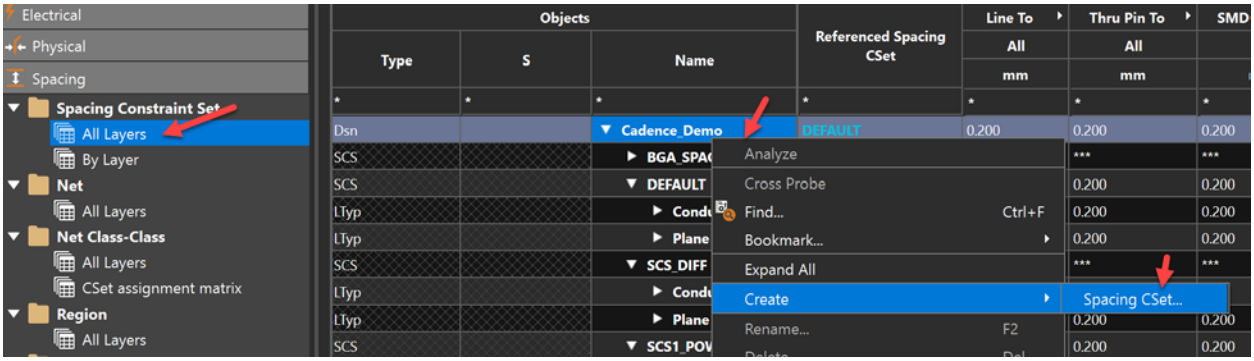


Notice that there is no value set for this Class to Class spacing. We can type in the values manually, but as usual, it is better to set a Constraint Set specifically for the spacing we want first, then apply that constraint where appropriate.

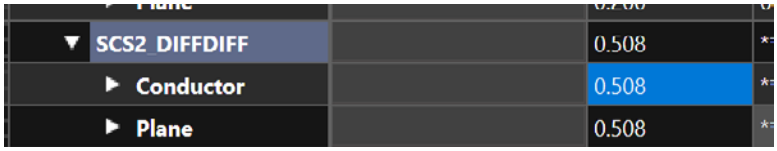
So, between this **CLS1_DIFF** Class and itself, we will make the trace to others spacing equal 20 mils as a minimum, as opposed to 60 mils (basically differential pair members of this class will be 20 mils from trace edge to trace edge to other differential pair members of the same Class).



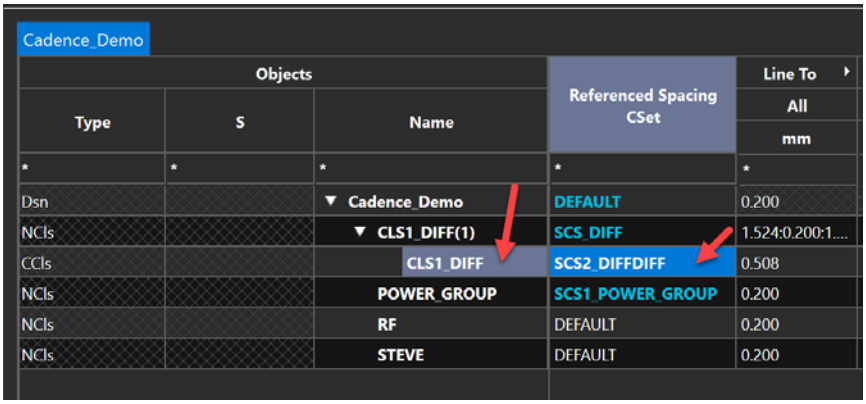
To make that 20-mil (0.508 mm) spacing, go to the **Spacing Constraint Set** – **All Layers** worksheet, right click the **Cadence_Demo** cell, then choose **Create – Spacing CSet…**



We name ours SCS2_DIFFDIFF, then click Ok, and it gets added to the list. Afterwhich, we set the Line To spacing column cell value to 20 mils (0.508 mm).



We can now use this Spacing Constraint Set to apply it to our Net Class-to-Class spacing, CLS1_DIFF to CLS1_DIFF. Navigate back to the **Net Class-Class > All Layers** worksheet. Then choose our newly created **SCS2_DIFFDIFF** constraint set and apply it as shown below.

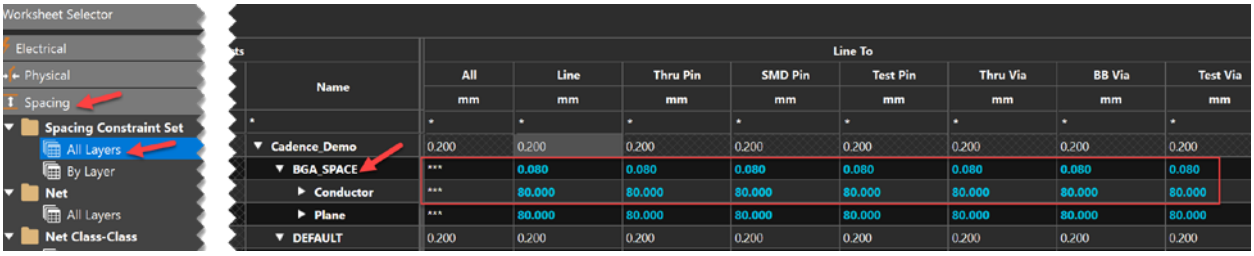


Now our differential pairs can get as close as 20 mils to other differential pairs within the same class (ruled by **SCS2_DIFFDIFF**), while all other objects that are not within that differential pair Net Class will have to be at least 60 mils away from any differential pair (ruled by **SCS_DIFF**).

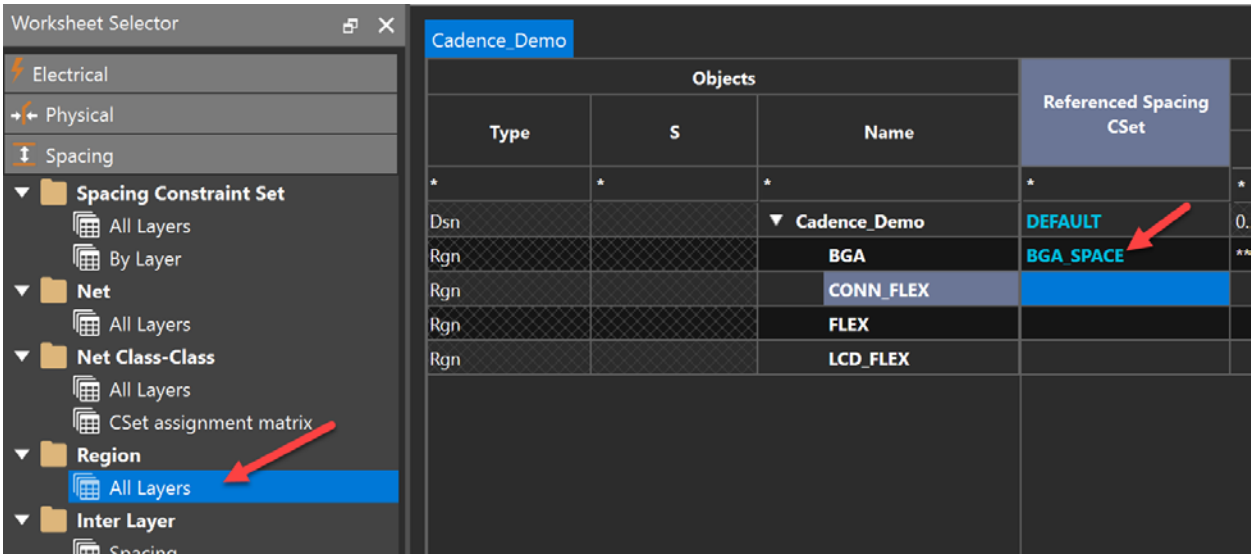
Then of course if we need to tighten or loosen the constraint (say 10 mil spacing instead of 20, we can do that in one location instead of many).

Constraint Region

For our constraint region, we created a BGA_SPACE spacing constraint for BGA areas.



Then we applied that constraint to the BGA region.

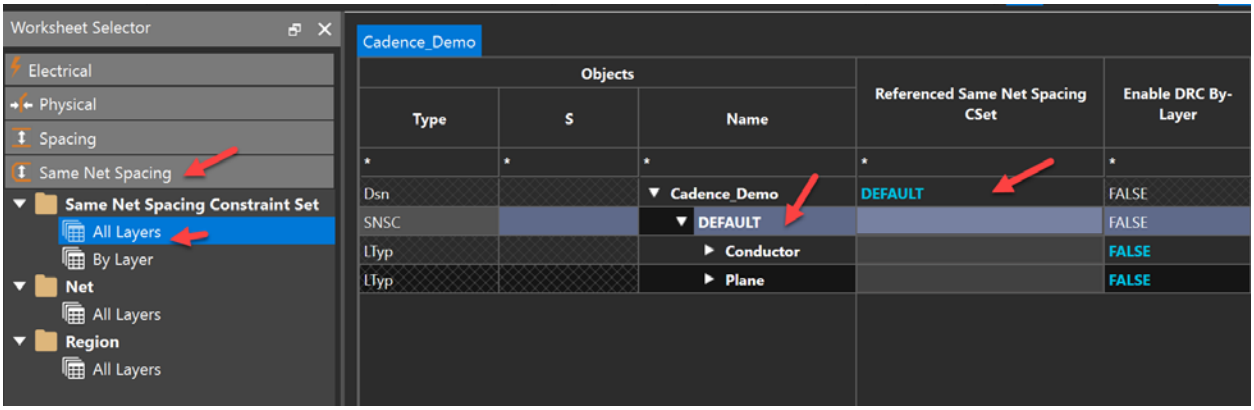


Now any objects within the BGA regions on the board will have their own specific spacing and physical rules. The Constraint Manager will adjust trace widths, spacing, etc. automatically while you are routing.

Advanced Same Net Spacing Constraints

In most cases you can leave Same Net Spacing Constraints alone. There are special cases where you might need to delve in here, though. In particular when you have shorts between planes and traces, or your thermal reliefs are giving you issues.

We will leave these constraints as is.



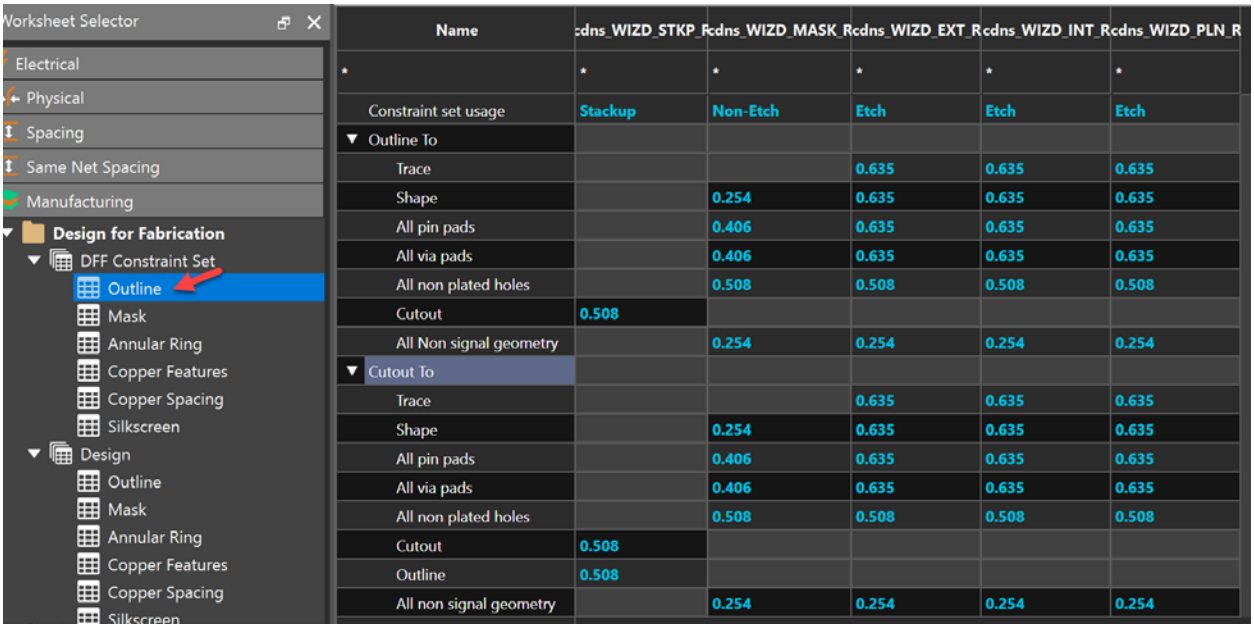
Advanced Manufacturing Constraints

Manufacturing Constraints have been applied in the following categories and as shown in the images below.

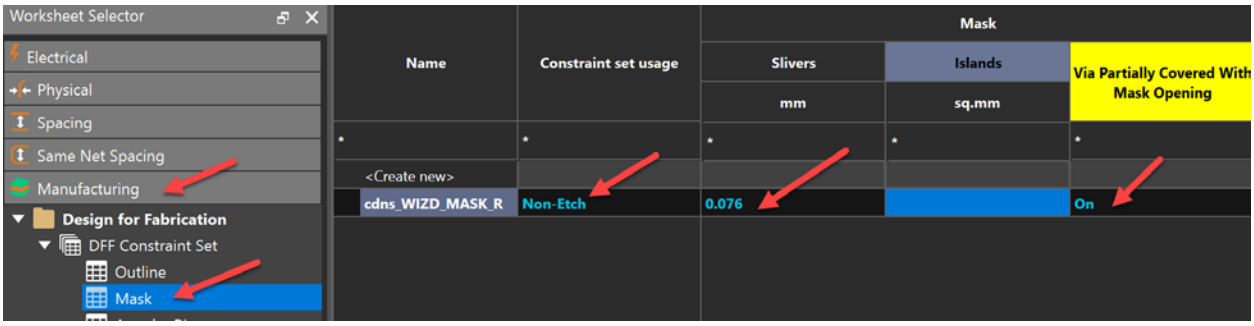
Design for Fabrication Constraints

Fabrication constraints have to do strictly with the printed circuit board features, not component arrangement. We address the constraints we set up in our design accordingly.

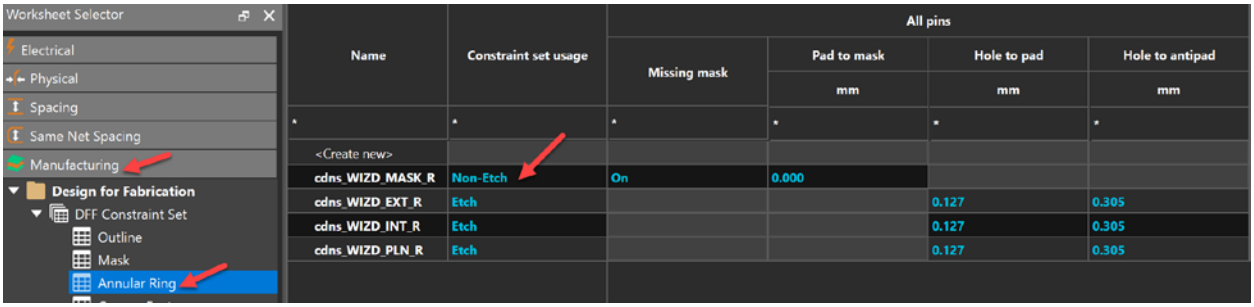
Outline

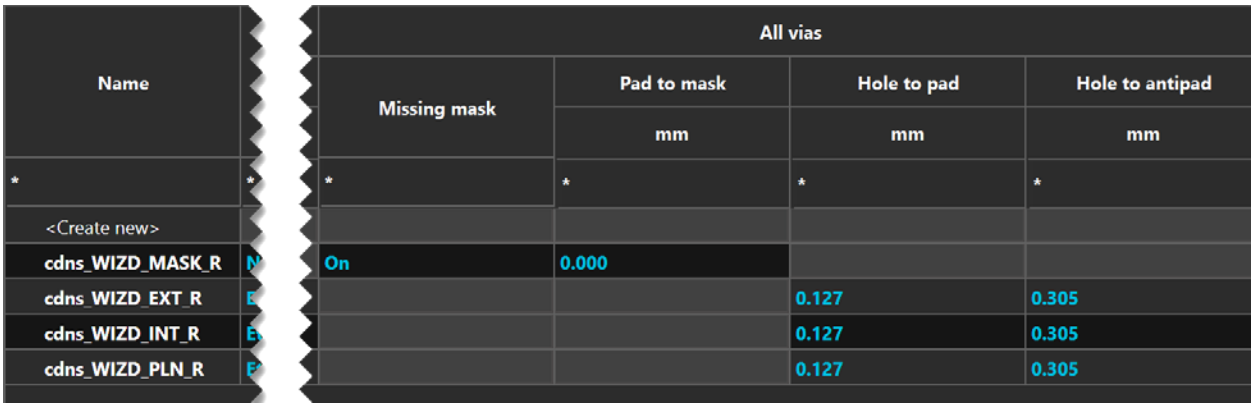


Mask



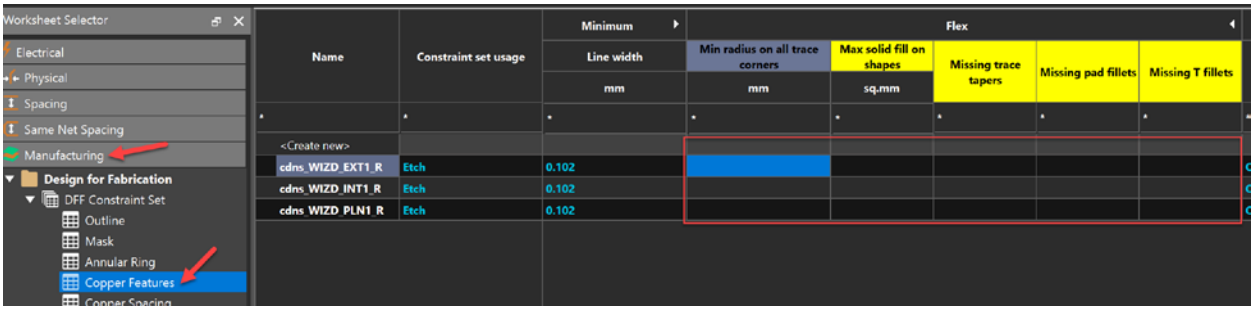
Annular Ring

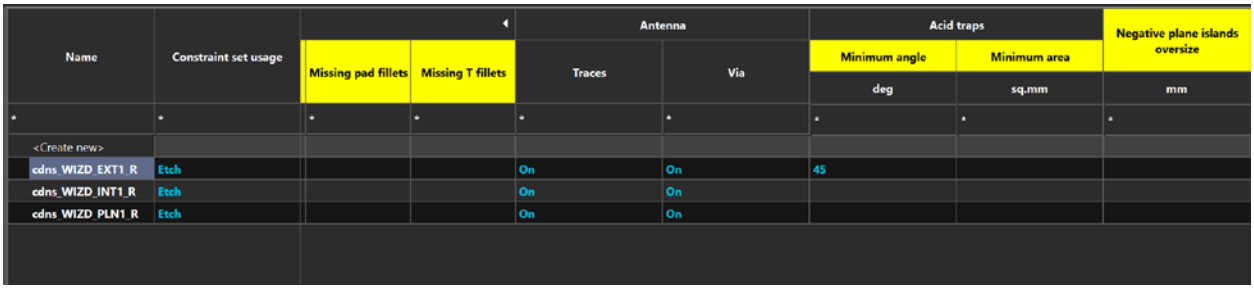




Copper Features

This section has a lot of the interesting constraints that engineers can require for their practical designs on the job, such as Flex, Acid Traps (for manufacturers still using acid bath technology) and Negative plane islands oversize.



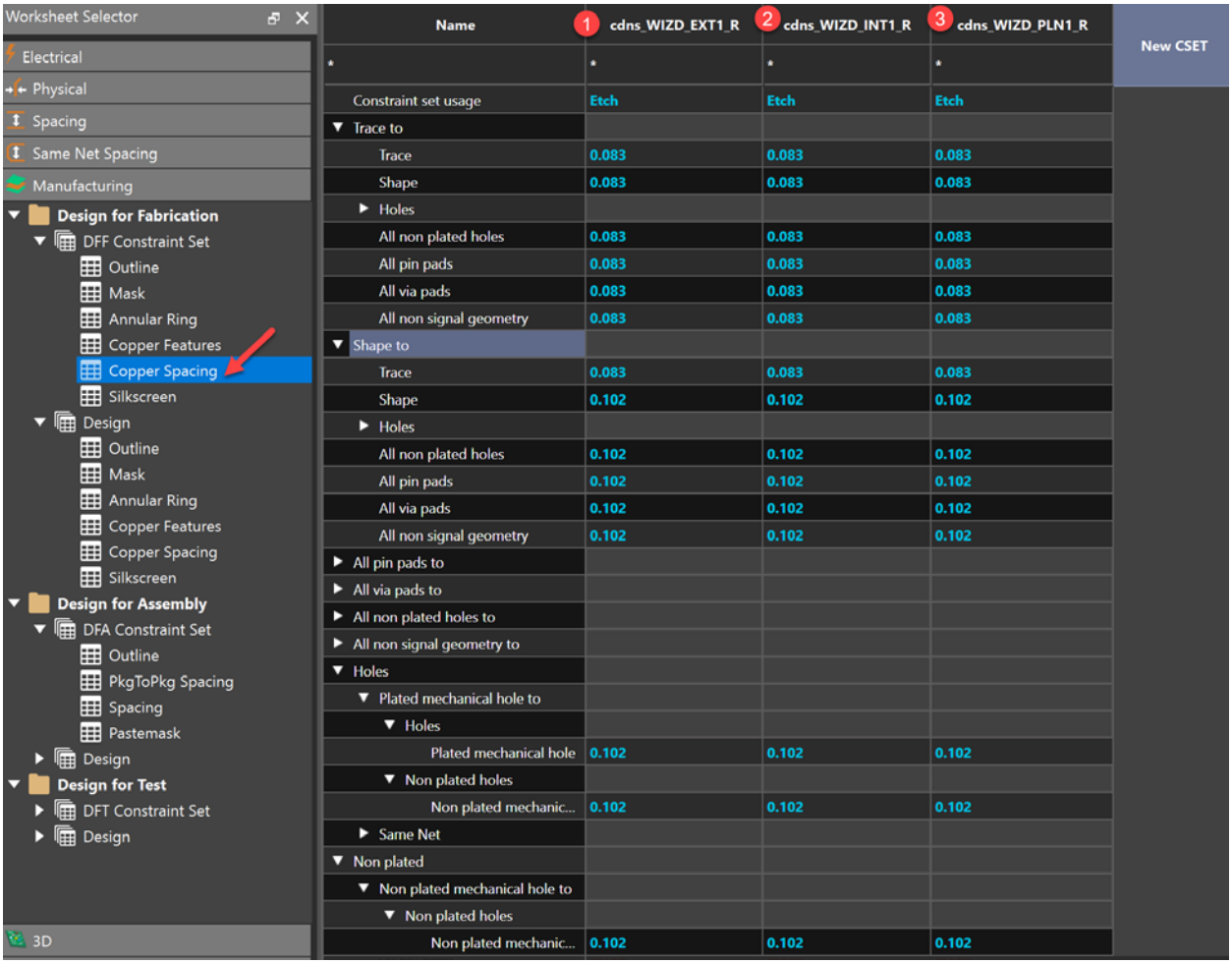


Name	Constraint set usage			Antenna		Acid traps		Negative plane islands oversize
		Missing pad fillets	Missing T fillets	Traces	Via	Minimum angle	Minimum area	
						deg	sq.mm	mm
*	*	*	*	*	*	*	*	*
<Create new>								
cdns_WIZD_EXT1_R	Etch			On	On	45		
cdns_WIZD_INT1_R	Etch			On	On			
cdns_WIZD_PLN1_R	Etch			On	On			

For Flex PCB Design parameters, it varies greatly depending on the manufacturer. Ask your manufacturer for assistance on the values needed for your Constraint Management tool.

Copper Spacing

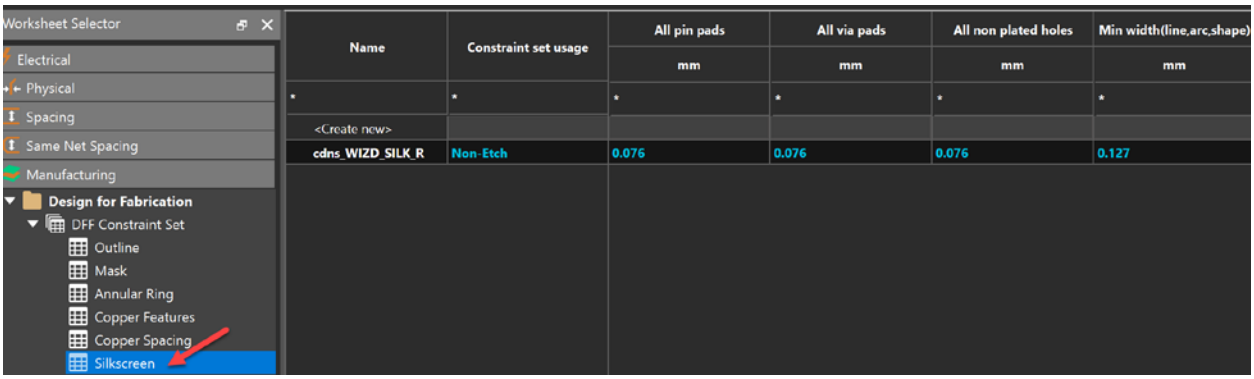
We have many manufacturing rules for copper spacing. Those rules vary from External to Internal layers and also planes. See the constraints applied below for an understanding of this idea.



Even down to the plated and non-plated holes we have set the object to object spacing in acute detail.

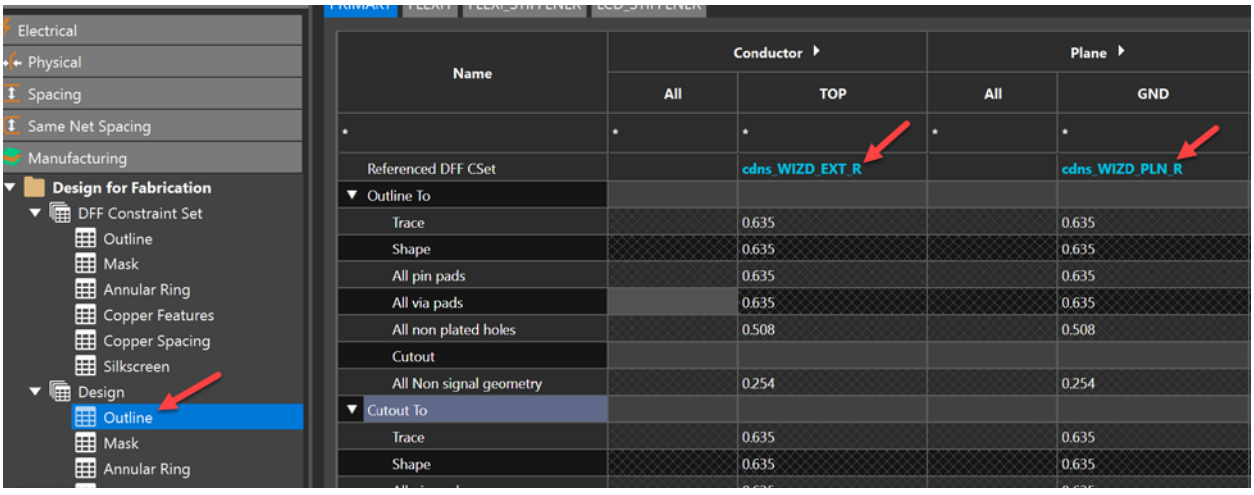
Silkscreen

Silkscreen has its own set of rules that the manufacturer needs to adhere to so that they can reliably manufacture your PCB at yield and at reasonable cost. We set the values below based on our manufacturer's capabilities and requirements (seen below).

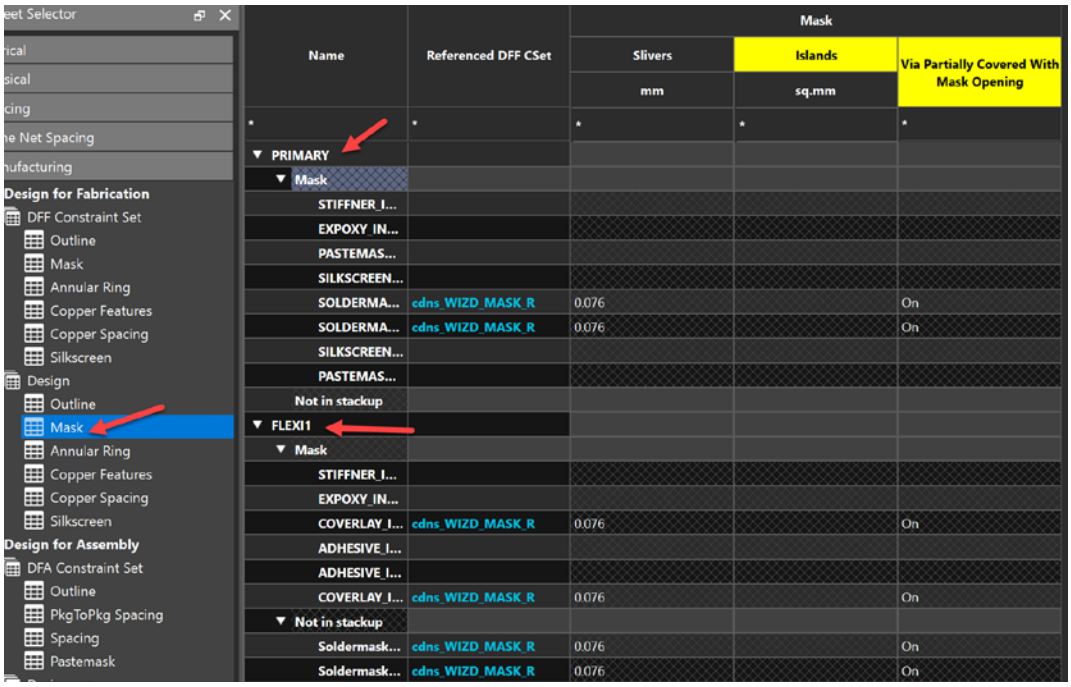


As usual for most PCBs we want to make sure there is no overlapping silkscreen text and none underneath our components, so we set those checks to On.

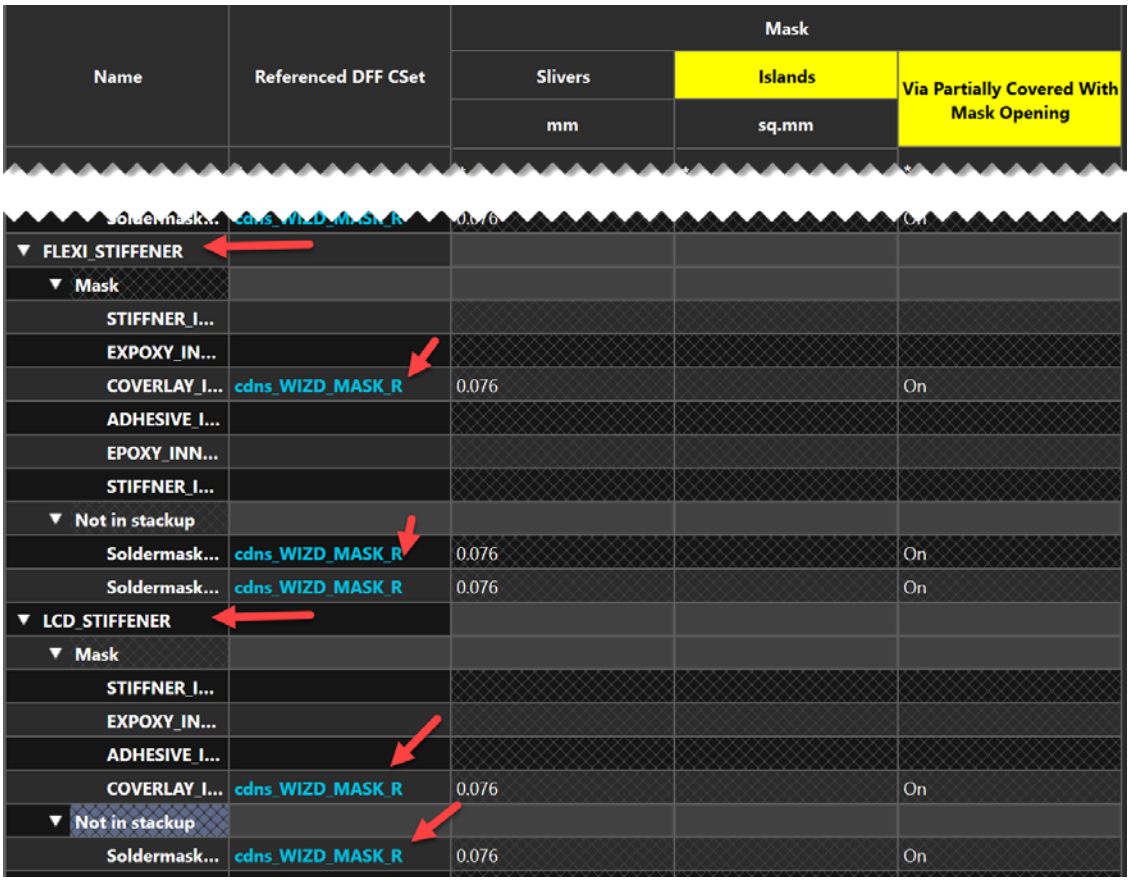
Our fabrication constraints are set to our manufacturer capabilities, now that the fabrication of the PCB is likely to have reasonable first-pass success. Be sure to apply the constraints in the Design section and its subsequent worksheets and objects.



Notice how we can use different constraint sets for different areas and stackups of the PCB as well. We have some flex regions on the board, so we would have custom values for our various regions. See the image below for an example.



Likewise for Flex Stiffener and LCD Stiffener areas.

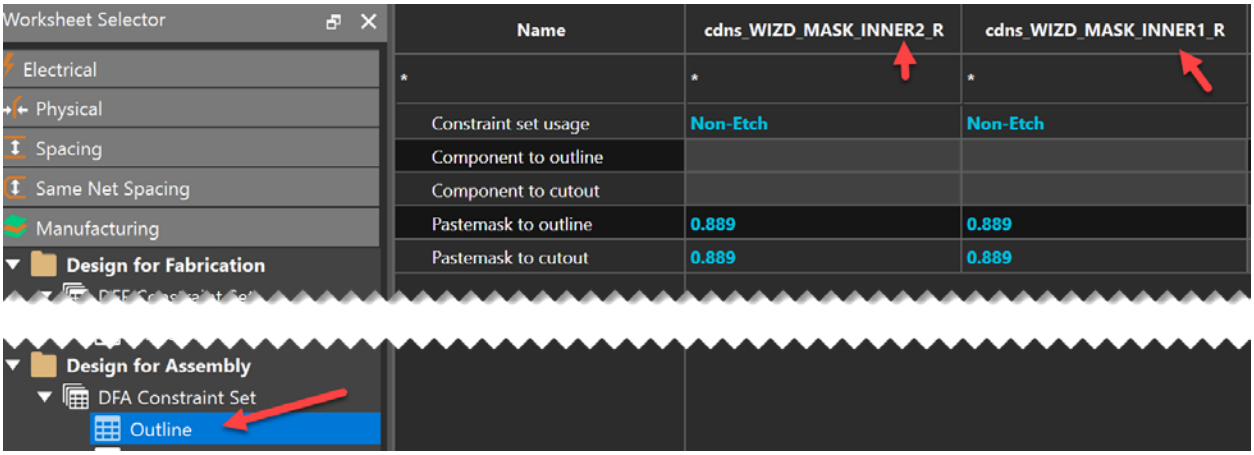


Next are the components, which fall under assembly.

Design for Assembly Constraints

Outline

Components need to have sufficient spacing from the outline of the board.



Name	cdns_WIZD_Etch_INNER2_R	cdns_WIZD_Etch_INNER1_R	cdns_WIZD_MASK_BOTTOM_R
*	*	*	*
Constraint set usage	Etch	Etch	Non-Etch
Component to outline	1.270	1.270	
Component to cutout	1.270	1.270	
Pastemask to outline			0.889
Pastemask to cutout			0.889

Name	cdns_WIZD_MASK_TOP_R	cdns_WIZD_Etch_BOTTOM_R	cdns_WIZD_Etch_TOP_R	New CSET
*	*	*	*	
Constraint set usage	Non-Etch	Etch	Etch	
Component to outline		1.270	1.270	
Component to cutout		1.270	1.270	
Pastemask to outline	0.889			
Pastemask to cutout	0.889			

Then, if need be, as shown above, you can always click on the far right to create a new custom Constraint Set (New CSET) to add to the list of assembly constraints.

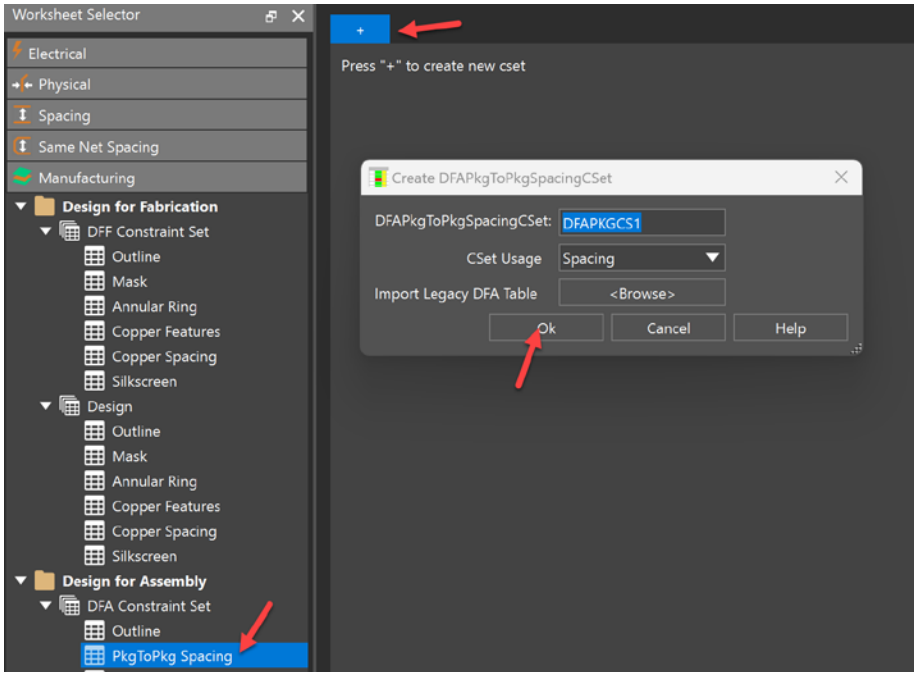
Package to Package Spacing

The IPC-2221 standard requires that components have a minimum spacing from the edge of a component to another component's edge or side, and the side of a component to another component's edge or side. This creates a matrix of spacing that can get complex rather quickly.

Steps to set up PkgToPkg Spacing:

To set that up, simply select the worksheet found at **Design for Assembly > PkgToPkg Spacing**.

Click the + symbol at the top to create a new CSET, then give it the default name, DFAPKGCS1, then click Ok.

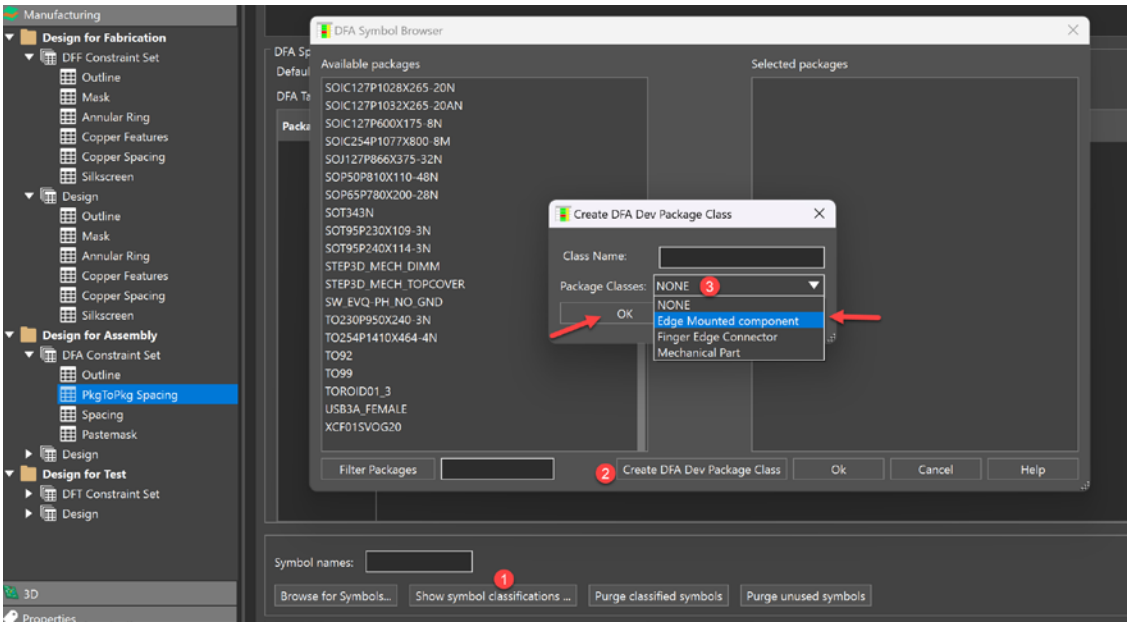


You are met with a blank window that uses the default 25 mil spacing for all edge to edge, edge to side, side to side and side to edge spacing values. However, depending on the component, you need certain spacing, so it is highly recommended to create symbol classifications, then have different symbols within those classifications (groups) so that each symbol can automatically have the right spacing applied to each type of symbol classification (e.g. all connectors, ICs, discretes, etc. having their own S:S, E:E, S:E, E:S spacing rules).

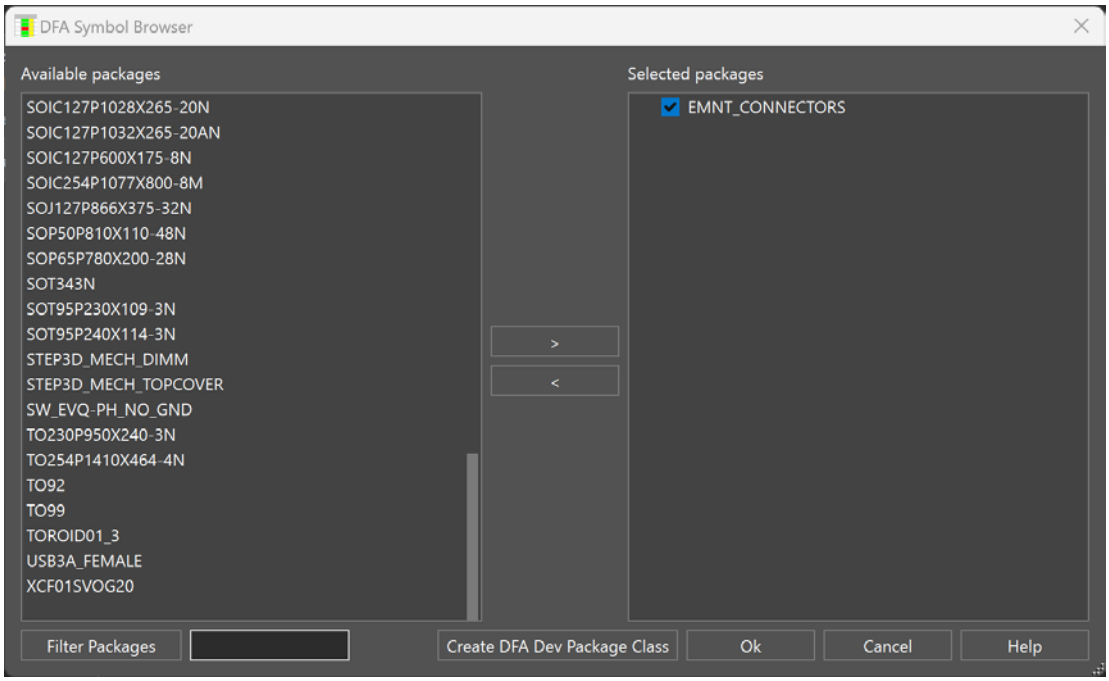
To keep things simple, assume all symbols have the same spacing rules. In that case, select **Show symbol classifications…**

In the DFA Symbol Browser window, select **Create DFA Dev Package Class**.

Then choose the Edge Mounted Component option for Package Classes.

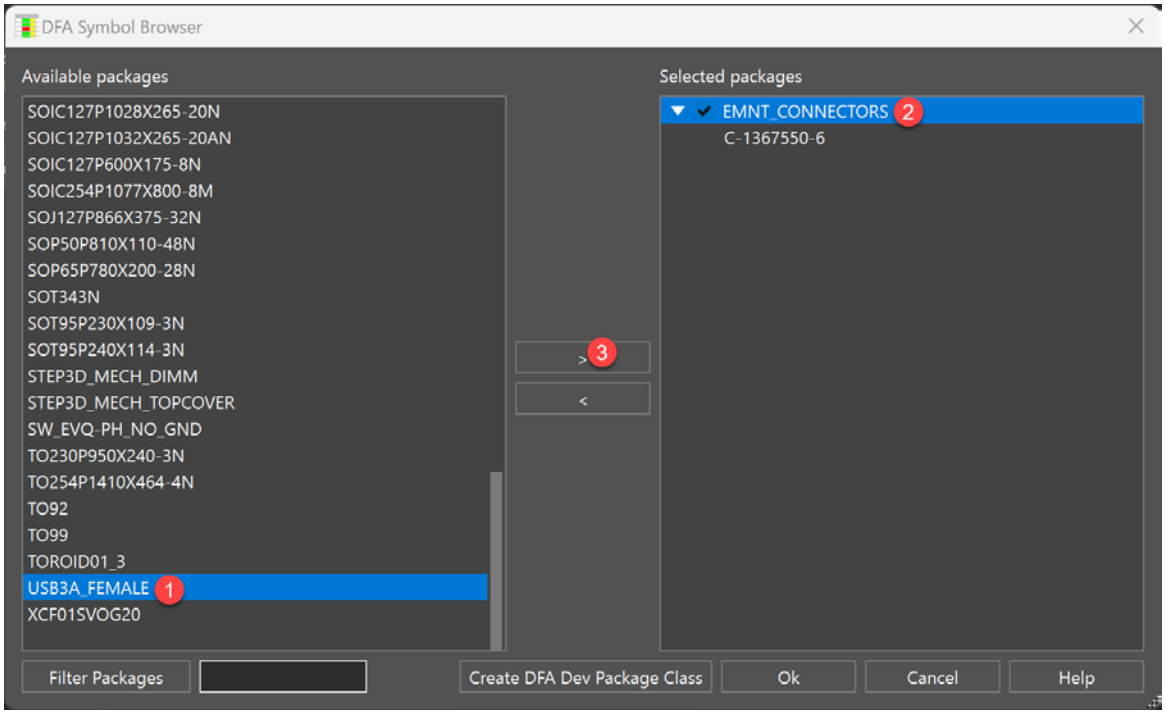


Name the class something like CONNECTORS for example, then click Ok. You get the window below.

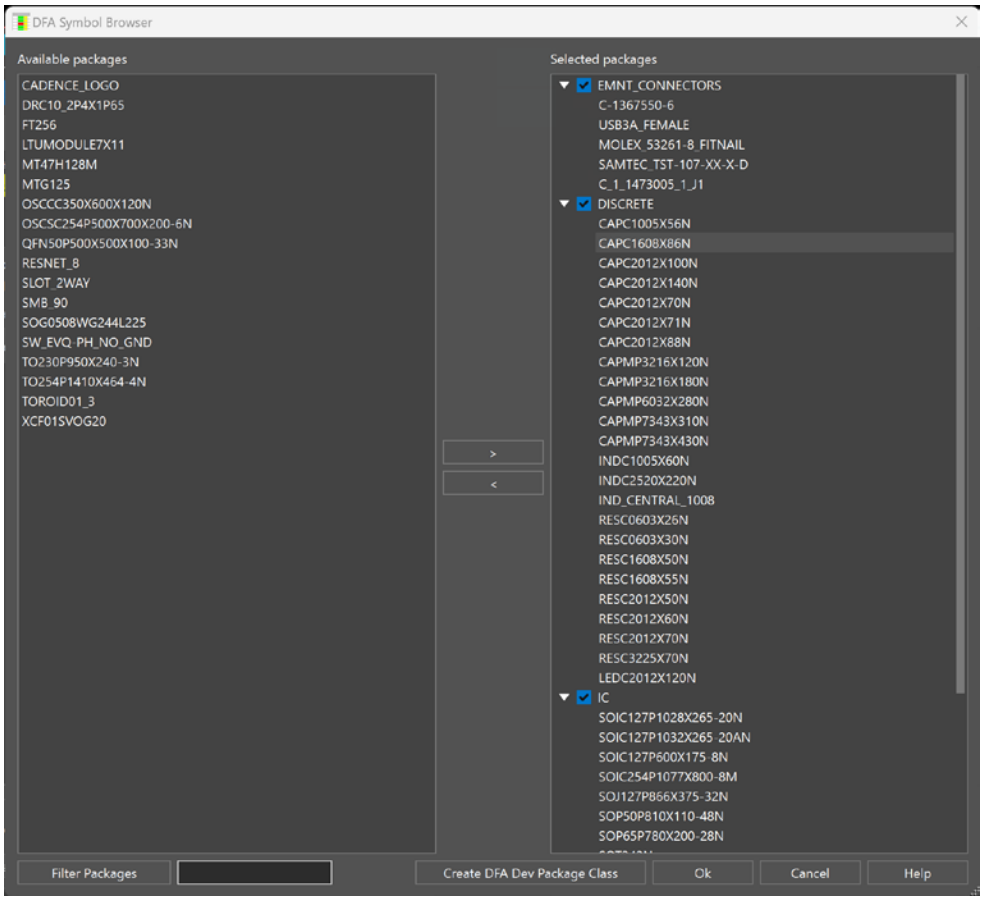


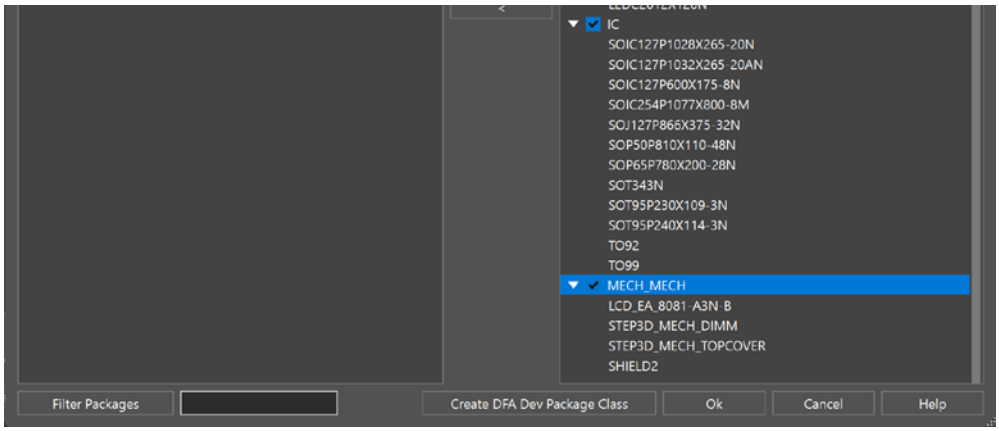
Now you can start adding components to that class, like any connector footprints/symbols.

To do that, select your desired symbols first (on the left), then the category (on the right), then click the **>** arrow to move that into that category.

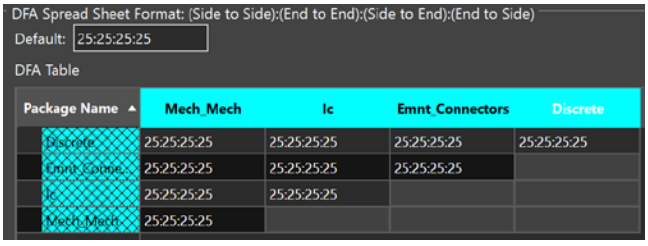


Creating more categories, we can get a list like this below.





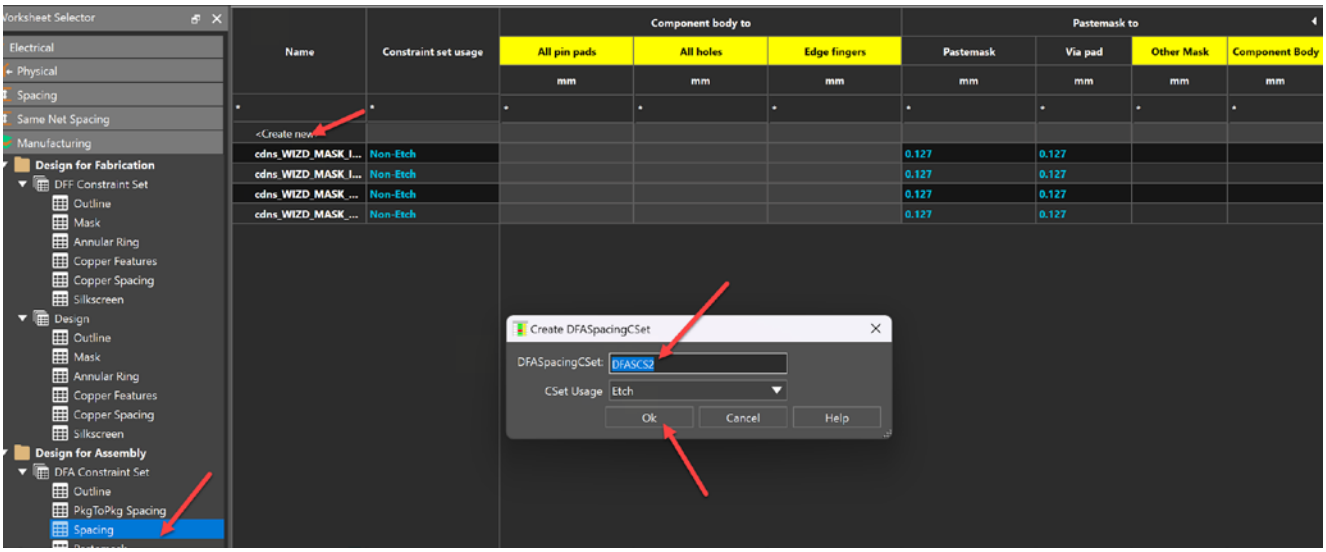
Even though some components are remaining on the left, click Ok. The matrix is created among the symbol categories. They can then have their spacings adjusted within the matrix as shown below.



Spacing

For general spacing of component assembly to other objects on the PCB, go to the **Design for Assembly > DFA Constraint Set > Spacing** worksheet.

You can click the **<Create new>** cell in the upper left corner to create your own DFA Constraint Set, however, we already have 4 created for us in the four rows shown below.



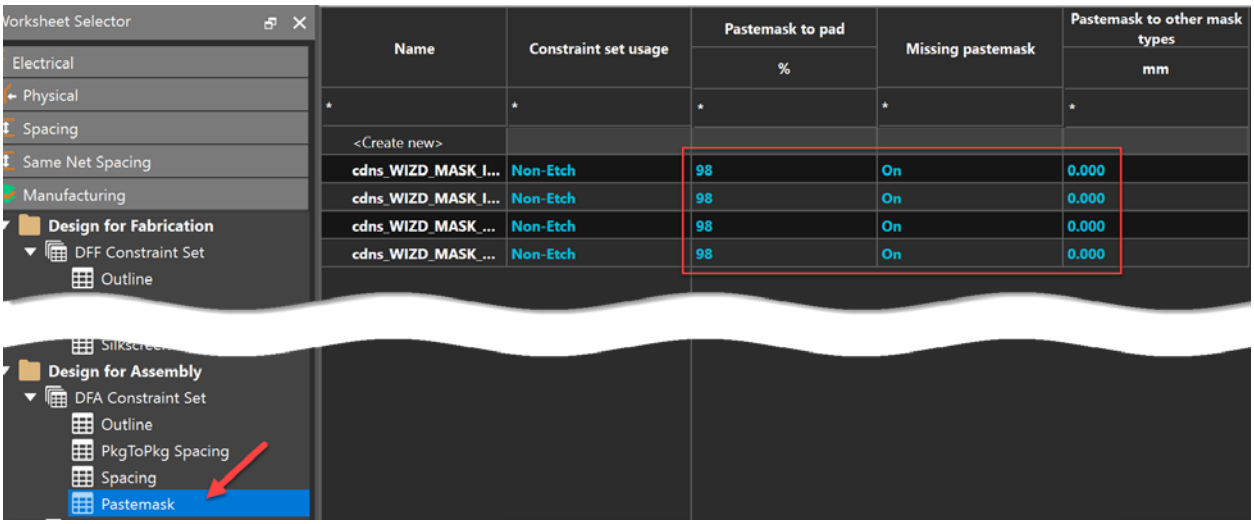
They mostly have spacing for Pastemask to other objects like Pastemask, Via pad, etc. (seen further on the right of the image above).

TIP: Double-click the **Pastemask to** column above to expand the view if yours is not showing it.

This section covers general spacing, which has mostly been taken over by the 3D domain within the Constraint Manager.

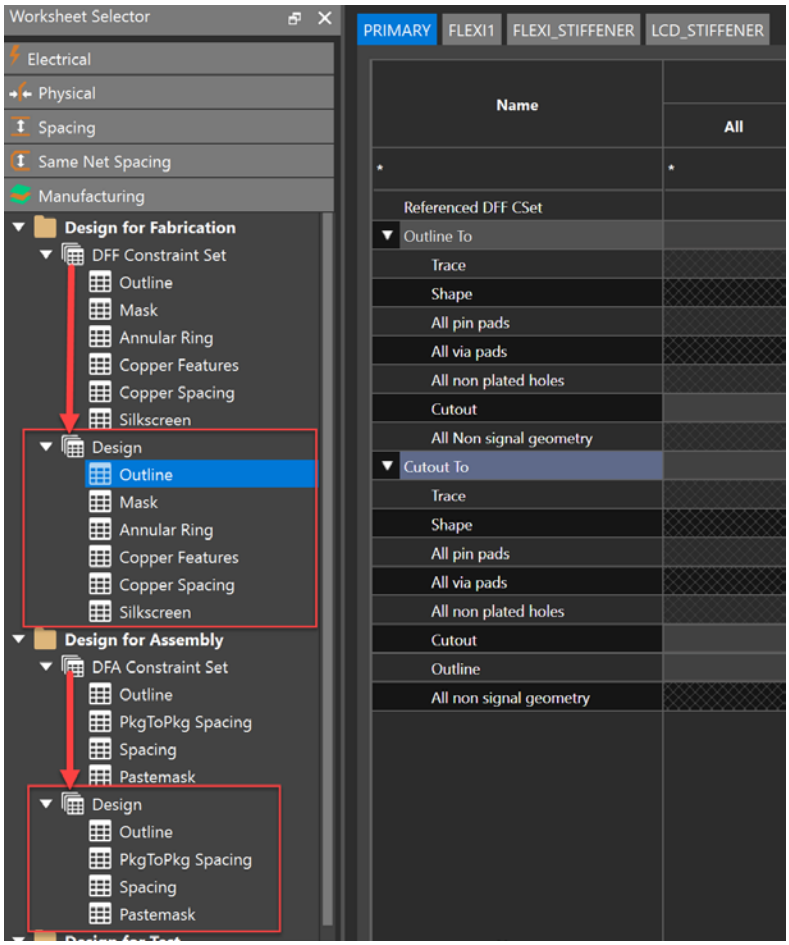
Pastemask

Finally within design for assembly (DFA), we have checks for how much pastemask is on a pad (Pastemask to pad %), if pastemask is missing and the distance of your pastemask to other mask materials.



Applied Constraints

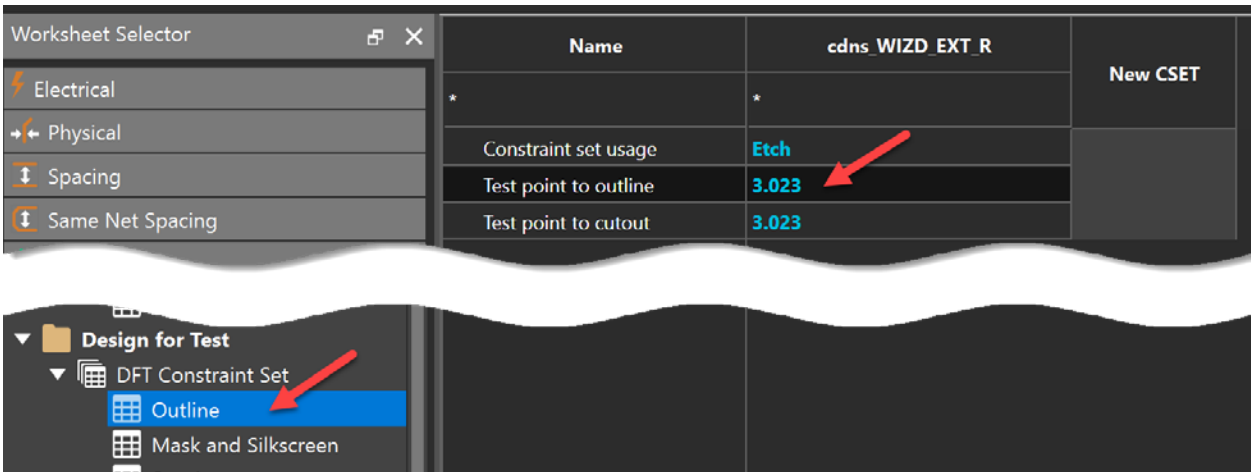
Now for all these constraint sets, they need to be applied to have any effect. So remember to go to the Design workbook, then select and apply each of these Constraint Sets accordingly.



Design for Test Constraints

Finally there are design for test constraints. Depending on your manufacturer, whether they use Bed of Nails Testing, JTAG, etc., you will need to set these values to their capabilities. Here are screenshots of the settings used for this project.

Outline



Mask and Silkscreen

Name	cdns_WIZD_MASK_R	New CSET
*	*	
Constraint set usage	Non-Etch	
Test point on solder mask	On	
Test point to silkscreen	0.381	

Spacing

Name	cdns_WIZD_EXT_R	New CSET
*	*	
Constraint set usage	Etch	
▼ Test point to		
Test point	1.778	
Component	1.016	
All pin pads	0.635	
All via pads	0.635	
All non plated holes	3.023	
Test point under component	On	

Probe

Name	cdns_WIZD_EXT_R	New CSET
*	*	
Constraint set usage	Etch	
Test point minimum pad size	0.889	

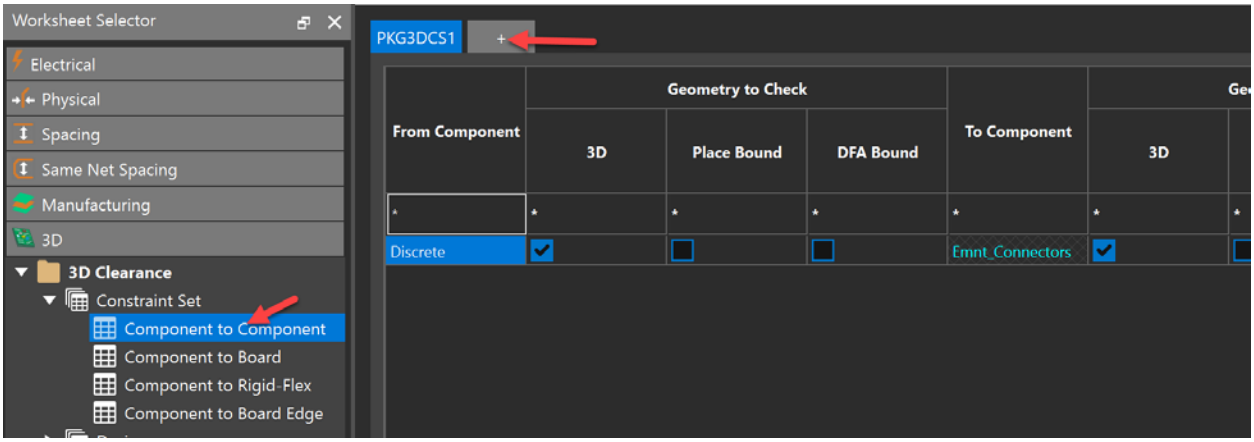
Remember to apply all the constraint sets that were created above to your design worksheet in the Constraint Manager.

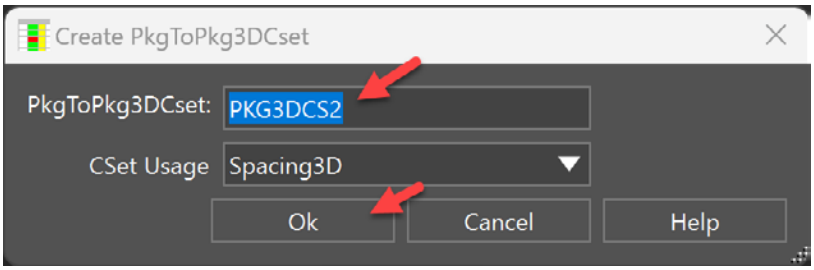
Advanced 3D Constraints

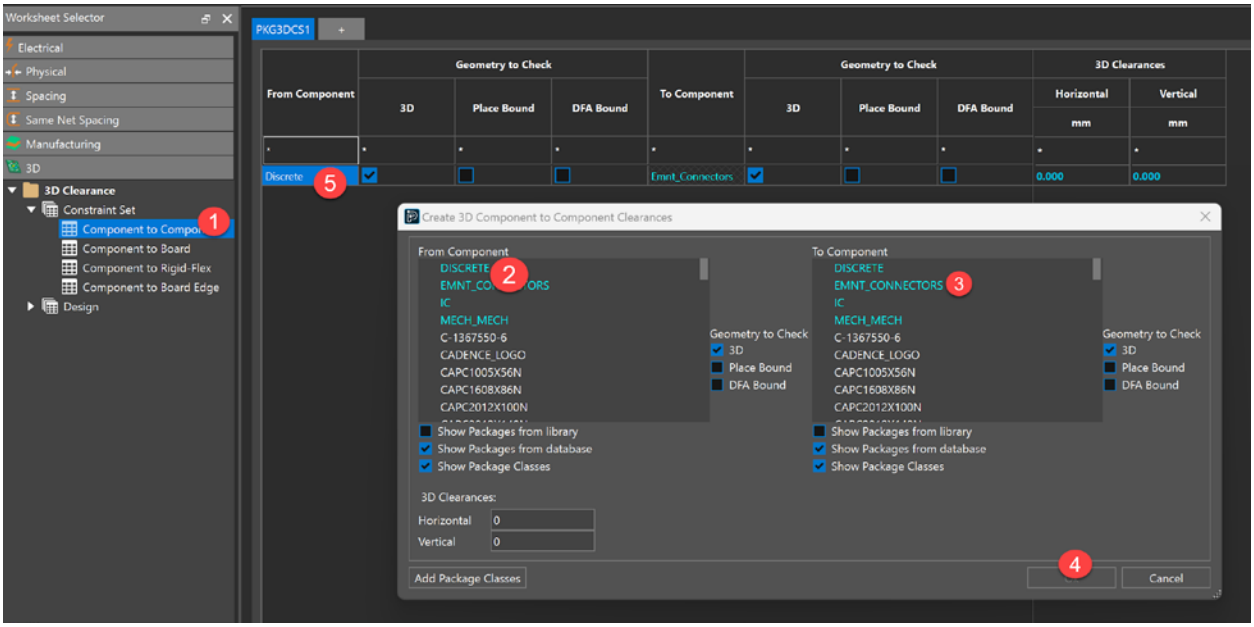
We can set spacing for all our devices and by device categories. Luckily the categories created from the Design for Assembly spacing constraint set earlier are applied to this section as well.

Component to Component

Basically, you want to create a 3D constraint set. Select the **Add a row** button at the bottom of the worksheet and choose the type of devices being spaced to each other. See the steps shown below.

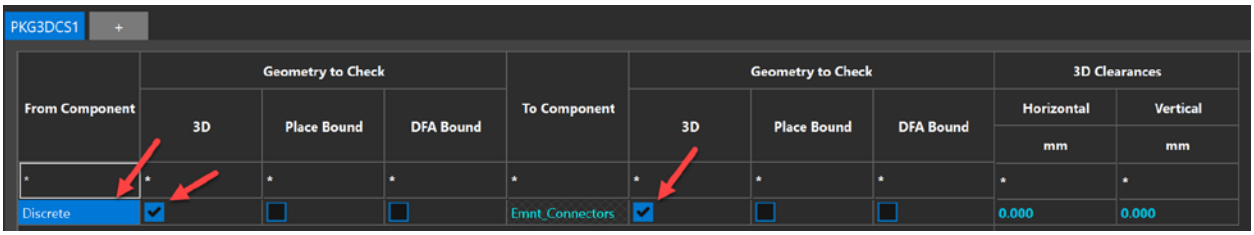






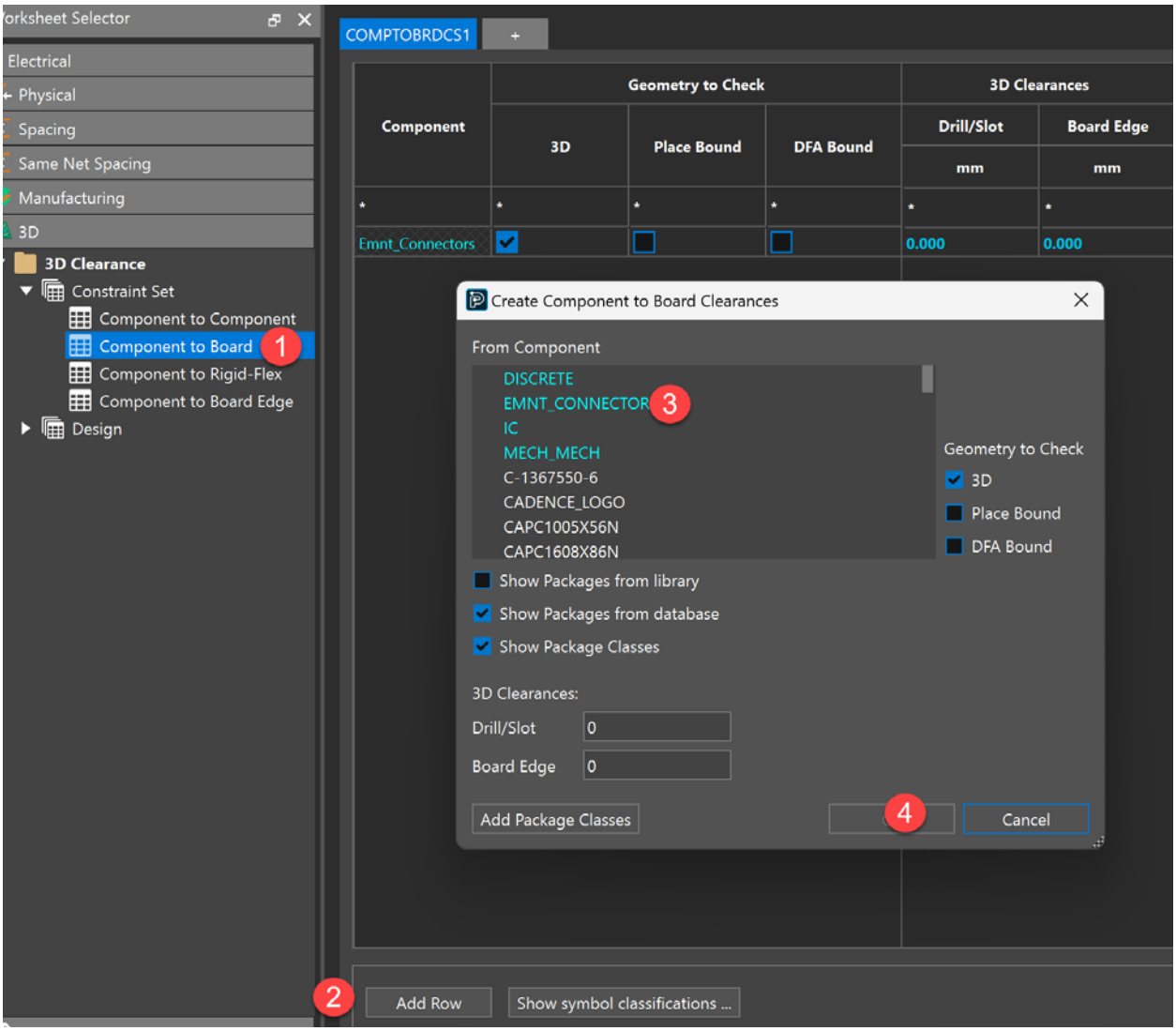
From the above image, click the buttons in the order shown and you will get a row applied to the Component-to-Component constraint set area.

Now you can check 3D to 3D spacing for your discrete components. Or the 3D to place bound, DFA bound, or all three for both categories (Discrete to Discrete).

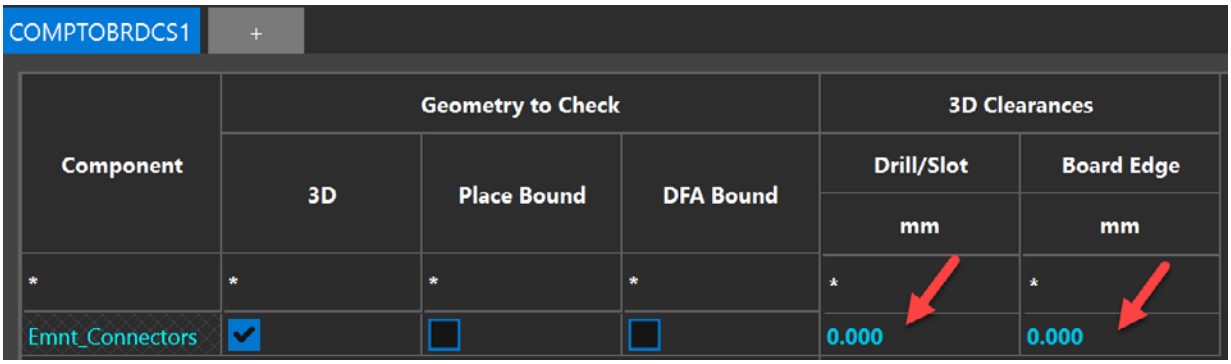


Component to Board

Like the previous section (Component to Component Spacing), you can add a row for your Component to Board spacing. Select **EMNT_CONNECTORS**, then click Ok.

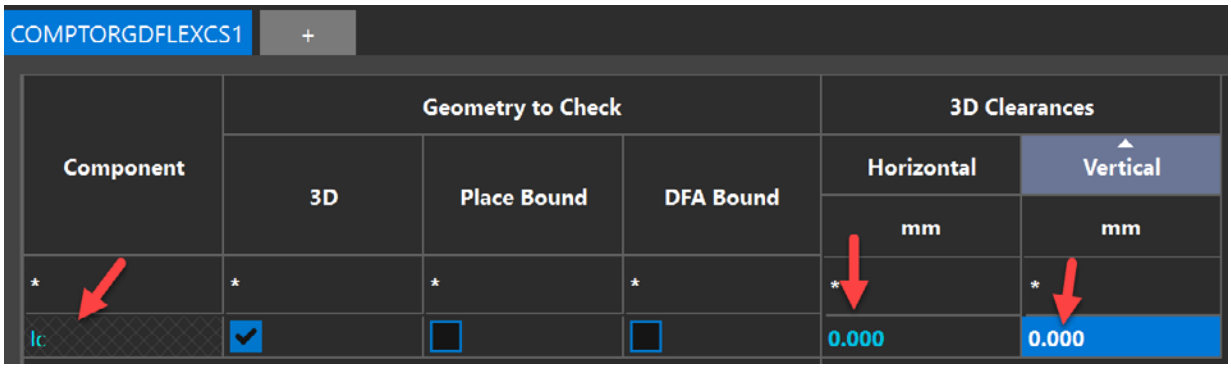


Now that the row is applied, you can set your **3D Clearances** column values for your connectors to **Drill/Slots** or the **Board Edge**.



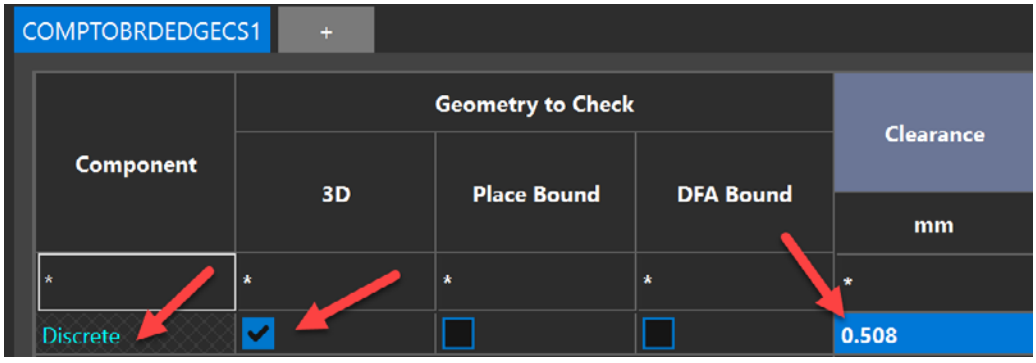
Component to Rigid-Flex

Follow similar steps in the Component to Rigid-Flex worksheet.

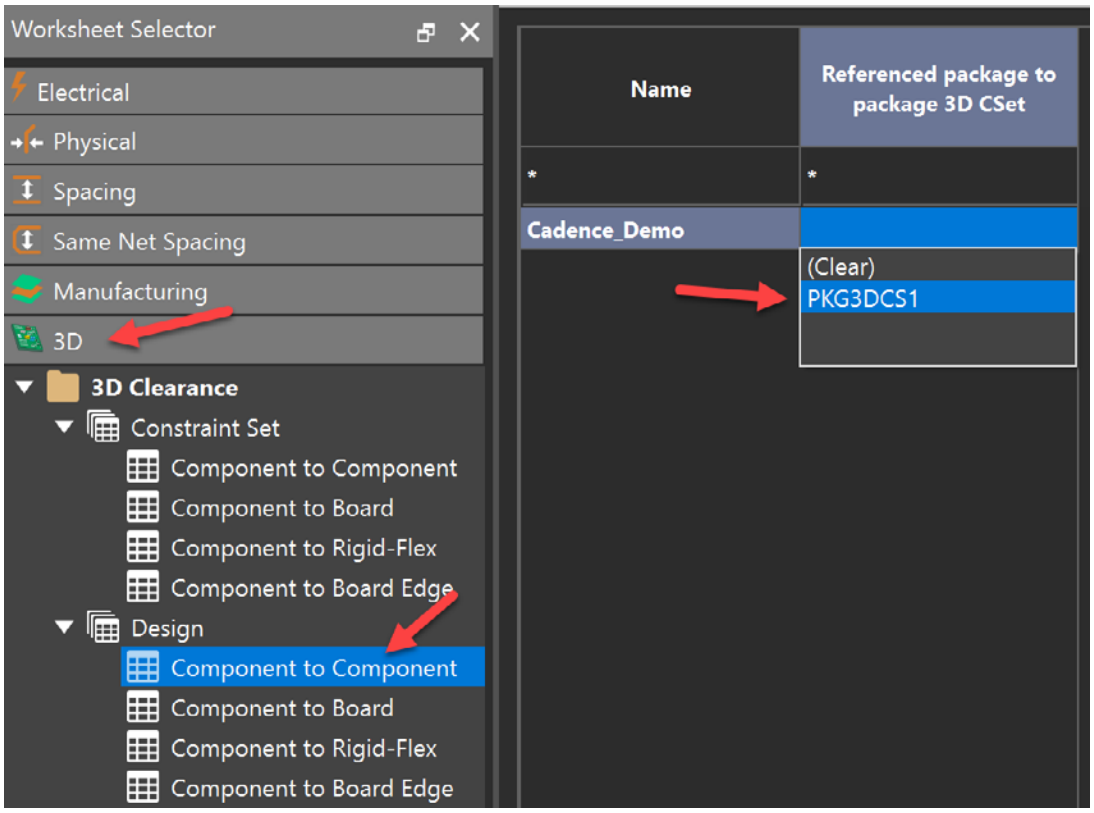


Component to Board Edge

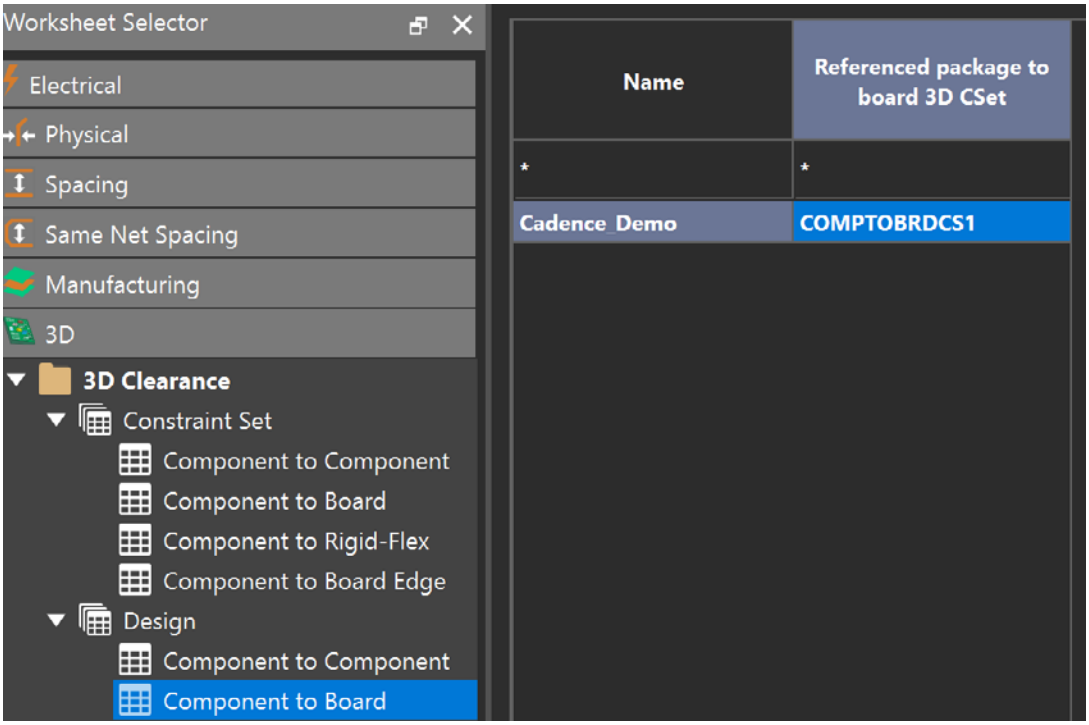
Select the Component to Board Edge worksheet, add a row and set the component categories you want to constraint with respect to the board edge (see below).

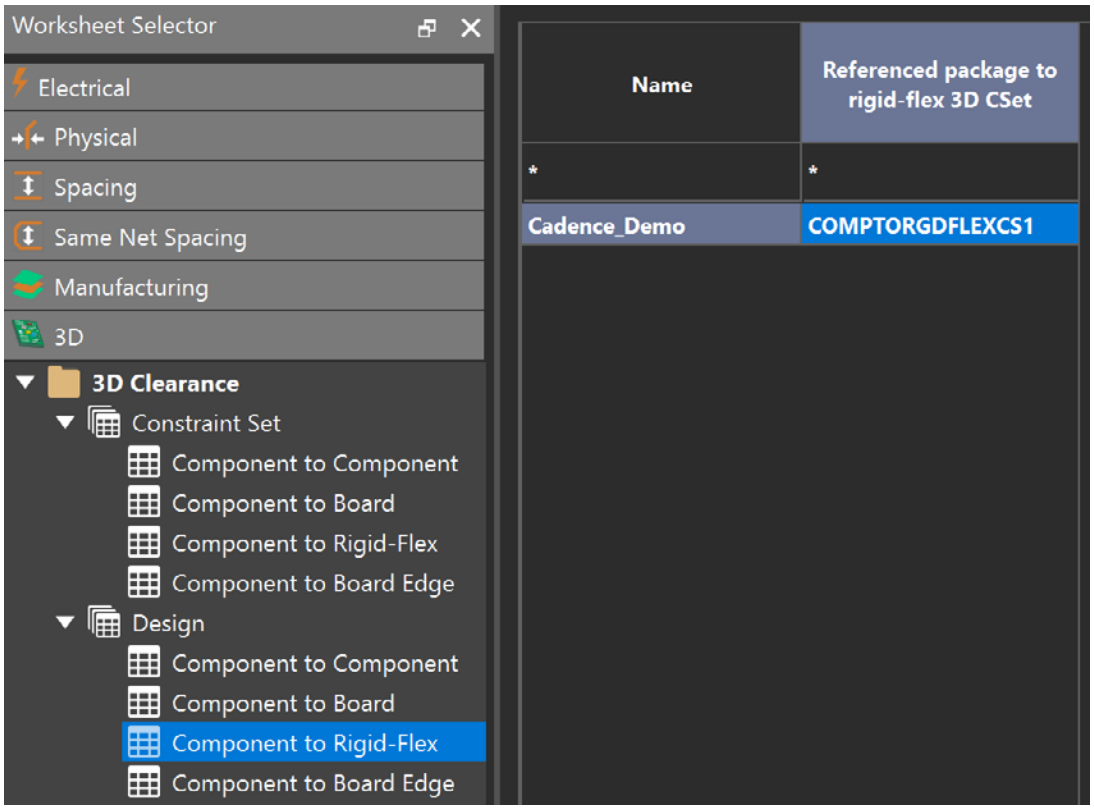


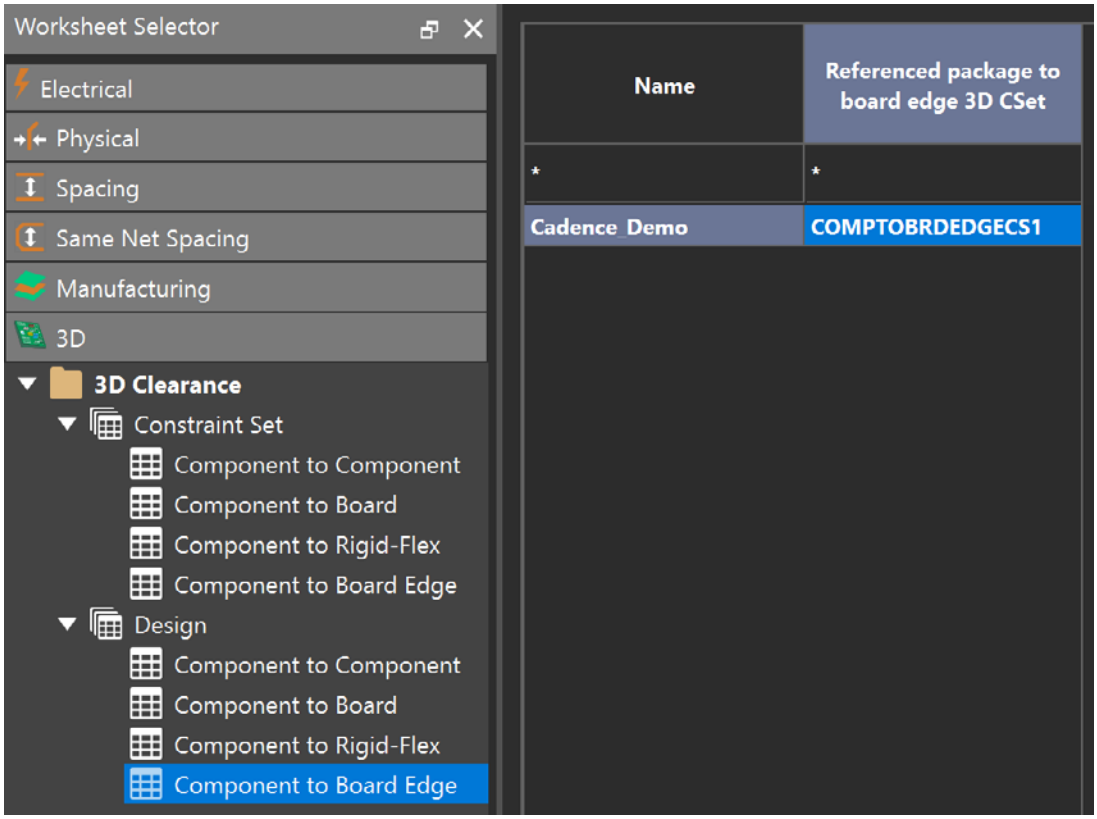
Then remember to apply these constraint sets to relevant parts of your design. For example, click the worksheet under **3D > Design > Component to Component**. Then select the constraint you want from the dropdown list and apply it.



Follow the same procedure to apply the constraint sets to your remaining design per category (see the images below).



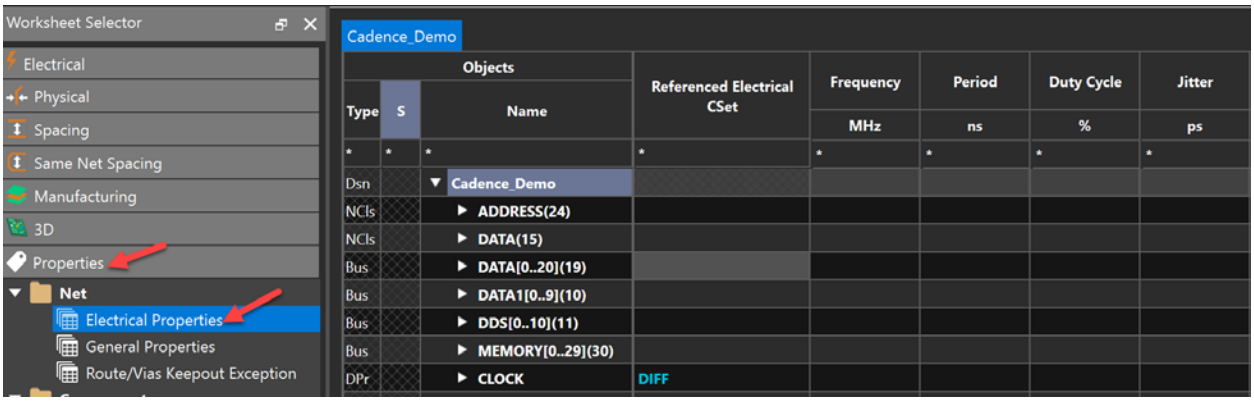

Worksheet Selector
Electrical
Physical
Spacing
Same Net Spacing
Manufacturing
3D
3D Clearance
Constraint Set
Component to Component
Component to Board
Component to Rigid-Flex
Component to Board Edge
Design
Component to Component
Component to Board
Component to Rigid-Flex
Component to Board Edge
Name
Referenced package to rigid-flex 3D CSet
*
*
Cadence_Demo
COMPTORGDFLEXCS1

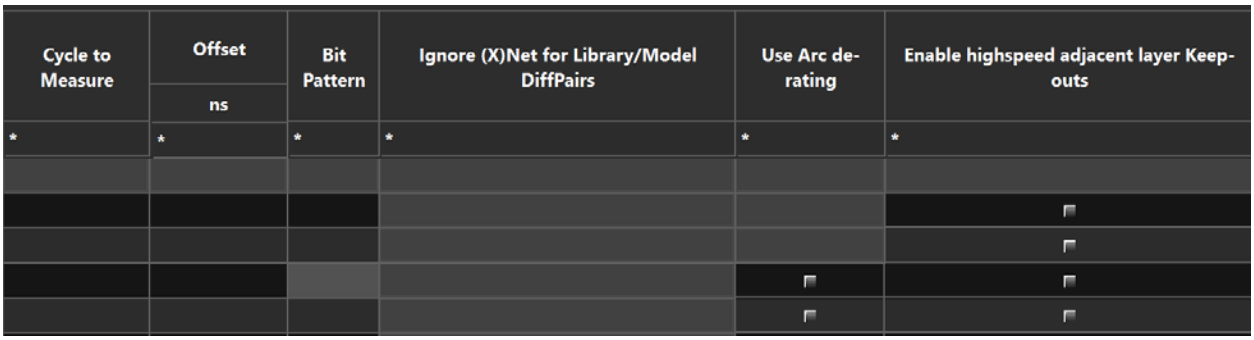

Worksheet Selector
Electrical
Physical
Spacing
Same Net Spacing
Manufacturing
3D
3D Clearance
Constraint Set
Component to Component
Component to Board
Component to Rigid-Flex
Component to Board Edge
Design
Component to Component
Component to Board
Component to Rigid-Flex
Component to Board Edge
Name
Referenced package to board edge 3D CSet
*
*
Cadence_Demo
COMPTOBRDEDGECS1

Advanced Properties

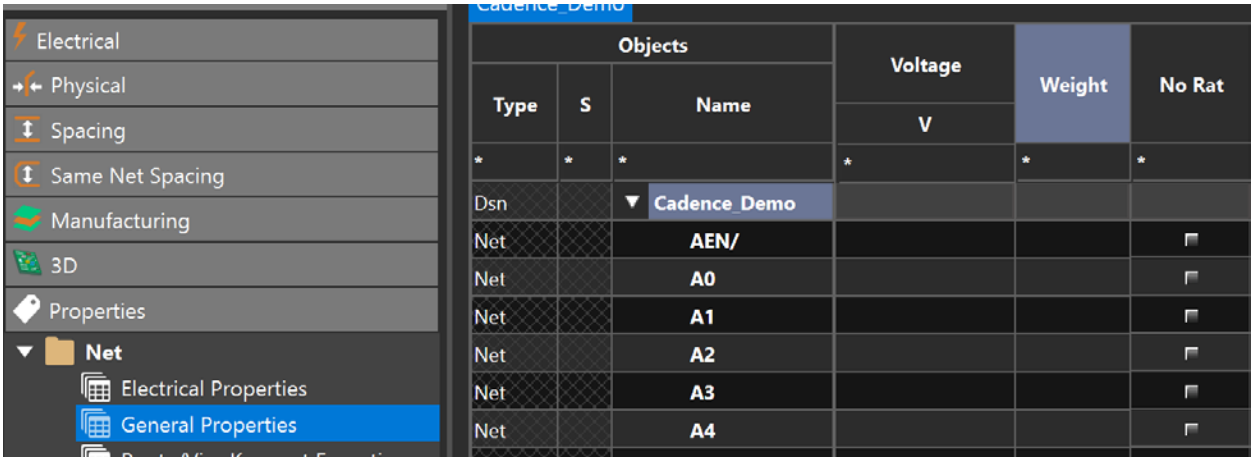
The Constraint Manager goes a step further and lets you set specific values, properties to each net and component that do not necessarily fit in the above categories. We will give a quick tour on the settings that can be set.

Electrical Properties





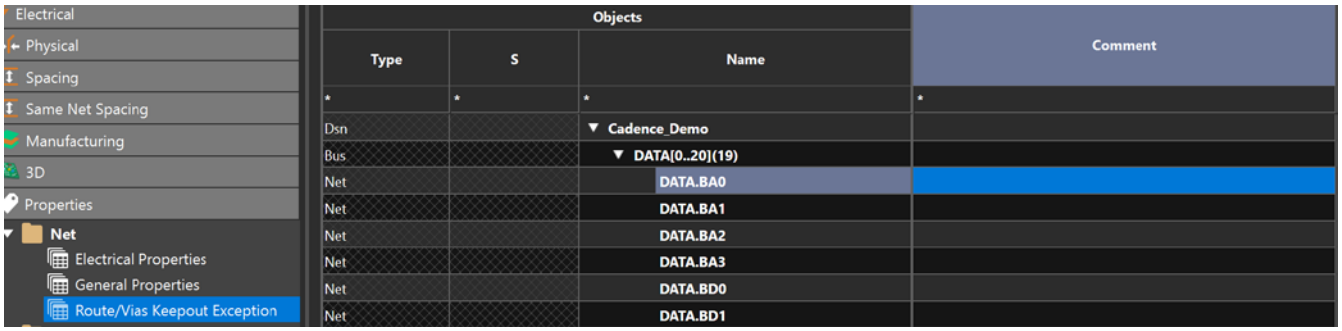
General Properties



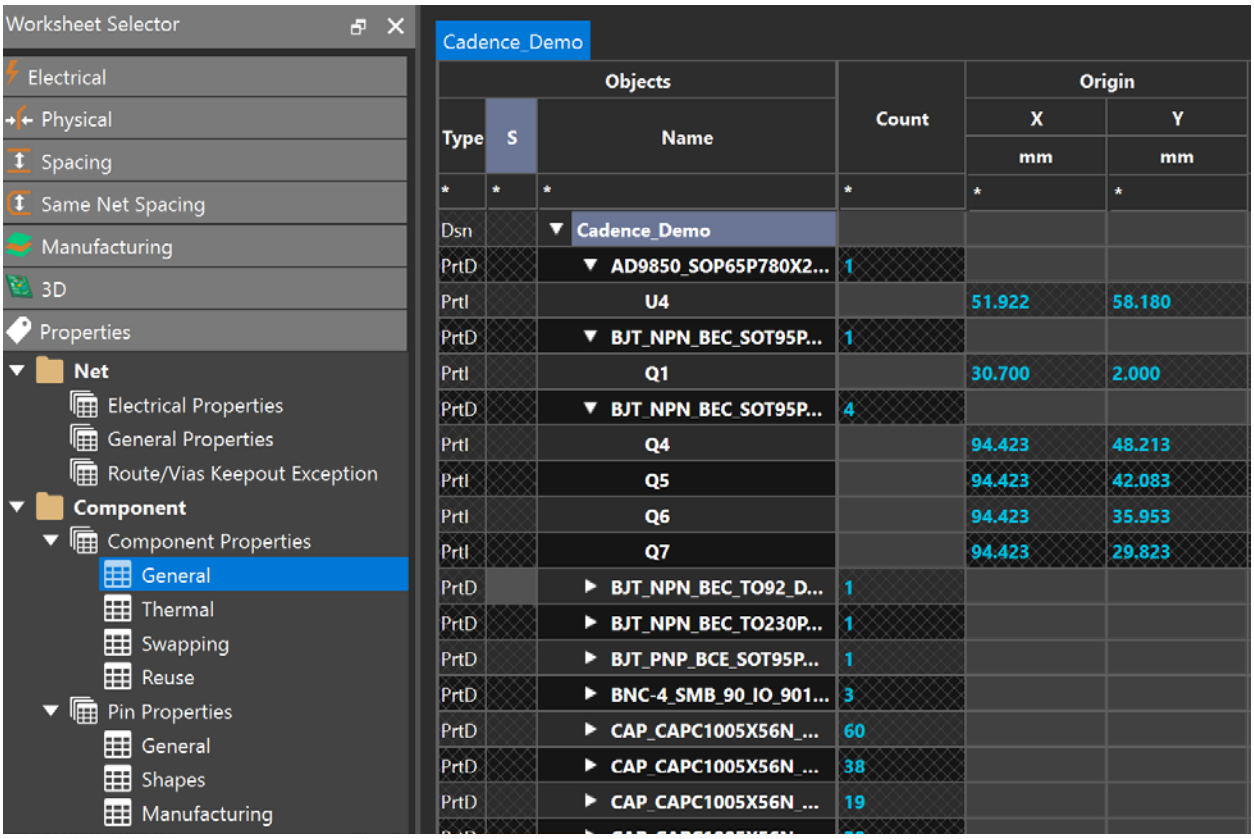
Route		Route Restrictions				Testpoints		
Priority	to Shape	Fixed	No Route	No Ripup	No Pin Escape	Prohibit	Quantity	Probe Number
*	*	*	*	*	*	*	*	*
	☐	☐	☐	☐	☐	☐		
	☐	☐	☐	☐	☐	☐		
	☐	☐	☐	☐	☐	☐		
	☐	☐	☐	☐	☐	☐		
	☐	☐	☐	☐	☐	☐		
	☐	☐	☐	☐	☐	☐		
	☐	☐	☐	☐	☐	☐		

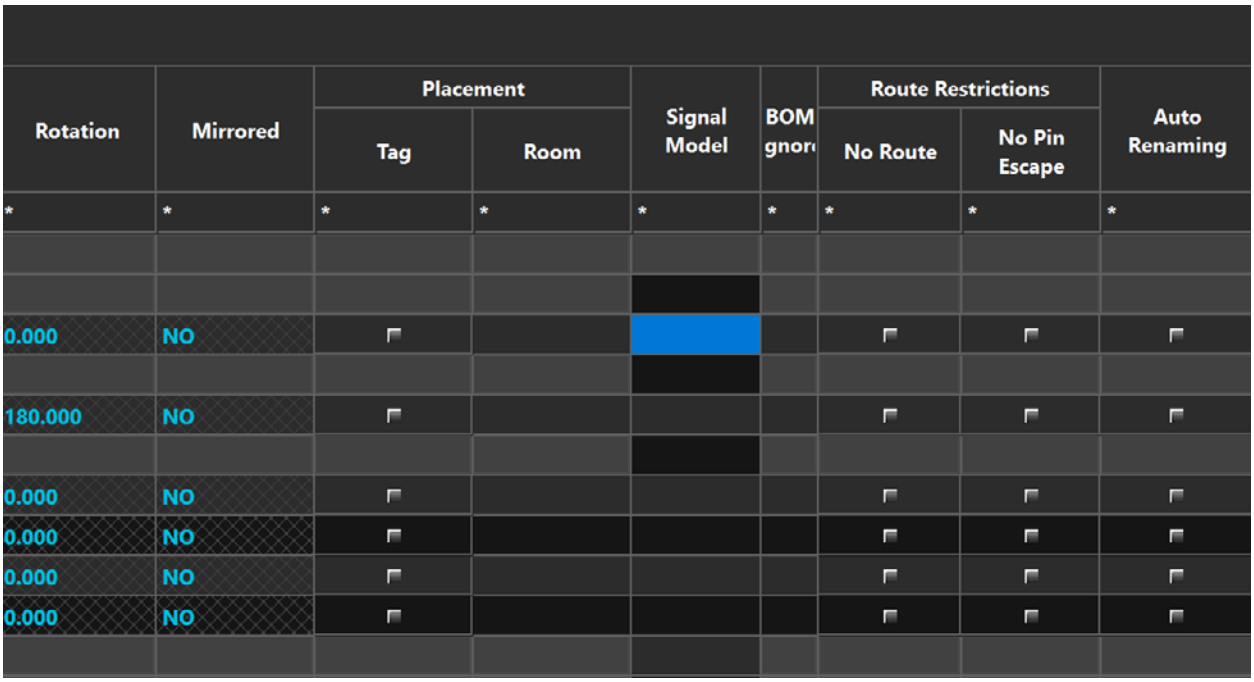
Backdrill		Shield							
Max PTH Stub mm	No Gloss	Shield	Type	ECL	EMC Critical Net	Ignore Unused Pads Suppression	Retain Net on Vias	Comment	
*	*	*	*	*	*	*	*	*	
	☐			☐		☐	☐		
	☐			☐		☐	☐		
	☐			☐		☐	☐		
	☐			☐		☐	☐		

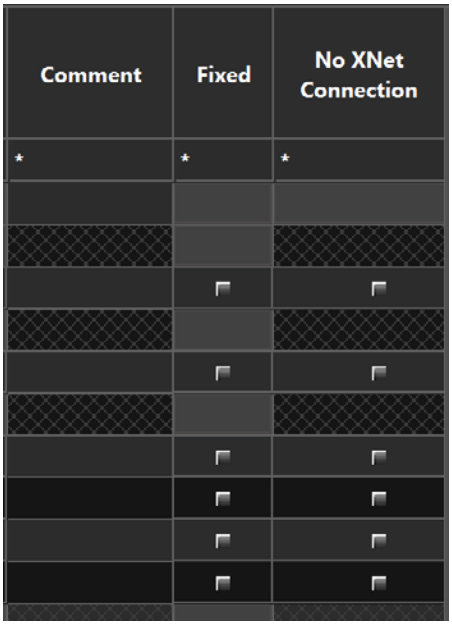
Route/Vias Keepout Exception



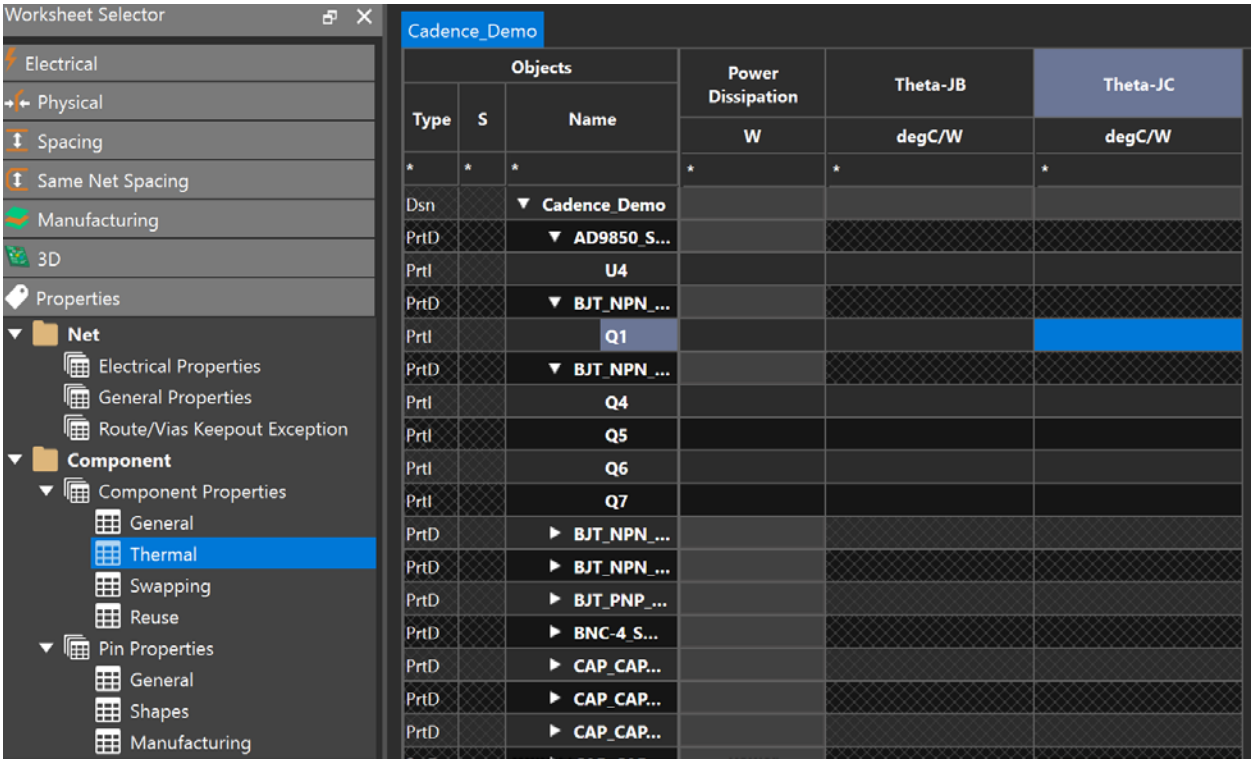
Component Properties – General



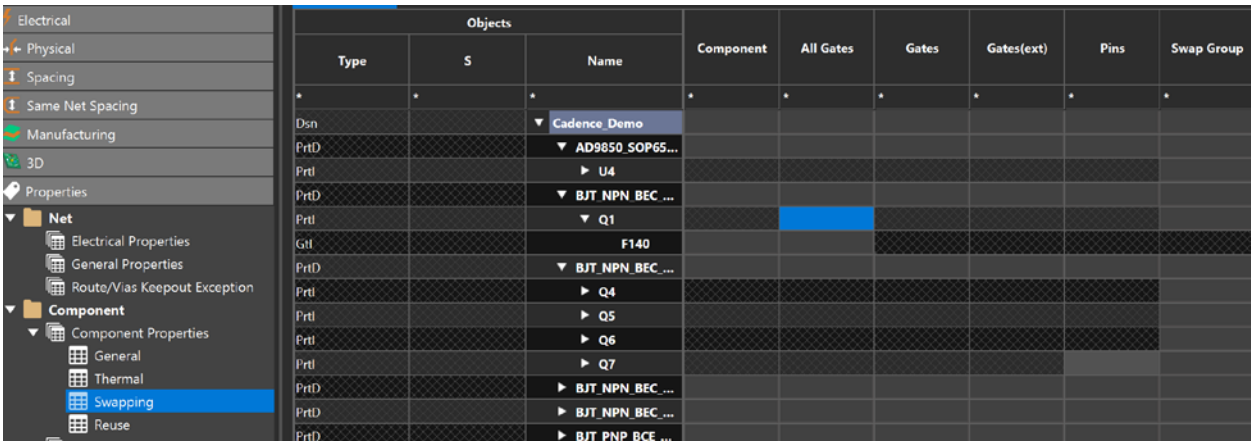




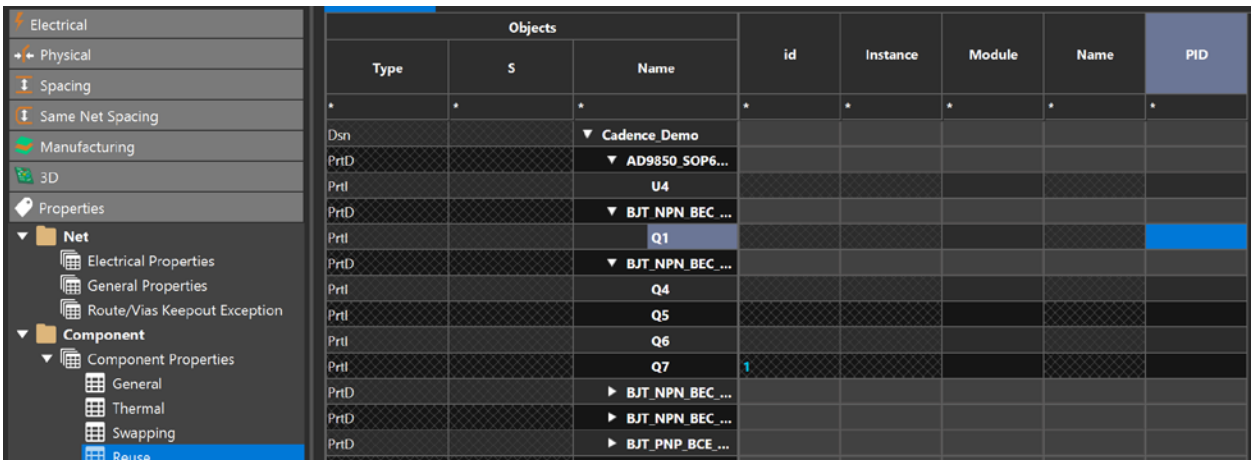
Component Properties – Thermal



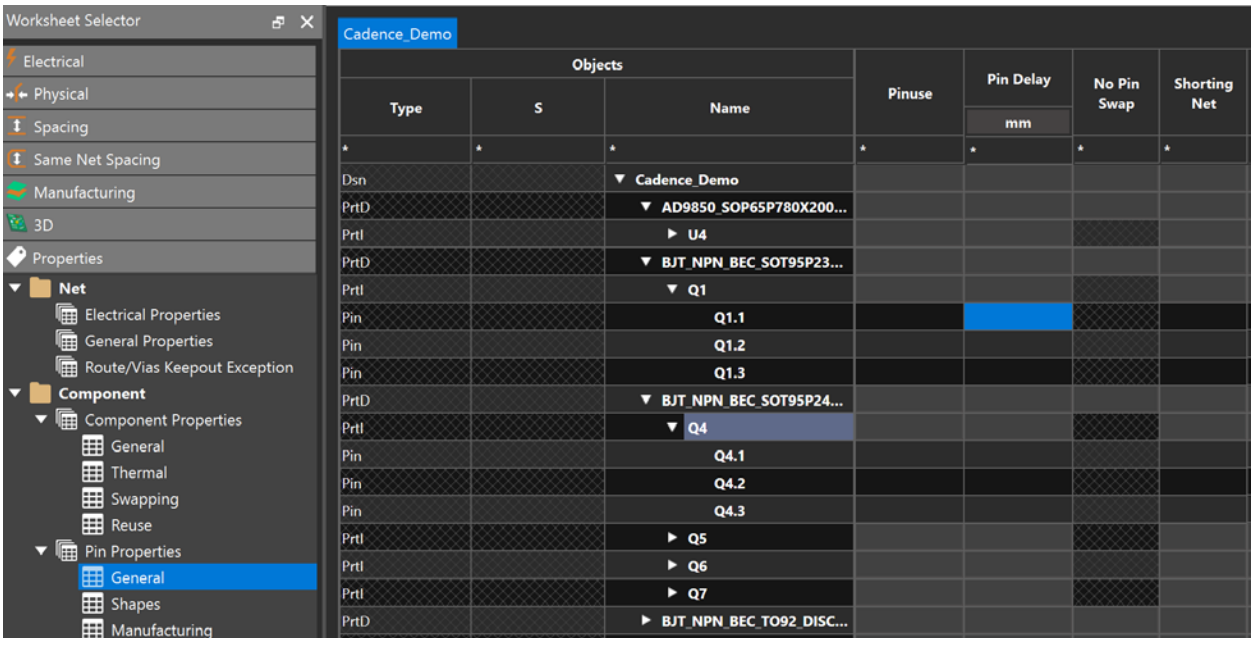
Component Properties – Swapping

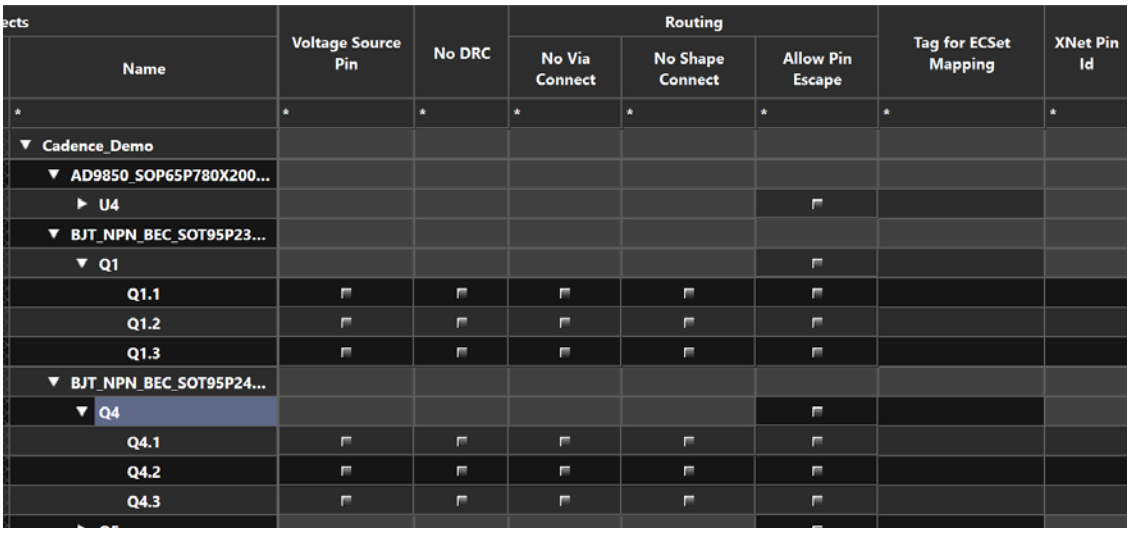


Component Properties – Reuse

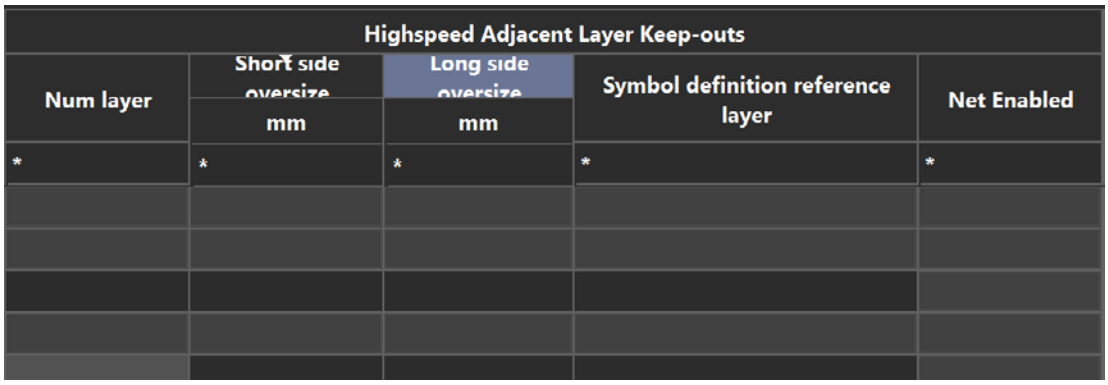


Pin Properties – General



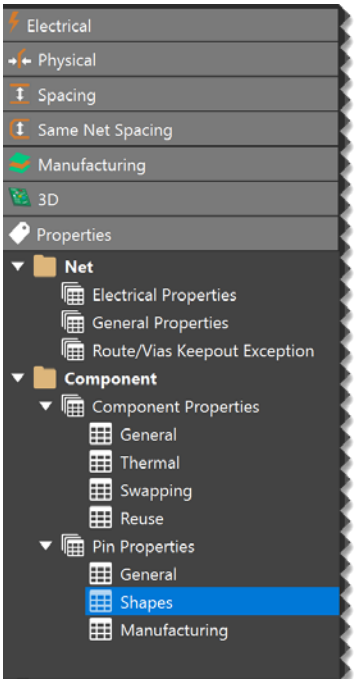


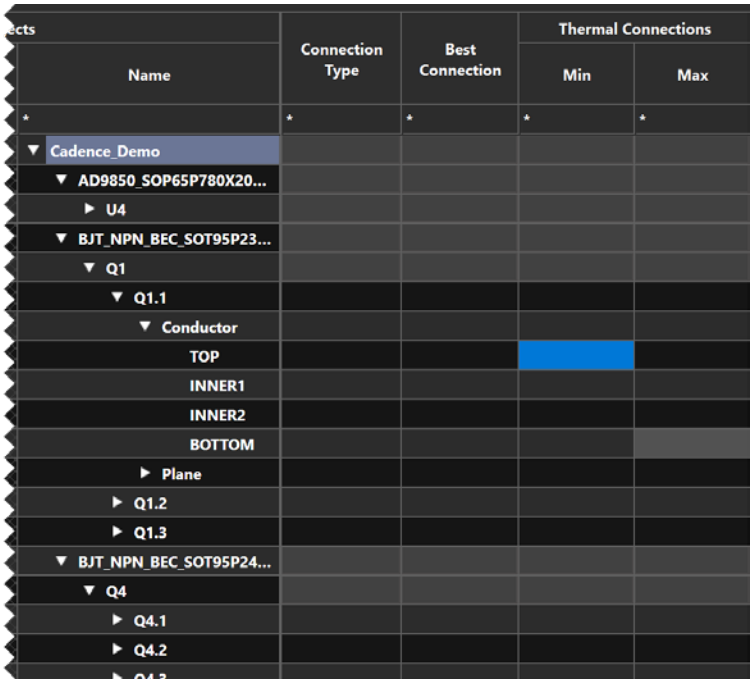
ects Name	Voltage Source Pin	No DRC	Routing: No Via Connect	Routing: No Shape Connect	Routing: Allow Pin Escape	Tag for ECSet Mapping	XNet Pin Id
*	*	*	*	*	*	*	*
▼ Cadence_Demo							
▼ AD9850_SOP65P780X200...							
▶ U4					☐		
▼ BJT_NPN_BEC_SOT95P23...							
▼ Q1					☐		
Q1.1	☐	☐	☐	☐	☐		
Q1.2	☐	☐	☐	☐	☐		
Q1.3	☐	☐	☐	☐	☐		
▼ BJT_NPN_BEC_SOT95P24...							
▼ Q4					☐		
Q4.1	☐	☐	☐	☐	☐		
Q4.2	☐	☐	☐	☐	☐		
Q4.3	☐	☐	☐	☐	☐		



Highspeed Adjacent Layer Keep-outs				
Num layer	Short side oversize mm	Long side oversize mm	Symbol definition reference layer	Net Enabled
*	*	*	*	*

Pin Properties – Shapes

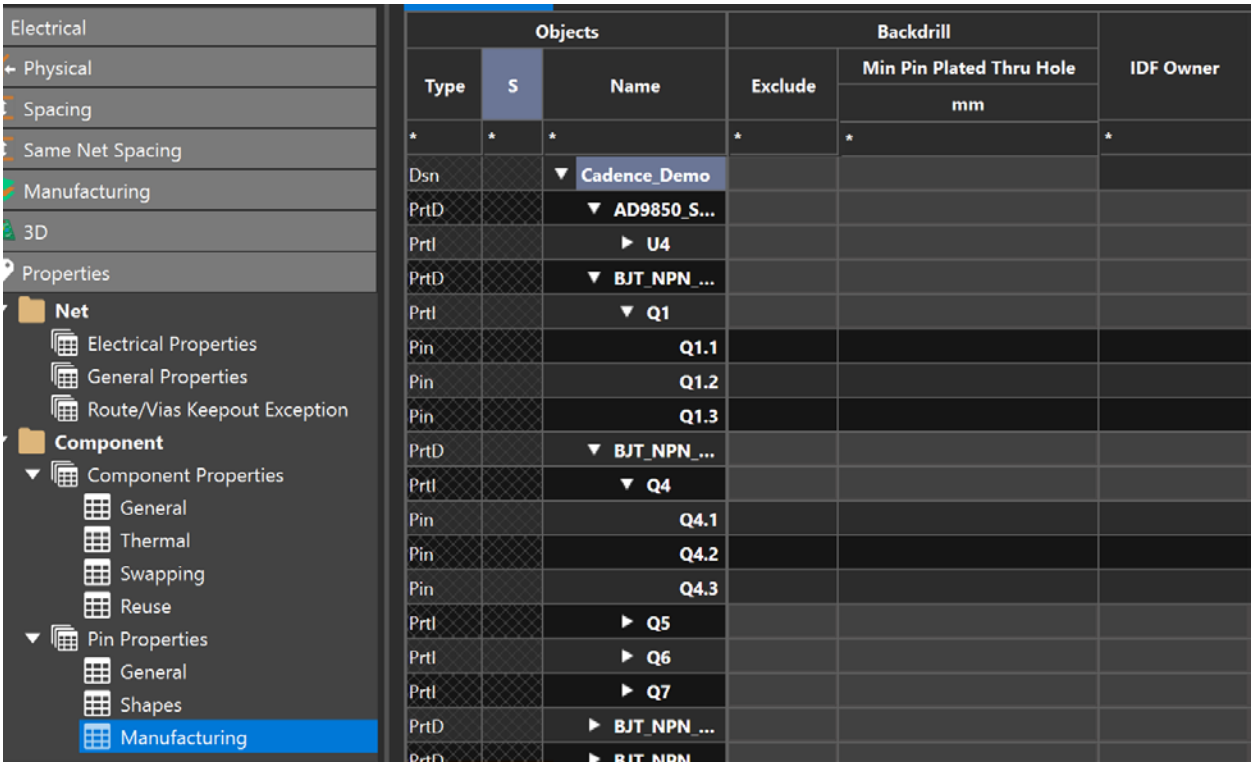




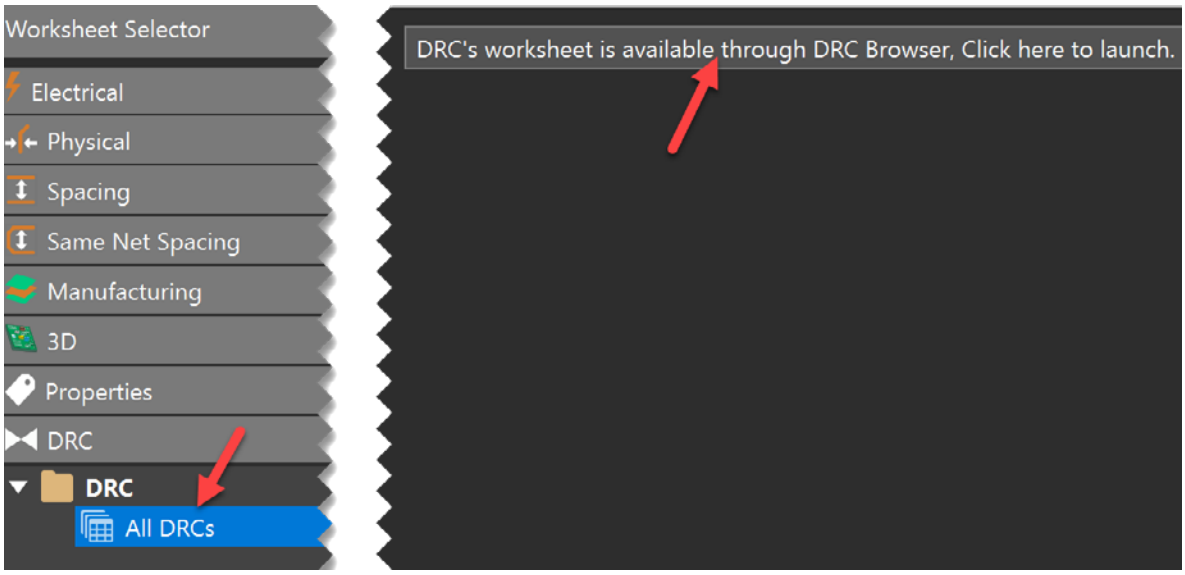
ects Name	Connection Type	Best Connection	Thermal Connections: Min	Thermal Connections: Max
*	*	*	*	*
▼ Cadence_Demo				
▼ AD9850_SOP65P780X20...				
▶ U4				
▼ BJT_NPN_BEC_SOT95P23...				
▼ Q1				
▼ Q1.1				
▼ Conductor				
TOP				
INNER1				
INNER2				
BOTTOM				
▶ Plane				
▶ Q1.2				
▶ Q1.3				
▼ BJT_NPN_BEC_SOT95P24...				
▼ Q4				
▶ Q4.1				
▶ Q4.2				

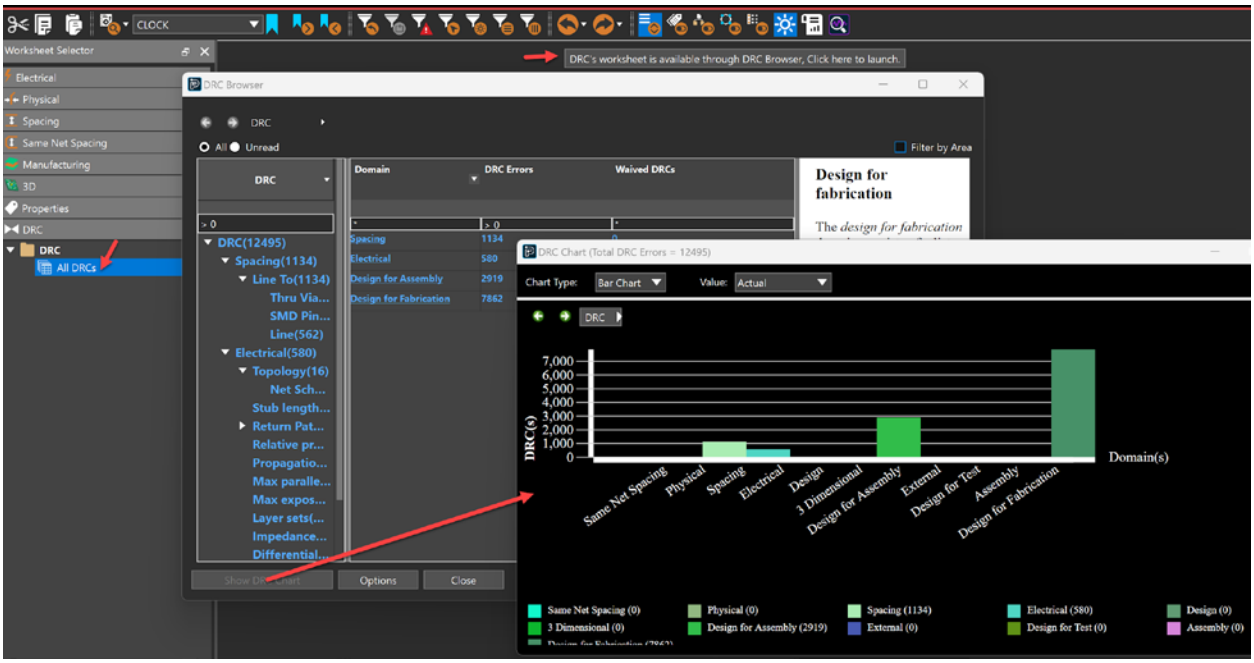
Thermal Clearance		Thermal Connect Width	
Clearance Type	Oversized	Fixed	Oversized
	mm	mm	mm
*	*	*	*

Pin Properties – Manufacturing



Advanced DRCs

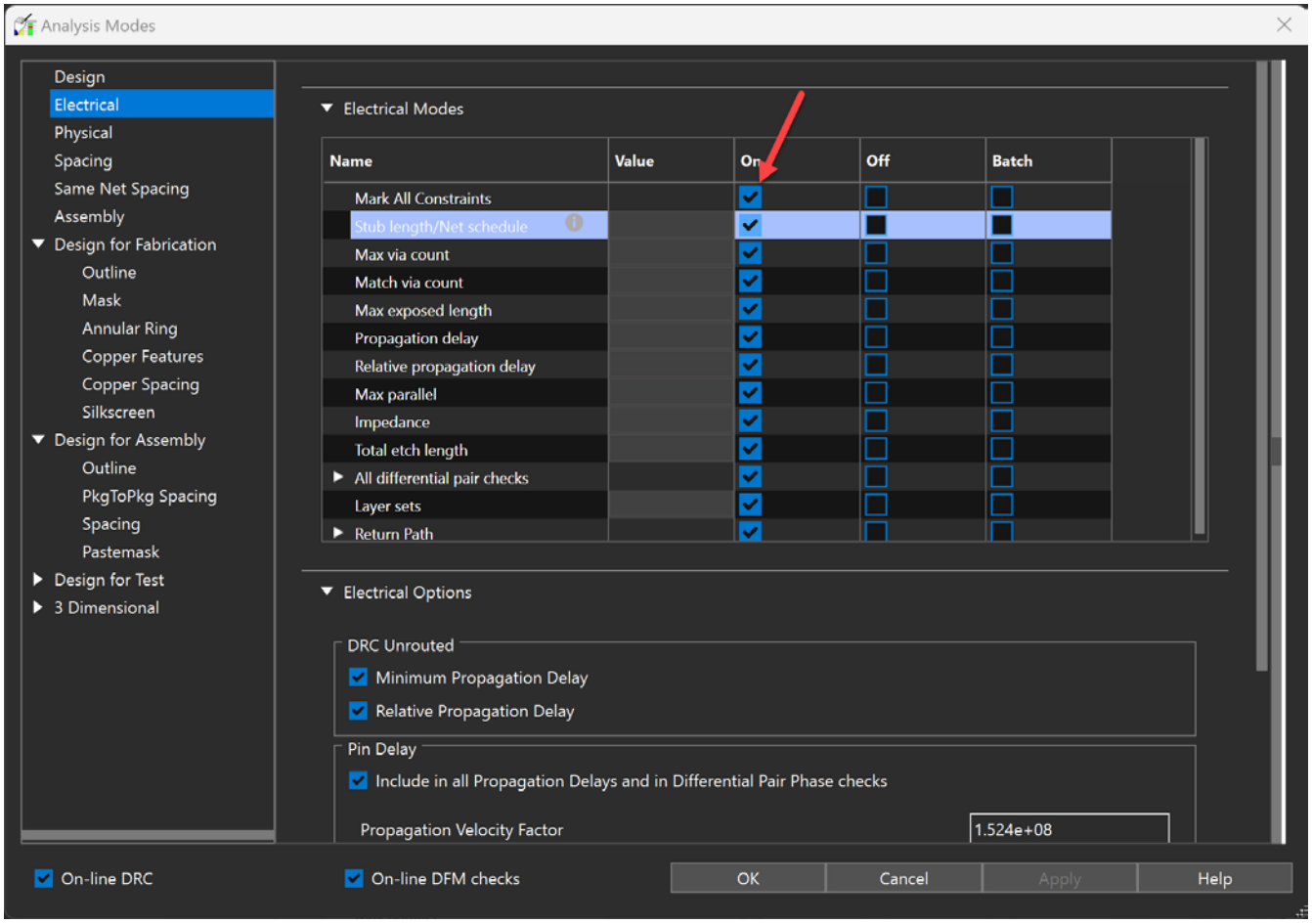




Constraint Analysis

The Constraint Manager can be configured to analyze only specific aspects of your design if desired. By default, some of the high-speed constraint considerations you would want are not enabled. If the constraint manager is not set to analyze a constraint, it will not do so in the worksheets.

Let's navigate to the Analysis tool. In the Constraint Manager go to **Analyze – Analysis Mode**. Then the Analysis Modes window appears. You can turn on all the rule checks by checking the top-most checkbox in any category. Also be sure to check options in the lower part of the window like for Minimum propagation Delay, Pin Delay and so on (see image below).

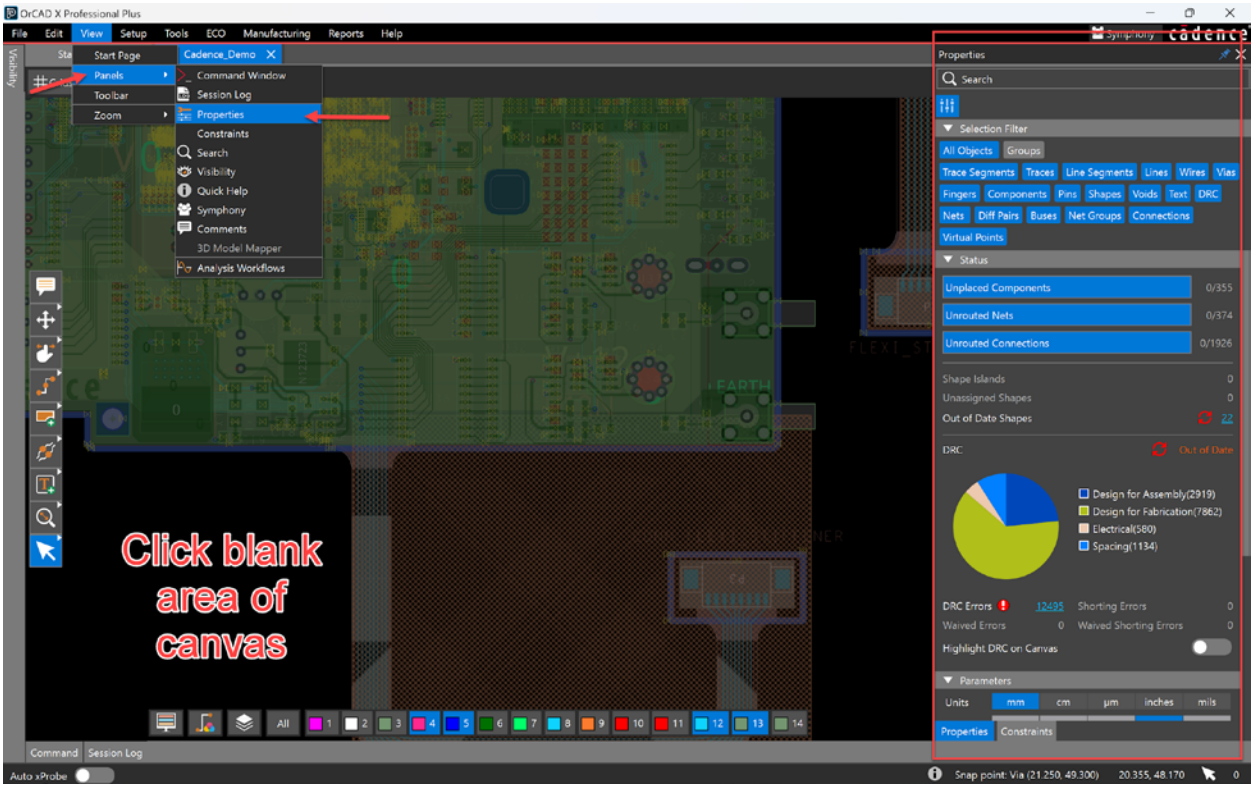


In general for most complex designs, turn everything on. However, note that the software will use more resources and may become evident in terms of system performance depending on the size of the design and the specifications of your machine.

Final Constraint Design Rule Check

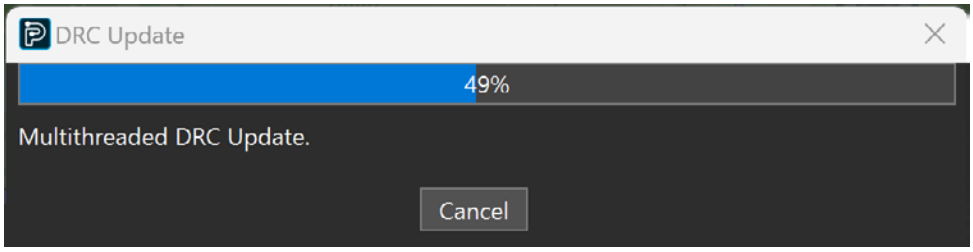
Let's perform a design rule check (DRC) to see if constraints created are being adhered to.

Close the Constraint Manager if it is open. Then as shown below, in OrCAD X Presto PCB Editor, navigate to the menu and select **View – Panels – Properties**. The Properties Panel will appear. Click on a blank area of the design canvas.

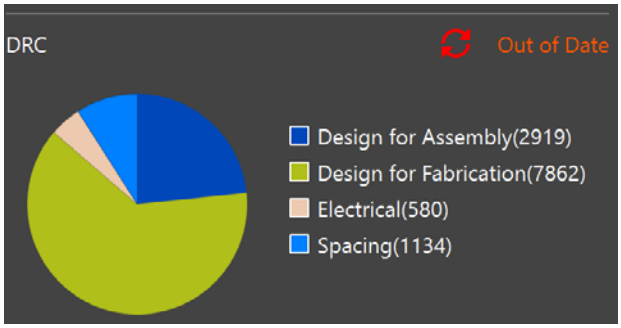


You can pin the panel to keep it active by clicking the thumbtack icon in the upper right corner of the panel.

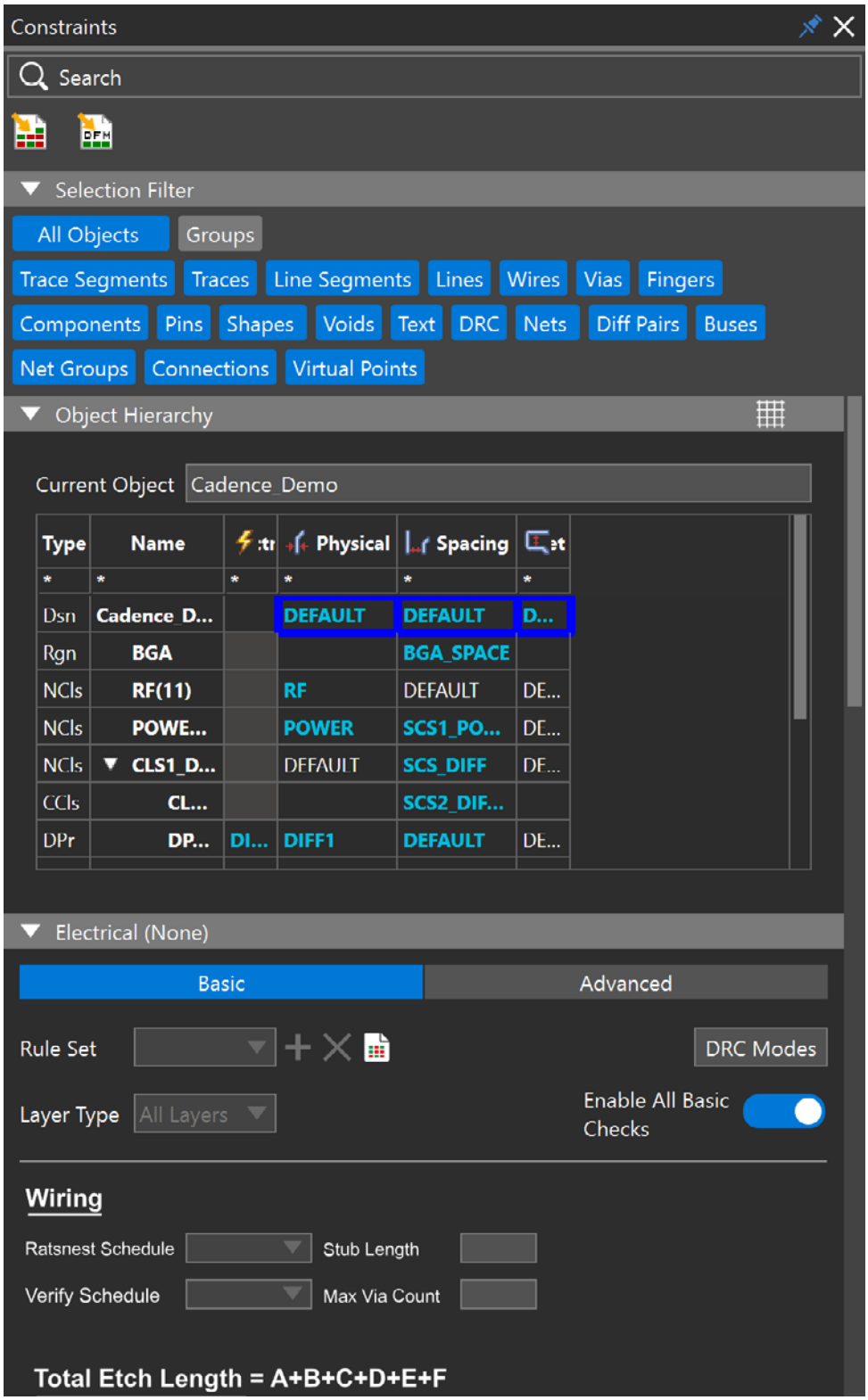
Then to update the design rule check results, click the Out of Date Out of Date icon. That will update the DRC analysis.

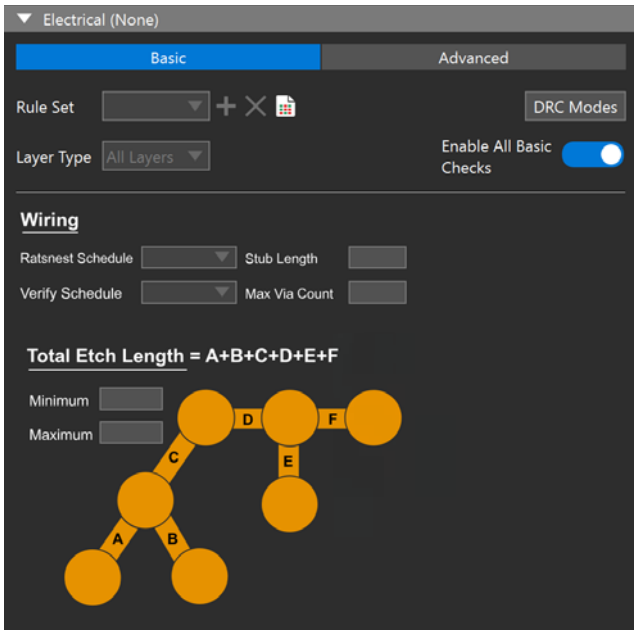


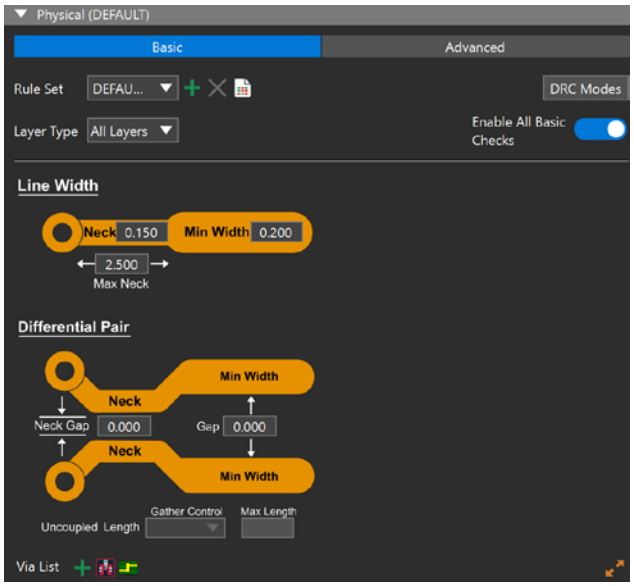
When finished, Presto will display the updated Pie Chart (see image below).

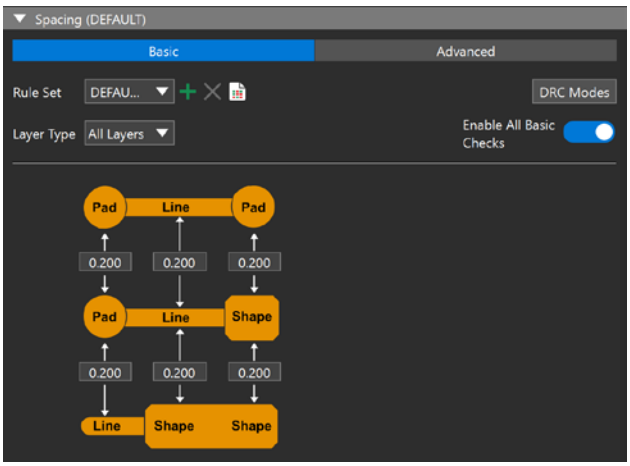


You can also review the constraints for your design using the Constraints Panel shown below. You can make it visible by going to the menu in Presto and choosing **View – Panels – Constraints**.




Electrical (None)
Basic
Advanced
Rule Set
DRC Modes
Layer Type
All Layers
Enable All Basic Checks
Wiring
Ratsnest Schedule
Stub Length
Verify Schedule
Max Via Count
Total Etch Length = A+B+C+D+E+F
Minimum
Maximum
A
B
C
D
E
F


Physical (DEFAULT)
Basic
Advanced
Rule Set
DEFAU...
DRC Modes
Layer Type
All Layers
Enable All Basic Checks
Line Width
Neck
0.150
Min Width
0.200
2.500
Max Neck
Differential Pair
Min Width
Neck
Neck Gap
0.000
Gap
0.000
Neck
Min Width
Uncoupled Length
Gather Control
Max Length
Via List


Spacing (DEFAULT)
Basic
Advanced
Rule Set
DEFAU...
DRC Modes
Layer Type
All Layers
Enable All Basic Checks
Pad
Line
Pad
0.200
0.200
0.200
Pad
Line
Shape
0.200
0.200
0.200
Line
Shape
Shape

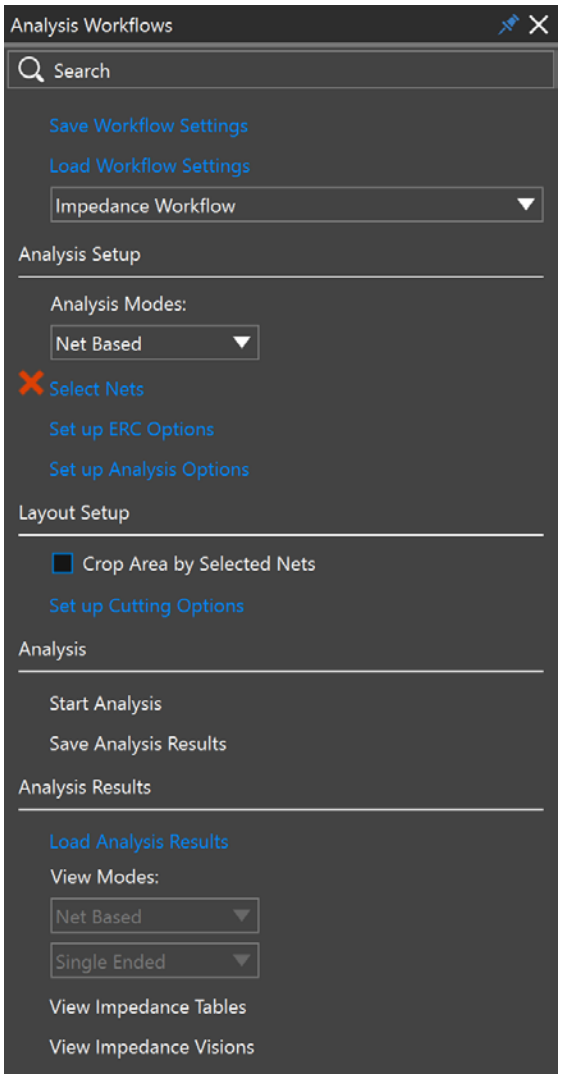
Board Simulation (Impedance and Crosstalk Analysis Using Sigrity X Aurora)

The entire purpose of proper constraint management is to make the hardware engineer/PCB designer adhere to design and requirement rules to avoid PCB re-spins.

While the Constraint Manager does an excellent task in managing constraints, simulation is the research tool that tells the Constraint Manager what rules need to follow.

In this section of the guide, we simulate to test and see how helpful the Constraint Manager is in ensuring we at least know when we are in and out of limits.

One of the simulations we can run is IR Drop analysis. To access the simulation features in Presto, go to **View – Panels – Analysis Workflows**.

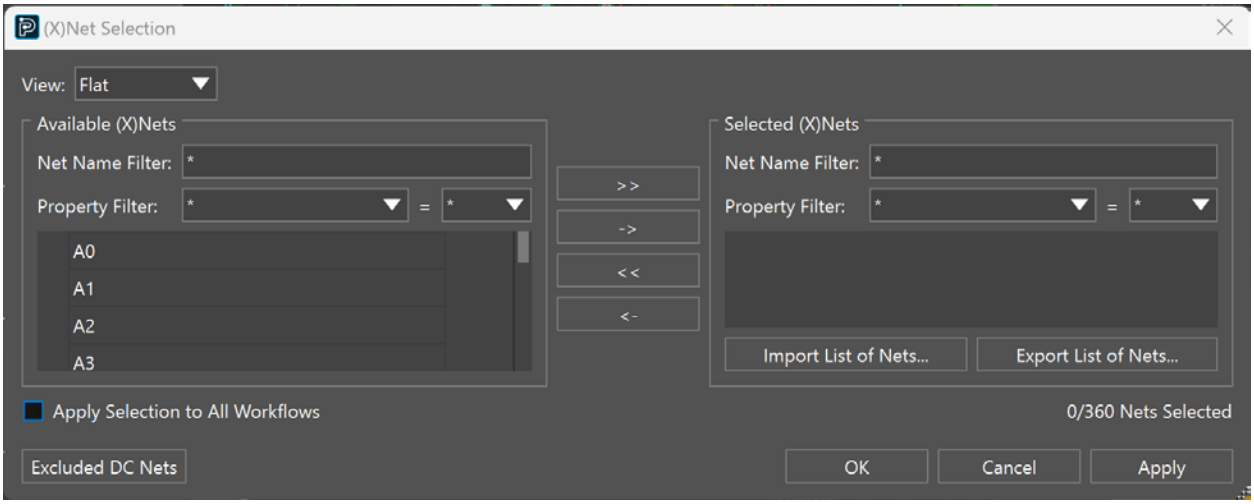


Note: To use these workflows, you need to have Cadence Sigrity X Aurora installed and it should also be the same version of OrCAD X you are using. For example, if you are using OrCAD X 24.1, then you should have Sigrity X Aurora 24.1 installed as a minimum requirement. You do not need a license for Sigrity X, however. OrCAD X just needs to use the Sigrity X tech stack to execute the simulation.

Impedance Workflow

Our first analysis will be the Impedance Workflow. To run the impedance workflow do the following:

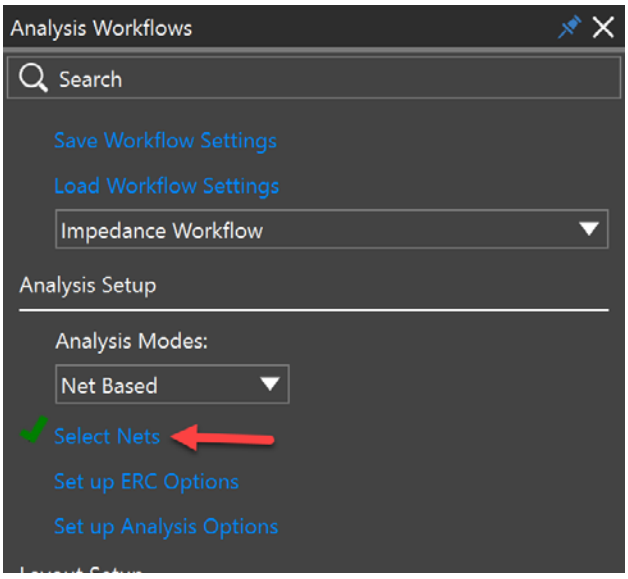
1. Choose Impedance Workflow.
2. Under Analysis Modes, select Net Based.
3. Below that, choose Select Nets.



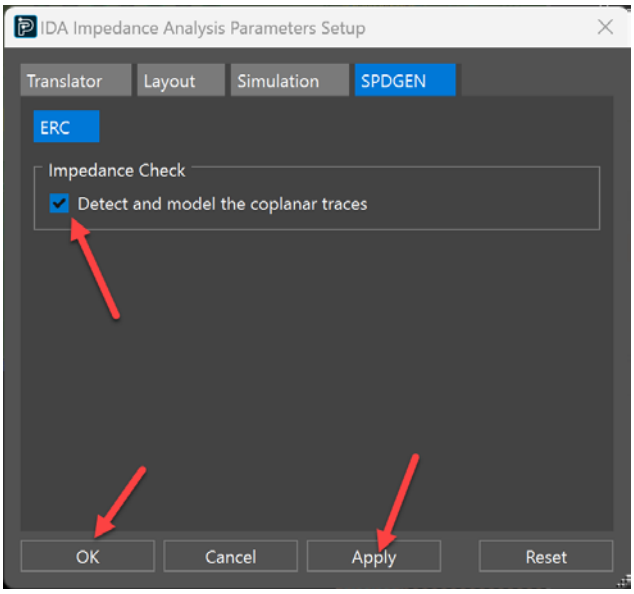
4. Select all the nets on the left (you can click one of the nets, then type Ctrl + A on your keyboard).
5. With all the nets highlighted, click the >> arrow to move all the nets to the right. This means we will analyze all the nets.

TIP: In most cases this is not necessary, and we can just add critical nets. The reason to choose fewer nets would be to help the software run more quickly, since simulation can be intensive for larger designs.

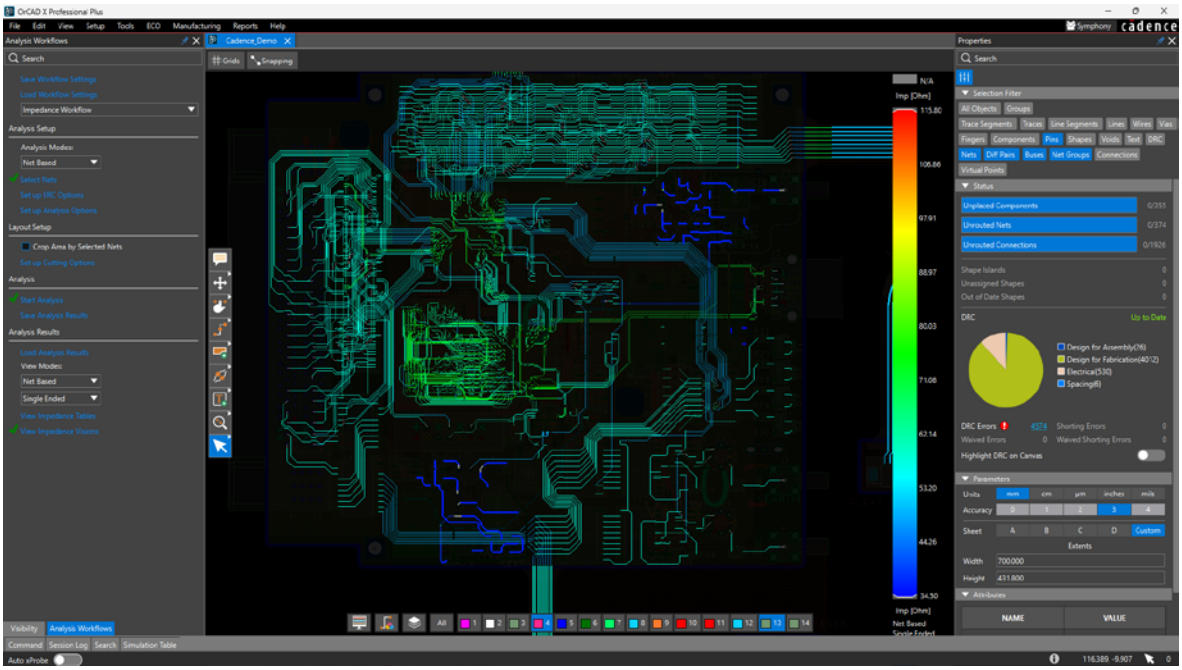
6. Click **Apply**, then **OK**. The Select Nets section will then have a check mark next to it.



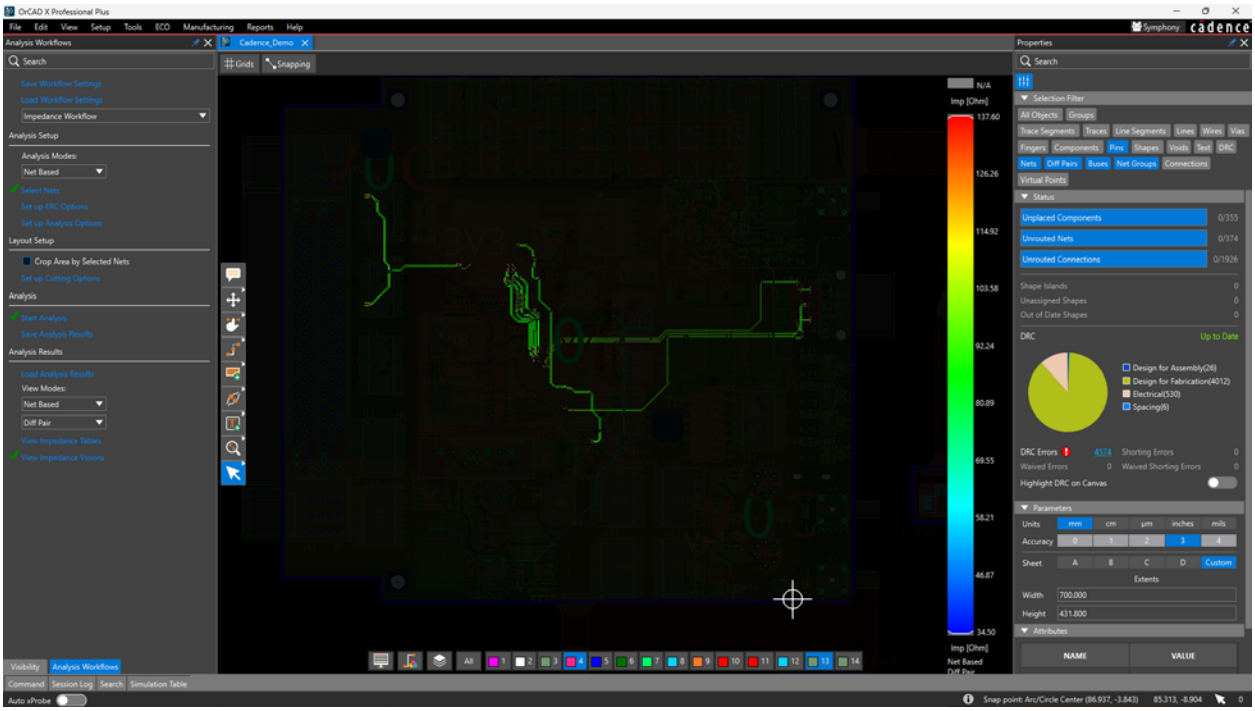
7. Click the “Set up ERC Options” text. In the new window, check **Detect and model the coplanar traces** if you want to include that. You can also activate the options across all tabs, but for now we will go with current settings (with **Detect and model the coplanar traces** enabled).
8. Click Apply then Ok.



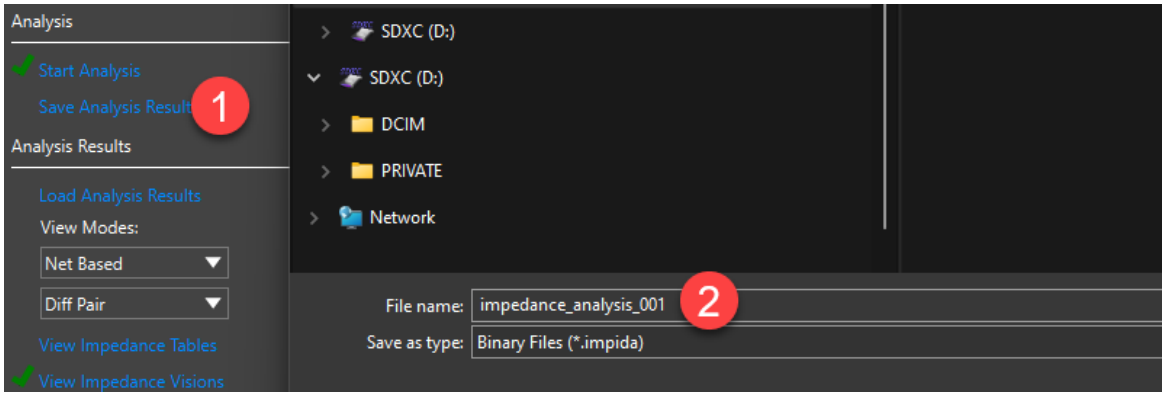
9. Then choose Start Analysis.
10. The analysis begins and the progress bar will increase to 100% when it is finished. It can take a few minutes, depending on the number of nets analyzed and the complexity of the PCB. Also, consider the different options you want for analysis. Don’t include more options than necessary. But if you select all options, that is fine, too.
11. When the simulation is complete, navigate to the lower left section of the **Analysis Workflows** Panel to select **Impedance View**.
12. Once selected, the board changes to shadow mode to highlight the nets on the board and all their impedances using a color scale.



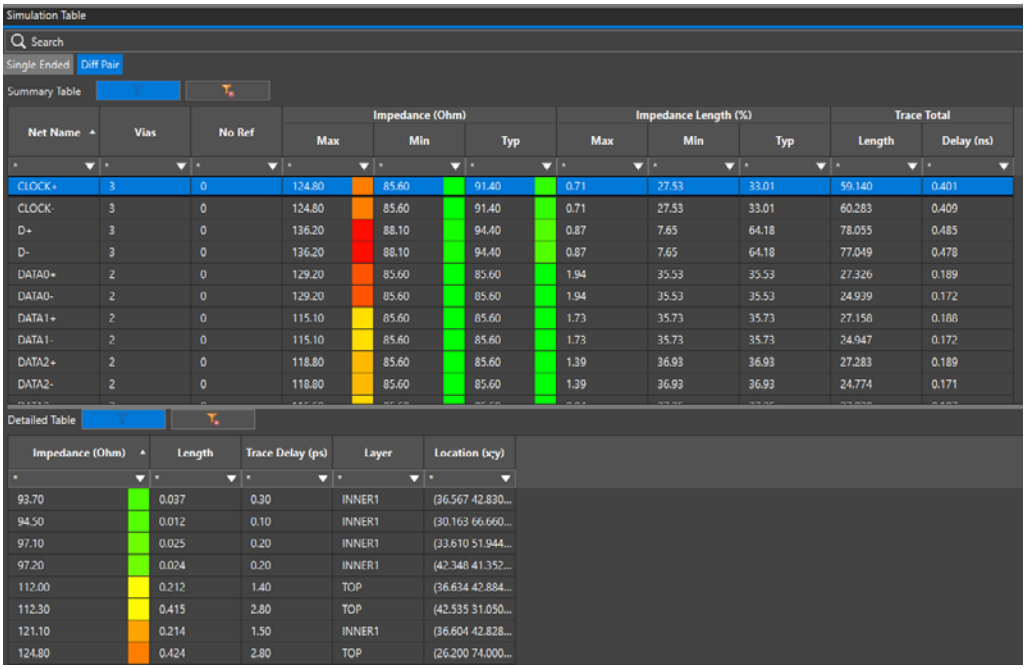
TIP: You can change the impedance view from single ended traces to differential pair traces by clicking under the Analysis Results section and selecting the dropdown where it says **Single Ended**. Change it to **Diff Pair**. Now the impedance trace view changes accordingly to show your differential pairs and their impedances from the color scale (see below).



Now you can adjust your routing and quickly simulate your design until your impedances are within acceptable limits for your design. There are more options to explore, but the most important is saving your results. To do that, click **Save Analysis Results**, then give the file a name and save it (see below).



TIP: The visualization is convenient to spot-analyze the results, but more detailed findings exist. Click the **View Impedance Tables** option within the Analysis Workflows panel, and you will get a full breakdown of all the traces and their impedances shown below.



Now you don't have to always use TopXplorer to find out whether your traces meet the impedance design requirements.

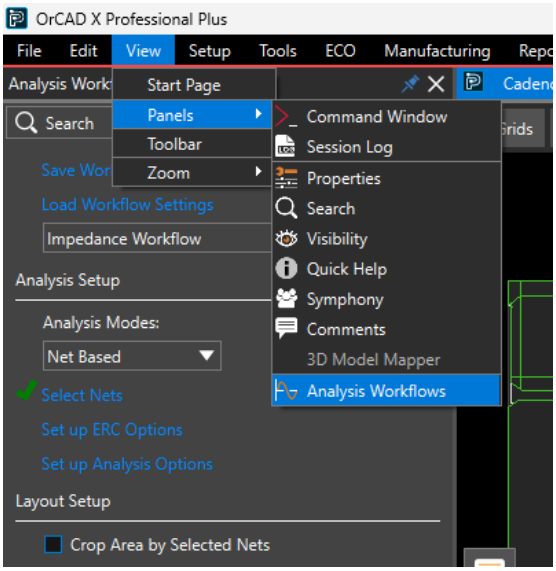
Next is coupling analysis to see how much crosstalk is on your traces, both visually and tabularly.

Coupling Analysis for Crosstalk

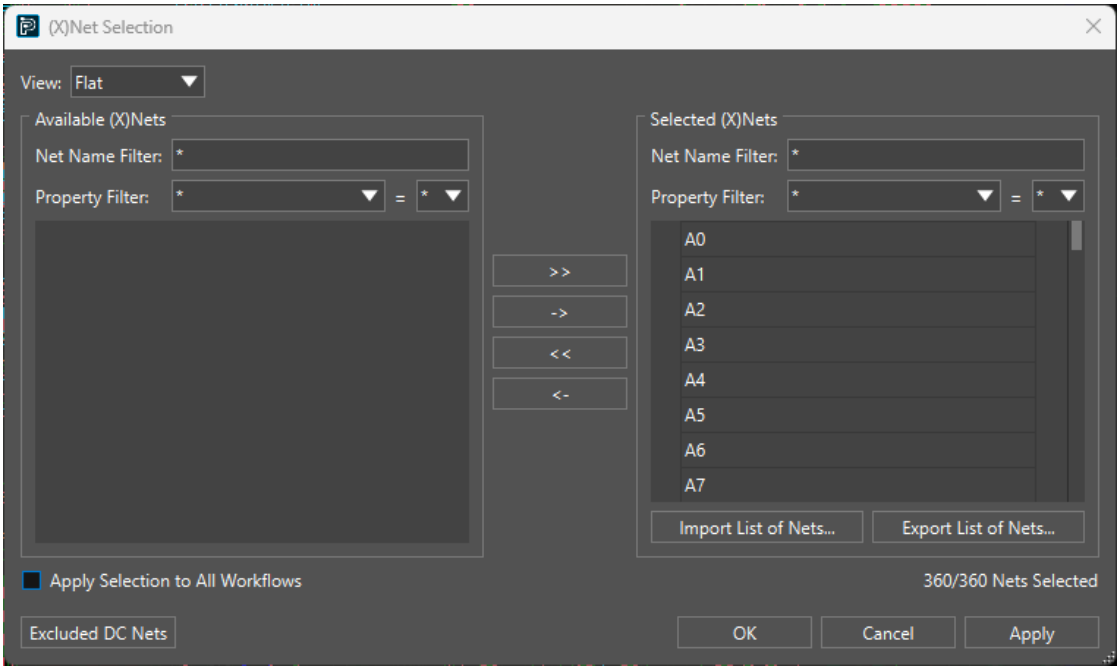
The next analysis we will look at is for coupling. Some traces can tolerate a certain level of coupling on them from aggressor traces before the signals are unacceptable. The coupling analysis provides tables and visual indicators of how much coupling and crosstalk are present on them at any time. That way, you can quickly test and iterate through your design decisions and adjust your routing accordingly.

To run coupling analysis do the following:

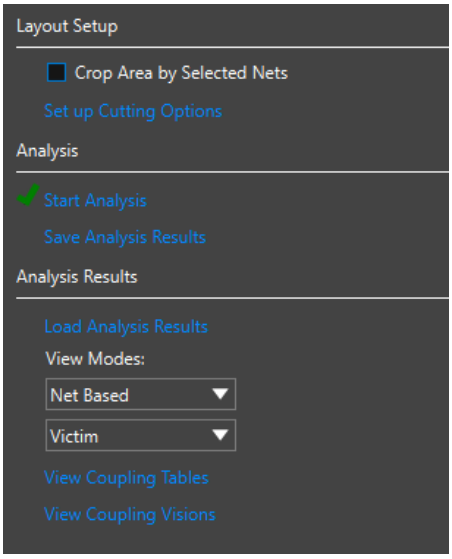
1. Go to **View – Panels – Analysis Workflows**.



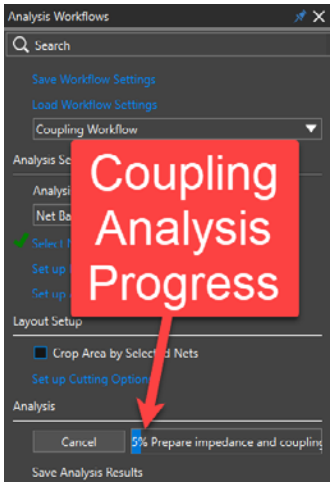
2. The Analysis Workflow panel is open. Select Coupling Workflow from the dropdown, keep the Analysis Modes on Net Based, then click the **Select Nets** option and you will get a pop-up window.



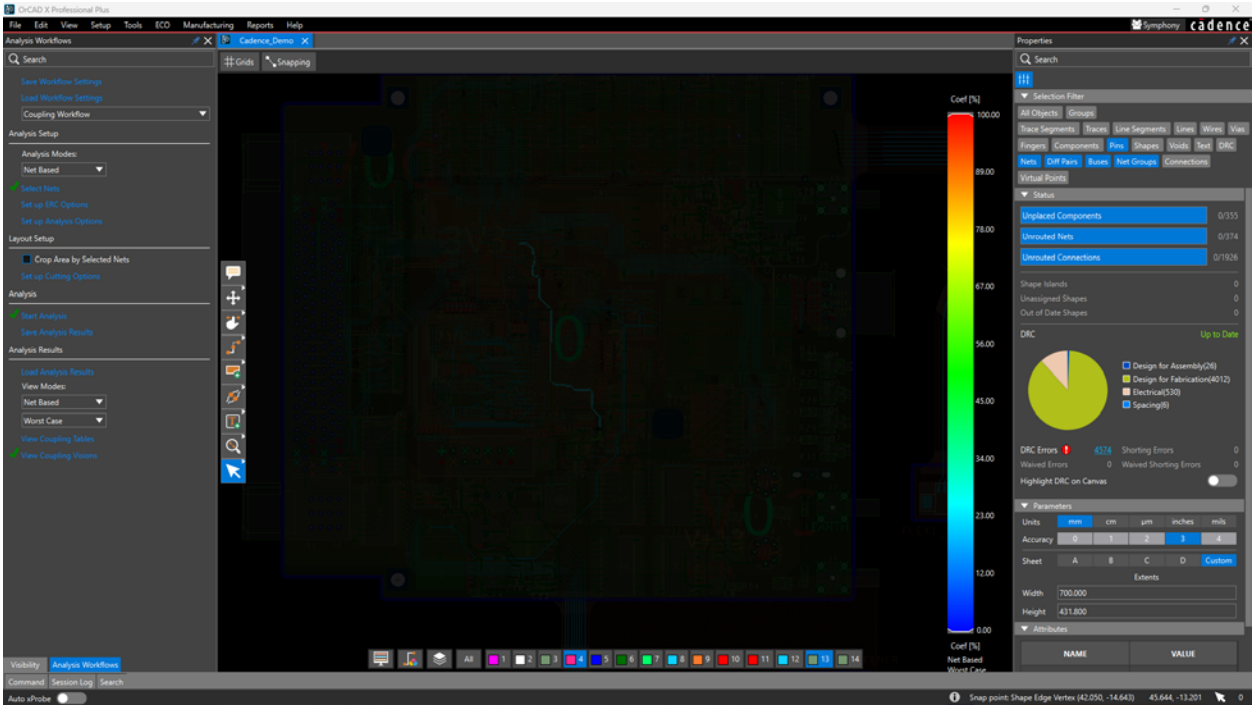
3. Select all the nets you're interested in analyzing, then click OK.
4. Within the Analysis Workflow panel, select Setup Analysis Options.
5. The **IDA Coupling Analysis Parameters Setup** window appears.
6. Choose any settings that apply to your design, then click **Apply**, then **OK**.
7. Click **Start Analysis**.



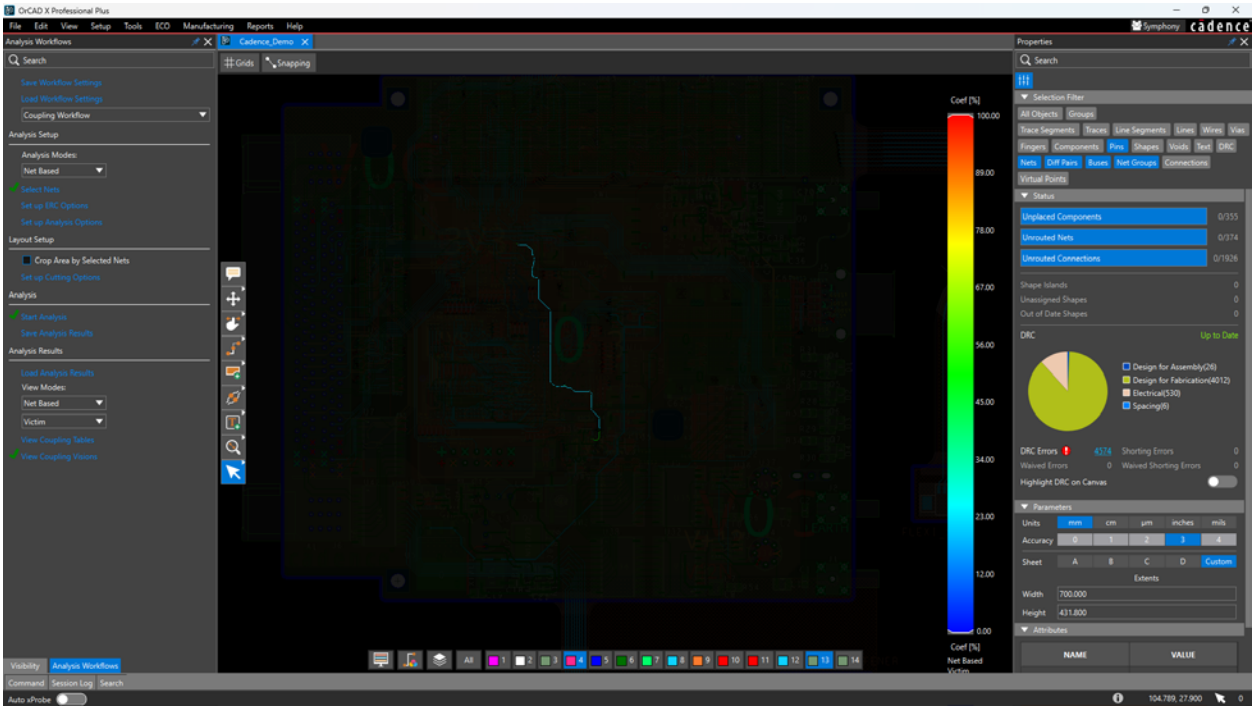
8. The coupling analysis begins and can simulate quickly or take a long time, depending on whether analysis was done prior to this step. In any case, the progress bar will let you know (see below).



9. Once finished, navigate to the Analysis Results section, then choose the option **Victim** or **Worst Case** and the views will change accordingly.

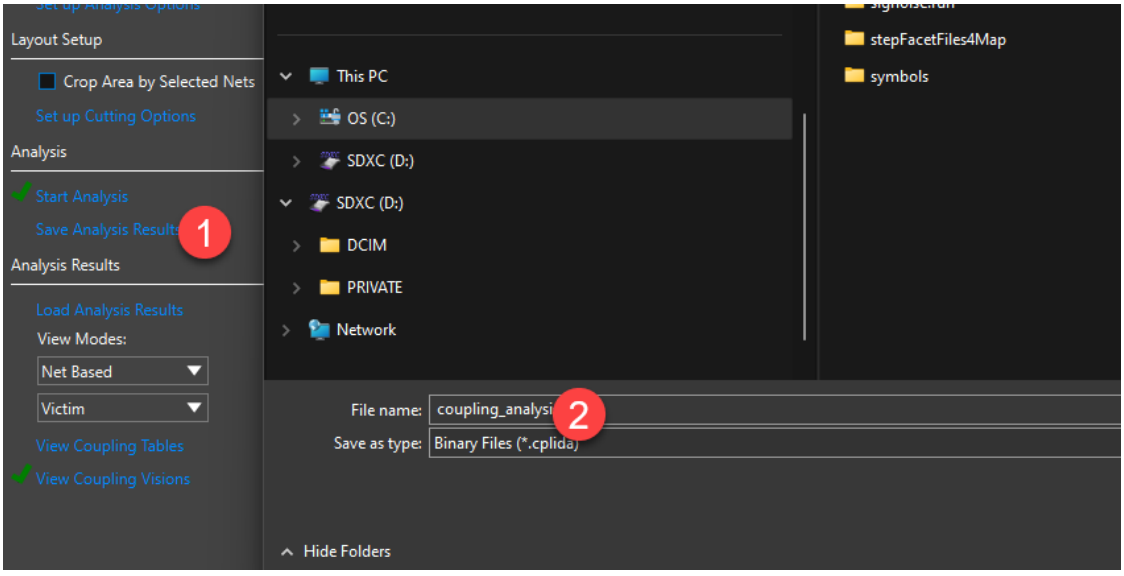


Worst case coupling view

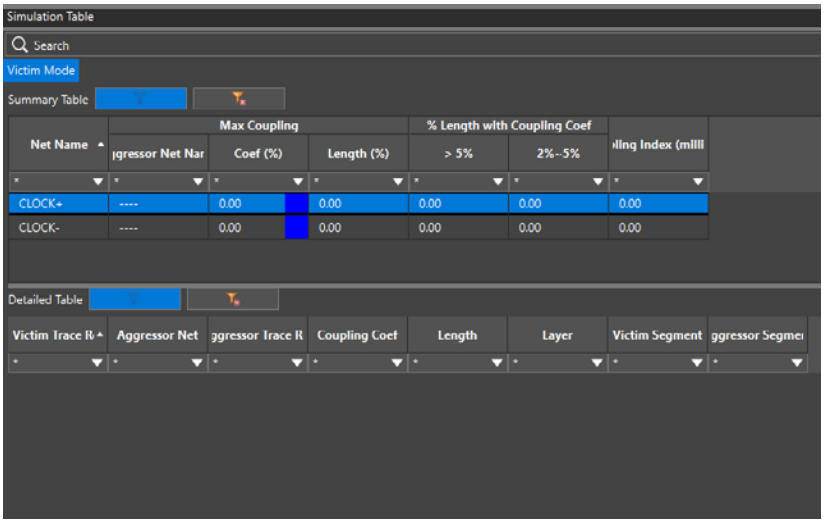


Victim trace coupling view

10. Save the results by clicking **Save Analysis Results** and giving the file a name, then clicking **Save** as shown below.



11. Your results get saved.
12. Before ending this mode, click the **View Coupling Tables** option in the image above and you will get the table shown below.



TIP: This feature is amazing, because you can make use of the table to uncover crosstalk issues before they show up as signal attenuation on the test bench!

Results

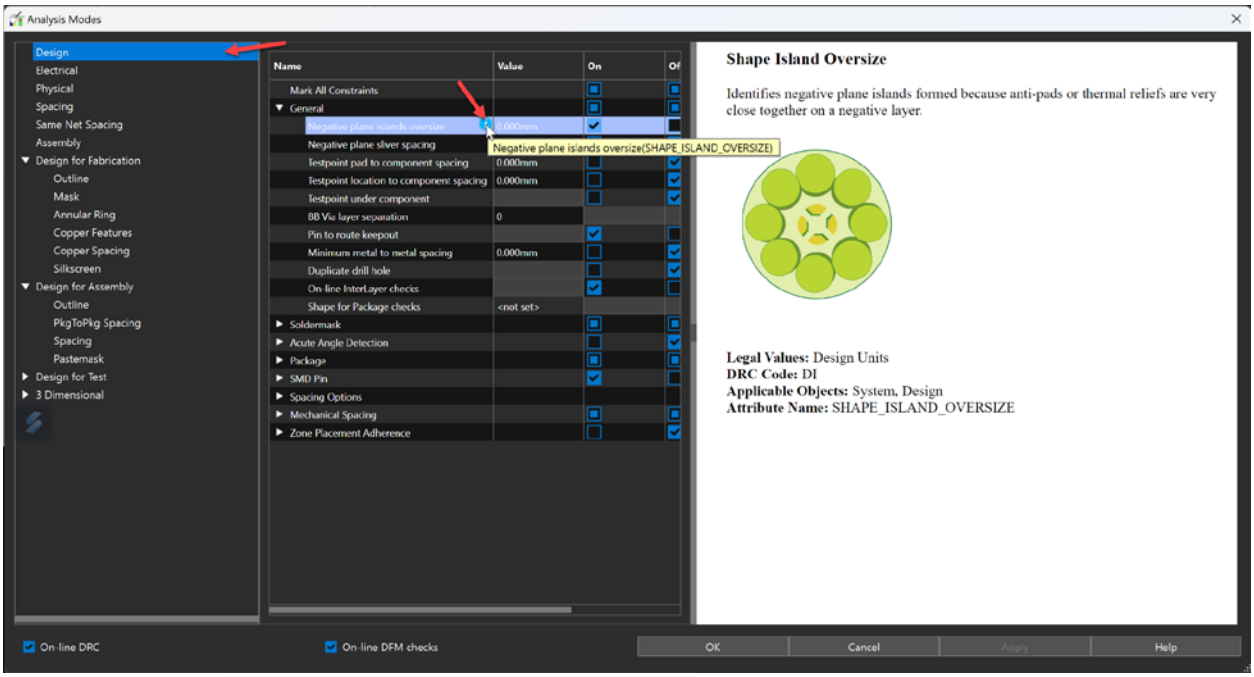
We have completed the design and due to proper constraint management, we have passed the design correctly using the constraints-driven approach to hardware and PCB design.

Conclusion of Part 5 - Project Example

In Part 5 of the OrCAD X Constraint Management Guide, we explored the practical application of constraints using the Cadence FPGA as a case study. This real-world example highlighted the importance of implementing and managing constraints effectively to ensure successful design outcomes. By demonstrating how to set, analyze, and verify constraints in both schematic and PCB layout, we provided a comprehensive overview of constraint management in a complex design environment equipping you with the knowledge and tools necessary to tackle modern PCB design challenges. By applying these principles, you can enhance the reliability, efficiency, and innovation of your PCB designs, ensuring they meet industry standards and project requirements. You also learned how to use the impedance and coupling workflows to quickly address signal integrity concerns on the fly. This power of analysis is extremely convenient because you won't have to be a signal integrity expert to get the job done. As you continue your design journey, remember that effective constraint management is key to unlocking the full potential of your PCB projects.

Appendix

The Constraint Manager has an immense library of constraints that it allows you to check for and not all constraints have been addressed. For a complete list of the constraints, in the Constraint Manager, choose the menu Analyze > Analysis Mode. A window will appear that shows all the constraints you can choose to analyze in your design.



The list is massive and provides visual aids and detailed explainer text to clarify what the constraint represents.