## DESIGN GUIDE

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## OrCAD X Constraint Management Guide

Part 5 of 5



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### Part 5 - Project Example in OrCAD X

In this part of the document, instead of walking you through the steps to execute each constraint set, we simply show you the constraints applied in the design and why. Let's look at the FPGA project that uses DDR2 and DDR3 memory.

Now that you know about constraint management in OrCAD X, the question remains, how do we implement constraints optimally from start to finish on a real design? In Part 5 we will guide you through utilizing the Constraint Manager from OrCAD X Capture to Presto PCB Editor to ensure you have a properly constrained design.

#### Hardware Design Project

Here is a picture of the project schematic shown below:



Figure 1. Project Schematic



Figure 2. 3D View of High-speed PCB assembly for Constraint Management Demo

#### Modern Hardware Design Process

- 1. Planning
- 2. Electronics Design
- 3. Components (selection, models, etc.)
- 4. Schematic Capture and Simulation
- 5. Constraint Management, Netlisting, and Bill of Materials
- 6. PCB Stackup and Signal Integrity Analysis
- 7. Constraints Management for PCB and Pre-routing
- 8. Component Placement
- 9. Wiring
- 10. Design Rule Checks and final touches

#### Organize the Nets

Identify nets that are suitable for net classes, net groups, and constraint regions.

#### **Define Net Classes**

At this stage the engineers have defined the net classes. To do that in OrCAD X Capture you would:

1. Open Constraint Manager from the main toolbar menu: PCB > Constraint Manager.



- 🎢 Constraint Manager (connected to CAPTURE) [DEMOJ] [Electrical / Net / Routing] File Edit Objects Column View Audit Tools Window Help To To TA To To To To -0 ≫ Ę Worksheet Selector 8 × DEMOJ Felectrical Objects Electrical Constraint Set Image: Signal Integrity Туре S Reflection/Edge Distortions \* Xtalk/SSN DEMOJ Dsn III Xtalk ADDRESS(24) NCIs Timing NCIs DATA(15) DATA[0..20](19) Bus Switch/Settle Delays Bus DATA1[0..9](10) Routing
- 2. Navigate to the **Electrical > Net > Routing > Wiring** worksheet.



 You will see all the nets listed in alphabetical order. Notice the name of the project DEMOJ and its row is labeled Dsn (DSN refers to the OrCAD X project file extension). Also notice the other rows are labeled as:

Net

DDR\_A6

- a. NCIs = Net Class
- b. Bus = Bus
- c. DPr = Differential Pair

Impedance

- d. XNet = Extended Net
- e. NGr = Net Group

- 4. These labels will help you to quickly identify the type of group or organization the nets are placed into.
- 5. Notice we have a net class named **DATA**(15) (it's named DATA but it has 15 members)



- 6. As shown in previous parts of the guide, you can create a net class by highlighting the nets you want in that class, then right clicking any of the highlighted nets, then choosing **Create Net Class**, naming that class then clicking OK.
- 7. That has been repeated to create the net classes shown below.

DEMOJ				
			Objects	
Туре	5		Name	Ret
*	*	*		*
Dsn	<u> </u>	8 🔺	Click a column to sort	
NCIs		8	alphabetically of numerically.	
NCIs		8	DATA(15)	
Bus		8	DATA[020](19)	
Bus	888888	8	DATA1[09](10)	
Bus	888888	8	DDS[010](11)	
Bus	888888	8	MEMORY[029](30)	
DPr	88888	8	CLOCK	ECS1
DPr		8	D D	ECS1

As shown in the first part of this document, Net Classes are often not enough to organize all our nets. Net Classes organize nets by physical and electrical properties, but oftentimes we also need to organize nets by function, regardless of their properties. Let's look at the Net Groups defined in this project.

#### **Define Net Groups**

We also need to define our net groups for the following (e.g. for HDMI, USB, DDR2, DDR3, or any important functional groups etc.) Within the Constraint Manager in OrCAD X Capture:

- 8. Go back to the **Electrical > Routing > Wiring** worksheet.
- 9. You will see all the nets in your design, along with their organizational labels (NCIs, DPr, etc.)

10. Let's create some net groups by right clicking a selection of nets, for example DQ0 – DQ7, then right click, choose **Create – Net Group...** 

DEMOJ									
		Objects				Торо	ology		
					Verify				Max
Туре	S	N	ame		Schedule	Sched	ule Actual	Margin	mm
	* *				*	*	*	*	*
NEL	20000000	DDK_DQ23					000000	1000000	
Net		DDR_DQ30							
Net		DDR_DQ31							
Net		DDS_CLK							
Net		DEN/							
Net	********	DHEN/							
Net		DI							
Net		DQ0							
Net		DQ1		Analyze					
Net		DQ2							
Net		DQ3		Select					
Net		DQ4		Deselect					
Net		DQ5	初.	F. 1					
Net		DQ6	~9	Find		Ctrl+F			
Net		DQ7		Bookmark		· · · · ·			
Net		DQ8							
Net		DQ9		Expand					
Net		DQ10		Expand All					
Net		DQ11							
Net		DQ12		Collapse					
Net		DQ13	_	Caraba			Chara		· · · ·
Net		DQ14 🥌		Create		· ·	Class		
Net		DQ15		Add to		•	Net Group.		
Net		D8		Remove			Differential	Pair	
Net		FPGA/					El control de		
Net		GAIN		Rename		F2	Electrical C	Set	
Net		HS/		Dulu		D.I		000000	-
Net		JTAG_D0		Delete		Del			
Whitet	X00000000	LED4		-			00000	1000000	

11. Then choose a name like NG1, then click **OK**. Typically, the default names work well for groups and classes.

etGroup:	NG1		
elections:			
Name	Туре	NetGroup	
DQ7	Net	NG1	
DQ6	Net	NG1	
DQ5	Net	NG1	
DQ4	Net	NG1	
DQ3	Net	NG1	
DQ2	Net	NG1	
DQ1	Net	NG1	
DQ0	Net	NG1	

12. Now you have a net group you can further create constraints (see below).

NGrp	MG1(8)
Net	DQ0
Net	DQ1
Net	DQ2
Net	DQ3
Net	DQ4
Net	DQ5
Net	DQ6
Net	DQ7
Ruc	

We will not create constraints here, but they will come in handy after all our groups, net classes and regions are set up. Next consider making a constraint region for the DDR2 and DDR3 devices.

#### **Decide On Constraint Regions**

In this schematic, we have memory modules and devices that will likely need special routing spacing. So let us make two constraint regions in preparation for that, even if we do not have to use them later.

- 1. Open the Constraint Manager in OrCAD X Capture.
- 2. In the constraint manager, go to **Physical > Region > All Layers**.

🎢 Constraint Manager (connected to CAPTURE) [DEMOJ] - [Physical / Region / All Layers]



We already have a region defined named BGA, but let's add DDR2 and DDR3 just in case we need special rules for those trace widths in that area of the PCB. In the image below, you can see the areas and chips where the BGA region would apply on the PCB.



Also, below you can see where the DDR regions we create will apply to the design.



Note: Physical region definition is for physical attributes only. We would need to create a region for spacing rules as well.

TIP: Recall that even though we have net classes and groups, we still need specific rules in certain parts of the PCB across different layers (or all) for that area sometimes so we can deviate from the default, class, and group net routing and spacing rules. Please refer to our complete section on Constraint Regions in a previous part of this guide.

3. To create a new Physical region, right click the cell named DEMOJ, Create - Region.

Flectrical			Objects			Line	Width	
+ Physical					Referenced Physica	I Min	Max	Min Wi
Y 📕 Physical Constraint Set	Туре	S	N	ame	Coct	mm	mm	mm
All Layers	*		•		•	*	•	*
🖩 By Layer	Dsn		d DEMOJ		DECAULT	0.000	<b>^.000</b>	0.150
🗸 📕 Net	Rgn	888888	BGA		Analyze			0.100
All Layers					Select			
🗸 📗 Region					Deselect			
All Layers				80	Deselect			
				-	Find	Ctrl+F		
					Bookmark	,	•	
-					Expand All			
			_	→ 🛯	Create	)	Class.	
					Add to	,	Regio	n 🔨 🔰
					Remove		Regio	n-Class
					D	50	Physic	al CSet

4. A Create Region window appears. Name the Region a relevant name, like DDR2 for example. Click OK.

Create Reg	ion		×
Region:	DDR2		
	Ok	Cancel	Help

Once that's done, your region will appear in alphabetical order with the other regions in the worksheet.

5. Repeat steps 3 through 4 to create a physical region named DDR3. You will then see the list of regions you created as shown below.



#### **Setting Spacing Regions**

Notice how the **Spacing** regions were automatically created in the Constraint Manager **Spacing - Region - All Layers** worksheet, like the Constraint Manager **Physical - Region - All Layers** worksheet.



🎢 Constraint Manager (connected to CAPTURE) [DEMOJ] - [Spacing / Region / All Layers]

File Edit Objects Column View Audit	Tools Wir	ndow He	lp		
X 🖡 🖡 🖏 -	<u> </u>	» <mark>&lt;</mark> (	<b>▼</b> <sub>6</sub> <b>▼</b> <sub>0</sub> <b>▼</b> <sub>4</sub> <b>▼</b> <sub>6</sub> <b>▼</b> <sub>8</sub>	🏹 🏹 😽 - 🦪	-
Worksheet Selector 🗗 🗙	DEMO1				
Flectrical			Objects		Li
+ Physical	Туре	s	Name	Referenced Spacing CSec	
Spacing     Spacing Constraint Set	*	*	*	*	*
All Lavers	Dsn	30000	DEMOJ	DEFAULT	0.200
By Laver	Rgn		BGA	BGA_SPACE	***
	Rgn		DDR2		
Net	Rgn		DDR3		
	Sp	ac	ing Reg	jions	
III Layers					

This region distinction is here to remind us that we need to define Physical constraint sets and Spacing constraint sets separately and add them as separate constraints onto physical and spacing net classes, groups and regions.

The overlapping constraint sets create a beautiful matrix of rules that make everything adhere to your requirements reliably, robustly and effortlessly.

Now that our groups, net classes and regions are set up, it is time to apply constraints to those objects.

#### Schematic Constraints Overview

In the modern hardware design process, constraint management must follow the design requirements, goals, features, and expectations for the product.

The constraints fallout from the signal integrity, power integrity, electrical, mechanical and electromagnetic requirements necessary for the product to be considered a success.

Notice on the schematic capture side, our Constraint Manager has some options for signal integrity requirements (such as signal reflections, edge distortions, etc.), crosstalk (Xtalk) performance, allowed simultaneous switching noise (SSN), and so on, while on the PCB side it does not.

Constraint Manager (connected to CAPTURE) [HS	D_FPGA] - [Electrical / Electrical Cons	straint Set / Signal I	ntegrity]			_	
File Edit Objects Column View Audit	Tools Window Help						- 8 ×
X 🖡 🖡 🖏 -	SigXplorer	T <sub>8</sub> T <sub>8</sub> T	s 🔨 🍝	- 🕗 - 📑 🗞	🍗 🍡 📲	× 🖬	0
Worksheet Selector & ×	Setup property definitions						$\sim$
5 Electrical	Precision		F	Reflection	Edge	Distortions	
Electrical Constraint Set	Options		Overshoot	Min Noise Margin	Edge	First Incid	ent
Signal Integrity	Update topology	ame	mV	mV	Sensitivity	Switch	
Keflection/Edge Distortions     Xtalk/SSN	Uprev topology		*	•	*	*	
T Xtalk	Customize Worksheets	A					
✓ Image Timing	Report	Fastur		Dorform	0000		
Switch/Settle Delays		Featur	es and	a Penorm	ance		
			Requir	ements			
Wiring			rtequii	emento			
Vias							
Impedance							
+ Physical							

In the modern hardware design process, the performance requirements are set at the design and schematic, not the PCB implementation phase, as that phase it is too late to think about signal integrity and performance.

In the following sections we create and apply as many of the rules (constraints) needed for the design to meet said requirements.

The main performance categories that we can constrain are electrical (e.g. impedance), physical (copper features like trace width), and spacing (e.g. distance from other objects to avoid EMC issues).

After that we will want to set some net properties as well.

These steps are all to facilitate the efficient execution of PCB layout for the PCB designer.

Counterintuitively, the more rules and restrictions we have, the easier it is to create and route a printed circuit board.

So, let's start with electrical constraints.

#### **Electrical Constraints**

In OrCAD X Capture let's set the electrical constraints to meet design needs.

Notice the Signal Integrity and Timing sections.

- 1. Skip these sections and go to the Electrical Routing Wiring worksheet.
- 2. Right click on the Dsn named DEMOJ Create Electrical CSet...
- 3. Give your constraint set a descriptive name like 'DDR3', then click OK.

The Constraint Manager lets you assign multiple electrical rules like the routing style, stubs lengths, parallel traces and layer sets. Set the following values as shown in the image below.

- 4. Once the DDR3 constraint set is created, click the cell under the Verify Schedule column and set it to Yes. This ensures that the constraints are checked during the routing process, which helps maintain signal integrity.
- 5. Set the Schedule to Daisy-chain. This routing pattern reduces the chances of signal reflections in the DDR3 topology by ensuring the signal terminates at the last DDR3 chip in the memory bank.

- Set Stub Length to 20 mils (0.508 mm). A shorter stub length reduces signal reflections, which is critical for maintaining signal integrity in high-speed designs. Depending on your design's signal propagation and rise times, stub lengths of 10, 20, or 30 mils may be acceptable.
- Set the Max Exposed Length to 1000 mils (25.400 mm). This value helps control the amount of potential electromagnetic interference (EMI) onto or emitted from the exposed traces. Adjust the Max Exposed Length based on specific design requirements to ensure optimal performance.



8. Set the Max Parallel value by clicking the cell. This will open up a new window.

		Objects			Topology		Stub	Max Exposed		
Туре	s	Name		Mapping Mode	Verify Schedule	Schedule	Length	Length	Max	Parallel
•		*		*			*	*		
)sn		DEMOJ		-						
CS		DDR3			Yes	Daisy-chain	0.508	25.400		-
ECS		ECS1			Yes	Daisy-chain				
			Co	onstraint: MAX_F	ARALLEL Im parallelism for v	vires				

9. Set the Length value in row 1 to 1500 mils (38.100 mm) and the Distance value in row 1 to say, 5 mils (0.127 mm), then click OK. Setting a limit to the distance that traces can run closely in parallel to each other limits crosstalk.

**TIP:** Crosstalk occurs when electromagnetic interference from one trace (the aggressor) affects a nearby trace (the victim), leading to unwanted noise and potential signal integrity issues in high-speed PCB designs. The amount of crosstalk increases with the parallel length of the traces, the distance between them, and the signal frequency, making it crucial to minimize parallel runs and maintain adequate spacing between traces to reduce this effect.

10. In the second row, let's consider traces that are closer together 4.2 mils (0.10668 mm). Those traces should not be allowed to run in parallel with each other as long as traces are 5 mils apart, because the coupling will be stronger from the smaller gap. Therefore, reduce the parallel length to 750 mils (19.050 mm). Please use the settings in the image below.

Parallel Segn	nents	×
Constraint: M Description: M Default Units: m Apply to:	AX_PARALLEL laximum parallelism for wire: m	s
Length:	Distance:	
38,100	0.127	Clear
	0.127	ОК
19.050	0.10668	Cancel
Length of tracks running parallel	Distance required between tracks	

- 11. Our last constraint is Layer Sets. Maybe we want to limit the DDR3 traces to only the top and bottom layers of the PCB for example (or TOP and INNER1 or BOTTOM and INNER2) to manage EMC and board capacitance. Click the Layer Sets cell, the Select Layer Sets window appears.
- 12. Click Define Layer Sets... The Define Layer Sets window appears. Then click Create.
- 13. Now name the layer set. For example, choose 'LS1'.

	054	u te		Topology					
				Verify		Stub Length	Max Exposed Length	Max Parallel	Layer Set
Type		Name	Mapping Mode	Schedule	Schedule	mm	mm	mm	
	• 🖡 S	elect Layer Sets					×	•	•
n									
s								0.000:0.000:0.0	-
i	Filter	:		Filter:					
		-	Create LayerSet: LSI	Ok Cancel	Create Dalata Cancel Help	Help			
		fine Layer Sets			OK	Cancel	Help		

14. Then the LS1 (No layers defined) list will appear, and you can click the arrow to expand the list.

Define Layer Sets	×
LS1 (No layers defined) TOP	
	Create
	Delete
Воттом	
OK Apply Cancel	Help

15. Select the checkboxes for the **TOP, GND, POWER,** and **BOTTOM** layers (see below). Click **Apply** then **OK**.

Define Layer Sets	×
<ul> <li>LS1 (No layers defined)</li> <li>TOP</li> <li>GND</li> <li>INNER1</li> <li>INNER2</li> <li>POWER</li> <li>BOTTOM</li> </ul>	Create Delete
OK Apply Cancel	Help

16. You'll be taken back to the Select Layer Sets window. Choose the LS1 item, then click the > arrow to move it to the right column, then click OK.

Select Layer Sets		×
Filter:	Filter:	
	,	
	4	
	>	
Define Layer Sets		OK Cancel Help

Now the DDR3 signals will not be allowed onto the layers INNER1 or INNER2. You may change these layer sets at any time.

17. Let's add more constraints to this DDR3 ECSet, like Vias – Max Via Count = 2, Impedance, Propagation delays, Total Etch Length, Differential Pair parameters, Relative propagation delay and Return Path.

Please see the images below for those values in the constraint set.

#### Max Via Count



#### Impedance

Worksheet Selector & X	DEMO1				
5 Electrical			Objects	Single-lir	ne Impedance
Y Electrical Constraint Set				Target	Tolerance
✓ Image Signal Integrity	Туре	S	Name	Ohm	Ohm
Reflection/Edge Distortions	*	*	*	•	*
Xtalk/SSN	Dsn		DEMOJ		
III Xtalk	ECS		DDR3	50	2 %
✓ Image Timing	ECS		ECS1	50	2%
Switch/Settle Delays					
✓ mathematical Routing					
III Wiring					
🛄 Vias 🥒					
Impedance 🌽					

#### Min/Max Propagation Delays



#### **Total Etch Length**



#### **Differential Pair Parameters**



#### **Relative Propagation Delay**

No entries are possible in the Electrical Constraint Set > Routing > Relative Propagation Delay worksheet.



#### **Return Path**

By clicking the options shown below, you can set the GND EARTH net as the return path for your DDR3 **Electrical Constraint Set** and clicking Ok.



Then fill in the rest of the details shown below:

- Reference Net(s) GND EARTH
- Reference Layer(s) Closest Plane
- Length Ignore 25 mils (0.635 mm)
- Max Pad Gap 10 mils (0.254 mm)
- Max Stitch Via Distance 20 mils (0.508 mm)
- Adjacent Void Spacing 60 mils (1.5 mm)

These values assume transfer rates in the 3.5 GHz to 5 GHz ranges and 10 picoseconds to 30 picosecond signal rise times.



**Note**: The **Max Stitch Via Distance** is a rule that defines the distance at which a return path via should be present from a via of the scoped signal (see image below).



- Apply these rules into your constraint set DDR3, then apply the constraint set to your nets by opening the Electrical > Net > Routing > Wiring worksheet.
- 19. Now let's apply the **Electrical Constraint Set (ECSet) DDR3** to the nets **DDR\_DQ0** through **DDR\_DQ7**. Click, drag, and highlight those nets. Right click on any of the highlighted net row names, then **Create Net Group**. Select the net name, then Click Ok.



20. Now you have a net group (named NG2(8)) where you can apply any constraint set you want. Apply the DDR3 constraint set by clicking on the **Referenced Electrical CSet** cell for the NG2(8) group (see below).

Constraint Manager (connected to CAPTL	IRE) [DEMO	I] - [Elec	trical / Net / Routing]																0
	Audit			. ▼⊛ ▼⊚ ▼⊜	₹ €	- 🛞 -	=_ «	6	° <b>o</b> II	<b>.</b>	<b>=</b> Q								-
Worksheet Selector 🗗 🖉	DEMO	21																	F
5 Electrical			Objects			Topolog	IV.			Stub Leng	th	Ex	posed Ler	ath	Par	allel		Law	er Sets
<ul> <li>Timing</li> <li>Switch/Settle Delays</li> </ul>	Туре	s	Name	Referenced Electrical CSet	Verify Schedule	Schedule	Actual	Margin	Max	Actual	Margin	Max	Actual	Margin	Max	Actual	Margin	Name	Actual
✓ I Routing			•																•
III Wiring	Den	0000						-	-	-	-	-	-	-	-	_	-		
III Vias	NCk	0000	ADDRESS(24)		-		00000		-	00000			000000			100000		-	00000
Impedance	NOS	12222	DATA(15)	-						100000						100000		-	10000
Hin/Max Propagation	NGro	10000	D NG1(8)				100000	0.000		100000	100000		100000	100000		100000	10000		10000
min/max Propagation	NGrp		MG2(8)	DDR3	Yes	Daisy-chain			0.508			25.400			0.000:0.000:0.00			LS1	
lotal Etch Length	Net	22223	DDR_DQ0	DDR3	Yes	Daisy-chain	88888	100000	0.508	100000		25.400	22222	XXXXX	0.000:0.000:0.00	000000	00000	LS1	
Differential Pair	Net	8888	DDR_DQ1	DDR3	Yes	Daisy-chain	×***		0.508	88888		25.400	XXXXX	200000	0.000:0.000:0.00	000000	00000	LS1	2000
Relative Propagation D	Net	8888	DDR_DQ2	DDR3	Yes	Daisy-chain	288888	1000000	0.508	200000	0000000	25.400	200000	200000	0.000:0.000:0.00	222222	88880	LS1	20000
E Return Path	Net	8888	DDR_DQ3	DDR3	Yes	Daisy-chain	88888	100000	0.508	188888	100000	25.400	88888	100000	0.000:0.000:0.00	22222	22222	LSI	2000
> I All Coortraints	Net	8888	DDR_DQ4	DDR3	Yes	Daisy-chain	88888		0.508	88888		25.400	88888	XXXXX	0.000:0.000:0.00	88888	8888	LS1	10000
All constraints	Net	8888	DDR_DQ5	DDR3	Yes	Daisy-chain			0.508	22222		25.400	2000	22222	0.000:0.000:0.00		20000	LS1	2000
V Net A	Net	8888	DDR_DQ6	DDR3	Yes	Daisy-chain	20000	100000	0.508	200000	0.0000	25.400	200000	200000	0.000:0.000:0.00	200000	20000	LS1	20000
<ul> <li>Image: Signal Integrity</li> </ul>	Net	8008	DDR_DQ7	DDR3	Yes	Daisy-chain	222223	100000	0.508	200000	000000	25.400	100000	100000	0.000:0.000:0.00	000000	00000	LS1	2000
Electrical Properties	Bus		DATA[020](19)																20000
E Reflection	Bus	XXXX	DATA1[09](10)				200000	<u>p</u>	1	- POCOCO	<u></u>		20000	200000		0.0000		4	20000
Edus Distantions	Bus	20000	DDS[010](11)				200000	200000		200000	2		200000			200000		-	200000
Enge Distortions	Bus		MEMORY[029](30)					P	-		<u></u>		×****			22222		4	
Estimated Xtalk	DPr			ECS1	Yes	Daisy-chain												-	20000
III Simulated Xtalk	DPr		D D	ECS1	Tes	Daisy-chain		1	-	0.0000						200000		-	
III SSN	DPr	0.000	DP_DATAD	ECST	Tes	Daisy-chain	00000	0.0000		00000						00000		-	0.000
× 🖻 Timina	DPT	0.000	DP_DAIA1	EGI	Tes	Daisy-chain			-									+	
Cuitch /Sattle Dalaus	DPr	0000	DP_DATA2	6054	Vec	Dainy chain	00000	00000		00000	0.000		0.000			000000		-	00000
EE Switch/Settle Delays	DPT	0000	DP1	ECS1	Vec	Daisy-chain	00000	100000		00000	1		00000			00000	00000	-	00000
E Setup/Hold (Common	DPr	00000	STDA SSPY	ECSI	Yec	Daisy-chain	00000			00000						00000		-	00000
Y 🔚 Routing	DPr		D STDA SSTX	FCS1	Ves	Daisy-chain	0.000	10000		0.000								-	0.000
III Wiring	Net	0000	AFN/			Contraction of the second	00000			00000						00000		-	00000

Now that you know how to create constraint sets and apply them to your nets, we will only show the constraint sets that can be created.

We'll show how to apply the constraints to your nets in the Physical and Spacing and Same Net Spacing sections of the OrCAD X Capture Constraint Manager tool.

We'll also show the Properties section of the Constraint Manager tool.

After that, we will look at the Constraint Manager on the PCB Editor side in OrCAD X.

#### **Physical Constraints**

Here is an example of the physical constraint sets created within Constraint Manager.

#### **Physical Constraint Set**

😭 Constraint Manager (connected to CAPTURE) [DEMO/] - [Physical / Physical Constraint Set / All Layers] - 🗖													o x		
File Edit Objects Column View Au	idit Tool	s W	findow Help												_ 8
8 🖡 🖗 🍢	~	, ,	<mark>  0   0  </mark> 0   0   0   0   0   0   0   0	0 TA T® 1	6 🍾	┓ (	<b>-</b> 🖗 -	5	10 °0 👘	o: 🔚 💽					
Worksheet Selector & X	DEMOJ														
5 Electrical			Objects		Line	Width	N	ock			Differential Pair			1	Vilow
+ Physical		_		Referenced Physical CSet	Min	Max	Min Width	Max Length	Min Line Spacing	Primary Gap	Neck Gap	(+)Tolerance	(-)Tolerance		-
Physical Constraint Set	Type	2	Name	,	mm	mm	mm	mm	mm	mm	mm	mm	mm	Etch	IS
All Layers	•	•	•		•	•	•	•	•	•	•	•	•	•	•
By Layer	Dsn	200	DEMOJ	DEFAULT	0.200	0.000	0.150	2.500	0.000	0.000	0.000	0.000	0.000	TRUE	ANYWHERE
🗸 📒 Net	PCS	888	DEFAULT		0.200	0.000	0.150	2.500	0.000	0.000	0.000	0.000	0.000	TRUE	ANDAGEDE
All Lavers	PCS 📻		DIFF1		0.127	0.000	0.100	5.000	0.107	0.127	0.117	0.010	0.010	TRUE	ANYWHERE
Realer	PCS	2000	POWER		0.500	0.000	0.200	7.000	0.000	0.000	0.000	0.000	0.000	TRUE	ANYWHERE
* Kegion	PCS	888	RF		0.500	0.000	0.200	5.000	0.000	0.000	0.000	0.000	0.000	TRUE	ANYWHERE
I All Layers															

#### Applied Constraint Set

Here is where you apply the constraints (see image below).

File Edit Objects Column Vie	w Audit Tools	Window	Help								
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Norksheet Selector	X DEMO1										
Electrical			Objects		Line	Width		leck	Static Phase	Differential Pa	ir
+ Physical				Referenced Physical	Min	Max	Min Width	Max Length	Tolerance	Referenced Intra	DP
Y 📒 Physical Constraint Set	Туре	5	Name	CSR	mm	mm	mm	mm	mm	Spacing CSet	1
All Layers	•	•	-	•	•			•		•	
By Layer	Dsn	000000	A DEMOJ	DEFAULT	0.200	0.000	0.150	2.500			_
Net 🥒	NCIs	0.0000	POWER_GROUP(10)	POWER	0.500	0.000	0.200	7.000			
All Lawrence	NCIs	5	RF(21)	RF	0.500	0.000	0.200	5.000			
All Layers	NCIs		STEVE_PH(9)	DEFAULT	0.200	0.000	0.150	2.500			
Region	NGrp	000000	> NG1(8)	DEFAULT	0.200	0.000	0.150	2.500			
All Layers	NGrp	000000	> NG2(8)	DEFAULT	0.200	0.000	0.150	2.500	20 ps		
	Bus	000000	DATA[0_20](19)	DEFAULT	0.200	0.000	0.150	2.500			_
	Bus	000000	DATA 1[09](10)	DEFAULT	0.200	0.000	0.150	2.500			
	Bus	200000	DDS[010](11)	DEFAULT	0.200	0.000	0.150	2.500			
	Bus	200000	MEMORY10_291(30)	DEFAULT	0.200	0.000	0.150	2.500			
	DPr	_	A CLOCK	DIFF1	0.127	0.000	0.100	5.000	6 mm		
	Net	000000	CLOCK+	DIFF1	0.127	0.000	0.100	5.000	6 mm		
	Net	200000	CLOCK-	DIFF1	0.127	0.000	0.100	5.000	6 mm		
	DPr	2000000	a D	DIFF1	0.127	0.000	0.100	5.000	6 mm		
	XNet	500000	D+	DIFF1	0.127	0.000	0.100	5.000	6 mm	2	
	XNet	000000	D-	DIFF1	0.127	0.000	0.100	5.000	6 mm	S	

#### **Spacing Constraints**

Here are the spacing constraint sets created for the design (shown below). There is a spacing constraint set for the BGAs in the design, called BGA\_SPACE. Then there is the DEFAULT constraint set for the entire design in general.

#### Spacing Constraint Set

🎢 Constraint Manager (connected to CAPTURE) [	[DEMOJ] - [Spa	icing / Spa	cing Constraint Set / All Laye	[5]								-	0	$\sim$
📕 File Edit Objects Column View Au	dit Tools \	Window	Help											- 8
84 🖪 🖗 🤷	<u> </u>	<mark>•</mark> • •		la 🖌 🖌	- 💮 -	to 🗞 🦰	°o "o 🔅	: 🖫 🍳						
Worksheet Selector & X	DEMOJ													
5 Electrical			Objects		Line To	Thru Pin To	SMD Pin To •	Test Pin To •	Thru Via To 🔸	BB Via To	Microvia To	Test Via To	Shape T	o #
+ Physical				eferenced Spacing CSet	All	All	All	All	All	All	All	All	All	
1 Spacing	Type	\$	Name		mm	mm	mm	mm	mm	mm	mm	mm	mm	
Y Spacing Constraint Set	•	-										-	-	
All Layers	Dsn		d DEMOJ	FAULT	0.200	0.200	0.200	0.200	0.200	0.200	0.200	0.200	0.200	200
By Laver	SCS		▲ BGA_SPACE								0.127			
	СТур		Conductor						•••		0.127			
• Net	СТур	2006-000	Diane					•••	•••	•••	0 127			
All Layers	scs		▲ DEFAULT		0.200	0.200	0.200	0.200	0.200	0.200	0.200	0.200	0.200	
V Net Class-Class	СТур	200000	Conductor		0.200	0.200	0.200	0.200	0.200	0.200	0.200	0.200	0.200	
All Layers	СТур	2000000	Plane		0.200	0.200	0.200	0.200	0.200	0.200	0.200	0.200	0.200	

#### Applied Constraint Set

As expected, the default constraint set is applied to most of the nets in the design.

🞢 Constraint Manager (connected to	CAPTURE	[DEMOJ] - [Spa	acing / Net	/ All Layers]			
File Edit Objects Column	View A	udit Tools	Window	Help			
8 🖡 🖡 🗛		~ 📈	<b>N N</b>	- To To To To To To To Co	• 🕗 • 📑 🗞	🍾 🗢 🛛	• ÷
Worksheet Selector	đΧ	DEMO1					
Flectrical				Objects		Line To	Thru
+++ Physical		-			Referenced Spacing CSet	All	
1 Spacing		Type	S	Name		mm	r
Spacing Constraint Set		*	*	*	*	•	*
All Lavers		Dsn		🖉 🔟 DEMOJ	DEFAULT	0.200	0.200
By Laver		NCIs	8 8 8 8 8 8 8	POWER_GROUP(10)	DEFAULT	0.200	0.200
im by Layer		NCIs	8 8 8 8 8 8 8	RF(21)	DEFAULT	0.200	0.200
V Net		NCIs	8 8 8 8 8 8 8	STEVE(1)	DEFAULT	0.200	0.200
🔚 All Layers 🥌		NGrp	8 8 8 8 8 8 8	NG1(8)	DEFAULT	0.200	0.200
V Net Class-Class		NGrp	8 8 8 8 8 8 8	NG2(8)	DEFAULT	0.200	0.200

Notice that our region-based constraint set is applied to the Regions worksheet in a specific BGA region instead of being applied to various nets.



**Note:** There are spacing regions for the DDR2 and DDR3 devices, but we have not created spacing constraints for either of these devices since they're using SOIC packaging instead of BGA packaging. Upon inspecting the pin sizes for the SOIC packaging, we don't need to adjust the default spacing or physical settings for our traces.

#### **Electrical Properties**

Within the Constraint Manager, we can assign properties and values to specific nets. This feature is extremely useful for doing PCB layout simulations (e.g. power IR drop analysis, signal integrity transmission line simulation). See the image below to find the electrical properties section.

onstraint Manager (connected to CAPTURE	) [DEMOJ]	] - [Proj	perties / Net / Electrical Properties]									- 0	×
File Edit Objects Column View	Audit To	ols \	Window Help									-	8
84 🖡 🖡 🍇	v		😼 😼 🐨 🐨 🐨 💊	🌄 🍝 - 🛞 -	=_ % ^	<b>0</b> II.	× 🖬 🔍						
Worksheet Selector 🖉 🗙	DEMO			,			_				1		
5 Electrical			Objects								•		Ť.
+ Physical				Referenced Electrical	Frequency	Period	Duty Cycle	Jitter	Cycle to	Offset	Bit	Library/Model	
1 Spacing	Type S Name		Name	C.A.	MHz	ns	%	% ps		ns	rattern	DiffPairs	
1 Same Net Spacing	•	•	•	•	•	•	•	•	•	•	•	•	1
Properties	Dsn		ADDRESS(24)										41
🛩 📒 Net 🛛 🥒	NCIS		DATA(15)										11
Electrical Properties	NGrp		▲ NG1(8)									0	Į.
General Properties	Net		DQ1										ŝ
Route/Vias Keepout Exception	Net		DQ2									0	<u>2</u> -
Component	Net		DQ3 DQ4										£
General	Net		DQS									0	£
Pin Properties	Net	0000	DQ6 DQ7										ŝ
General	NGrp	00000	▲ NG2(8)	DDR3								-	1
	Net	0000	DDR_DQ0	DDR3								<u>U</u>	4

Notice that in the **Properties > Net > Electrical Properties** worksheet, you can set so many parameters:

- Frequency (the rate of pulses per second on a net. Also, the inverse of the Period)
- Period (the time between when a signal repeats itself. e.g. the time from the beginning of one pulse to the beginning of the next pulse)
- > Duty Cycle (the length of time a pulse on the net will be high within the signal period)
- > Jitter (the amount of jitter expected on the trace for that net)
- Bit Pattern (this is the signal pulses that are expected on a net, such as 01011001)

Then, in the **General Properties** section, we already have voltages set for some of the nets (see image below). Setting voltages helps assist circuit simulation for impedance drops and signal integrity analysis.

Properties	Net	N2993541	
/ Not	Net	PGOOD	
	Net	Q1E	
Electrical Properties	Net	Q2E	
🔚 General Properties 🚄	Net	RDY/	
Route/Vias Keepout Exception	Net	RESET	
Component	Net	RESET/	
Component	Net	SEL	
<ul> <li>Component Properties</li> </ul>	Net	SHIELD1	1.5V
I General	Net	SHIELD2	1.5V
Pin Properties	Net	STDA_SSRX+	
General	Net	STDA_SSRX-	
	Net	STDA_SSTX+	
	Net	STDA_SSTX-	
	Net	TCLK	
	Net	TDO	
	Net	TMS	
	Net	V+12	1.5V
	Net	VCC VCC	1.5V
	Net	VCLKC	
	Net	VDX0	
	Net	VDX1	
	Net	VDX2	
	Net	VDX3	
	Net	VDX4	
	Net	VDX5	
	Net	VDX6	
	Net	VDX7	
	Net	VTTREF	
	Net	V12N	1.5V
	Net	WAIT/	
	Net	0	OV
	Net	0V9	0.9V
	Net	XXX 1V2	1.2V
	Net	1V8	1.8V
	Net	2V5	2.5V
	Net	3V3	3.3V
	Net	SV 5V	5V

The remaining worksheets, such as Component > Component Properties > General and Component > Pin Properties > General, are not set.

This concludes the schematic side of the constraint manager and its use. Now we will push these constraints to the PCB layout side to maintain project integrity.

After that, we will simply review the constraints found in the PCB layout for our demo board.

- Within the Constraint Manager worksheet, Create a Constraint Set that you will apply later.
- Apply that Constraint Set to a class, group or region in your design.
- Repeat similar steps for all kinds of constraints (Physical, Electrical, Spacing, Manufacturing and so on).

#### PCB Constraints Overview

The same constraint manager that is available within OrCAD X Capture also exists within OrCAD X Presto PCB Editor. To find it:

- 1. Close the current Constraint Manager in Capture. Constraints are saved instantly so there is no need to save it.
- 2. Navigate to the Capture project file hierarchy and you should have your board design file as part of your project (see image below).



3. Select the board file, then update the board by clicking Menu PCB - Update Layout.



4. The Update Layout window will appear.

II Update	e Layout	$\times$
Schematic	c:\users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demoj\pcbdemo1\demoj.opj	
Layout	:: \users \kirsc \documents \cadenceworkingdir \cdssetup \orcad_capture \23.1.0 \demos \demoj \pcbdemo 1 \allegro \demoj -complete_vx.brd 💌	
Info There ar	e no connectivity differences to show.	
	Sync Canc	el

5. Click the gear icon and ensure you set Select Layout Tool to OrCAD X Presto.

y n yonin (ogulaero			intelliation bata encarg
	Design Sync Setup	~	
	$\checkmark$ Layout Tool and Design Sync Optic	DNS	
	Layout Folder	allegro	
	Allow Etch Removal	No -	
	Create User Defined Properties	Yes 👻	
Update Layout	Select Layout Tool	OrCAD X Presto -	×
Schematic c: \users \kirsc \doc	V Placement		
Layout ::\users\kirsc\docu	Place Change Component	Always -	j-complete_vx.brd 🔻
Info	Ignore Fixed Property	No 👻	
There are no connectivity di			
1	✓ Constraints		
\$	Constraints	Changes Only 👻	Sync Cancel
	Show Difference Report	Yes 👻	
	V PCB Netlist		
	Configuration file	C:\Cadence\SPB_23.1	
		Ok Cancel Help	

#### 6. Click Ok.

7. Then in the previous window, Click Sync.

This will open OrCAD X Presto PCB Editor and also generate a summary report of all changes found in the Capture Constraint Manager that might have been pushed to the PCB layout.

Image: Second	Constraint Difference Report			- 0				
Constraint Sets       Report time       Thu Sep 5 22:30:29 2024         E       E       Software       23.1 (S006)         DDR3       ECS1       Layout       C:\users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demoj\pcbdemo1\allegro\demoj-complete_vx.brd         Schematic       c:\users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demoj\pcbdemo1\allegro\demoj-complete_vx.brd         Schematic       c:\users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demoj\pcbdemo1\allegro\demoj-complete_vx.brd         NG1       Baseline File       C:\Users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demoj\pcbdemo1\allegro\pstcmdb         NG1       Destination       Yes         Update       Ves       Update         Update       CrossSection, Electrical, Physical, Spacing, Same Net Spacing, NetClasses, Properties         Nets [8]       White list       C:\Cadence\SPB_23.1\share\local\constrgr\cds_flow_config.txt - No valid filters found.         Objects with conflicts       0       0         Stantant       Sets       ElectricalCSet: 2         DiffPairs       1       1	Summary		2 9 2	n n case-sensitive	j			
A ElectricalCSets       Software       23.1 (S006)         IPIGPTAINES [1]       Layout       c:\users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demoj\pcbdemo1\allegro\pstcmdb         A DiffPairs [1]       D       Schematic       c:\users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demoj\pcbdemo1\allegro\pstcmdb         LayerSets [1]       ES1       Schematic       c:\users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demos\demoj\pcbdemo1\allegro\pstcmdb         NG1       Baseline File       C:\Users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demos\demoj\pcbdemo1\allegro\pstcmdb         NG1       Destination       C:\Users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demos\demoj\pcbdemo1\allegro\pstcmdb         NG1       Destination       Yes       Update Mode       Diff3         Update Mode       Diff3       Constraint       CrossSection, Electrical, Physical, Spacing, Same Net Spacing, NetClasses, Properties         White list       C:\Cadence\SPB_23.1\share\local\consmgr\cds_flow_config.txt - No valid filters found.       Objects with       0         Object type       Total changed objects       Constraint_Sets       ElectricalCSet: 2       DiffPairs         DiffPairs       1       1       DiffPairs       1	[2]	Report time	Thu Sep 5 22:30:29 2024		٦			
ECS1       Layout       c:\users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demoj\pcbdemo1\allegro\demoj- complete_xx.brd         0       LayerSets [1]       LS1         LS1       Baseline File       C:\Users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demoj\pcbdemo1\allegro\petrumb         NG1       Baseline File       C:\Users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demos\demoj\pcbdemo1\allegro\petrumb         NG1       Baseline File       C:\Users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demos\demoj\pcbdemo1\allegro\petrumb         NG1       Baseline File       C:\Users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demos\demoj\pcbdemo1\allegro\petrumb         DR2       DoR2       Update Mode       Diff3         DDR3       Constraint       CrossSection, Electrical, Physical, Spacing, Same Net Spacing, NetClasses, Properties         White list       C:\Cadence\SPB_23.1\share\local\consmgr\cds_flow_config.txt - No valid filters found.         Objects with conflicts       0         Object type       Total changed objects         Constraint Sets       ElectricalCSet: 2         DlffPairs       1	<ul> <li>ElectricalCSets</li> <li>[2]</li> <li>DDR3</li> </ul>	Software version	23.1 (\$006)					
b       Schematic       c:\users\kirsc\documents\cadenceworkingdir\cdssetup\orcad_capture\23.1.0\demos\demoj\pcbdemo1\allegro\pstcmdb         I LagreSets [1]       LS1       Schematic       c:\users\kirsc\dopData\Local\Temp\Tmp000006bc.dcf         NG1       NG2       Regions [2]       DDR2       Update Mode       Diff3         DDR3       > Xnets [8]       Constraint       CrossSection, Electrical, Physical, Spacing, Same Net Spacing, NetClasses, Properties       White list       C:\Cadence\SPB_23.1\share\local\consmgr\cds_flow_config.txt - No valid filters found.         Objects with conflicts       0       0       Objects type       Total changed objects         Constraint Sets       ElectricalCSet: 2       DiffPairs       1	ECS1	Layout	c:\users\kirsc\documents\cadencev complete_vx.brd	$vorkingdir\cdssetup\orcad\_capture\23.1.0\demos\demoj\pcbdemo1\allegro\demoj\demoj\allegro\demoj\demoj\demoj\demof\demo\demof\demo\demo\demof\dem\demof\demof\demof\demof\demof\demof\demof\demof\demof\demof\demo\demof\demo\demo\demo\de\demof\demo\demo\demo\demo\demo\dem$				
LS1 A NetGroups [2] NG1 NG2 A Regions [2] DDR2 DDR3 > Xnets [8] Herein C:\Users\kirsc\AppData\Loca\\Temp\Tmp000006bc.dcf Yes Update Mode Diff3 Constraint Information CrossSection, Electrical, Physical, Spacing, Same Net Spacing, NetClasses, Properties White list C:\Cadence\SPB_23.1\share\loca\consmgr\cds_flow_config.txt - No valid filters found. Objects with o Constraint Sets Constraint Sets Constraint Sets DiffPairs 1	D ⊿LaverSets [1]	Schematic	c:\users\kirsc\documents\cadencew	vorkingdir\cdssetup\orcad_capture\23.1.0\demos\demoj\pcbdemo1\allegro\pstcmdb.da	at			
A NetGroups [2] NG1 NG2       Destination design updated       Yes         A Regions [2] DDR2 DDR3 > Xnets [8]       Update Mode       Diff3         Constraint Information       CrossSection, Electrical, Physical, Spacing, Same Net Spacing, NetClasses, Properties         White list       C:\Cadence\SPB_23.1\share\local\consmgr\cds_flow_config.txt - No valid filters found.         Objects with conflicts       0         Object type       Total changed objects         Constraint Sets       ElectricalCSet: 2         DlffPairs       1	LS1	Baseline File	C:\Users\kirsc\AppData\Local\Temp	v\Tmp000006bc.dcf				
<ul> <li>▲ Regions [2] DDR2 DDR3 ▶ Xnets [8]</li> <li>Update Mode Diff3 Constraint Information CrossSection, Electrical, Physical, Spacing, Same Net Spacing, NetClasses, Properties</li> <li>White list C:\Cadence\SPB_23.1\share\local\consmgr\cds_flow_config.txt - No valid filters found.</li> <li>Objects with conflicts</li> <li>Object type</li> <li>Summary</li> <li>Constraint Sets</li> <li>ElectricalCSet: 2</li> <li>DiffPairs</li> <li>I</li> </ul>	NetGroups [2] NG1 NG2	Destination design updated	Yes					
DDR2 DDR3 > Xnets [8] Constraint Information CrossSection, Electrical, Physical, Spacing, Same Net Spacing, NetClasses, Properties White list C:\Cadence\SPB_23.1\share\local\consmgr\cds_flow_config.txt - No valid filters found. Objects with conflicts 0 0 Summary Constraint Sets ElectricalCSet: 2 DiffPairs 1	A Regions [2]	Update Mode	Diff3					
Vitters [6]     White list     C:\Cadence\SPB_23.1\share\local\consmgr\cds_flow_config.txt - No valid filters found.       Objects with conflicts     0       Summary       Object type       Total changed objects       Constraint Sets     ElectricalCSet: 2       DiffPairs     1	DDR2 DDR3	Constraint Information	CrossSection, Electrical, Physical, Spacing, Same Net Spacing, NetClasses, Properties					
Objects with conflicts     0       Summary       Object type     Total changed objects       Constraint Sets     ElectricalCSet: 2       DiffPairs     1	v Allets [0]	White list	C:\Cadence\SPB_23.1\share\local\consmgr\cds_flow_config.txt - No valid filters found.					
Summary       Object type     Total changed objects       Constraint Sets     ElectricalCSet: 2       DiffPairs     1		Objects with conflicts	0					
Object type         Total changed objects           Constraint Sets         ElectricalCSet: 2           DiffPairs         1				Summary				
Constraint Sets         ElectricalCSet: 2           DiffPairs         1			Object type	Total changed objects				
DiffPairs 1		Constraint Sets		ElectricalCSet: 2				
		DiffPairs		1	Ξ,			

You can even save the constraints report summary for future team use and notes, just in case something goes wrong with the transferred constraints. We can track why.

In your new environment, OrCAD X Presto PCB Editor, you can now use the Constraint Manager here.



#### PCB Stack up

In OrCAD X Presto PCB Editor, note the PCB stack up for this board. To do that:

1. Go to the menu at the top, then select **Tools – Cross Section**.

<b>#</b> 0	oss-section l	Editor															- 0	×
Expor	t Import	Edit View	w Filters														cād	dence
De la	man																	
	insi)											Ð	Θ	<u>(</u> )				
	OBJECT			TYPES				THICKNESS		PH	YSICAL 4	~	~	~				
	NA	ME	LAYER	LAYER FUNCTION	MANUFACTURE	CONSTRAINT	VALUE	(+)TOL	(-)TOL	LAYER ID	MATERIAL							
			Surface														Primary	
	тор		Conductor	Conductor	8		0.035	0	0	1	1oz Copper		Surface					
			Dielectric	Dielectric			0.2				Fr-4							
2	GND		Plane	Plane			0.035			2	1oz Copper	I '`	Conductor		_			
			Dielectric	Dielectric			0.2				Fr-4		Delectric					
3	INNER1		Conductor	Conductor			0.035			3	1oz Copper		GND Plane					
	1		Dielectric	Dielectric			0.6				Fr-4		Dielectric					
4	INNER2		Conductor	Conductor			0.035			4	1oz Copper		1 Conductor					
			Dielectric	Dielectric			0.2				Fr-4	1 110			_			
5	POWER		Plane	Plane			0.035				1oz Copper		Dielectric			لسالس		
			Dielectric	Dielectric			0.2				Fr-4	4 IND	12 Conductor					
6	BOTTON	4	Conductor	Conductor			0.035			6	1oz Copper		Dielectric					
			Surface									L				العدا العد		
												II ''	NAMES FORME					
													Dielectric					
												6 80110	M Conductor			÷	÷	
													Surface					
1																		
into																		
Tota	l thickness:																	
Tota	I thickness w	vithout masks:	1.61 mm															
Lay	ers:																	
	Conductor:																	
	Plane:																	
	Maski																	
														Ok	Canc	el Acol		telo
																		,

2. Click Ok to close the stack up.

In the next section we will cover the main constraints you will want to apply for any simple to complex printed circuit board. In this case for our project, we are applying simple constraints to this complex board first, then the advanced constraints.

#### Opening The Constraint Manager (PCB Side)

The following constraints can be applied to standard PCBs (please refer to the previous sections of this document to learn how to implement these constraints).

Open Constraint Manager in OrCAD X Presto PCB Editor by clicking on the main menu and choosing **Tools - Constraint Manager**.

P Or	CAD X Pr	ofession	al Plus				
File	Edit	View	Setup	Tools	ECO	Manufacturing	Re
Visi	Sta	rt Page		🔡 Con	straint N	lanager	
bility	#Grids	s s	napping	Cros	ss Sectio	n	

The Constraint Manager opens, and the worksheet categories are visible on the left of the window.

🖉 Cade	ence_De	emo	- PCB Cor	nstraints - [	Electrical	/ Electrica	l Const	raint Se	et / Ro	outin
File	Edi	t	Objects	Column	View	Analyze	e Au	dit	Tools	W
≫	同	ļ	<mark>≣</mark> o -			<b></b>		o <mark>.</mark>	<	<b>7</b>
Works	heet Se	lect	or		ъ×	Cardan				
🕴 Elec	trical				_	Cader	ice_Den	no		
-	Electr	ical	Constrain	t Set						
•	Ro	utir	ng				Туре			S
		W	iring			*		*		
		Vi	as			Dsn				
		l Im	ipedance			ECS				***
		I™ ITa	in/Max Pro	pagation L	elays					
			fferential P	Pair						
	Ē	Re	lative Prop	bagation De	elay					
		Re	turn Path	-						
▼ 🖿	Net									
•	Ro Ro	utir	ng							
		W	iring							
	≝	Vi	as							
		ј Im I м	ipedance	nagation F	) o lavro					
			tal Etch Le	nath	relays					
		Di	fferential P	Pair						
		Re	lative Prop	agation De	elay					
		Re	turn Path							
<b>→(</b> + Ph	ysical									
🚺 Sp	acing									
🚺 Sa	me Net	Spa	acing							
😂 Ma	anufact	urin	g							
🗟 3D	)									
V Pro	operties	;								
M DF	RC					Wiring	Vias	Imped	lance	Mir

#### All Constraints for Analysis

The Constraint Manager can analyze most potential bottlenecks for a printed circuit board and apply constraints accordingly. To find out the kinds of constraints we can enforce on our PCB, have the Constraint Manager open.

Standard Electrical Constraints

In this section we can control the following:

- Wiring
- Vias
- Impedance
- Min/Max propagation delays
- Total Etch Length
- Differential Pair
- Relative Propagation Delay
- Return Path

🚰 Cadence_Demo - PCB Constraints - [Electrical /	Electrical Constraint	Set / Routing]								
File Edit Objects Column View	Analyze Audit	Tools Window	Help							
>< 🗊 👼 🖏 · × 🖡 👆 🍫 💫 Ta Ta Ta Ta Ta Ta Ta Ca ·   ≣a 🐔 ta										
Worksheet Selector & 🛪 🗙	Cadence_Demo									
👎 Electrical		Objects			Topology		Stub	Max Exposed	Mary Decelled	
Electrical Constraint Set		e	Nama	Manning Made	Verify	Schadula	Length	Length	Max Parallel	Layer Sets
▼ I Routing	type	3	reame	mapping mode	Schedule	Schedule	mm	mm	mm	
Wiring	•	•	•	•						
Vias Vias	Dsn		▼ Cadence_Demo							
Impedance	ECS		DIFF		Yes	Daisy-chain	0.254	17.780		

Standard Physical Constraints

In this section we control the following:

- Referenced Physical CSet
- Line Width (Min, Max)
- Neck (Min Width, Max Length)
- > Differential Pair (Min Line Spacing, Primary Gap, Neck Gap, (+)Tolerance, (-)Tolerance
- Vias
- BB Via Stagger (Min, Max)
- Allow (Pad-Pad Connect, Etch, Ts)

Then under the Net workbook folder named All Layers we have even more options:

- Line Width (Min Max)
- Neck (Min Width, Max Length)
- Uncoupled Length (Gather Control Max)
- Static Phase Tolerance
- Dynamic Phase (Max Length, Tolerance)
- > Differential Pair (Referenced Intra-DP Spacing CSet, Min Line Spacing, Primary Gap, Neck Gap, (+)Tolerance, (-)Tolerance)
- Vias
- BB Via Stagger (Min, Max)
- Allow (Pad-Pad Connect, Etch, Ts)

#### Standard Spacing Constraints

Then we have spacing necessary to maintain signal integrity for cross talk, and avoid manufacturing defects in general.

#### Under the **Spacing Constraint Set > All Layers** worksheet:

- Line To...
- Thru Pin To...
- SMD Pin To...
- Test Pin To...
- Thru Via To...
- BB Via To...
- Microvia To...
- Test Via To...
- Bond Finger To...
- Hole To...
- Min BB Via Gap

Then there is the **Net Class-Class > All Layers** worksheet which contains the same constraints as above but allows you to <u>set</u> constraints between Net Classes instead of only single nets one by one.

Standard Same Net Spacing Constraints

For the most part, Same Net Spacing can be left as is, unless you need to change the thermal relief on the layer. But even then, that can be changed in your design properties.

**TIP**: If you end up having shorting errors between traces and planes, then this constraints area might be the culprit. You'll want to adjust your **Shape to...** spacing setting such that shapes have some distance away from all other objects for isolation purposes.

For example, let's say you wanted all power planes and shapes (members of the POWER\_GROUP) at least ~7.87 mils (0.2 mm) away from copper pads, even if the through-hole or surface mount pad is part of the same net (you may want to do this to provide thermal relief spacing).

You would go to the **Spacing > Net > All Layers** worksheet, then in the POWER\_GROUP(10) cell, right click the cell, choose **Change all design unit attributes...** 

🎢 Cadence_Demo - PCB Constraints - [Spacing	/ Net / All Layer	s]					
File Edit Objects Column View	Analyze A	udit Tools Wi	ndow Help				
운 🖡 🏮 🖏 ·	<b></b> ,	0 0 70	To TA TO TO TO TO	<b>O</b> • <b>O</b> •		» 🍢 🔊	۵ 🖫
Worksheet Selector 🛛 🗗 🗙	Cadence Dem	0					
🕈 Electrical			Objects			Line To	• т
+ Physical					Referenced Spacing	All	
1 Spacing	Туре	s	Name		Cset	mm	
Spacing Constraint Set	•				•		•
All Layers	Dsn		Cadence_Demo		DEFAULT	0.200	0.20
🖩 By Layer	NCIs		POWER_GROUP(10)		DECALIET	0.200	0.20
🔻 🛅 Net	Net		GND EARTH	Analyze			0.20
🛱 All Layers 🦊	Net		V+12	Cross Prol	be		0.20
🔻 🚞 Net Class-Class	Net		VCC	🤷 Find		Ctrl+F	0.20
All Layers	Net		V12N	Bookmark	<b></b>		0.20
CSet assignment matrix	Net		0	Expand			0.20
▼ ■ Region	Net		× 1V2	Expand Al			0.20
All Layers	Net		1V8	Collapse			0.20
▼ Inter Layer	Net		2V5	Create			0.20
I 🖽 Spacing	Net		3V3	Add to			0.20
	Net		SV 5V	Net Class	members		0.20
	NCIs		► RF(11)	Remove			0.20
	NCIs		STEVE(1)	Rename		F2	0.20
	Bus		DATA[020](19)	Delete		Del	0.20
	Bus		DATA1[09](10)	Compare		L'ei	0.20
	Bus		DDS[010](11)	Compare.	···		0.20
	Bus		MEMORY[029](30)	Constraint	t set References		0.20
	DPr		CLOCK	Change al	il design unit attributes	-	0.20
	DPr		× • •		DEFAULT	0.200	0.20

In the new window, set the value to 0.20 (since we're in millimeters and this field doesn't automatically convert the units), then click 0k.

Note that this will override the DEFAULT constraint set that's being applied to all the nets in that POWER\_GROUP(10). So it is recommended to create a Constraint set for POWER nets first, then apply that to the **Spacing > Net > All Layers** worksheet (see below).



SpacingCSet: SCS1_POWER_GROUP		
Ok Cancel	Help	

SCS	▼ SCS1_POWE		l (	n 200 - 0	.200
Цтур	Conduct	Analyze			00.000
LTyp	Plane	Cross Probe	2		00.000
		🗟 Find		Ctrl+F	
		Bookmark		•	
		Expand			
		Expand All			
		Collapse			
		Create		•	
		Rename		F2	
		Delete		Del	
		Compare			
		Constraint	Set References		
		Copy Const	raints from		
	$\rightarrow$	Change all	design unit attribute	es	

Conductor		0.200	0.200
► Plane		0.200	0.200
▼ SCS1_POWER_GROUP		0.200	0.200
Conductor		0.200	0.200
Plane		0.200	0.200
Set Value			×
Set Design Units	value		
0.2			
ОК	Cancel		.e

Click OK, then all the rows for that constraint set (SCS1\_POWER\_GROUP) get set to 0.2 mm.

Now we can apply the constraint set to the **Spacing >Net > All Layers** worksheet by selecting it from the dropdown options shown below and applying it to the **POWER\_GROUP**.

🗲 Electrical		Objects						
→ Physical	Tura	c .	Nama	Referenced Spacing CSet				
I Spacing	Туре		Name					
▼ Spacing Constraint Set	*			*				
All Layers	Dsn		▼ Cadence_Demo	DEFAULT	0.200			
🖩 By Layer	NCls		POWER_GROUP(10)	DEFAULT 🖉 🗸	0.200			
▼ 🛄 Net	Net		GND EARTH	BGA_SPACE	200			
🖩 All Layers 🖊	Net		V+12	DEFAULT	200			
▼ 📗 Net Class-Class	Net		vcc	SCST_FOWER_GROOF	200			
All Layers	Net		V12N	DEFAULT	0.200			
Get assignment matrix	Net	000000000000000000000000000000000000000		DEFAULT	0.200			

Standard Manufacturing Constraints

Now in the Manufacturing section we have many checks to consider:

Design for Fabrication

- Outline
- Mask
- Annular Ring
- Copper Features
- Copper Spacing
- Silkscreen

Design for Assembly

- Outline
- PkgToPkg Spacing
- Spacing
- Pastemask

#### Design for Test

- Outline
- Mask and Silkscreen
- Spacing
- Probe

#### Standard 3D Constraints

Now it's not enough to just do 2D constraints. 3D is considered.

- Component to Component
- Component to Board
- Component to Rigid-Flex

Component to Board Edge

Properties

We also have properties being held inside Constraint Manager that came over from the schematic, such as:

Net

- Electrical Properties
  - Frequency
  - Period
  - Duty Cycle
  - Jitter
  - Cycle to Measure
  - Offset
  - Bit Pattern
  - Enable highspeed adjacent layer Keep-outs
- General Properties
  - Voltage
  - Weight
  - Route (Priority vs. to Shape)
- Route/Vias Keepout Exception

Component

- Component Properties
  - General
  - Thermal
  - Swapping
  - Reuse
- Pin Properties
  - General (Pinuse, Pin Delay, Shorting Net, Voltage Source Pin)
  - Shapes
  - Manufacturing

## Standard DRCs

In the following sections we will show you the constraint sets that are created and then the nets (and objects) those constraint sets apply to.

#### Applying Standard PCB Constraints

With the Constraint Manager open, we need to set various constraints for the PCB.

Standard Electrical Constraints

Even in some low-speed boards, we need 50 Ohms of Impedance. So we set the impedance to 50 ohms for single-ended PCBs at 10% tolerance, since that is what most manufacturers can handle.

🖗 Electrical	Objects			Single-line	e Impedance
▼ 📕 Electrical Constraint Set	Time C Nome		Target	Tolerance	
▼ IIII Routing	Туре		Name	Ohm	Ohm
🗮 Wiring	*	*	*	•	•
🔛 Vias	Dsn		▼ Cadence_Demo		
Impedance	ECS		DIFF	50	10 %
🔠 Min/Max Propagation Delays					
🌐 Total Etch Length					
🔠 Differential Pair					
🖽 Relative Propagation Delay					

Then that impedance gets applied to whichever net it applies to. Like the CLOCK+ and CLOCK- signals below:

▼ ■ Net	Bus	MEMORY[029](30)				*****	
▼ I Routing	DPr		DIFF	50	10 %		11.412
H Wiring	Net	► CLOCK+	DIFF	50	10 %		11.412
H Vias	Net	► CLOCK-	DIFF	50	10 %		11.412
Impedance	DPr	► D	DIFF	50	10 %		20.982
Min/Max Propagation Delays	DPr	DP_DATA0	DIFF	50	10 %		19.27
III Total Etch Length	DPr	► DP_DATA1	DIFF	50	10 %		19.27
		h				000000	\$20X0X0X0X0X0X

The rest of the constraints are in the high-speed applications section later in this guide.

Standard Physical Constraints

For physical constraints we have the following:

#### Trace Width

Trace Width (Line Width) is set in the Physical CSet to 0.500 mm (19.685 mils) for power traces.

🌠 Cadence_Demo - PCB Constraints - [Physical	/ Physical C	onstrain	t Set / All Layers]							
File Edit Objects Column View	Analyze	Audi	t Tools Window Help							
الم	<b>_</b>		No To To T	5 70 7	j <b>™</b>		- 支 🗞	<mark>یہ</mark> ہے د	<b>'</b> = Q	
Worksheet Selector 🛛 🗗 🗙	Cadence_	Demo								
Electrical			Objects	Referenced	Lin	e Width		Neck		
🔸 Physical			News	Physical	Min	Max	Min Width Max Length		Min Line Spaci	
Physical Constraint Set	туре	<u> </u>	Name	CSet	mm	mm	mm	mm	mm	
🖩 All Layers	•			*	*		•	•		
By Layer	Dsn		▼ Cadence_Demo	DEFAULT	0.200	0.000	0.150	2.500	0.000	
▼ Net	PCS		► DEFAULT		0.200	0.000	0.150	2.500	0.000	
All Layers	PCS		DIFF1		0.127	0.000	0.100	5.000	0.107	
▼ Region	PCS		► POWER		0.500	0.000	0.200	9.000	0.000	
II All Layers	PCS		► RF		0.500	0.000	0.200	5.000	0.000	

Assign Constraint set to the **POWER\_GROUP** nets.

+ ← Physical ←	Туре	s	Name	Referenced Physical CSet	Mi
All Layers		*	*	•	*
🖩 By Layer	Dsn		▼ Cadence_Demo	DEFAULT	0.200
▼ 🛄 Net	NCIs	¥888	▼ POWER_GROUP(10)	POWER	0.500
All Layers	Net		GND EARTH	POWER	0.500
▼Region	Net	¥888	V+12	POWER	0.500
All Layers	Net		vcc	POWER	0.500

#### **Differential Pairs**

In most boards you will have differential pairs, so notice the differential pairs set below.

worksneet selector	Cadence_D	emo									<b>_</b>	
🕺 Electrical		Objects			Neck		Differential Pair					
+ Physical			Nama	Min Width	Max Length	Min Line Spacing	Primary Gap	Neck Gap	(+)Tolerance	(-)Tolerance		
Physical Constraint out	iype	*	riame	mm	mm	mm	mm	mm	mm	mm		
🔚 All Layers 📕						•						
By Layer	Dsn		Cadence_Demo	0.150	2.500	0.000	0.000	0.000	0.000	0.000	VIA	
▼ Net	PCS		DEFAULT	0.150	2.500	0.000	0.000	0.000	0.000	0.000	VIA	
I All Layers	PCS		DIFF1	0.100	5.000	0.107			0.010	0.010	VIA	
Region	PCS		POWER	0.200	9.000	0.000	0.000	0.000	0.000	0.000	VIA	
I All Layers	PCS		► RF		5.000	0.000	0.000	0.000	0.000	0.000		

#### **Constraint Set Values**

The values from the image are:

- Min Line Spacing = 0.107 mm
- Primary Gap = 0.127 mm
- Neck Gap = 0.117 mm
- (+)Tolerance = 0.010 mm
- (-)Tolerance = 0.010 mm

#### Applied Constraint Set to diffpairs in the design

+++ Physical	Туре	s	Name	CSet		
All Lavers	•	*		•		
🛗 By Layer	Dsn		▼ Cadence_Demo	DEFAULT		
▼ 💼 Net	NCIs	<b>\$</b> 200	▼ POWER_GROUP(10)	POWER		
🔚 All Layers 🛛 🕂 👘	Net		GND EARTH	POWER		
🕶 🛄 Region	Net	1000	V+12	POWER		
l 🌐 All Layers	Net		vcc	POWER		
	Net	***	V12N	POWER		
	Net		0	POWER		
	Net	<b>1</b> 888	1V2	POWER		
	Net		1V8	POWER		
	Net		2V5	POWER		
	Net		3V3	POWER		
	Net	***	5V	POWER		
	NCIs		► RF(11)	RF		
	NCIs.	***	► STEVE_PH(9)	DEFAULT		
	Bus		► DATA[020](19)	DEFAULT		
	Bus		► DATA1[09](10)	DEFAULT		
	Bus		► DDS[010](11)	DEFAULT		
	Bus	***	MEMORY[029](30)	DEFAULT		
	DPr	-		DIFF1		
	Net	1888	CLOCK+	DIFF1		
	Net		CLOCK-	DIFF1		
	DPr	***	► D	DIFF1		
	DPr		► DP_DATA0	DIFF1		
	DPr	<b>1</b> 888	► DP_DATA1	DIFF1		
	DPr		► DP_DATA2	DIFF1		
1 Spacing	DPr	***	► DP_DATA3	DIFF1		
I Same Net Spacing	DPr		► DP1	DIFF1		

		Differential Pair				
Referenced Intra-DP Spacing CSet	Min Line Spacing	Primary Gap	Neck Gap	(+)Tolerance	(-)Tolerance	Vias
	mm	mm	mm	mm	mm	
*	*	*	*	*	*	*
-	0.000	0.000	0.000	0.000	0.000	VIA
	0.000	0.000	0.000	0.000	0.000	VIA
	0.000	0.000	0.000	0.000	0.000	
	0.000	0.000	0.000	0.000	0.000	VIA

-2000		0.000		0.000	
					VIA
0.107	0.127	0.117	0.010	0.010	VIA
0.107	0.127	0.117	0.010	0.010	VIA
0.107	0.127	0.117	0.010	0.010	VIA

#### Physical Region

We have BGA and Flex areas where we use a different set of rules for minimum **Line Width**. We can also set **Differential Pair** values, **Minimum Neck** width and so on. In these cases, we simply apply any existing constraint sets we want to use to manage those regions of the board. You can also directly enter the values you want for these regions (shown in blue text).

🚰 Cadence_Demo - PCB Constraints - [Physica	l / Region / All Laye	rs]							
File Edit Objects Column View	Analyze Aud	lit Tools Windo	ow Help						
≫ 🖡 🖡 🖏 ·	<b></b>	» 🍾 🏹	• 🔨 🏷 🏹	То 🛇 - 🔁 📘	<mark>5</mark> 🗞 🎝 🔽	b 🍢 🔆 🕞	Q.		
Worksheet Selector 🗗 🗙	Cadence_Demo								
👎 Electrical		Objects	5		Line	Width	Neck		
→ ← Physical	Tura		News	Referenced Physical	Min	Max	Min Width	n Width	
🔻 🚞 Physical Constraint Set	Туре	<b>`</b>	Name		mm mm		mm		
All Layers			•	- I- E	•	*	•	•	
🖩 By Layer	Dsn		Cadence_Demo	DEFAULT	0.200	0.000	0.150	2.	
▼ 🛄 Net	Rgn		BGA		0.100		0.100		
All Layers	Rgn		CONN_FLEX		0.300		0.100		
▼ Region	Rgn		FLEX		0.400				
All Layers	Rgn		LCD_FLEX		0.400		0.100		

However, the best method is to create a Physical Constraint Set (see below),

Then assign it to the appropriate region.

- Standard Spacing Constraints
- Standard Same Net Spacing Constraints
- Standard Manufacturing Constraints
- Standard 3D Constraints
- Standard Properties
- Standard DRCs
## **Applying High-Speed and Advanced Constraints**

The following constraints can be applied to complex and/or high-speed PCBs (please refer to the previous sections of this document to learn more about implementing those constraints).

## **Advanced Constraints Application**

Advanced Electrical Constraints

## Wiring topology

Set specific routing paths for technologies like DDR3 and T-branch to minimize signal attenuation due to PCB material properties. Or Daisy Chain or star topologies.



Image: Diagram showing the prioritized routing of critical nets on a PCB.

**Definition**: Wiring topology involves organizing the connections between different nets on a PCB to achieve a certain outcome, such as minimizing signal reflections, signal attenuation or voltage drops.

Example: Let's ensure that a pulse-width modulated net follows a daisy-chain topology.

## Steps:

- 1. Open the Constraint Manager, then go to the **Electrical > Routing > Wiring** worksheet.
- 2. In the Type column, you can right click your **Dsn** cell, create a new Electrical Constraint Set (ECS). Notice in the image below, an ECSet has already been created.
- 3. Select the drop-down in the **Schedule** column and choose your net topology.

Worksheet Selector 🗗 🗙		Cadence_	Dem	no									
Electrical		Objects			Objects		Тороюду				Max Exposed	Mary Described	
Electrical Constraint Set		<b>.</b>			News	Manalas Mada	Verify	Calculut	_	Length	Length	Max Parallel	Layer Sets
Routing		Type		3	Name	Mapping Mode	Schedule	Schedul	e	mm	mm	mm	
🔠 Wiring 🥌	ŀ	•				•		•				•	
III Vias	l	Dsn			▼ Cadence_Demo			Í 1	ļ				
	E	ecs	88		DIFF		Yes	Daisy-chain		0.203	17.780	0.000:0.000:0.0	DIFF_CLOCK
Min/Max Propagation Delays													
Total Etch Length													
Differential Pair													

You have options such as:

- Minimum Spanning Tree
- Daisy-chain
- Source-load Daisy-chain
- Star
- Far-end Cluster
- (Clear)

Each topology has its own benefits, depending on the application.

- 4. Once you have set the topology for that ECSet, you can apply it to the appropriate nets found in the spreadsheet under **Electrical > Net > Routing > Wiring**.
- 5. In this example, however, you can also directly apply a net schedule (see below).

Differential Pair	Net	FAN_PWM				$\otimes$	l
Relative Propagation Delay	Net	FAN_PWM_Q*	_	$\rightarrow$	Daisy-chain	$\otimes$	2
Return Path	Net	FAN_TACH					l
▼ 📄 Net	Net	FAN_TACH_CON			Daisy-chain	$\otimes$	
✓ ➡ ➡ Routing	Net	FORCE_OFF*					l
🖶 Wiring	Net	FORCE_OFF_DELAY				$\otimes$	
🔛 Vias	Net	FORCE_RECOVERY*					ļ
	000000000000000000000000000000000000000						c

**Note:** Depending on your use case, you can use either constraint sets, or a specific rule application as needed, like in this example. However, please use constraint sets as often as possible to catch most cases first before applying net-specific one-off rules. Using constraint sets modularizes and streamlines your PCB design constraint process and makes you more efficient. The constraint set method also reduces the likelihood of errors and forgotten constraints. You can also import, and export constraint sets across your team so that everyone adheres to similar standards. The less you do unique constraint values that are outside (or override) the constraint sets, the fewer problems you will have.

Benefit of a good Wiring Topology: Improves signal integrity and timing by ensuring critical connections are made efficiently.

## Stub Length (Max Stub Length)

Stubs that lead off traces and pads can act as antennas. Those antennas are problematic for electromagnetic field compatibility and electromagnetic interference (EMC and EMI).



PCB trace stub on top view of PCB

In the image below, we show exactly what gets checked in the software for stub length.

## **Maximum Stub Length**

Checks the maximum stub length in design units for daisy chain routing.

**Note:** When a pin is routed to a connect line, the stub is the line of etch between the pin and the connect line.

The stub length constraint is validated only if NET\_SCHEDULE is enabled and RATSNEST\_SCHEDULE is set to either MIN\_DAISY\_CHAIN or MIN\_SOURCE\_LOAD\_DAISY.

>

This check ignores pins at the end of clines, dangling clines, and test points. The chosen net schedule impacts the rule check.



Legal Values: Design Units DRC Code: ES Applicable Objects: Xnet, Net, ElectricalCSet, NetClass, DiffPair, Bus, NetGroup Attribute Name: STUB LENGTH

Image: A stub as defined in OrCAD X Presto PCB Editor.

**Purpose**: To restrict the number of stubs on a trace's vias or on a net wiring topology to reduce signal reflections and maintain signal integrity. For high-speed designs, aim for zero or minimal stubs. When stubs are unavoidable, keep them as short as possible.

Applies to: USB, HDMI and any other high-speed interfaces that need minimal fanouts or stubs to operate efficiently.

Importance: Affects current-carrying capacity and signal integrity.

**Application**: Power distribution, high-speed signals.

Steps:

1. Open the Constraint Manager using **Tools - Constraint Manager**.

**TIP**: As usual we will make a constraint set that holds the rules/constraints, then we apply that constraint set to a net, class, group or region.

2. Create an electrical constraint set under **Electrical > Electrical Constraint Set > Routing > Wiring**. Right click the **Dsn** cell's name.

## 3. Choose Create - Electrical CSet...

Cadence_Demo - PCB Constraints - [Electric	al / Electrica	al Constrain	t Set / Ro	outing]					
File Edit Objects Column View	/ Analyze	e Audit	Tools	Window	Help				
8 🖡 🍺 🖏 📃	<b></b>		<b>~</b>	To To T	<b>. T</b> o 1	™ ™	<b>)- 🕗-</b>	≡₀ ‰ *₀	°• °• ×
Worksheet Selector 🗗 🗙	Cadence	_Demo							
🕴 Electrical			Object	ts			Topology	Stub	
Electrical Constraint Set	Tumo	6		Nama		Manning Mada	Verify	Sahadula	Length
▼ 🖩 Routing	Туре	<b>`</b>		Name		Mapping Mode	Schedule	Schedule	mm
Wiring	*	*	*		/	*	*	*	*
III Vias	Dsn		V Ci	adence_Demo					
	ECS DIFF				Ar	nalyze	Daisy-chain	0.254	
Min/Max Propagation Delays					Cr	oss Probe			
Iotal Etch Length					🖏 Fir	nd	Ctrl+F		
Differential Pair					Bo	ookmark	•		
					Fx	nand All		1	1
▼ Net				_		iparta 7 m		Electrical CSat	
▼ Im Routing						eate	50	Liectrical CSet	
					Re	ename	+2		
					De	elete	Del		

- 4. Give the ECSet a name and it will be added to the spreadsheet.
- 5. Once added, enter a desired maximum stub length for the ECSet.
- 6. For example, let's say you want your stubs to be no more than 8 mils (0.0203 mm), so you enter '8 mils' in the rule shown below for the **DIFF** signal constraint set.

Cadence_	Demo						
		Objects		Topology		Stub	Max
-				Verify		Length	
Туре	S	Name	Mapping Mode	Schedule	Schedule	mm	
*	*	*	*	*	*	*	*
Dsn		▼ Cadence_Demo					
ECS		DIFF		Yes	Daisy-chain	0.203	

- 7. Now let's apply that constraint and the stub rule it has.
- 8. In the Constraint Manager go to **Electrical > Net > Routing > Wiring**.

9. Choose from the **Referenced Electrical CSet** column and set it to your desired net.

🎢 Cadence_Der	no - PCB Constraints - [	Electrical / Net	t / Routing]							
File Edit	Objects Column	View An	alyze Auc	lit Tools	Window	Help				
× 🖡 🖡	j B <sub>0</sub> -		<b>-</b>	> <mark>-</mark> <	<b>T</b> s <b>T</b> s (	<u>7</u> 70 7	• 🕶 🔽	<b>S</b> - (	<b>}</b> - ≡ <sub>⊗</sub> ≪	
Worksheet Sele	ector t	5 × Cad	ence_Demo							
🕴 Electrical					Obje	cts				
▼ 📄 Electric ▼ 🖩 Rou	al Constraint Set		Туре	s		Nam	ne		Referenced Electrical CSet	Verify Schedule
	Wiring	•						•		•
	Vias	Dsn			▼ Cadeno	e_Demo				
	Impedance	NCIs			► AD	DRESS(24)				
	Min/Max Propagation D	Pelays NCIs			► DA	TA(15)				
	Differential Dair	Bus			► DA	TA[020](19)				
	Differential Pair	Bus			► DA	TA1[09](10)				
	Return Path	Bus			► DD	S[010](11)				
▼ ■ Net		Bus			► ME	MORY[029](30	D)			1
▼ 📾 Rou	iting	DPr			🕨 🔻 clo	оск		C	DIFF 🗸 🗸	Yes
	Wiring	Net				CLOCK+		C	DIFF	Yes
Ē	Vias	Net				CLOCK-			Clear)	Yes
Ē	Impedance	DPr			V D			L		Yes
	Min/Max Propagation D	elays Net				D+		C	DIFF	Yes
	Total Etch Length	Net				D-		C	DIFF	Yes
	Differential Pair	DPr			► DP	DATA0		C	DIFF	Yes
	Relative Propagation De	elay DPr			► DP	DATA1		C	DIFF	Yes
					4					

10. In the Constraint Manager, analyze whether the rules are being adhered to by a particular net class, group, or differential pair, by right clicking that Object name and choosing **Analyze** (as shown below).

Return Path	Bus	DDS[010](11)				
▼ ■ Net	Bus	MEMORY[029](30)				
▼	DPr	▼ CLOCK			Voc	Daisy-chain
Wiring	Net	CLOCK+	Ana	lyze		Daisy-chain
III Vias	Net	CLOCK-	Cros	s Probe		Daisy-chain
Impedance	DPr	▼ D	🤷 Find		Ctrl+F	Daisy-chain
Min/Max Propagation Delays	Net	D+	Boo	kmark		Daisy-chain

11. You will then see results on whether Stub Length limits are being adhered to for any traces that need that constraint set applied.

Cadence_Demo							Г					
		Objects			Topology				Stub Leng	th	Exp	
Туре	s	Name	Referenced Electrical CSet	Verify Schedule	Schedule	Actual	Margin	Max mm	Actual mm	Margir mm	Max mm	
*			*					*	-			
Dsn		▼ Cadence_Demo								-10.475		
NCIs		ADDRESS(24)										
NCls		► DATA(15)										
Bus		► DATA[020](19)										
Bus		► DATA1[09](10)										
Bus		► DDS[010](11)									-	
Bus		► MEMORY[029](30)										
DPr		CLOCK	DIFF	Yes	Daisy-chain			0.203		-0.509		
Net		CLOCK+	DIFF	Yes	Daisy-chain	FAIL		0.203	0.664	-0.461		
Net		CLOCK-	DIFF	Yes	Daisy-chain	FAIL		0.203	0.712	-0.509		
DPr		▼ D	DIFF	Yes	Daisy-chain			0.203		-1.151		

**Reminder**: Stub Length Limits are used to ensure tight signal integrity and minimal reflections and antennas, namely for nets that carry signals with extremely short rise times (30 picoseconds or less, 5 GHz or higher frequencies).

Similar to stub length limits, we need to limit total trace length on the outer layers of the PCB to avoid EMI that are picked up by or transmitted from said traces.

## Maximum Exposed Length

Set a maximum length for exposed stubs to prevent unintentional antenna effects. This is particularly important for high-frequency signals where wavelengths are shorter. A general rule of thumb is to keep stub lengths below 1/20th of the signal's wavelength, but please note that each situation depends on **simulating** the conditions for your specific stack-up, your dielectric and conductor materials, signals being transmitted and preliminary signal integrity analysis. Rules of thumb, while can often be a good enough solution sooner, can still lead to re-spun boards later without proper simulation.

TIP: You can perform signal integrity analysis and simulations pre-layout, during layout and post-layout using TopXplorer.

To ensure that you're on track with your signal integrity goals, use information on signals propagating through your design and are using IBIS models for your transmitting ICs and simulate them in TopXplorer.

For example, this differential pair, CLOCK (CLOCK+ and CLOCK-) from the images in the Stub Length section of this part can be analyzed as it is right now. You want to simulate the circuit topology, test some conditions to find out what will make it compliant with your Stub Length requirements.

To do such analyses on any net, right click the Net Class/Group/Diff Pair object name, select Explore Topology.

**IMPORTANT NOTE:** If you get an error message regarding licenses not being available, you first need to download and install the correct version of Cadence Sigrity X Aurora software (for example if using OrCAD X 24.1, then install Sigrity 24.1 and its subsequent updates for that base version 24).

After that, even when installed, you may need to create and set the Environment variable (SIGRITY\_EDA\_DIR = C:\Cadence\ Sigrity2024.1) in both the local and system environment variables in Windows.

Finally, open LMTools (would be installed from the License Manager software from Cadence) from the Windows Start menu. Then go to the Start/Stop/Reread tab, click the ReRead License File button, then after waiting for 10-20 seconds, click the Stop Server button, then wait another 5-10 seconds, then click Start Server.

After another 5-20 seconds (the LMTOOLS by Flexera window might stop responding during this time, but it will respond eventually), you can run TopXplorer from the Constraint Manager.

LMTOOLS by Flexera –		×
File Edit Mode Help		
Service/License File   System Settings   Utilities Start/Stop/Reread   Server Status   Server Diags   Config Services	Borrowing	1
License servers installed as Windows services on this computer	1	
Start Server Stop Server ReRead License File		
Edit Advanced settings Force Server Shutdown NOTE: This box must be checked to shut down a license ser when licenses are borrowed.	ver	
VD is starting, please check vendor daemon's status in debug log		

We will not show how to use TopXplorer, but only how to access it, since using TopXplorer is outside the scope of this document.

Steps to find a trace(s)' topologies in TopXplorer for signal integrity and transmission line analysis:

1. Within Constraint Manager, right click an object (like a differential pair like CLOCK), then select **Explore Topology.** 

		Objects					
Туре	s	Name			Referenced Electrical CSet	Ve Sche	rif: edu
*	*	*			*	*	
Dsn		▼ Cadence_Demo					
NCls		ADDRESS(24)					
NCls		► DATA(15)					
Bus		► DATA[020](19)					
Bus		DATA1[09](10)					
Bus		► DDS[010](11)					
Bus		MEMORY[029](30)					
DPr		CLOCK			DIFF	Yes	1
Net		CLOCK+		Analyze			
Net		CLOCK-		Cross Prob	e		
DPr		▼ D	P	Find		Ctrl+F	
Net		D+		Bookmark		•	
Net		D-		Expand			
DPr		► DP_DATA0		Expand All			
DPr		► DP_DATA1		Collapse			
DPr		► DP_DATA2		Create		•	
DPr		► DP_DATA3		Add to		•	
DPr		► DP1		Diff Pair me	embers		
DPr		► STDA_SSRX		Remove			
DPr		► STDA_SSTX		Ponamo		E2	
Net		AEN/		Delete			
Net		BRD/		Common			
Net		BRESET		Compare			
XNet		BUF_OUT		Constraint	Set References.		
XNet		BUF_OUT		Explore Top	ology		

2. A window like the one below opens and you can explore various features and tools to analyze your signals, considering the actual board they are on, in real-time.



We will stop there for now, but know that you can do all sorts of things like different analysis types and options, frequency response and even S-parameter extraction. The findings from such analysis methods can be back-propagated as desirable constraints back into the Constraint Manager. Then the PCB designer can use those new constraints as the rule of law to finish laying out the PCB to meet requirements.



Results-driven design (i.e. from simulation findings and requirements) is a mandatory part of the process to support first-time right design and fewer design iterations and re-spins. TopXplorer is a signal integrity tool that adheres to the results driven design standard for modern PCB designers and hardware engineers.

Let us switch gears back to maximum exposed length. In the next set of steps, we will show how to set the maximum exposed length of conductive material that is allowed on the outer layers of the PCB (top and/or bottom).

Steps on how to change maximum exposed length outside the PCB:

- 1. Similar to the stub length rule application, open the Constraint Manager.
- 2. Create an electrical CSet in the **Electrical Constraint Set > Routing > Wiring** worksheet OR use an **existing** CSET (e.g. DIFF).



3. Set the Max Exposed Length to say, 750 mils (17.780 mm).

**Design Note**: This value was chosen arbitrarily as half the 1500 mil critical trace length for a USB 3.2 differential pair signal operating at 5 GHz Nyquist frequency (i.e. 10 Gbps) from a Texas Instruments controller from their datasheet recommendations. The reason being that the rise time for that chip and a 10 Gbps per second signal hovers typically around 20-30 picoseconds and the speed of travel to avoid reflection is around the 1500 mil mark. Then, we decide to cut that in half to be more on the cautious side, since we want at most, both outer top layer and outer bottom layer traces to result in that 1500 mil limit. However, you **must** verify with the chip manufacturer and/or designers the expected signal speed and acceptable

critical length to know what a 'safe' outer layer trace length should be. For instance, if your signals are pushing 40 Gbps (20 GHz Nyquist) and quadruple the MT/s of USB 3.2 then cut 1500 mils down to a quarter of what we put for USB 3.2. (i.e. 1500 mils / 4 = 375 mils). But that's a rule of thumb. Verify with TopXplorer. The real-world requirements can vary significantly depending on dielectric and conductive materials of the PCB, coating, environment, etc. If you do need to use a rule of thumb and don't have access to simulation, then a very conservative value is 1/20th the signal wavelength. Verify with simulation later.

## 4. Finally, go to **Electrical > Net > Routing > Wiring**.

5. Click and apply the appropriate ECSet onto the desired net by selecting the ECSet from the **Referenced Electrical CSet** column. The rule is automatically applied to that net.

Return Dath	Bus	► DDS[010](11)		
▼ Net	Bus • MEMORY[029](30)			
▼ I Routing	DPr	CLOCK	DIFF	Yes
Wiring	Net	CLOCK+	DIFF	Yes
Uias	Net	CLOCK-	DIFF	Yes
	DPr	V D	DIFF	Yes
Min (May Propagation Dola	ve Not	D+	DIFF	Vos

Objects			Topology	,			Stub Length			Exposed Length		
Nama	Referenced Electrical CSet	Verify	Cabadula	Artual	Maraia	Max	Actual	Margin	Max	Actual	Margin	
Name		Schedule	Schedule		wargin	mm	mm	mm	mm	mm	mm	
	*					*						
▼ Cadence_Demo								-10.475			-55.190	
ADDRESS(24)												
► DATA(15)												
► DATA[020](19)									2			
► DATA1[09](10)												
► DDS[010](11)												
MEMORY[029](30)												
🔻 сlock	DIFF	Yes	Daisy-chain			0.203		-0.509	17.780		12.089	
CLOCK+	DIFF	Yes	Daisy-chain	FAIL		0.203	0.664	-0.461	17.780	5.222	12.558	
CLOCK-	DIFF	Yes	Daisy-chain	FAIL		0.203	0.712	-0.509	17.780	5.691	12.089	
	DUPP	V	Data data	× * * * *	******	0.000			17 700	- XXXXXXX	F3 730	

Notice how the CLOCK signal adheres to the Exposed Length restriction (green color means it adheres/is good), with margin to spare (12.089 mm to work with).

As an experiment, adjust the margin to something like 1 mil and see what happens to the same row being analyzed. It will turn red immediately, since the Constraint Manager is always active.

## Key Note:

For the rest of this project application, follow the instructions from previous parts of the guide as the steps are the same. We will show images of our implementation for this design.

## Maximum parallel trace length

Limit the length that signal traces run parallel to each other to reduce coupling and crosstalk. This is especially crucial for high-speed differential pairs. The acceptable length depends on factors like trace spacing, layer stack-up, and signal frequency. So the values below are just examples. We set the allowed Max parallel traces for two situations for this Constraint Set.



The Rule immediately applies in the Constraint Manager and the design adheres to the rule.

Felectrical	Objects		Stub Length			E	xposed Ler	ngth	Parallel				
Electrical Constraint Set			Norma		Max	Actual	Margin	Max	Actual	Margin	Max	A	Margin
▼ m Routing	туре	3	Name	Margin	mm	mm	mm	mm	mm	mm	mm	Actual	mm
Uring Wiring	•		•	•					•	•	•	•	•
Uias .	Dsn		▼ Cadence_Demo				-10.475			-55.190			
Impedance	NCIs		ADDRESS(24)		3								
Min/Max Propagation Delays	NCIs		► DATA(15)										
Differential Dair	Bus		DATA[020](19)										
Palative Propagation Delay	Bus		► DATA1[09](10)										
Return Path	Bus		► DDS[010](11)										
▼ ■ Net	Bus		MEMORY[029](30)										
▼ I Routing	DPr		▼ СLОСК		0.203		-0.509	17.780		12.089	0.000:0.000:0.000		
I Wiring	Net		CLOCK+		0.203	0.664	-0.461	17.780		12.558	0.000:0.000:0.000	PASS	
III Vias	Net		CLOCK-		0.203	0.712	-0.509	17.780	5.691	12.089	<del>0.000.0.000.0.000</del>	Pass	

## Layer restrictions

Control EMI by limiting the layers through which a trace can be routed. For example, keep high-speed signals on internal layers sandwiched between ground planes for better shielding.

In our design, we want the CLOCK+ and CLOCK- signals to **not** be routed on the PCB surface. It is sensitive to noise and controls the timing for important devices in the design. So, we set the allowed routed layers to the internal layers (as seen below).





			· · ·							
Э≪ 📮 🎁 🔯 т сlock	▼	N 10 1	0 🔽 🐨 🖓	To To To 🤇	)• 🕗• 🛛	🧓 🗞 🔂	<mark>}₀ ‼₀</mark> <mark>}</mark>	🔀 🔚 🔍		
Vorksheet Selector 5 X Cadence_Demo										
👎 Electrical			Objects		Topology		Stub	Max Exposed	Mary Decelled	
Electrical Constraint Set		_	News		Verify	6.1	Length	Length	max Parallel	Layer Sets
Routing	Type	<b>`</b>	Name	Mapping Mode	Schedule	Schedule	mm	mm	mm	
III Wiring	•			•				•	•	
Vias .	Dsn		▼ Cadence_Demo							
Impedance	ECS		DIFF		Yes	Daisy-chain	0.203	17.780	0.000:0.000:0.0	DIFF_CLOCK
Min/Max Propagation Delays										

The routing adheres to this layer set rule (at least for CLOCK+ and CLOCK-) but does give some indication/warning about the lengths of trace material that were ignored in the process. Strictly speaking, it is not realistic for **no** amount of trace to fall outside a layer restriction. So, some is acceptable/ignored.

Objects	gtl	h	Ð	posed Len	gth	Par	rallel		Layer Sets			
		Margin	Max	Actual	Margin	Max		Margin				Length Ignored
Name		mm	mm	mm	mm	mm	Actual	mm	Name	Actual	Margin	mm
			٠	•	•	•	*	•	*	*	•	•
▼ Cadence_Demo		-10.475			-55.190							
ADDRESS(24)												
► DATA(15)												
DATA[020](19)												
DATA1[09](10)												
DDS[010](11)												
MEMORY[029](30)												
CLOCK		-0.509	17.780		12.089	0.000:0.000:0.000			DIFF_CLOCK			
CLOCK+		-0.461	17.780	5.222	12.558	0.000:0.000:0.000	PASS		DIFF_CLOCK	PASS		5.222
CLOCK-		-0.509	17.780	5.691	12.089	0.000:0.000:0.000	PASS		DIFF_CLOCK	PASS		5.692
<b>V</b> D	8	1 101	17 700		52 720	0,000-0,000-0,000	XXXXXX					000000000000000000000000000000000000000

To visualize this, here is the CLOCK+ signal trace shown below.



Now that this is finished, let's move to Vias.

## Maximum via count

Set the maximum number of vias for a trace or net to maintain impedance control and minimize parasitic capacitance. Each via introduces discontinuities and can degrade signal integrity, especially at high frequencies.

The maximum number of vias we will allow on traces that take on the DIFF Constraint set is 4 Vias (ideally it should be 2-3, but 4 can work in our case).

Here is the Constraint set being modified:

Worksheet Selector 🗗 🗙	Cadence_D	emo			
🕈 Electrical			Objects		
🔻 📗 Electrical Constraint Set	_			Max Via	Via Structures
▼ 🖩 Routing	Туре	S	Name	count	
🔛 Wiring	*	*	*	*	*
🧮 Vias 🥢	Dsn		▼ Cadence_Demo		
Impedance	ECS		DIFF	4	
Min/Max Propagation Delays		4			

And here is how the design holds up to that constraint:

Keturn Path	Bus	► DATA1[09](10)			
▼ m Routing	Bus	► DDS[010](11)			
Wiring	Bus	► MEMORY[029](30)			
Vias	DPr	CLOCK	DIFF	4	1
Impedance	Net	CLOCK+	DIFF	4	
Min/Max Propagation Delays	Net	CLOCK-	DIFF	4	3 1
🔠 Total Etch Length	DPr	▼ D	DIFF	4	1

The actual count is green, meaning we are within our 4-via limit. The margin is 1, so we can add one via and still be within the limit.

## Characteristic impedance

Specify target impedance values (e.g.,  $50\Omega$  for single-ended traces,  $100\Omega$  for differential pairs) to minimize reflections and ensure compatibility with specific communication protocols. This involves controlling trace width, spacing, and dielectric properties.

Our manufacturer said they can do 50 0hm single ended impedance on traces but within a 10% tolerance without charging significantly more money. So, we'll go with that option below.

**Note:** The differential impedance can be calculated from the Cross Section Editor for the PCB Stackup. It is found in the OrCAD X Presto PCB Editor menu item **Tools – Cross Section**. How to use the tool to do the calculations is outside the scope of this guide. For now, assume that a 50-ohm single-line impedance is roughly an 85 to 130 Ohm differential impedance.

But use the calculated values for differential impedance from the Cross Section tool, then input those values into the Differential Pair part of the Constraint Set.

The single-ended impedance range could end up being violated for differential traces, depending on the situation, and still be okay for the design to perform.



**TIP**: For Tolerance, you can simply type a value, then the software will assume you mean Ohms. For example, type in 10, then hit Enter. Your software will set it to 10 Ohm. You can type in 10 % instead, however, and it will adjust the Ohm accordingly without you having to calculate it.

The PCB designer routed the traces and they fall outside the single ended impedance range, but that's fine. For traces that need single-ended to be 50 Ohms, it works out fine.

🖽 Return Path								
▼ ■ Net <b>4</b>	Bus	► MEMORY[029](30)						
▼ Im Routing	DPr	CLOCK	DIFF	50	)	10 %		11.412
Wiring	Net	▼ CLOCK+	DIFF	50	)	10 %		11.412
III Vias	Rslt	All Clines		50		10 %	60:66	. 11.412
Impedance	Net	▼ CLOCK-	DIFF	50	)	10 %		11.412
Min/Max Propagation Delays	Rslt	All Clines		50		10 %	60:66	. 11.412
III Total Etch Length	DPr	○   ○ ○ ○ ○ ○ ○ ○ □ □ □	DIFF	50		10 %		20.982

## Propagation delay modeling

Create accurate models of signal propagation delays to account for potential signal degradation during operation. This helps with timing analysis and ensuring proper synchronization in high-speed designs.

We set the Constraint Set values to the ones shown below (**All Drivers/All Receivers** at a **Maximum Delay** of 500 picoseconds = 0.5 nanoseconds).

		· · ·	<u> </u>			
Worksheet Selector 🛛 🗗 🗙	Cadenc	:e_Dem	•			
👎 Electrical			Objects		Mar Dalara	No. Dalar
Electrical Constraint Set	Turne		Nama	Pin Pairs	Min Delay	Max Delay
▼ I Routing	туре	<b>`</b>	Name		mm	mm
🔠 Wiring	*	*	*	*	*	*
🗮 Vias 🥒	Dsn		▼ Cadence_Demo			
Impedance	ECS		DIFF	All Drivers/All Receivers		0.5 ns
Min/Max Propagation Delays		40000				
🌐 Total Etch Length						
Differential Pair						

Then when we check our design (which takes pin delay into consideration) we see that we're within our constraints (we are still within the DIFF Constraint ECSet, as a reminder).

🖿 Net 🔶 🗕	Bus	MEMORY[029](30)					0000000	
▼ 📾 Routing	DPr	▼ CLOCK	DIFF	All Drivers/All Receivers	<b></b> >	0.5 ns		0.07557
III Wiring	Net	▼ CLOCK+	DIFF	All Drivers/All Receivers		0.5 ns		0.08322
🛄 Vias 🥒	PPr	U50.31:U1.H4				0.5 ns	0.41678	0.08322
Impedance	PPr	U50.31:U2.J11				0.5 ns		
Min/Max Propagation Delays	Net	▼ CLOCK-	DIFF	All Drivers/All Receivers		0.5 ns		0.07557
Total Etch Length	ppr	1150 30-111 H3				0.5 ns		

## Total etch length limits

Set maximum trace lengths to avoid critical timing issues and signal degradation. This is particularly important for high-speed signals where longer traces can lead to increased attenuation and skew.

Let's say our total etch must not exceed 85 mm based on calculations from the materials, dissipation factor of the dielectric, conductive material type, etc. That rule gets applied to the Constraint Set under **Maximum Total Etch**, as shown below.

Worksheet Selector 🗗 🕹	<	Cadence_De	mo			
Electrical				Objects	Minimum Total	Maximum Total
Electrical Constraint Set				Name	Etch	Etch
▼ 🖩 Routing		Туре	<b>`</b>	Name	mm	mm
🔠 Wiring		*	*	*	*	*
🔠 Vias		Dsn		▼ Cadence Demo		
🔠 Impedance		ECS		DIFF		85.000
🛗 Min/Max Propagation Delay	5		<u></u>			
🔠 Total Etch Length 🥌						
🌐 Differential Pair						
🔠 Relative Propagation Delay						

Then we check if we're within spec, it shows that we are well within range.

ectrical			Objects		Total Etch Length			Total Etch Length		
Electrical Constraint Set	_	-		Referenced Electrical	Min	Actual	Margin	Max	Actual	Margin
▼ 🛅 Routing	Туре	\$	Name	Cont	mm	mm	mm	mm	mm	mm
Wiring	•	•	•	•						
III Vias	Dsn		Cadence_Demo							6.945
Impedance	NCIs		ADDRESS(24)							
Min/Max Propagation Delays	NCls		► DATA(15)							
Total Etch Length	Bus		► DATA[020](19)					1		
Differential Pair	Bus		► DATA1[09](10)							
Relative Propagation Delay	Bus		► DDS[010](11)					1		
Not Return Path	Bus		MEMORY[029](30)							
Routing	DPr	× • • • • • • • • • • • • • • • • • • •	▼ CLOCK	DIFF				85.000	4	24.717
Wiring	Net		CLOCK+	DIFF		59,140		85.000	59,140	25.860
III Vias	Net		CLOCK-	DIFF		60.283		85.000	60.283	24.717
Impedance	DPr		V D	DIFF				85.000		6.945
Min/Max Propagation Delays	Net		D+	DIFF				85.000	78.055	6.945
Total Etch Length	Net		D-	DIFF				85.000		
Differential Data	00	SS		DIST			1000000000	05 000		100000000000000000000000000000000000000

#### Differential pair rules

Implement specific rules for differential pairs to ensure optimal signal propagation. This includes:

- **Dynamic phase tolerance:** Allow for slight variations in differential pair length matching to account for manufacturing tolerances.
- Static phase control: Set strict length matching requirements to minimize skew between the positive and negative signals.
- **Maximum uncoupled length:** Specify the maximum length that differential pair traces can be routed separately before recoupling.

Interestingly, the differential pair rules are split in which sheet we can use to constrain that differential pair (i.e. we can use Electrical Constraints or Physical Constraints). We recommend using the Electrical Constraint Set rules for Differential Pairs for Uncoupled Length, Static Phase Tolerance and Dynamic Phase, then use Physical Constraint sets for the other parameters on that Differential Pair.

As shown below, we set some differential pair rules in our Electrical Constraint set.

Worksheet Selector 🗗 🗙	Cadence	_Demo						
🗲 Electrical			Objects	Uncoup	Uncoupled Length		Dynam	ic Phase
▼ 📄 Electrical Constraint Set		_	Name	Gather	Max	Tolerance	Max Length	Tolerance
▼ I Routing	Type	<b>`</b>	Name	Control	mm	mm	mm	mm
Wiring	*	•	*	*				
Vias	Dsn		▼ Cadence_Demo					
	ECS		DIFF	Ignore	2.000	6 mm	0.508	10 mil
Min/Max Propagation Delays								

Then in the Net section we can apply them.

	Cadence_Demo	4		
👎 Electrical			Objects	
🔻 🚞 Electrical Constraint Set	_			Referenced
▼ 🖩 Routing	Туре	S	Name	Electrical CSet
🔛 Wiring	•	*	•	* *
🗰 Vias	Dsn		Cadence_Demo	
Impedance	NCIs		ADDRESS(24)	
Min/Max Propagation Delays	NCls		► DATA(15)	
Total Etch Length	Bus		► DATA[020](19)	
Differential Pair	Bus		► DATA1[09](10)	
Relative Propagation Delay	Bus		► DDS[010](11)	
	Bus		MEMORY[029](30)	
▼ I Routing	DPr		🔻 сlock	DIFF
Wiring	Net		▼ CLOCK+	DIFF
III Vias	RePP		U50.31:U1.H4	
Impedance	RePP		U50.31:U2.J11	
Min/Max Propagation Delays	Net		▼ CLOCK-	DIFF
III Total Etch Length	RePP		U50.30:U1.H3	
🔠 Differential Pair 🧖	RePP		U50.30:U2.J12	
Relative Propagation Delay	DPr			DIFF

We see the routing is within range for our signal integrity related constraints we made in the **Electrical Constraint Set** named DIFF.

Objects	Pin	Delay	Uncoupled Length					Static Phase		Dynam	c Phase	
	'in 1	Pin 2	Gather	Length Ignored	Max	Actual	Margin	Tolerance			Max Length	Tolerance
Name	nm	mm	Control	mm	mm	mm	mm	mm	Actual	Margin	mm	mm
•										•		
▼ Cadence_Demo							0.035					
ADDRESS(24)												
► DATA(15)												
► DATA[020](19)												
► DATA1[09](10)												
► DDS[010](11)												
► MEMORY[029](30)					r <del> </del>							
▼ CLOCK			Ignore		2.000		0.168	6 mm		4.905 mm	0.508	10 mil
▼ CLOCK+			Ignore		2.000		0.417	6 mm			0.508	10 mil
U50.31:U1.H4			Ignore	1.472	2.000	1.583	0.417	6 mm			0.508	10 mil
U50.31:U2.J11			Ignore	1.660	2.000	0.828	1.172	6 mm			0.508	10 mil
CLOCK-			Ignore		2.000		0.168	6 mm		4.905 mm	0.508	10 mil
U50.30:U1.H3			Ignore	1.516	2.000	1.832	0.168	6 mm	1.095 mm	4.905 mm	0.508	10 mil
U50.30:U2.J12			Ignore	1.906	2.000	0.828	1.172	6 mm	1.052 mm	4.948 mm	0.508	10 mil

## Relative signal velocity

Understand and account for the relative speed at which signals travel through different PCB materials and trace geometries. This knowledge is crucial for accurate timing calculations and can help prevent board re-spins due to signal integrity issues.

Relative propagation delay applies for Match Groups that need to be length matched within their local group of signals. For instance, if we have signals for DDR like DDR\_DQ0-DDR\_DQ7 and they all need to have their signals arrive within 15 picoseconds of one another or less. There is a way to let the Constraint Manager know this.

In Constraint Manager, in the Electrical category, go to your Net > Relative Propagation Delay worksheet.

Highlight the nets you want to add to a matching group (i.e. DDR\_DQ0 through DDR\_DQ7, for 8 bit), then right click, **Create** - **Match Group...** 

Net	Net	DDR_CS2			
▼ 🖩 Routing	Net	DDR_DQ0	Analyze		
III Wiring	Net	DDR_DQ1	Cross Probe		
III Vias	Net	DDR_DQ2	Eind Eind	Ctrl+E	
Impedance	Net	DDR_DQ3	- Prindini Reel/meerly	Cultr	
Min/Max Propagation Delays	Net	DDR_DQ4			
Total Etch Length	Net	DDR_DQ5	Expand		
🏭 Differential Pair 🛛 🖊	Net	DDR_DQ6	Expand All		
Relative Propagation Delay	Net	DDR DQ7	Collapse		
🧱 Return Path	Net	DDR_DQ8	Create		Class
	Net	DDR_DQ9	Add to	•	Match Group 🚩
	Net	DDR_DQ10	Remove		Net Group
	Net	DDR_DQ11	Rename	F2	Pin Pair
	Net	DDR_DQ12	Delete	Del	Differential Pair
	Net	DDR_DQ13	Compare		Electrical CSet
	Net	DDR_DQ14	Constraint Set References		
	Net	DDR DQ15	Synlara Tanalagy		

Give the match group a name.

Create MatchG	iroup				×
MatchGroup:		MG1			
Selections:					
Name	~	Туре		MatchGrou	p
DDR_DQ7		Net		DDR_DQ	
DDR_DQ6		Net		DDR_DQ	
DDR_DQ5		Net		DDR_DQ	
DDR_DQ4		Net		DDR_DQ	
DDR_DQ3		Net		DDR_DQ	
DDR_DQ2		Net		DDR_DQ	
DDR_DQ1		Net		DDR_DQ	
DDR_DQ0		Net		DDR_DQ	
Preserve Exist	ing M	embership			
Ok		Cancel	He	elp	

Then click Ok. You will get the following image below and the option to change what Constraint Manager cares to constrain.

Objects			Pin Delay			Relative Delay	
News	Referenced Electrical CSet	Pin Pairs	Pin 1	Pin 2	Scope	Delta:Tolerance	Artural
Name			mm	mm		mm	Actual
•	•		•				
▼ Cadence_Demo					Г		
DATA_DIFFS(8)		All Drivers/All Receivers			Global	0 mm:2.54 mm	
► DDR_DQ(32)		All Drivers/All Receivers	1		Global	0 mm:2.54 mm	
▼ MG1(8)		All Drivers/All Receiver: 🔻			Global	0 ns:5 %	
DDR_DQ0		Longest Pin Pair			Global	0 ns:5 %	
DDR_DQ1		Longest Driver/Receiver			Global	0 ns:5 %	
DDR_DQ2		(Clear)			Global	0 ns:5 %	
DDR_DQ3		All Drivers/All Receivers	-		Global	0 ns:5 %	
DDR_DQ4		All Drivers/All Receivers			Global	0 ns:5 %	
DDR_DQ5		All Drivers/All Receivers			Global	0 ns:5 %	
DDR_DQ6		All Drivers/All Receivers			Global	0 ns:5 %	
DDR_DQ7		All Drivers/All Receivers			Global	0 ns:5 %	
ADDRESS(24)							
DATA(15)							

The largest benefit for this constraint type at all is to minimize skew. Skew occurs when two or more signal traces are carrying signals that need to arrive at the receiver at a similar time, but they do not. Instead one signal arrives so early or late, that the information they are supposed to share (using parallel communication) gets out of sync or 'skewed', then the data becomes corrupt. If that happens often enough, you may get a blue screen of death (BSOD) on a computer, as an example of a system that is not unfamiliar with skew.

Note that you can force the trace lengths within a match group to always match their lengths with the Longest Pin Pair found in that group. For example, let's say the longest trace you routed was DDR\_DQ5 at 1600 mils (40.64 mm).

That means any trace in that Match Group DDR\_DQ0 - DDR\_DQ7 must also be 1600 mils (40.64 mm) with some tolerance (but not too much). So the longer we make the longest trace, the longer we must make the other traces to match it. Otherwise, the signals would have skew.

# Match by Longest Driver/Receiver

This is similar to matching by longest pin pair, but the pins just need to be a driver from an IC and a receiver from an IC.

# Match Length to All Driver/All Receivers

This applies the rules to all traces at the same time, but you must specify a target net for the other nets to try and match their lengths with. To do that, go back to the Constraint Manager. Go to the **Electrical > Net > Routing > Relative Propagation Delay** worksheet. Then right click the **Delta:Tolerance** column for one of the nets (e.g. for DDR\_DQ2). Then choose **Set as Target**.

Objects	Pin	Delay			Relative Delay		
	Pin 1	Pin 2	Scope	Delta:Tolerance			
Name	mm	mm		mm	Actual	Margin	
*		*	*	*	*	*	*
Cadence_Demo						0.042 mm	
► DATA_DIFFS(8)			Global	0 mm:2.54 mm		0.042 mm	8
► DDR_DQ(32)			Global	0 mm:2.54 mm			8
▼ MG1(8)			Global	0 ns:5 %			
DDR_DQ0			Global	0 ns:5 %			
DDR_DQ1			Global	0 ns:5 %			
DDR_DQ2			Global	0 ns:5 %			8
DDR_DQ3			Global	0 ns:5 %	Analyze		
DDR_DQ4			Global	0 ns:5 %	Go to source		8
DDR_DQ5			Global	0 ns:5 %	Compare		8
DDR_DQ6			Global	0 ns:5 %	Change		8
DDR_DQ7			Global	0 ns:5 %	Set as target		8

The Constraint Manager will want all other nets within that match group to be within a certain difference (we call it **Delta: Tolerance**) in length from that target net's length. Meaning that if DDR\_DQ2 were suddenly 70 mils long, then all other traces from DDR\_DQ0 and DDR\_DDR3 to DDR\_DQ7 must be 70 mils (1.778 mm) long within a 0 mm difference, and a tolerance of arriving 5% within that length is acceptable for skew for our application.

Important Note: Please note that all values are unique to each specific use case.

## Return path management

Define allowed return paths underneath signal traces to maintain signal integrity and minimize EMI. A continuous, low-impedance return path is crucial for high-frequency signals. Consider using solid ground planes and avoiding splits or gaps in the return path.

For our application, we set the Reference Net to 0, which is our 'Ground' reference (we set layer 2 off as the ground plane).



We then set Reference Layer(s) to the plane that aligns with the behavior of the signals and/or routing of said signals. To keep things simple we select Closest Plane. Just note that if you route your traces on say, the bottom layer (layer 6), and the closest plane happens to be layer 5 of 6, then your signal return path may flow along layer 5 instead of layer 2 (the layer that holds the net 0 that we used as the reference net in the previous cell). With that likely being a voltage difference from the 0 net ground plane, then noise and unwanted EMI may occur. If that is not acceptable, consider using the **Table...** option from the dropdown menu shown below to choose specific planes.



We went with **Closest Plane** for this example. In the remaining cells that go to the right, you can specify the amount of acceptable gaps in the return path, the length of copper to ignore, adjacent void spacings and so on. Managing the return path for signals is just as important as managing the signal routes themselves for impedance control, signal integrity (to reduce impedance discontinuity, and therefore discourage signal reflections) and electromagnetic compatibility. Max Pad Gap set to 30 mils (0.762 mm) and the Length Ignore set to 40 mils (1.016 mm).

Objects	Trace Reference							
News	Reference	Reference	Length Ignore	Max Pad Gap				
Name	Net(s)	Layer(s)	mm	mm				
*	*	*	*	*				
▼ Cadence_Demo								
DIFF	0	Closest Plane	1.016	0.762				

As usual, any values entered are immediately applied to the nets that use this Electrical Constraint Set as seen below. Looks like the design is constrained nicely!



We are at the end of the Electrical Constraints examples that you will need for most high-speed digital designs. Let us continue with Physical Constraints, especially for differential pairs.

# Advanced Physical Constraints

In this section we address the physical constraints in an example physical constraint set that you need to apply for practical high-speed or complex designs. It is understood that you already know how to create constraint sets and apply them to net classes, groups and regions. So, we will only show the constraint set, then where they got applied while giving some context to their importance.

## Trace Width

For physical constraints we already set the Line Width (trace width), the minimum width (narrows down to 0.100 mm = 3.93 mils) and maximum length we allow a neck to run (about 5 mm = 196 mils, but no longer).

Worksheet Selector	Cadence	e_Demo						
🗧 Electrical			Objects	Referenced	Line	Width	N	leck
++ Physical		_	Nama	Physical	Min	Max	Min Width	Max Length
▼ 📕 Physical Constraint Set	Туре	<u> </u>	Name	CSet	mm	mm	mm 🥖	mm
🖩 All Layers 🚽	*			*	•		•	•
By Layer	Dsn		▼ Cadence_Demo	DEFAULT	0.200	0.000	0.150	2.500
▼ Net	PCS		► DEFAULT		0.200	0.000	0.150	2.500
	PCS		► DIFF1		0.127	0.000	0.100	5.000
Region	PCS		POWER		0.500	0.000	0.200	9.000
비田 All Layers	PCS		► RF		0.500	0.000	0.200	5.000

## Differential Pair Advanced Physical Constraints

The Differential Pair values are set as shown below.

Cadence	Cadence_Demo											
Objects Differential Pair												
<b>.</b>		News	Min Line Spacing	g Primary Gap	Neck Gap	(+)Tolerance	(-)Tolerance					
Туре		Name	mm	mm	mm	mm	mm					
*	*	*	*		*	*	*					
Dsn		Cadence_Demo	0.000	0.000	0.000	0.000	0.000					
PCS		DEFAULT	0.000	0.000	0.000	0.000	0.000					
PCS		► DIFF1	0.107	0.127	0.117	0.010	0.010					
PCS		► POWER	0.000	0.000	0.000	0.000	0.000					
PCS		► RF	0.000	0.000	0.000	0.000	0.000					

Then finally we have Vias set for all the Physical Constraint Sets as well.

Cadence_	Demo							
		Objects		BB	/ia Stagger		Allow	
<b>.</b>	_	News	Vias	Min	Max	Pad-Pad	Feel.	-
Туре	<b>`</b>	Name		mm	mm	Connect	Etch	IS
*						*	*	
Dsn		▼ Cadence_Demo	VIA	0.127	0.000	ALL_ALLOWED	TRUE	ANYWHERE
PCS		► DEFAULT	VIA	0.127	0.000	ALL_ALLOWED	TRUE	ANYWHERE
PCS		► DIFF1	VIA	0.127	0.000	ALL_ALLOWED	TRUE	ANYWHERE
PCS		► POWER	VIA	0.127	0.000	ALL_ALLOWED	TRUE	ANYWHERE
PCS		► RF	VIA	0.127	0.000	ALL_ALLOWED	TRUE	ANYWHERE

Notice how all the rules within the constraint sets are applied accordingly (seen below).

Worksheet Selector 8	× Cad	ence_D	em	•								
🕴 Electrical				Objects		Line Width			Neck	Uncouple	ed Length	Static
🖡 Physical					Referenced Physical	Min	Max	Min Width	Max Length		Max	Phase Tolerane
🔻 🛅 Physical Constraint Set	עיי	pe	5	Name	C.M	mm	mm	mm	mm	Gather Control	mm	
All Layers												
By Layer	Dsn			▼ Cadence_Demo	DEFAULT	0.200	0.000	0.150	2.500			
▼ 🛄 Net	NCIS			POWER_GROUP(10)	POWER	0.500	0.000	0.200	9.000			
All Layers	NCIs			► RF(11)		0.500	0.000	0.200	5.000			
▼ Region	NCB			STEVE_PH(9)	DEFAULT	0.200	0.000	0.150	2.500			
I All Layers	Bus			<ul> <li>DATA[020](19)</li> </ul>	DEFAULT	0.200	0.000		2.500			
	Bus			DATA1[09](10)	DEFAULT	0.200	0.000	0.150	2.500			
	Bus			DDS[010](11)	DEFAULT	0.200	0.000	0.150	2.500			
	Bus	****	8	MEMORY[029](30)	DEFAULT	0.200	0.000	0.150	2.500			
	DPr			► CLOCK	DIFF1	0.127	0.000	0.100	5.000	Ignore	2.000	6 mm
	DPr			► D	DIFF1	0.127	0.000	0.100	5.000	Ignore	2.000	6 mm
	DPr			DP_DATA0			0.000	0.100	5.000	Ignore	2.000	
	DPr			DP_DATA1	DIFF1	0.127	0.000	0.100	5.000	Ignore	2.000	6 mm
	DPr			DP_DATA2	DIFF1	0.127	0.000	0.100	5.000			
	DPr			DP_DATA3	DIFF1	0.127	0.000	0.100	5.000	Ignore	2.000	6 mm
	DPr			► DP1	DIFF1	0.127	0.000	0.100	5.000	Ignore	2.000	6 mm
	DPr			STDA_SSRX	DIFF1	0.127	0.000	0.100	5.000	Ignore	2.350	6 mm
	DPr			STDA_SSTX			0.000	0.100	5.000	Ignore	2.000	6 mm

Setting the physical and electrical rules for your differential pairs almost completes differential pairs for your designs. You need to assign spacing constraints to your differential pairs for them to be considered fully 'ready' for high-speed/complex layouts. We will cover the spacing constraints and space-to-space class constraints required for differential pairs.

# Advanced Spacing Constraints

Notice we have standard spacing constraints applied like you would for any standard design, high-speed or not.

Worksheet Selector & X	Cadence_Demo									
🕴 Electrical		Objec	ts		Line To	• Thru Pin T	т. •	Thru Via To	► BB Via To	Microvia To 🔸
++ Physical				Referenced Spacing	All	All		All	All	All
1 Spacing	Туре	\$	Name	- Corr	mm	mm		mm	mm	mm
▼ Spacing Constraint Set						•				
All Layers	Dsn		▼ Cadence_Demo	DEFAULT	0.200	0.200	-	0.200	0.200	0.200
By Layer	SCS		BGA_SPACE		•••			•••		0.127
🔻 🛅 Net	SCS		▼ DEFAULT		0.200	0.200		0.200	0.200	0.200
🔚 All Layers	Цтур		Conductor		0.200	0.200		0.200	0.200	0.200
▼ 💼 Net Class-Class	Шур		► Plane		0.200	0.200		0.200	0.200	0.200
All Layers	SCS		SCS1_POWER_GROUP		0.200	0.200		0.200	0.200	0.200
CSet assignment matrix	Цтур		Conductor		0.200	0.200		0.200	0.200	0.200
Region	tTyp		➢ ▶ Plane		0.200	0.200		0.200	0.200	0.200
All Layers										

Those rules will be applied immediately to any nets using the Constraint Set.

Of keen interest is how to set up spacing for differential pairs. Let's say we want the differential pair traces to be 60 mils (1.524 mm) away from all other objects (except between their own single-ended traces within the diff pairs of course).

In this case, we create a Spacing Constraint Set named SCS\_DIFF (shown below) and set its **Line To** value to 60 mils (1.524 mm). You can double-click the Line To column to see what all objects we are requiring the differential pairs to be at least 60 mils away from, in case you need to do some fine-tuning there.

Worksheet Selector 🗗	Cadence_Demo					
🕴 Electrical		ОЬј	ects		Line To	Т
🔸 Physical			News	Referenced Spacing	All	
1 Spacing	Туре	<u> </u>	Name		mm	
Spacing Constraint Set	•	•	*	*		
All Layers 🔶	Dsn		Cadence_Demo	DEFAULT	0.200	0.20
🖩 By Layer	SCS		BGA_SPACE		***	***
🔻 🛄 Net	SCS		▼ DEFAULT		0.200	0.20
🖩 All Layers	LTyp		Conductor		0.200	0.20
▼ 📗 Net Class-Class	LTyp		Plane		0.200	0.20
🖩 All Layers	SCS		SCS_DIFF		1.524:0.200:1	***
CSet assignment matrix	LTyp		🖉 🕨 🕨 Conductor 🌽		1.524	***
▼ Region	LTyp		Plane		0.200	0.20

But what about differential pair to differential pair spacing? In our design, we don't need diff pairs (like TX and RX) to be more than 20 mils apart. So we need to tell the Constraint Manager that the SCS\_DIFF class members only need to be 20 mils apart from other SCS\_DIFF class members. That will require a Net Class-to-Class spacing.

Before Creating a Class-to-Class spacing, we must ensure that we have Net Classes applied where appropriate. Navigate to the **Net > All Layers** worksheet, then highlight all the nets you want inside a differential pair net class that we will call CLS1\_ DIFF (shown below).

		Objects	
Туре	s	Name	Referenced Spacing CSet
•	•	•	•
Dsn		▼ Cadence_Demo	DEFAULT
NCIs		▼ CLS1_DIFF(6)	DEFAULT
DPr		► DP_DATA0	DEFAULT
DPr		DP_DATA1	DEFAULT
DPr		► DP_DATA2	DEFAULT
DPr		► DP_DATA3	DEFAULT
DPr		► STDA_SSRX	DEFAULT
DPr		► STDA_SSTX	DEFAULT

If you forget any nets, you can CTRL select those as well, then right click and choose **Add To** – **Class** to add them to the CLS1\_DIFF net class.

STDA_SSRX			DEFAULT	0.200	0.2	200	0.200
STDA_SSTX				0 200	0.2	200	0.200
► POWER_GROUP(10)	<u> </u>	Ana	alyze			00	0.200
► RF(11)		Cro	ss Probe			00	0.200
► STEVE(1)	1	Find		Ctrl+I	-	00	0.200
► DATA[020](19)		Boc	okmark		•	00	0.200
► DATA1[09](10)		Exp	and			00	0.200
► DDS[010](11)		Exp	and All			00	0.200
MEMORY[029](30)		Col	lapse			00	0.200
► CLOCK		Cre	ate		•		***
► D		Add	l to		•	Class	
► DP1		Diff	Pair members			Bus	
AEN/		Ren	nove			Net Group	
A0	<u> </u>	Pon	ame	E2		00	0.200
۸ <u>۱</u>		Ren	ame	F2		00	0.200

Now, currently the members of that Net class have default spacing to other nets. We need to change that to the spacing constraint set we created instead SCS\_DIFF.

			Objects		Li
	Type S		Name	Referenced Spacing CSet	
*		*	*	*	*
Dsn			▼ Cadence_Demo	DEFAULT	0.200
NCls			CLS1_DIFF(6)	DEFAULT 🔍	0.200
DPr			DP_DATA0	BGA_SPACE	200
DPr			► DP DATA1	DEFAULT SCS DIFF	200
DPr			► DP_DATA2	SCS1_POWER_GROUP	200
DPr			► DP_DATA3	DEFAULT	0.200
DPr			► STDA_SSRX	DEFAULT	0.200
DPr			► STDA_SSTX	DEFAULT	0.200

However, that will only cause the members of that Net Class to be distanced 60 mils away from other nets outside of the class of differential pairs. While that's desirable, we want the differential pairs to only need to be 20 mils apart or more amongst themselves.



Otherwise, if differential pairs had to be 60 mils away from other diff pairs, it would be near impossible to route differential pairs on a dense PCB. They would be forced to stay 60 mils away from each other, which is not necessary in many cases.

## Class-to-Class Spacing for Differential Pairs to Differential Pairs Spacing

So, for this reason, Class-to-Class spacing is introduced, so that any **CLS1\_DIFF** class object can be 20 mils from any other **CLS1\_DIFF** class object (one differential pair to another).

To implement said class-to-class spacing, click the **Net Class-Class > All Layers** worksheet. Right-click the Cadence\_Demo design, choose **Create** – **Class-Class**.



In this new window, we want the net class on the left to be spaced a certain distance from the net class on the right (CLS1\_ DIFF to itself, basically). Select those classes (CLS1\_DIFF on the left and CLS1\_DIFF on the right as shown), then click Apply, then Ok.

Create ClassClasses	×
NetClasses:	NetClasses:
CLS1_DIFF	CLS1_DIFF
POWER_GROUP	POWER_GROUP
RF	RF
STEVE	STEVE
	Ok Apply Close Help

A new row will appear on the worksheet as a CCIs object underneath a NCIs object...i.e. the CLS1\_DIFF Net class nested under itself as a class-to-class spacing row.

It means that any Net Class underneath that class is what the upper-level class is being spaced against (**CLS1\_DIFF** to **CLS1\_DIFF** spacing). Even if the class is itself like we demonstrate here, that's okay to do.

Cadence_Demo					
	Objects		Line To 🔸		
Toma		News	Referenced Spacing CSet	All	
Туре	3	Name		mm	
*	*	*	*	*	*
Dsn		▼ Cadence_Demo	DEFAULT	0.200	0.2
NCls		▼ CLS1_DIFF(1)	SCS_DIFF	1.524:0.200:1	***
CCls		CLS1_DIFF			
NCIs		POWER_GROUP	SCS1_POWER_GROUP	0.200	0.2
NCIs		RF	DEFAULT	0.200	0.2
NCls		STEVE	DEFAULT	0.200	0.2

Notice that there is no value set for this Class to Class spacing. We can type in the values manually, but as usual, it is better to set a Constraint Set specifically for the spacing we want first, then apply that constraint where appropriate.

So, between this **CLS1\_DIFF** Class and itself, we will make the trace to others spacing equal 20 mils as a minimum, as opposed to 60 mils (basically differential pair members of this class will be 20 mils from trace edge to trace edge to other differential pair members of the same Class).



To make that 20-mil (0.508 mm) spacing, go to the **Spacing Constraint Set** – **All Layers** worksheet, right click the **Cadence\_Demo** cell, then choose **Create – Spacing CSet**...

🕴 Electrical		Object	ls	Line To 🔸	Thru Pin To	SMD	
→ ← Physical	Turna	S Nome		Referenced Spacing CSet	All	All	
1 Spacing	туре	3	Name		mm	mm	
▼ Spacing Constraint Set	•		• /	•			
All Layers	Dsn		▼ Cadence_Demo	DEFAULT	0.200	0.200	0.200
🖩 By Layer	SCS		► BGA_SPA( Analyz	:e		***	***
🔻 📗 Net	SCS		▼ DEFAULT Cross	Probe		0.200	0.200
All Layers	LТур		🕨 🕨 Kondı 🔤 Find		Ctrl+F	0.200	0.200
▼ 📗 Net Class-Class	LТур		► Plane Bookn	nark		0.200	0.200
🛱 All Layers	SCS		▼ SCS_DIFF Expan	d All		*** 📕	***
🔚 CSet assignment matrix	LТур		► Condi Create		•	Spacing CSet	_
▼ 📕 Region	LТур		► Plane		52	0.200	0.200
All Layers	SCS		SCS1 POV	ie	F2	0.200	0.200

We name ours SCS2\_DIFFDIFF, then click Ok, and it gets added to the list. Afterwhich, we set the Line To spacing column cell value to 20 mils (0.508 mm).

	0.200	-
▼ SCS2_DIFFDIFF	0.508	*:
Conductor	0.508	*:
Plane	0.508	*:

We can now use this Spacing Constraint Set to apply it to our Net Class-to-Class spacing, CLS1\_DIFF to CLS1\_DIFF. Navigate back to the **Net Class-Class > All Layers** worksheet. Then choose our newly created **SCS2\_DIFFDIFF** constraint set and apply it as shown below.

	Object	s		Line To 🔸
Type	s	Name	Referenced Spacing CSet	All
ijpe				mm
*	*	*	*	*
Dsn		▼ Cadence_Demo	DEFAULT	0.200
NCls		CLS1_DIFF(1)	SCS_DIFF	1.524:0.200:1
CCls		CLS1_DIFF	SCS2_DIFFDIFF	0.508
NCls		POWER_GROUP	SCS1_POWER_GROUP	0.200
NCls		RF	DEFAULT	0.200
NCIs.		STEVE	DEFAULT	0.200

Now our differential pairs can get as close as 20 mils to other differential pairs within the same class (ruled by **SCS2\_ DIFFDIFF**), while all other objects that are not within that differential pair Net Class will have to be at least 60 mils away from any differential pair (ruled by **SCS\_DIFF**).

Then of course if we need to tighten or loosen the constraint (say 10 mil spacing instead of 20, we can do that in one location instead of many).

## **Constraint Region**

For our constraint region, we created a BGA\_SPACE spacing constraint for BGA areas.

Worksheet Selector	2								
Electrical	ts					Line To			
🔸 Physical	Name	All	Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via
🕽 Spacing 👉 🖉	Name	mm	mm	mm	mm	mm	mm	mm	mm
🔻 📄 Spacing Constraint Set 🔰	<u>.</u>								•
📾 All Layers 🚄 🖊 🔪	▼ Cadence_Demo	0.200	0.200	0.200	0.200	0.200	0.200	0.200	0.200
🔚 By Layer 🛛 🚽	BGA_SPACE		0.080	0.080	0.080	0.080	0.080	0.080	0.080
🔻 🛄 Net 🔰	Conductor	•••	80.000	80.000	80.000	80.000	80.000	80.000	80.000
📕 All Layers 🛛 👌	Plane	***	80.000	80.000	80.000	80.000	80.000	80.000	80.000
🔻 📄 Net Class-Class 🛛 🚽	▼ DEFAULT	0.200	0.200	0.200	0.200	0.200	0.200	0.200	0.200

Then we applied that constraint to the BGA region.

Worksheet Selector 🗗	× Cadence_De	emo			
👎 Electrical		Ob	jects		
→ ← Physical	Туре	s	Name	Referenced Spacin CSet	g
Spacing     Spacing Constraint Set	•	*	•	*	•
All Layers	Dsn		Cadence_Demo	DEFAULT	0.
🖩 By Layer	Rgn		BGA	BGA_SPACE	**
🔻 🛅 Net	Rgn		CONN_FLEX		
🖩 All Layers	Rgn		FLEX		
🔻 🚞 Net Class-Class	Rgn		LCD_FLEX		
🖩 All Layers 🖩 CSet assignment matrix					
▼ Region	11				
▼ Inter Layer					
E Spacing					

Now any objects within the BGA regions on the board will have their own specific spacing and physical rules. The Constraint Manager will adjust trace widths, spacing, etc. automatically while you are routing.

# Œ

# Advanced Same Net Spacing Constraints

In most cases you can leave Same Net Spacing Constraints alone. There are special cases where you might need to delve in here, though. In particular when you have shorts between planes and traces, or your thermal reliefs are giving you issues.

We will leave these constraints as is.

Worksheet Selector 🗗 🗙	Cadence_Demo				
👎 Electrical		Objec	ts		
+ ← Physical \$ Spacing	Туре	s	Name	Referenced Same Net Spacing CSet	Enable DRC By- Layer
I Same Net Spacing	*	*	*	•	*
Same Net Spacing Constraint Set	Dsn		Cadence_Demo	DEFAULT	FALSE
	SNSC		T DEFAULT		FALSE
By Laver	LTyp		Conductor		FALSE
▼ Net	ЦТур		► Plane		FALSE
<ul> <li>■ All Layers</li> <li>▼ ■ Region</li> <li>■ All Layers</li> </ul>					

Advanced Manufacturing Constraints

Manufacturing Constraints have been applied in the following categories and as shown in the images below.

## **Design for Fabrication Constraints**

Fabrication constraints have to do strictly with the printed circuit board features, not component arrangement. We address the constraints we set up in our design accordingly.

## Outline

Vorksheet Selector 🗗 🗙	Name	:dns_WIZD_STKP_	cdns_WIZD_MASK_I	Rcdns_WIZD_EXT_F	cdns_WIZD_INT_R	Rcdns_WIZD_PLN_R
Electrical	•		•			•
🔶 Physical	Constraint set usage	Stackup	Non-Etch	Etch	Etch	Etch
1 Spacing	▼ Outline To	- uning				
1 Same Net Spacing	Trace			0.635	0.635	0.635
Manufacturing	Shape		0.254	0.635	0.635	0.635
Design for Fabrication	All pin pads		0.406	0.635	0.635	0.635
▼ m DFF Constraint Set_	All via pads		0.406	0.635	0.635	0.635
III Outline	All non plated holes		0.508	0.508	0.508	0.508
🗮 Mask	Cutout	0.508				
🇱 Annular Ring	All Non signal geometry		0.254	0.254	0.254	0.254
🗰 Copper Features	Cutout To					
🖽 Copper Spacing	Trace			0.635	0.635	0.635
Silkscreen	Shape		0.254	0.635	0.635	0.635
▼ 🖩 Design	All pin pads		0.406	0.635	0.635	0.635
0utline	All via pads		0.406	0.635	0.635	0.635
🔠 Mask	All non plated holes		0.508	0.508	0.508	0.508
🌐 Annular Ring	Cutout	0.508				
Copper Features	Outline	0.508				
Copper Spacing	All non signal geometry		0.254	0.254	0.254	0.254

## Mask

Worksheet Selector 🗗 🕻	×				Mask	
🗲 Electrical		Name	Constraint set usage	Slivers	Islands	Via Partially Covered With
+ ← Physical				mm	sq.mm	Mask Opening
I Spacing				*		•
Same Net Spacing		Create new>				
- Manufacturing		:dns_WIZD_MASK_R	Non-Etch	0.076		On 📕
Design for Fabrication						
Outline						
III Mask						

# Annular Ring

Worksheet Selector 5	×						
🕈 Electrical		Name	Constraint set usage	Pad to mask	Hole to pad	Hole to antipad	
<ul> <li>← Physical</li> </ul>				Missing mask	mm	mm	Hole to antipad mm • 0.305 0.305 0.305
Spacing     Same Net Spacing		•	•				
S Manufacturing		<create new=""></create>					
Design for Exhrication		cdns_WIZD_MASK_R	Non-Etch 🦰	On	0.000		
		cdns_WIZD_EXT_R	Etch			0.127	0.305
		cdns_WIZD_INT_R	Etch			0.127	0.305
		cdns_WIZD_PLN_R	Etch			0.127	0.305
Annular Ring							

	<b>k</b> :	All vias							
Name	R (		Pad to mask	Hole to pad	Hole to antipad				
		o Missing mask	mm	mm	mm				
*	k -	*	*	*	*				
<create new=""></create>									
cdns_WIZD_MASK_R		On	0.000						
cdns_WIZD_EXT_R		•		0.127	0.305				
cdns_WIZD_INT_R	6			0.127	0.305				
cdns_WIZD_PLN_R	P			0.127	0.305				

# **Copper Features**

This section has a lot of the interesting constraints that engineers can require for their practical designs on the job, such as Flex, Acid Traps (for manufacturers still using acid bath technology) and Negative plane islands oversize.

Worksheet Selector 🛛 🗗 🗙			Minimum 🕨	Flex			•	
Electrical	Name	Constraint set usage	Line width	Min radius on all trace	Max solid fill on shapes	Missing trace		
+ Physical			mm	mm	sq.mm	tapers	Missing pad fillets	Missing T fillets
1 Spacing								
1 Same Net Spacing								
Manufacturing	<create new=""></create>							
	cdns_WIZD_EXT1_R	Etch	0.102					
Design for Fabrication	cdns_WIZD_INT1_R	Etch	0.102					
	cdns_WIZD_PLN1_R	Etch	0.102					
Mask								
🖽 Annular Ring 🧹								
🖽 Copper Features 📕								
E Copper Spacing								

		4 Antenna			Acid	Negative plane islands		
Name	Constraint set usage		s Missing T fillets	Traces	Via	Minimum angle	Minimum area	oversize
		wissing pad mied				deg	sq.mm	mm
•								
<create new=""></create>								
cdns_WIZD_EXT1_R	Etch			On	On	45		
cdns_WIZD_INT1_R	Etch			On	On			
cdns_WIZD_PLN1_R	Etch			On	On			

For Flex PCB Design parameters, it varies greatly depending on the manufacturer. Ask your manufacturer for assistance on the values needed for your Constraint Management tool.

## **Copper Spacing**

We have many manufacturing rules for copper spacing. Those rules vary from External to Internal layers and also planes. See the constraints applied below for an understanding of this idea.

Worksheet Selector 🗗 🕹	K Name	<pre>cdns_WIZD_EXT1_R</pre>	2 cdns_WIZD_INT1_R	3 cdns_WIZD_PLN1_R	
🕈 Electrical					New CSET
→← Physical	Constraint set usage	Etch	Etch	Etch	
🚺 Spacing	▼ Trace to				
Same Net Spacing	Trace	0.083	0.083	0.083	
anufacturing	Shape	0.083	0.083	0.083	i
Design for Fabrication	► Holes				
▼ I DFF Constraint Set	All non plated holes	0.083	0.083	0.083	i .
Outline	All pin pads	0.083	0.083	0.083	
 ∰ Mask	All via pads	0.083	0.083	0.083	
🔠 Annular Ring	All non signal geometry	0.083	0.083	0.083	
🔠 Copper Features	▼ Shape to				
🖽 Copper Spacing 🖊	Trace	0.083	0.083	0.083	
🔛 Silkscreen	Shape	0.102	0.102	0.102	i .
▼ 🖩 <u>De</u> sign	► Holes				
Outline	All non plated holes	0.102	0.102	0.102	j .
🛗 Mask	All pin pads	0.102	0.102	0.102	
Annular Ring	All via pads	0.102	0.102	0.102	i
Copper Features	All non signal geometry	0.102	0.102	0.102	
Copper Spacing	All pin pads to				
	All via pads to				
Design for Assembly	All non plated holes to				
	All non signal geometry to				
	▼ Holes				
	<ul> <li>Plated mechanical hole to</li> </ul>				
Pastemask	▼ Holes				
▶ m Design	Plated mechanical hole	0.102	0.102	0.102	i i
▼ Design for Test	Non plated holes				
Image: The set of t	Non plated mechanic	0.102	0.102	0.102	
▶ 🖩 Design	Same Net				
	▼ Non plated				
	Non plated mechanical hole to				
	▼ Non plated holes				
强 3D	Non plated mechanic	0.102	0.102	0.102	

Even down to the plated and non-plated holes we have set the object to object spacing in acute detail.

## Silkscreen

Silkscreen has its own set of rules that the manufacturer needs to adhere to so that they can reliably manufacture your PCB at yield and at reasonable cost. We set the values below based on our manufacturer's capabilities and requirements (seen below).

Worksheet Selector 🛛 🗗 🗙	L	All pin pads		All via pads	All non plated holes	Min width(line,arc,shape)
Electrical	Name	Constraint set usage	mm	mm	mm	mm
+ ← Physical	•					
1 Spacing	<create new=""></create>					
1 Same Net Spacing	cdns_WIZD_SILK_R	Non-Etch	0.076	0.076	0.076	0.127
nanufacturing						
Design for Fabrication						
▼ I DFF Constraint Set						
Annular Ring						
Copper Features						
E Copper Spacing						

As usual for most PCBs we want to make sure there is no overlapping silkscreen text and none underneath our components, so we set those checks to On.

News				Total and the	T	Text to line	Text to shape	Text to text
Name	Constraint s			lext overlap	lext under component	mm	mm	mm
	•				*		•	•
<create new=""></create>		5						
cdns_WIZD_SILK_R	Non-Etch		On		On	0.127	0.127	0.127

Our fabrication constraints are set to our manufacturer capabilities, now that the fabrication of the PCB is likely to have reasonable first-pass success. Be sure to apply the constraints in the Design section and its subsequent worksheets and objects.

Electrical					
++ Physical			Conductor 🕨		Plane 🕨
1 Spacing	Name	All	тор	All	GND
Same Net Spacing	•		•		•
- Manufacturing	Referenced DFF CSet		cdns_WIZD_EXT_R		cdns_WIZD_PLN_R
Design for Fabrication	▼ Outline To				
▼ IIII DFF Constraint Set	Trace		0.635		0.635
Outline	Shape		0.635		0.635
Mask	All pin pads		0.635		0.635
Annular Ring	All via pads		0.635		0.635
Copper Features	All non plated holes		0.508		0.508
	Cutout				
	All Non signal geometry		0.254		0.254
	Cutout To				
III Mask	Trace		0.635		0.635
Annular Ring	Shape		0.635		0.635
		100000000000		666666666666666666666666666666666666666	000000000000000000000000000000000000000

Notice how we can use different constraint sets for different areas and stackups of the PCB as well. We have some flex regions on the board, so we would have custom values for our various regions. See the image below for an example.

eet Selector 🗗 🗙				Mask	
rical	Name	Referenced DFF CSet	Slivers	Islands	Via Partially Covered With
sical			mm	sg.mm	Mask Opening
cing					
ne Net Spacing	· /	•	·	<u>*</u>	·
ufacturing					
Design for Fabrication	Mask				
Design for Fabrication	STIFFNER_I				
	EXPOXY_IN				
	PASTEMAS				
	SILKSCREEN				
	SOLDERMA	cdns_WIZD_MASK_R	0.076		On
Copper Features	SOLDERMA	cdns_WIZD_MASK_R	0.076		On
Silkscreen	SILKSCREEN				
	PASTEMAS				
	Not in stackup				
III Mask	▼ FLEXI1				
🖽 Annular Ring	▼ Mask				
Copper Features	STIFFNER_I				
Copper Spacing	EXPOXY_IN				
III Silkscreen	COVERLAY I	cdns WIZD MASK R	0.076		On
Design for Assembly	ADHESIVE I				
III DFA Constraint Set	ADHESIVE I				
🇱 Outline	COVERLAY I	cdns WIZD MASK R	0.076		On
🗰 PkgToPkg Spacing	Not in stackup				
III Spacing	Soldermask	cdns WIZD MASK R	0.076		On
🎛 Pastemask	Soldermask	cdns WIZD MASK R	0.076		On

Likewise for Flex Stiffener and LCD Stiffener areas.

		Mask						
Name	Referenced DFF CSet	Slivers	Islands	Via Partially Covered With				
		mm	sq.mm	Mask Opening				
sonennadk	<u></u>							
▼ FLEXI_STIFFENER								
▼ Mask								
STIFFNER_I								
EXPOXY_IN	<b>∠</b>							
COVERLAY_I	cdns_WIZD_MASK_R	0.076		On				
ADHESIVE_I								
EPOXY_INN								
STIFFNER_I								
Not in stackup								
Soldermask	cdns_WIZD_MASK_R	0.076		On				
Soldermask	cdns_WIZD_MASK_R	0.076		On				
▼ LCD_STIFFENER								
▼ Mask								
STIFFNER_I								
EXPOXY_IN	/							
ADHESIVE_I								
COVERLAY_I	cdns_WIZD_MASK_R	0.076		On				
Not in stackup								
Soldermask	cdns_WIZD_MASK_R	0.076		On				

Next are the components, which fall under assembly.

## Design for Assembly Constraints

## Outline

Components need to have sufficient spacing from the outline of the board.

Worksheet Selector	8 >	<	Name	cdns_WIZD_MASK_INNER2_R	cdns_WIZD_MASK_INNER1_R
Electrical			*	• 🕇	• <
+(+ Physical		I	Constraint set usage	Non-Etch	Non-Etch
1 Spacing			Component to outline		
🚺 Same Net Spacing			Component to cutout		
🚽 Manufacturing			Pastemask to outline	0.889	0.889
▼ 📄 Design for Fabrication			Pastemask to cutout	0.889	0.889
A / T / T A D'SE (Relacive) at Sel V A		4			**********
Design for Assembly					
V 🕞 DFA Constraint Set					
🔠 Outline 🥌					

Name	cdns_WIZD_Etch_INNER2_R	cdns_WIZD_Etch_INNER1_R	cdns_WIZD_MASK_BOTTOM_R
	*	*	*
Constraint set usage	Etch	Etch	Non-Etch
Component to outline	1.270	1.270	
Component to cutout	1.270	1.270	
Pastemask to outline			0.889
Pastemask to cutout			0.889

Name	cdns_WIZD_MASK_TOP_R	cdns_WIZD_Etch_BOTTOM_R	cdns_WIZD_Etch_TOP_R	No. COFT
		*	•	New CSET
Constraint set usage	Non-Etch	Etch	Etch	
Component to outline		1.270	1.270	
Component to cutout		1.270	1.270	
Pastemask to outline	0.889			
Pastemask to cutout	0.889			

Then, if need be, as shown above, you can always click on the far right to create a new custom Constraint Set (New CSET) to add to the list of assembly constraints.

## Package to Package Spacing

The IPC-2221 standard requires that components have a minimum spacing from the edge of a component to another component's edge or side, and the side of a component to another component's edge or side. This creates a matrix of spacing that can get complex rather quickly.

## Steps to set up PkgToPkg Spacing:

To set that up, simply select the worksheet found at **Design for Assembly > PkgToPkg Spacing**.

Click the + symbol at the top to create a new CSET, then give it the default name, DFAPKGCS1, then click Ok.



You are met with a blank window that uses the default 25 mil spacing for all edge to edge, edge to side, side to side and side to edge spacing values. However, depending on the component, you need certain spacing, so it is highly recommended to create symbol classifications, then have different symbols within those classifications (groups) so that each symbol can automatically have the right spacing applied to each type of symbol classification (e.g. all connectors, ICs, discretes, etc. having their own S:S, E:E, S:E, E:S spacing rules).

To keep things simple, assume all symbols have the same spacing rules. In that case, select Show symbol classifications...

In the DFA Symbol Browser window, select Create DFA Dev Package Class.

Then choose the Edge Mounted Component option for Package Classes.

Search Manufacturing	Tana		~
▼ 📄 Design for Fabrication	DFA Symbol Browser		×
▼ m DFF Constraint Set	p . Available packages	Selected packages	
III Outline Detail	SOIC 127010287265 20N		
III Mask DFA	a SOIC127P1032X265-20AN		
III Annular Ring	solc127P600X175-8N		
E Copper Features	SOIC254P1077X800-8M		
🖽 Copper Spacing	SOJ127P866X375-32N		
III Silkscreen	SOP50P810X110-48N		
🔻 🛅 Design	SOP65P780X200-28N		
0utline	SOT343N	Dev Package Class X	
🌐 Mask	SOT95P230X109-3N		
🔠 Annular Ring	SU195P24UX114-SN Class Name:		
E Copper Features	STEP3D_MECH_DIMIN		
🔛 Copper Spacing	SW EVO-PH NO GND		
E Silkscreen	TO230P950X240-3N OK	Edge Mounted component	
Design for Assembly	TO254P1410X464-4N	Finger Edge Connector	
▼ Im DFA Constraint Set	TO92	Mechanical Part	
III Outline	ТО99		
PkgToPkg Spacing	TOROID01_3		
III Spacing	USB3A_FEMALE		
🗱 Pastemask	XCF01SVOG20		
🕨 🛅 Design			
▼ Design for Test	Filter Packages 2 Ci	eate DFA Dev Package Class Ok Cancel	Help
DFT Constraint Set			
Design			
Symb	ol names:		
🚨 3D Brov	vse for Symbols Show symbol classifications Purge of	lassified symbols Purge unused symbols	
Properties			

Name the class something like CONNECTORS for example, then click Ok. You get the window below.

DFA Symbol Browser	X
: Available packages	Selected packages
SOIC127P1028X265-20N SOIC127P1032X265-20AN SOIC127P600X175-8N SOIC254P1077X800-8M SOI27P866X375-32N SOP50P810X110-48N SOP50P810X110-48N SOP65P780X200-28N SOT343N SOT95P230X109-3N SOT95P240X114-3N STEP3D_MECH_DIMM STEP3D_MECH_TOPCOVER SW_EVQ-PH_NO_GND T0230P950X240-3N T0254P1410X464-4N T092 T099 TOROID01_3 USB3A_FEMALE XCF01SV0G20	<ul> <li>&gt;</li> <li></li> <li></li> </ul>
Filter Packages	reate DFA Dev Package Class Ok Cancel Help

Now you can start adding components to that class, like any connector footprints/symbols.

To do that, select your desired symbols first (on the left), then the category (on the right), then click the > arrow to move that into that category.



Creating more categories, we can get a list like this below.





Even though some components are remaining on the left, click Ok. The matrix is created among the symbol categories. They can then have their spacings adjusted within the matrix as shown below.

DFA Spread Sheet Format: (Side to Side):(End to End):(Side to End):(End to Side) Default: 25:25:25:25 DFA Table							
Package Name 🔺	Mech_Mech	lc	Emnt_Connectors	Discrete			
Discrete	25:25:25:25	25:25:25:25	25:25:25:25	25:25:25:25			
00030006	25:25:25:25	25:25:25:25	25:25:25:25				
	25:25:25:25	25:25:25:25					
Meth Meth	25:25:25:25						
### Spacing

For general spacing of component assembly to other objects on the PCB, go to the **Design for Assembly > DFA Constraint Set > Spacing** worksheet.

You can click the **<Create new>** cell in the upper left corner to create your own DFA Constraint Set, however, we already have 4 created for us in the four rows shown below.



They mostly have spacing for Pastemask to other objects like Pastemask, Via pad, etc. (seen further on the right of the image above).

TIP: Double-click the Pastemask to column above to expand the view if yours is not showing it.

This section covers general spacing, which has mostly been taken over by the 3D domain within the Constraint Manager.

#### Pastemask

Finally within design for assembly (DFA), we have checks for how much pastemask is on a pad (Pastemask to pad %), if pastemask is missing and the distance of your pastemask to other mask materials.

Vorksheet Selector	8	×	Norma	C	Pastemask to pad		Pastemask to other mask types
Electrical			Name	Constraint set usage	%	Missing pastemask	mm
+ Physical			•	•			
t Spacing			<create new=""></create>				
t Same Net Spacing			cdns_WIZD_MASK_I	Non-Etch	98	On	0.000
nanufacturing			cdns_WIZD_MASK_I	Non-Etch	98	On	0.000
🕈 🚞 Design for Fabrication			cdns_WIZD_MASK	Non-Etch	98	On	0.000
▼ 🖩 DFF Constraint Set			cdns_WIZD_MASK	Non-Etch	98	On	0.000
Uutline				L			
		1					
T Design for Assembly							
PkgToPkg Spacing	/						
Spacing							
Pastemask							

## **Applied Constraints**

Now for all these constraint sets, they need to be applied to have any effect. So remember to go to the Design workbook, then select and apply each of these Constraint Sets accordingly.



#### Design for Test Constraints

Finally there are design for test constraints. Depending on your manufacturer, whether they use Bed of Nails Testing, JTAG, etc., you will need to set these values to their capabilities. Here are screenshots of the settings used for this project.

## Outline

Worksheet Selector	5	×	Name	cdns_WIZD_EXT_R	
👎 Electrical			*	*	New CSET
🔸 Physical			Constraint set usage	Etch	
I Spacing			Test point to outline	3.023	
<b>(1</b> ) Same Net Spacing			Test point to cutout	3.023	
<ul> <li>▼ Design for Test</li> <li>▼ m DFT Constraint Set</li> <li>■ Outline</li> <li>■ Mask and Silkscreen</li> </ul>	,				

### Mask and Silkscreen

Name	cdns_WIZD_MASK_R	
*	*	New CSET
Constraint set usage	Non-Etch	
Test point on solder mask	On	
Test point to silkscreen	0.381	

## Spacing

Name	cdns_WIZD_EXT_R	
*	*	New CSET
Constraint set usage	Etch	
▼ Test point to		
Test point	1.778	
Component	1.016	
All pin pads	0.635	
All via pads	0.635	
All non plated holes	3.023	
Test point under component	On	

#### Probe

	Name	cdns_WIZD_EXT_R	New COTT
*		*	New CSET
	Constraint set usage	Etch	
	Test point minimum pad size	0.889	

Remember to apply all the constraint sets that were created above to your design worksheet in the Constraint Manager.

### Advanced 3D Constraints

We can set spacing for all our devices and by device categories. Luckily the categories created from the Design for Assembly spacing constraint set earlier are applied to this section as well.

#### Component to Component

Basically, you want to create a 3D constraint set. Select the **Add a row** button at the bottom of the worksheet and choose the type of devices being spaced to each other. See the steps shown below.



Create PkgToPkg3DCset					
PkgToPkg3DCset:	PKG3DCS2				
CSet Usage	Spacing3D				
	Ok		Cancel	Help	

Worksheet Selector 🛛 🗗 🗙	PKG3DCS1 +									
7 Electrical ↓↓ Physical			Geometry to Chec	k			Geometry to Chec	k	3D Cle	arances
1 Spacing	From Component	3D	Place Bound	DFA Bound	To Component	30	Place Bound	DFA Bound	Horizontal	Vertical
Same Net Spacing									mm	mm
Sector Manufacturing	•									
	Discrete 5					<b>~</b>			0.000	0.000
Constraint Set Component to Compo Component to Board Component to Rigid-Flex		From D	e 3D Component to Component	o Component Clear	ances	Tc	o Component DISCRETE	•	_	×
Component to Board Edge     M Design		El K M C C C C C C C C C C C C C C C C C C	MNT_CO_GOS ECH_MECH -1367550 6 ADENCE_LOGO APC1005X56N APC1005X56N APC1005X56N APC1005X56N MOV Packages from iow Package from io	; ibrery database s	Geom ♥ 31 ♥ Pi	etry to Check ) ace Bound FA Bound	EMNT_CONNECTOR IC MECH_MECH C-1367550-6 CADEINCE_LOGO CAPC1050X56N CAPC1508X56N CAPC1508X56N CAPC2012X100N Show Packages from Show Packages from Show Package Class	n librery n database ies	Groot	netry to Check ID Mace Bound IFA Bound
		Add Pa	ickage Classes							Cancel

From the above image, click the buttons in the order shown and you will get a row applied to the Component-to-Component constraint set area.

Now you can check 3D to 3D spacing for your discrete components. Or the 3D to place bound, DFA bound, or all three for both categories (Discrete to Discrete).

P	KG3DCS1 +									
			Geometry to Chec	k			Geometry to Check	3D Clearances		
	From Component	20	Dis as Reveral	DIA Round	To Component	20	Dia se Davard	DCA Down d	Horizontal	Vertical
		30	Place Bound	DFA Bound		su /	Place Bound	DFA Bound	mm	mm
	• 🖌	•				•				
	Discrete	<b>~</b>			Emnt_Connectors	<b>~</b>			0.000	0.000

#### Component to Board

Like the previous section (Component to Component Spacing), you can add a row for your Component to Board spacing. Select **EMNT\_CONNECTORS**, then click Ok.



Now that the row is applied, you can set your **3D Clearances** column values for your connectors to **Drill/Slots** or the **Board Edge**.

COMPTOBRDCS1	+				
		Geometry to Check		3D Clea	arances
Component	20			Drill/Slot	Board Edge
	30	Place Bound	Ind DFA Bound	mm	mm
*	*	*	*	*	*
Emnt_Connectors	✓			0.000	0.000

#### Component to Rigid-Flex

Follow similar steps in the Component to Rigid-Flex worksheet.

COMPTORGDFLEXC	S1 +				
		Geometry to Check		3D Clea	arances
Component			DEA Desced	Horizontal	▲ Vertical
	30	Place Bound	DFA Bound	mm	mm
*	*	*	*	*	* 📕
lc	<b>~</b>			0.000	0.000

### Component to Board Edge

Select the Component to Board Edge worksheet, add a row and set the component categories you want to constraint with respect to the board edge (see below).

COMPTOBRDEDGEC	CS1 +			
		Geometry to Check		
Component	20			Clearance
	SD	Place Bound	DFA Bound	mm
*	*	*	*	*
Discrete				0.508

Then remember to apply these constraint sets to relevant parts of your design. For example, click the worksheet under **3D** > **Design > Component to Component**. Then select the constraint you want from the dropdown list and apply it.

Worksheet Selector	Y	
Electrical		Name Referenced package to package 3D CSet
→ ← Physical		
1 Spacing		<u>•</u>
Same Net Spacing		Cadence_Demo
😌 Manufacturing		(Clear) PKG3DCS1
🗟 3D		
▼ 📕 3D Clearance		
🔻 📠 Constraint Set		
🔠 Component to Componen	t	
🔠 Component to Board		
🔠 Component to Rigid-Flex		
🔠 Component to Board Edge		
🔻 🖩 Design		
Component to Component	t	
🖽 Component to Board		
Component to Rigid-Flex		
E Component to Board Edge	9	

Follow the same procedure to apply the constraint sets to your remaining design per category (see the images below).

Worksheet Selector 🗗 🗙		
Felectrical	Name	Referenced package to board 3D CSet
→ ← Physical		
1 Spacing	·	*
1 Same Net Spacing	Cadence_Demo	COMPTOBRDCS1
💙 Manufacturing		
🚳 3D		
▼ 📕 3D Clearance		
▼ 🖩 Constraint Set		
E Component to Component		
🖽 Component to Board		
🖽 Component to Rigid-Flex		
🖽 Component to Board Edge		
🔻 🔚 Design		
E Component to Component		
Component to Board		



Worksheet Selector	8	×		
🗲 Electrical			Name	Referenced package to board edge 3D CSet
→ ← Physical				
I Spacing			*	*
🚺 Same Net Spacing			Cadence_Demo	COMPTOBRDEDGECS1
😂 Manufacturing				
🛍 3D				
<ul> <li>3D Clearance</li> <li>Constraint Set</li> <li>Component to Compo</li> <li>Component to Board</li> <li>Component to Rigid-F</li> <li>Component to Board</li> <li>Component to Board</li> <li>Component to Board</li> <li>Component to Compo</li> </ul>	onen Flex Edge	it ≆ t		
Component to Board	-lex Edge	9		

# Advanced Properties

The Constraint Manager goes a step further and lets you set specific values, properties to each net and component that do not necessarily fit in the above categories. We will give a quick tour on the settings that can be set.

### **Electrical Properties**

Worksheet Selector 🗗 🗙	Cader	Cadence_Demo								
🖗 Electrical			Objects		_					
→ ← Physical		R		Referenced Electrical	Frequency	Period	Duty Cycle	Jitter		
t Spacing	Туре	5	Name		MHz	ns	%	ps		
Same Net Spacing	•		*	*				*		
- Manufacturing	Dsn		▼ Cadence_Demo							
wandacturing	NCls		ADDRESS(24)							
🐸 3D	NCls		DATA(15)							
Properties	Bus		DATA[020](19)							
▼ 🛅 Net	Bus		DATA1[09](10)							
Electrical Properties	Bus		DDS[010](11)							
General Properties	Bus		MEMORY[029](30)							
Route/Vias Keepout Exception	DPr	***	► CLOCK	DIFF						

Cycle to Measure	Offset	Bit Pattern	lgnore (X)Net for Library/Model DiffPairs	Use Arc de- rating	Enable highspeed adjacent layer Keep- outs		
	ns						
*	*	*	*	*	*		
					<b>•</b>		
					<b>F</b>		
				-			
				F	<b>–</b>		

#### **General Properties**

🐓 Electrical			Objects	Valtaria					
→ 🕂 Physical	Turns	c	Name	voitage	Weight	No Rat			
🚺 Spacing	Туре		Name	v					
Same Net Spacing	•	*	*	*	*	*			
Manufacturing	Dsn		▼ Cadence_Demo						
	Net		AEN/						
SD 3D	Net		A0			E.			
Properties	Net		A1						
▼ 🛄 Net	Net		A2			F			
Electrical Properties	Net	3888	A3			п			
General Properties	Net		A4			F			

Ro	ute		Route Ro	estrictions		Testpoints			
Priority	to Shape	Fixed	Fixed No Route		No Pin Escape Prohibit		Quantity	Probe Number	
*	*	*	*	*	*	*	*	*	
	F	=	F	•	=	F			
	F	F	F	F	F	F			
	E	F	F	E	F	E			
	F	F	F	F	F	F			
	E	F	F		F				
	F	F	F	F	-	F			
	=		=	•	•	•			

Backdrill		Sh	ield						
Max PTH Stub	No Gloss	66-14	<b>T</b>	ECL	EMC Critical Net	Ignore Unused Pads Suppression	Retain Net on Vias	Comment	
mm		Shield	Туре				•••••		
*	*	*	*	*	•	•	*	*	
	m			=			-		
	F			F		F	-		
	E C			=			-		
	F			F		F	-		

### Route/Vias Keepout Exception

Electrical			Objects	
🔶 Physical	Tuno	c	Name	Comment
1 Spacing	Type	,	Name	
Same Net Spacing	•			•
Manufacturing	Dsn		▼ Cadence_Demo	
	Bus		▼ DATA[020](19)	
- 3D	Net		DATA.BA0	
🧭 Properties	Net		DATA.BA1	
🔻 🛄 Net	Net		DATA.BA2	
Electrical Properties	Net		DATA.BA3	
General Properties	Net		DATA.BD0	
Route/Vias Keepout Exception	Net		DATA.BD1	

### Component Properties – General

Worksheet Selector 🗗 🗡	< Cade	ence_l	Demo				
🕴 Electrical			Objects		Origin		
+ <b>∲</b> ← Physical	Tune	Type S Name		Count	x	Y	
1 Spacing	туре				mm	mm	
Same Net Spacing	*	*	*	*	*	*	
	Dsn		Cadence_Demo				
	PrtD		▼ AD9850_SOP65P780X2	1			
100 3D	Prtl		U4		51.922	58.180	
🥐 Properties	PrtD		▼ BJT_NPN_BEC_SOT95P	1			
▼ 📕 Net	Prtl		Q1		30.700	2.000	
Electrical Properties	PrtD	***	▼ BJT_NPN_BEC_SOT95P	4			
🖩 General Properties	Prtl		Q4		94.423	48.213	
Route/Vias Keepout Exception	Prtl	***	Q5		94.423	42.083	
Component	Prti		Q6		94.423	35.953	
Component Properties	Prtl	***	Q7		94.423	29.823	
General General	PrtD		▶ BJT_NPN_BEC_TO92_D	1			
Thermal	PrtD	888	BJT_NPN_BEC_TO230P	1			
Swapping	PrtD		BJT_PNP_BCE_SOT95P	1			
Reuse	PrtD	888	▶ BNC-4 SMB 90 IO 901	3			
▼ II Pin Properties	PrtD		► CAP CAPC1005X56N	60			
General	PrtD	****	► CAP CAPC1005X56N	38			
Shapes	PrtD		CAP CAPC1005X56N	19			
🖽 Manufacturing				12222222222			

		Pla	cement			Route Re		
Rotation	Mirrored	Tag	Room	Signal Model	BOM gnor	No Route	No Pin Escape	Auto Renaming
*	*	*	*	*	*	*	*	*
0.000	NO	F				F	F	F
180.000	NO	F				F	F	E
0.000	NO	F				F	F	F
0.000	NO	Ē				F	F	F
0.000	NO	- F				F	F	F
0.000	NO	-				•	•	

Comment	Fixed	No XNet Connection
*	*	*
	F	F
	F	F
	Г	F
	E	F
	F	F
	=	=
100000000000000000000000000000000000000		

### Component Properties – Thermal

Worksheet Selector 🗗 🗙	Cader	nce_D	emo				
🐓 Electrical			Objects	Power	Thata JB	Theta IC	
+++ Physical	Tumo	e.	Nama	Dissipation	Theta-JD	degC/W	
1 Spacing	Туре	3	Name	w	degC/W		
Same Net Spacing	*	*	*	*	*	*	
Manufacturing	Dsn		▼ Cadence_Demo				
	PrtD	888	▼ AD9850_S				
30	Prtl		U4				
Properties	PrtD		▼ BJT_NPN				
▼ 📗 Net	Prtl		Q1				
Electrical Properties	PrtD	888	▼ BJT_NPN				
General Properties	Prti	888	Q4				
Route/Vias Keepout Exception	Prtl	***	Q5				
▼ Component	Prtl		Q6				
Component Properties	Prtl		Q7				
🔛 General	PrtD		► BJT_NPN				
Thermal Thermal	PrtD	888	▶ BJT_NPN				
Swapping	PrtD		▶ BJT_PNP				
Reuse	PrtD	888	▶ BNC-4_S				
▼ II Pin Properties	PrtD		► CAP CAP				
General	PrtD	888	► CAP CAP				
H Shapes	PrtD		► CAP CAP				
🖽 Manufacturing		<del>looo</del>	4			000000000000000000000000000000000000000	

### Component Properties – Swapping

Electrical		Objects	i						
+ Physical	Turne	e	Nama	Component	All Gates	Gates	Gates(ext)	Pins	Swap Group
1 Spacing	Туре	3	Name						
1 Same Net Spacing	•		•	•					
Manufacturing	Dsn		Cadence_Demo						
2 ap	PrtD		▼ AD9850_SOP65						
30	Prtl		> ► U4						
💎 Properties	PrtD		▼ BJT_NPN_BEC						
🔻 🛄 Net	Prtl		▼ Q1						
Electrical Properties	Gtl		F140						
🖩 General Properties	PrtD		▼ BJT_NPN_BEC						
Route/Vias Keepout Exception	Prti								
Component	Prtl		► Q5						
Component Properties	Prtl		► Q6						
General General	Prtl		► Q7						
III Thermal	PrtD		► BJT NPN BEC						
Swapping	PrtD		► BJT NPN BEC						
Reuse	PrtD		BJT PNP BCE						

#### Component Properties – Reuse

F Electrical		Objects						
+ Physical	Turne	e	Nama	id	Instance	Module	Name	PID
3 Spacing	Туре	`	Name					
I Same Net Spacing	•			*				*
Manufacturing	Dsn		Cadence_Demo					
	PrtD		▼ AD9850_SOP6					
SD	Prtl		U4					
Properties	PrtD		▼ BJT_NPN_BEC					
▼ 🛅 Net	Prtl		Q1					
Electrical Properties	PrtD		▼ BJT_NPN_BEC					
General Properties	Prtl		Q4					
Route/Vias Keepout Exception	Prtl		Q5					
▼ Component	Prtl		Q6					
<ul> <li>Component Properties</li> </ul>	Prtl		Q7	1				
🛗 General	PrtD		► BJT_NPN_BEC					
I Thermal	PrtD		► BJT_NPN_BEC					
Swapping	PrtD		► BJT_PNP_BCE					

## Pin Properties – General

Worksheet Selector 🗗 🗶	Cadence_Demo						
🐓 Electrical		Obj	jects				
🔸 Physical	Time		News	Pinuse	Pin Delay	No Pin Swap	Shorting Net
I Spacing	Туре		Name		mm		
Same Net Spacing	*			*			
- Manufacturing	Dsn		▼ Cadence_Demo				
	PrtD		▼ AD9850_SOP65P780X200				
ST S	Prtl		► U4				
Properties	PrtD		▼ BJT_NPN_BEC_SOT95P23				
▼ 🛅 Net	Prtl		<b>▼</b> Q1				
Electrical Properties	Pin		Q1.1				
🖩 General Properties	Pin		Q1.2				
Route/Vias Keepout Exception	Pin		Q1.3				
▼ 📄 Component	PrtD		▼ BJT_NPN_BEC_SOT95P24				
Component Properties	Prtl		▼ Q4				
General General	Pin		Q4.1				
III Thermal	Pin		Q4.2				
Swapping	Pin		Q4.3				
Reuse	Prtl		► Q5				
Im Properties	Prtl		► Q6				
	Prtl		≥ ► Q7				
Manufacturing	PrtD		► BJT_NPN_BEC_TO92_DISC				

ects				Routing			
Name	Voltage Source Pin	age Source No DRC Pin		No Shape Connect	Allow Pin Escape	Tag for ECSet Mapping	XNet Pin Id
*	•	*	*	*	*	*	*
▼ Cadence_Demo							
▼ AD9850_SOP65P780X200							
► U4					-		
▼ BJT_NPN_BEC_SOT95P23							
▼ Q1					-		
Q1.1	-	Π	п	-	-		
Q1.2	-	F	F	F	-		
Q1.3	-	Π	п	-	-		
▼ BJT_NPN_BEC_SOT95P24							
▼ Q4					-		
Q4.1	-	F	F	F	-		
Q4.2	-	F	F	=	-		
Q4.3	-	F	F	F	-		

	Highspeed Adjacent Layer Keep-outs						
Num layer	Short side oversize mm	Long side oversize mm	Symbol definition reference layer	Net Enabled			
*	*	*	*	*			

### Pin Properties – Shapes

Felectrical	ects			Thermal C	onnections
🔸 Physical	Name	Connection Type	Best Connection	Min	Max
1 Spacing					
🚺 Same Net Spacing	·	*	*	*	*
😅 Manufacturing	Cadence_Demo				
3D	▼ AD9850_SOP65P780X20				
Properties	▶ ∪4				
	BJT_NPN_BEC_SOT95P23				
Inet     Inetrical Droportion	V Q1				
	V Q1.1				
	Conductor				
	ТОР				
Component	INNER1				
Component Properties	INNER2				
H General	воттом				
III Thermal	► Plane				
Swapping	► Q1.2				
_ ⊞ <sup>Reuse</sup>	► Q1.3				
▼ II Pin Properties	▼ BJT NPN BEC SOT95P24				
General	<b>V</b> 04				
H Shapes	▶ 041				
🖽 Manufacturing	<b>N</b> 042				

	Thermal Connect Width			
l Fix	ed	Oversized		
m	m	mm		
*		*		
	d Fix mi * 	Image: straight of the straig		

#### Pin Properties – Manufacturing

Electrical			Objects		Backdrill		
+ Physical			Norma	Buchuda	Min Pin Plated Thru Hole	IDF Owner	
Spacing	Туре	3	Name	Exclude	mm		
Same Net Spacing	*	*	*	*	*	*	
Manufacturing	Dsn		Cadence_Demo				
	PrtD		▼ AD9850_S				
2 3D	Prtl		► U4				
Properties	PrtD		▼ BJT_NPN				
r 🚞 Net	Prtl		▼ Q1				
Electrical Properties	Pin		Q1.1				
🖩 General Properties	Pin		Q1.2				
Route/Vias Keepout Exception	Pin		Q1.3				
7 📄 Component	PrtD		▼ BJT_NPN				
<ul> <li>Component Properties</li> </ul>	Prtl		▼ Q4				
	Pin		Q4.1				
Thermal	Pin		Q4.2				
Swapping	Pin		Q4.3				
Reuse	Prtl		► Q5				
	Prti		► Q6				
	Prtl		► Q7				
Snapes	PrtD		▶ BJT_NPN				
	Path						

## Advanced DRCs





### **Constraint Analysis**

The Constraint Manager can be configured to analyze only specific aspects of your design if desired. By default, some of the high-speed constraint considerations you would want are not enabled. If the constraint manager is not set to analyze a constraint, it will not do so in the worksheets.

Let's navigate to the Analysis tool. In the Constraint Manager go to **Analyze – Analysis Mode**. Then the Analysis Modes window appears. You can turn on all the rule checks by checking the top-most checkbox in any category. Also be sure to check options in the lower part of the window like for Minimum propagation Delay, Pin Delay and so on (see image below).

Design						
Electrical	▼ Electrical Modes		/			
Physical			/			
Spacing	Name	Value	On	Off	Batch	
Same Net Spacing	Mark All Constraints					
Assembly	Stub length/Net schedule		×			
<ul> <li>Design for Fabrication</li> </ul>	Max via count					
Outline	Match via count			H	H	
Mask	Max exposed length		Image: A state of the state		n n	
Annular Ring	Propagation delay			- H	п	
Copper Features	Relative propagation delay		<b>~</b>	i i i i i i i i i i i i i i i i i i i	n n	
Copper Spacing	Max parallel			E I	П	
Silkscreen	Impedance		Image: A state of the state		Π	
<ul> <li>Design for Assembly</li> </ul>	Total etch length			Ē	Ē	
Outline	All differential pair checks		Image: A start and a start			
PkgToPkg Spacing	Layer sets		<b>~</b>			
Spacing	Return Path		Image: A state of the state			
Pastemask						
Design for Test	<ul> <li>Electrical Options</li> </ul>					
3 Dimensional						
	DRC Unrouted					
	Minimum Propagation Dela	у				
	Relative Propagation Delay					
	Pin Delay					
	Include in all Propagation E	Delays and in Dif	ferential Pair Pha	se checks		
	Propagation Velocity Factor				1.524e+08	
Z On line DBC			01/			

In general for most complex designs, turn everything on. However, note that the software will use more resources and may become evident in terms of system performance depending on the size of the design and the specifications of your machine.

#### **Final Constraint Design Rule Check**

Let's perform a design rule check (DRC) to see if constraints created are being adhered to.

Close the Constraint Manager if it is open. Then as shown below, in OrCAD X Presto PCB Editor, navigate to the menu and select **View – Panels – Properties**. The Properties Panel will appear. Click on a blank area of the design canvas.



You can pin the panel to keep it active by clicking the thumbtack icon in the upper right corner of the panel. Then to update the design rule check results, click the Out of Date Out of Date icon. That will update the DRC analysis.



When finished, Presto will display the updated Pie Chart (see image below).



You can also review the constraints for your design using the Constraints Panel shown below. You can make it visible by going to the menu in Presto and choosing **View – Panels – Constraints**.

Constra	ints						× 🖈
Q Sea	arch						
1	DFM						
🔻 Sel	ection Filter						
All O	<mark>bjects</mark> Gro	oups					
Trace S	egments Tra	aces l	Line Segmen	ts Lines V	Vires	Vias Fingers	
Compo	onents Pins	Shape	es Voids	Text DRC	Nets	Diff Pairs Buses	
Net Gr	oups Conne	ctions	Virtual Poir	nts			
▼ Ob	iect Hierarchv			_		Ħ	1
Curre	ent Object Ca	dence_	Demo				
Туре	Name	🗲 :tr	+ Physical	L Spacing	<b>E</b> :t		
*	*	*	*	*	*		
Dsn	Cadence_D		DEFAULT	DEFAULT	D		
Rgn	BGA			BGA_SPACE			
NCls	RF(11)		RF	DEFAULT	DE		
NCls	POWE		POWER	SCS1_PO	DE		
NCls	▼ CLS1_D	•	DEFAULT	SCS_DIFF	DE		
CCls	CL			SCS2_DIF			
DPr	DP	DI	DIFF1	DEFAULT	DE		
▼ Ele	ctrical (None)						- 1
	Ba	asic				Advanced	
Rule Se	et		+× 🖬			DRC M	odes
Laver T	vpe All Lave	rs 🔻				Enable All Basic	
						Checks	
Wirin	ıg						
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Verify \$	Schedule		Max Via	Count			
Tota	l Etch Leng	jth = A	\+B+C+D+	·E+F			

▼ Electrical (None)	
Basic	Advanced
Rule Set 📃 🔹 🕂 🔛	DRC Modes
Layer Type All Layers	Enable All Basic Checks
Wiring	
Ratsnest Schedule Stub Length	
Verify Schedule Max Via Count	
Total Etch Length = A+B+C+D+E+F Minimum Maximum C C E E	





#### Board Simulation (Impedance and Crosstalk Analysis Using Sigrity X Aurora)

The entire purpose of proper constraint management is to make the hardware engineer/PCB designer adhere to design and requirement rules to avoid PCB re-spins.

While the Constraint Manager does an excellent task in managing constraints, simulation is the research tool that tells the Constraint Manager what rules need to follow.

In this section of the guide, we simulate to test and see how helpful the Constraint Manager is in ensuring we at least know when we are in and out of limits.

One of the simulations we can run is IR Drop analysis. To access the simulation features in Presto, go to **View - Panels -Analysis Workflows**.

Analysis Workflows 💉 🗙
Q Search
Save Workflow Settings
Load Workflow Settings
Impedance Workflow
Analysis Setup
Analysis Modes:
Net Based 🔹
🗙 Select Nets
Set up ERC Options
Set up Analysis Options
Layout Setup
Crop Area by Selected Nets
Set up Cutting Options
Analysis
Start Analysis
Save Analysis Results
Analysis Results
Load Analysis Results
View Modes:
Net Based 🔍
Single Ended 🔍
View Impedance Tables
View Impedance Visions

**Note**: To use these workflows, you need to have Cadence Sigrity X Aurora installed and it should also be the same version of OrCAD X you are using. For example, if you are using OrCAD X 24.1, then you should have Sigrity X Aurora 24.1 installed as a minimum requirement. You do not need a license for Sigrity X, however. OrCAD X just needs to use the Sigrity X tech stack to execute the simulation.

#### Impedance Workflow

Our first analysis will be the Impedance Workflow. To run the impedance workflow do the following:

- 1. Choose Impedance Workflow.
- 2. Under Analysis Modes, select Net Based.
- 3. Below that, choose Select Nets.

View: Flat	Selected (X)Nets   Net Name Filter: *   Property Filter: *   <   <-   Import List of Nets   Export List of Nets
Apply Selection to All Workflows	0/360 Nets Selected
Excluded DC Nets	OK Cancel Apply

4. Select all the nets on the left (you can click one of the nets, then type Ctrl + A on your keyboard).

5. With all the nets highlighted, click the >> arrow to move all the nets to the right. This means we will analyze all the nets.

**TIP:** In most cases this is not necessary, and we can just add critical nets. The reason to choose fewer nets would be to help the software run more quickly, since simulation can be intensive for larger designs.

6. Click **Apply**, then **OK**. The Select Nets section will then have a check mark next to it.

Analysis Workflows	* ×
Q Search	
Save Workflow Settings	
Load Workflow Settings	
Impedance Workflow	▼
Analysis Setup	
Analysis Modes:	
Net Based 🔹	
Select Nets	
Set up ERC Options	
Set up Analysis Options	

- 7. Click the "Set up ERC Options" text. In the new window, check **Detect and model the coplanar traces** if you want to include that. You can also activate the options across all tabs, but for now we will go with current settings (with **Detect and model the coplanar traces** enabled).
- 8. Click Apply then Ok.

DA Impedance Analysis Parameters Setup	×
Translator Layout Simulation SPDGEN	
ERC	
Impedance Check	
Detect and model the coplanar traces	
$\uparrow$	
	_
OK Cancel Apply	Reset

- 9. Then choose Start Analysis.
- 10. The analysis begins and the progress bar will increase to 100% when it is finished. It can take a few minutes, depending on the number of nets analyzed and the complexity of the PCB. Also, consider the different options you want for analysis. Don't include more options than necessary. But if you select all options, that is fine, too.
- 11. When the simulation is complete, navigate to the lower left section of the **Analysis Workflows** Panel to select **Impedance View**.
- 12. Once selected, the board changes to shadow mode to highlight the nets on the board and all their impedances using a color scale.



**TIP**: You can change the impedance view from single ended traces to differential pair traces by clicking under the Analysis Results section and selecting the dropdown where it says **Single Ended**. Change it to **Diff Pair**. Now the impedance trace view changes accordingly to show your differential pairs and their impedances from the color scale (see below).



Now you can adjust your routing and quickly simulate your design until your impedances are within acceptable limits for your design. There are more options to explore, but the most important is saving your results. To do that, click **Save Analysis Results**, then give the file a name and save it (see below).

Analysis 	> 🌋 SDXC (D:)
Start Analysis	✓ ₩ SDXC (D:)
Save Analysis Result	> 🛅 DCIM
	> 🛅 PRIVATE
Load Analysis Results View Modes:	> 🤰 Network
Net Based 🔻	
Diff Pair 🔻	File name: impedance_analysis_001
View Impedance Tables	Save as type: Binary Files (*.impida)
View Impedance Visions	

**TIP**: The visualization is convenient to spot-analyze the results, but more detailed findings exist. Click the **View Impedance Tables** option within the Analysis Workflows panel, and you will get a full breakdown of all the traces and their impedances shown below.

Simulation Table																
Q Search																
Single Ended Diff																
Summary Table	Summary Table															
						Impedance (Ohm)					Impedance Length (%)				Trace Total	
Net Name 🔺		Vias	No	Ref	Max		Mi	<b>۱</b>	Тур		Мах		Min	Тур	Length	Delay (ns)
*		•		•		•		T		V		•	• 🔻	• 🔻	*	• <b>v</b>
CLOCK+	3		0		124.80		85.60		91.40		0.71		27.53	33.01	59.140	0.401
CLOCK-					124.80		85.60		91.40				27.53	33.01	60.283	0.409
D+					136.20		88.10		94.40		0.87		7.65	64.18	78.055	0.485
D-					136.20		88.10		94.40		0.87			64.18	77.049	0.478
DATA0+					129.20		85.60		85.60		1.94					0.189
DATA0-					129.20		85.60		85.60		1.94				24.939	
DATA1+					115.10		85.60		85.60					35.73		
DATA1-					115.10		85.60		85.60				35.73	35.73	24.947	
DATA2+					118.80		85.60		85.60		1.39		36.93	36.93	27.283	0.189
DATA2-					118.80		85.60		85.60		1.39		36.93	36.93	24.774	
	-			-	*** **		AF 70					_		27.26	07.000	
Impedance (	Ohm)	▲ Le	ngth	Trace I	Delay (ps)	La	yer	Locati	on (x;y)							
•		•	-		•		-		•							
93.70		0.037		0.30		INNER		(36.56	7 42.830							
94.50		0.012				INNER			3 66.660							
97.10		0.025				INNER			0 51.944							
97.20		0.024				INNER		(42.34	3 41.352							
112.00		0.212		1.40				(36.63	4 42.884							
112.30		0.415		2.80				(42.53)	5 31.050							
121.10		0.214				INNER		(36.60	1 42.828							
124.80		0.424		2.80				(26.20	74.000							

Now you don't have to always use TopXplorer to find out whether your traces meet the impedance design requirements.

Next is coupling analysis to see how much crosstalk is on your traces, both visually and tabularly.

#### Coupling Analysis for Crosstalk

The next analysis we will look at is for coupling. Some traces can tolerate a certain level of coupling on them from aggressor traces before the signals are unacceptable. The coupling analysis provides tables and visual indicators of how much coupling and crosstalk are present on them at any time. That way, you can quickly test and iterate through your design decisions and adjust your routing accordingly.

To run coupling analysis do the following:

1. Go to View - Panels - Analysis Workflows.



2. The Analysis Workflow panel is open. Select Coupling Workflow from the dropdown, keep the Analysis Modes on Net Based, then click the **Select Nets** option and you will get a pop-up window.

(X)Net Selection				×
View: Flat   Available (X)Nets  Net Name Filter: *  Property Filter: *  = *	>> -> <<	Selected (X)Nets Net Name Filter: * Property Filter: * A0 A1 A2 A3		
		A4 A5 A6 A7 Import List of Nets	Export	List of Nets
Apply Selection to All Workflows			360/	360 Nets Selected
Excluded DC Nets		ОК	Cancel	Apply

- 3. Select all the nets you're interested in analyzing, then click OK.
- 4. Within the Analysis Workflow panel, select Setup Analysis Options.
- 5. The IDA Coupling Analysis Parameters Setup window appears.
- 6. Choose any settings that apply to your design, then click **Apply**, then **OK**.
- 7. Click Start Analysis.

Layout Setup
Crop Area by Selected Nets
Analysis
Analysis Results
Load Analysis Results
View Modes:
Net Based 🔍
Victim 🔻

8. The coupling analysis begins and can simulate quickly or take a long time, depending on whether analysis was done prior to this step. In any case, the progress bar will let you know (see below).



9. Once finished, navigate to the Analysis Results section, then choose the option **Victim** or **Worst Case** and the views will change accordingly.



### Worst case coupling view

CITCAD X Professional Plus		- 0 ^
File Edit View Setup Tools ECO Manufact	turing Reports Help	Symphony cadence
Analysis Workflows 💉 🗶	Cedence,Demo X	Properties 💉 🗶
Q Search	#Grids Snapping	Q, Search
Save Workflow Settings		##
Load Workflow Settings	Coef [N]	V Selection Filter
Coupling Workflow	100.00	All Objects Groups
Analysis Setup		Trace Segments Traces Line Segments Lines Wires Vias
Analysis Modes:		Fingers Components Pins Shapes Voids Text DRC
Net Based 💌	800	Nets Diff Pars Buses Net Groups Connections
Select Nets		V Status
Set up ERC Options		Herberg de la contraction de l
Set up Analysis Options	75.00	Unplaced Components U/355
Layout Setup		Unrouted Nets 0/374
Crop Area by Selected Nets		Unrouted Connections 0/1926
Set up Cutting Options		Shace Islands 0
Analysis		Unassigned Shapes 0
🗸 Start Analysis		Out of Date Shapes 0
Save Analysis Results		DRC Up to Date
Analysis Results		
Load Analysis Results		Design for Assembly(26)
View Modes:		Design for Fabrication(4012)     Electrical(530)
Net Based 💌	45.00	Spacing(6)
Victim 🔻		
View Coupling Tables		DBC Emere ASTA Sharting Emere
View Coupling Visions	34.00	Waived Errors 0 Waived Shorting Errors 0
		Highlight DRC on Canvas
		-
		Inite man inches mils
	12.00	Sheet A II C U Custom
		Wetth 700,000
		Height 431,000
		▼ Attributes
Visibility Analysis Workflows	📮 💃 📚 A4 🧰 1 🗰 2 📖 3 🗰 4 🗰 7 🗰 4 🗰 7 🗰 4 🗰 9 🗰 10 🗰 11 🗰 12 🛄 14 Net Exced	NAME VALUE
Command Session Log Search		
Auto xProbe		104.789, 27.900 to 0

Victim trace coupling view

10. Save the results by clicking **Save Analysis Results** and giving the file a name, then clicking **Save** as shown below.

Layout Setup		🚞 stepFacetFiles4Map
Crop Area by Selected Nets	🗸 📮 This PC	🔤 symbols
Set up Cutting Options	> 🚟 OS (C:)	
Analysis 	> 🖉 SDXC (D:)	
🚽 Start Analysis	✓ 🖉 SDXC (D:)	
Save Analysis Results	> 🛅 DCIM	
Analysis Results	> 🦰 PRIVATE	
Load Analysis Results	> 🞦 Network	
View Modes:		
Net based •		
Victim 🔻	File name: coupling_analysi	
View Coupling Tables	Save as type: Binary Files (*.cplida)	
View Coupling Visions		
	∧ Hide Folders	

- 11. Your results get saved.
- 12. Before ending this mode, click the **View Coupling Tables** option in the image above and you will get the table shown below.



**TIP**: This feature is amazing, because you can make use of the table to uncover crosstalk issues before they show up as signal attenuation on the test bench!

#### Results

We have completed the design and due to proper constraint management, we have passed the design correctly using the constraints-driven approach to hardware and PCB design.

### Conclusion of Part 5 - Project Example

In Part 5 of the OrCAD X Constraint Management Guide, we explored the practical application of constraints using the Cadence FPGA as a case study. This real-world example highlighted the importance of implementing and managing constraints effectively to ensure successful design outcomes. By demonstrating how to set, analyze, and verify constraints in both schematic and PCB layout, we provided a comprehensive overview of constraint management in a complex design environment equipping you with the knowledge and tools necessary to tackle modern PCB design challenges. By applying these principles, you can enhance the reliability, efficiency, and innovation of your PCB designs, ensuring they meet industry standards and project requirements. You also learned how to use the impedance and coupling workflows to quickly address signal integrity concerns on the fly. This power of analysis is extremely convenient because you won't have to be a signal integrity expert to get the job done. As you continue your design journey, remember that effective constraint management is key to unlocking the full potential of your PCB projects.

## Appendix

The Constraint Manager has an immense library of constraints that it allows you to check for and not all constraints have been addressed. For a complete list of the constraints, in the Constraint Manager, choose the menu Analyze > Analysis Mode. A window will appear that shows all the constraints you can choose to analyze in your design.



The list is massive and provides visual aids and detailed explainer text to clarify what the constraint represents.

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