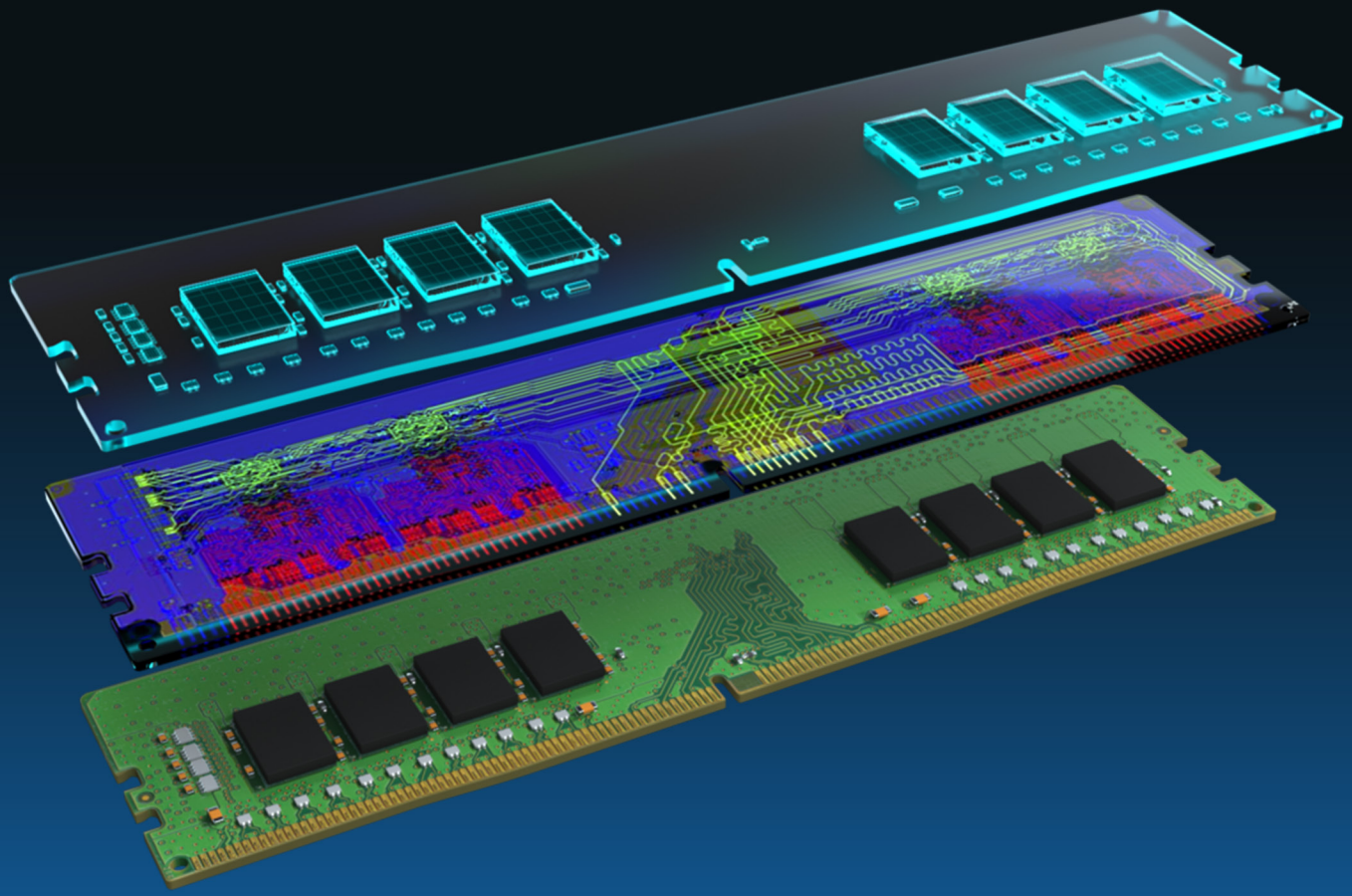
TECHNICAL **EBOOK**

cadence®

OrCAD X High-Speed Digital Design Guide

Part 1 of 3: Understanding High-Speed Digital Design Problems



Contents

Part 1: Understanding High-Speed Digital Design Problems 3

The High-Speed Design Challenge 3

Enter OrCAD X and Presto PCB Editor 4

Introduction to High-Speed PCB Design 4

- What Defines High-Speed Design? 4
- Key Areas of Concern in High-Speed Design 5
  - Constraint Management in OrCAD X 5
- High-Speed Design Problems in Practice 6
  - 1. Impedance Discontinuities 6
  - Common Causes of Impedance Discontinuities 6
  - Solution Implementation in OrCAD X 7
  - Practical Tips for Managing Impedance in High-Speed Designs 7
  - 2. Signal Reflections, Ringing, and Crosstalk 7
  - Signal Reflections and Ringing 8
  - Crosstalk Between Traces 8
  - Practical Tips for Mitigating Reflections and Crosstalk 9
  - 3. Ground Bounce and Power Distribution Noise (PDN) 9
  - 4. Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC) 11
  - Managing These Issues with OrCAD X 12

PCB Transmission Lines and Controlled Impedance 12

- Types of Transmission Lines 12
- Key Factors Affecting Impedance Control 13
- Basics of Routing Differential Pairs and Length Matching 14

PCB Stackup Design 14

- High-Level Overview of Stackup for High-Speed Designs 14
- Material Selection Considerations 15
- Practical Tips for Stackup Design 16

Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC) 16

- Electromagnetic Interference (EMI) 16
- Electromagnetic Compatibility (EMC) 16
- Practical Tips for Managing EMI and EMC in High-Speed Designs 17

Power Integrity 17

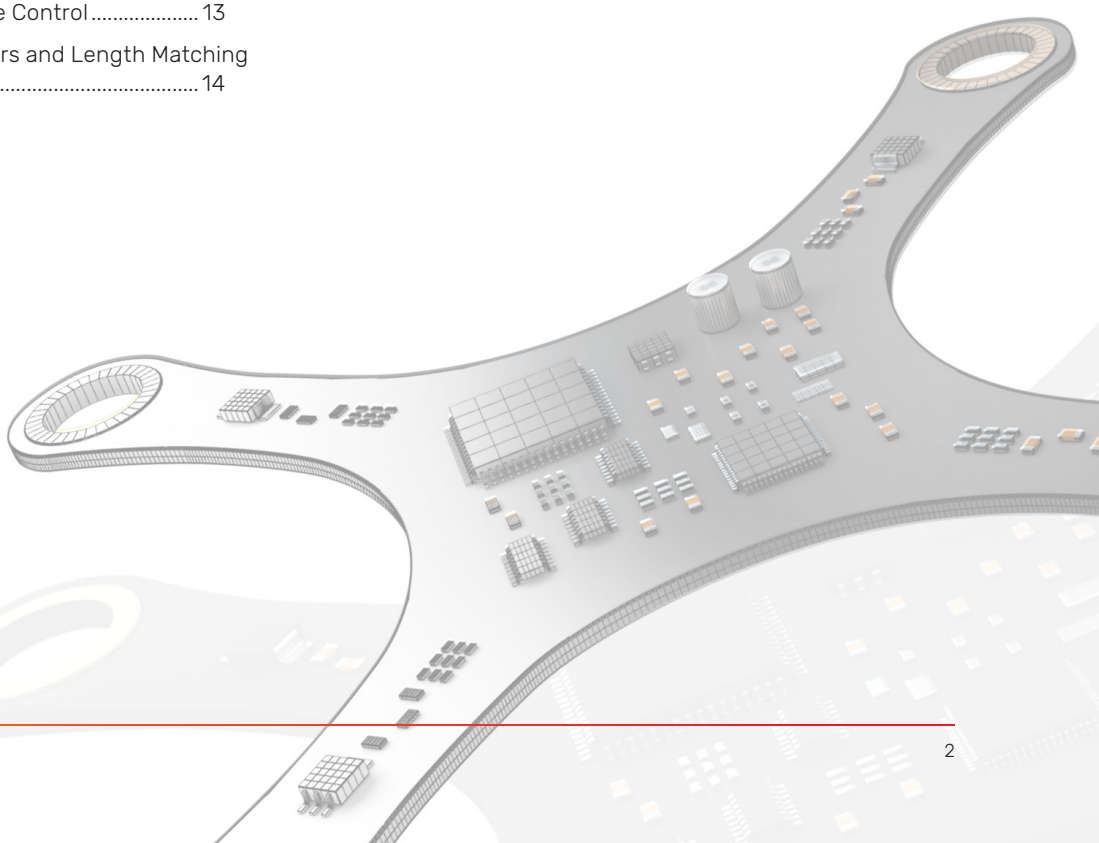
- Overview of Power Distribution Network (PDN) Design 17
- Key Causes of PDN Noise 17
- Simplified Design and Analysis Methods 18
- Practical Tips for PDN Design 18

High-Speed PCB Layout Design 19

- Key Component Placement Strategies 19
- High-Level Routing Techniques 20
- Signal Return Paths and Via Design 20
- Practical Tips for High-Speed Layout 21

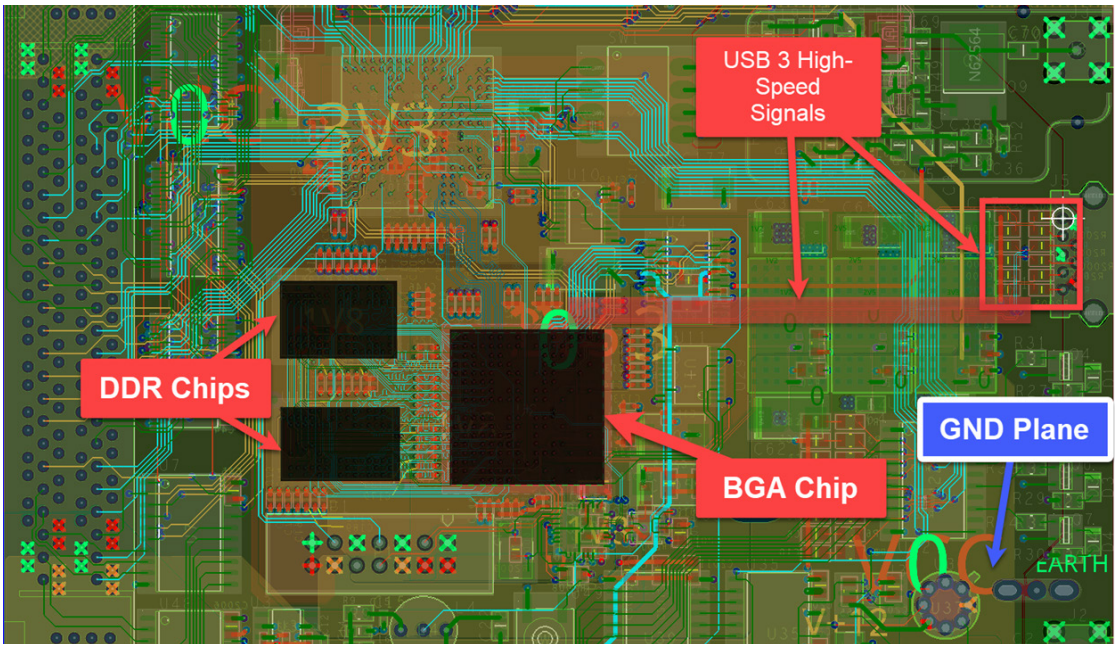
Post-Route Verification and Analysis 22

- Design Rule Checks and Post-Layout Analysis 22
- Design Rule Checks (DRC) 22
- Signal Integrity Analysis 22



Part 1: Understanding High-Speed Digital Design Problems

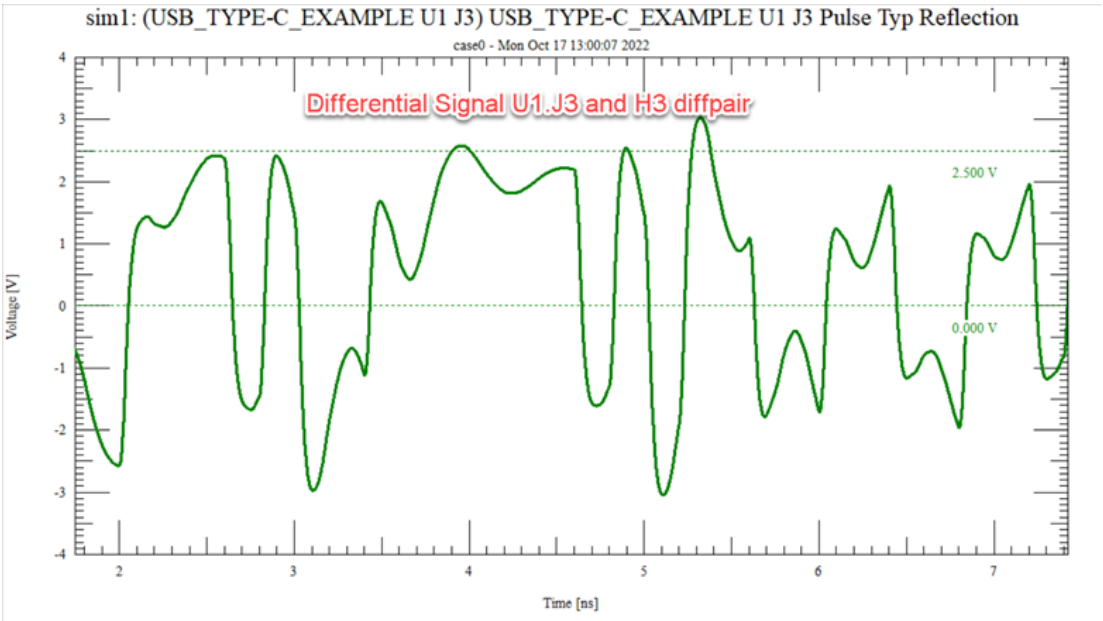
In today's world of rapidly advancing technology, engineers face mounting pressure to design faster, more reliable, and increasingly compact devices. Imagine you're handed a project—a high-frequency circuit with components that push the limits of design, like DDR memory modules and HDMI interfaces running at multi-gigahertz speeds. It's a scenario that demands more than traditional PCB design practices; it requires a structured approach to manage the risks that come with high-speed signals.



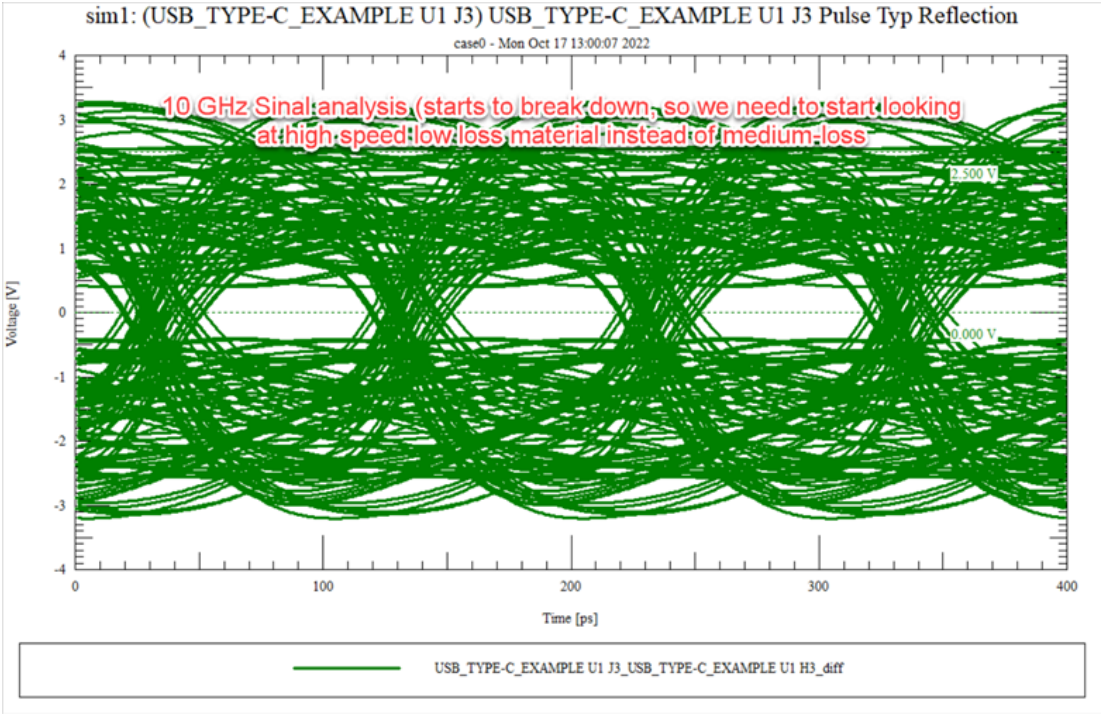
FPGA + DDR2 + DDR3 High-Speed PCB layout

The High-Speed Design Challenge

In the above design, signals are operating at frequencies of billions of oscillations per second. This means even the slightest error in layout can result in significant problems in signal transmission (see images below).



Signal on a trace that experiences too much crosstalk



Collapsing eye diagram of signal trace with too much signal attenuation

As shown in the two images above, at high frequencies (typically 1 GHz and above) and with fast rise times, even minor layout oversights can lead to significant issues. Impedance mismatches can cause signal reflections and degradation. Crosstalk between densely packed traces can blur data signals, while improper power distribution can compromise device performance. These challenges apply not only to RF applications but also to high-speed digital interfaces like USB 3.2 (5-10 Gbps) and PCIe Gen 4 (16 GT/s). The risks are high, and the margin for error is razor-thin, often leading to prototypes that pass initial tests but fail in real-world conditions.

Enter OrCAD X and Presto PCB Editor

This guide offers a pathway through these high-speed challenges, leveraging OrCAD X and Presto PCB Editor as powerful allies in your design process. With constraint-driven design capabilities and comprehensive tools for managing signal integrity, power integrity, and EMI control, these tools allow you to develop reliable, high-performance circuits faster.

In this guide, you will find step-by-step approaches for constraint management, transmission line setup, stack-up design, and post-layout verification. Designed with practicality in mind, each section provides hands-on guidance to help you transition from schematic to finished layout, avoiding costly issues in high-speed designs.

Introduction to High-Speed PCB Design

High-speed PCB design is a specialized field within electronics design that deals with circuits operating at higher frequencies and data rates. These high-speed signals, typically found in applications such as data processing, telecommunications, and consumer electronics, introduce unique challenges that go beyond traditional PCB design practices.

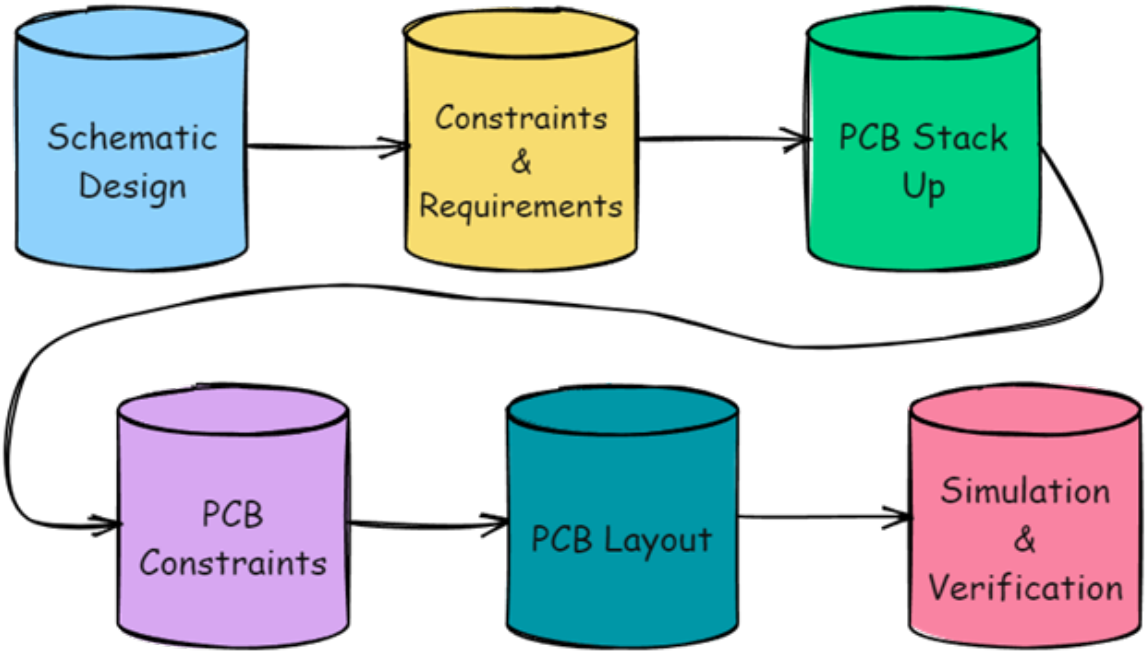
What Defines High-Speed Design?

In essence, high-speed designs are characterized by:

- **High Signal Frequencies:** Signals often exceed frequencies of 50 MHz, where signal behavior diverges from standard low-frequency circuits.
- **Fast Signal Rise Times (<100 ps):** Rapid changes in signal voltage or current lead to reflections, crosstalk, and EMI, making signal integrity a central focus.
- **High Data Transfer Rates:** Designs with data rates above 1 Gbps (0.5 GHz), such as USB 3.0 or DDR interfaces, require careful management of impedance and trace lengths to maintain signal quality.

As frequencies increase, phenomena like signal distortion, ground bounce, and power integrity issues become more pronounced. OrCAD X provides tools that help manage these elements by setting design constraints and enabling precise control over every aspect of PCB design.

Here is the modern constraint-driven approach to hardware design shown below.



Constraint-driven Hardware Design Process

This process leads to few iterations the earlier we incorporate design requirements and constraints at the early stages of the design process.

Key Areas of Concern in High-Speed Design

Incorporating design requirements and constraints includes introducing specific issues that must be addressed at various stages:

- **Signal Integrity (SI):** Ensuring the quality and fidelity of high-speed signals across the PCB is paramount. Impedance control, differential pair matching, and reducing reflection are all critical elements in SI management.
- **Power Integrity (PI):** Power distribution and decoupling must support rapid switching and high current demands without introducing noise or compromising voltage stability. A well-designed Power Distribution Network (PDN) is crucial.
- **Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC):** High-speed signals can radiate and receive unwanted interference, affecting neighboring circuits. Proper shielding, grounding, and trace layout practices mitigate EMI risks and ensure EMC compliance.

This guide will tackle each of these issues, showing how **OrCAD X Capture and Presto PCB Editor** offer practical tools to control these factors, optimize designs, and streamline the path from concept to production-ready PCB.

Constraint Management in OrCAD X

OrCAD X adopts a constraint-driven design methodology, enabling engineers to proactively define parameters for high-speed design elements at the outset of a project. By establishing constraints for signal integrity, power distribution, and EMI control, you can ensure that your high-speed requirements are met throughout the design process.

This constraint-driven approach aligns with the standard requirements-based and architectural methodology prevalent in the industry. This methodology considers numerous factors upfront, using desired benefits and end goals to determine features and specifications such as voltages, noise levels, current levels, and frequency of operation.

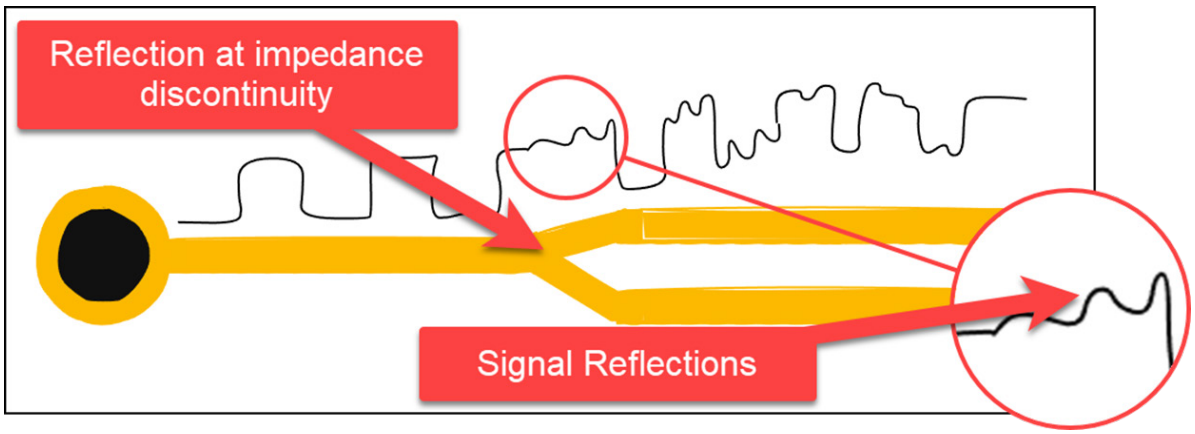
To ensure that design decisions align with project goals and are achieved within acceptable parameters—including time, physical constraints, and electrical efficiency—these features and specifications must be systematically captured. Constraint management in OrCAD X Capture addresses this need with a robust library of constraints that are seamlessly integrated into the design process. This empowers engineers to develop PCBs with confidence, knowing that they will meet product goals. Moreover, if a product or PCB falls short, the constraints framework facilitates troubleshooting by identifying the root cause of the issue and potential solutions.

High-Speed Design Problems in Practice

High-speed PCB design requires more than just placing components and routing traces—it involves managing complex electrical phenomena that emerge at high frequencies (> 1 Gbps) and managing the time flow of signals, while maintaining signal integrity.

Below are the primary high-speed design issues you may encounter and a quick overview of how OrCAD X provides practical solutions for each one.

1. Impedance Discontinuities



Impedance discontinuity from routing causing signal reflections and ringing

- **Problem:** When a signal encounters abrupt changes in impedance, such as through vias, connectors, or trace width changes, reflections occur. These reflections can cause signal distortion, including ringing and waveform degradation.
- **Solution:** Speak with your manufacturer to determine their exact controlled impedance capabilities and boards for your high-speed designs. Maintaining proper impedance is of paramount importance.
- **Tips:** Use impedance-controlled routing for critical high-speed signals, such as differential pairs, and verify performance through its built-in signal analysis tools.

In high-speed PCB design, controlling impedance is critical to maintaining signal integrity. When the impedance of a signal path varies, it causes reflections that degrade the quality of the signal, leading to issues like ringing, overshoot, and data errors. Here, we'll explore common causes of impedance discontinuities, and how OrCAD X helps to manage and mitigate them effectively.

Common Causes of Impedance Discontinuities

Impedance mismatches are introduced when the geometry or environment of a signal trace changes abruptly. Some typical scenarios include:

1. Layer Transitions through Vias:
   - **Problem:** When a high-speed signal transitions between layers through a via, the change in surrounding material (e.g., from trace to via barrel) alters the impedance, resulting in reflections.
   - **Solution:** Use controlled impedance routing settings and set up design rules for via impedance. The Constraint Manager allows you to specify via geometries and layer transitions that minimize impedance disruptions.

2. Trace Width Variations:
   - **Problem:** Impedance is affected by the width of a trace, the spacing from adjacent traces, and the distance to the ground plane. Any change in width, for instance when routing around components, can cause impedance fluctuations.
   - **Solution:** Set trace width constraints to enforce a consistent width across critical high-speed paths. The Design Rule Checks (DRCs) will flag any violations, ensuring that critical traces remain uniform.
3. Proximity to Other Components or Ground Planes:
   - **Problem:** High-speed traces that pass too close to other components or ground planes can experience unintended coupling, impacting impedance.
   - **Solution:** Adjust the clearance constraints in Constraint Manager to maintain the proper spacing between high-speed traces and other components or ground planes.

Solution Implementation in OrCAD X

The Constraint Manager is a powerful tool that allows designers to set and monitor impedance requirements throughout the design. Here's how to set up these constraints to address impedance discontinuities:

1. Setting Up Controlled Impedance:
   - In **Constraint Manager**, define trace width, spacing, and layer stack-up settings to achieve the desired impedance level (typically 50Ω for single-ended signals, 90Ω for differential pairs). Specify these rules for all high-speed nets.
   - The DRC feature will continuously verify that traces meet the defined impedance requirements, flagging any nets that deviate.
2. Defining Via Structures for Layer Transitions:
   - Assign specific via structures to high-speed nets. By defining via parameters (diameter, pad size, and drill depth), you can limit the impedance impact of layer transitions.
   - Use the **Via Management** Tool to select or design via structures that minimize impedance mismatches when transitioning between layers.
3. Enforcing Trace Width Consistency:
   - Apply trace width constraints to high-speed nets in **Constraint Manager** to ensure consistent width along the entire path. This is particularly important for differential pairs, where width and spacing must remain constant to preserve impedance.
   - The tool will flag any deviations, making it easy to correct these issues during routing.

Practical Tips for Managing Impedance in High-Speed Designs

- **Avoid Routing Over Split Planes:** Routing a high-speed trace over a split ground or power plane introduces significant impedance variations. Keep high-speed traces on continuous planes where possible.
- **Use Short, Wide Traces for Vias:** When transitions are unavoidable, use short, wide traces near vias to reduce impedance variation.
- **Simulation and Verification:** Run signal integrity simulations to validate the impact of design changes on impedance. The integrated simulation tools allow you to assess reflections and signal quality, enabling pre-layout verification.

2. Signal Reflections, Ringing, and Crosstalk

Issues like signal reflections and crosstalk can compromise data integrity and lead to inconsistent performance. Let's explore this phenomena, their causes, and how OrCAD X offers solutions for mitigating their effects.

Signal Reflections and Ringing

- **Problem:** Signal reflections occur when a high-speed signal encounters an impedance mismatch along its path. These reflections can cause ringing, which is the oscillation of the signal around its desired level, often manifesting as overshoot or undershoot. This is particularly problematic in high-speed designs, where even minor deviations can lead to data errors and timing issues.

- **Solution:** Set up controlled impedance routing for critical signals, especially single-ended and differential pairs, using the Constraint Manager. By defining impedance targets for high-speed traces, you ensure impedance consistency and reduce reflections.
- Implementation Steps:
  - In **Constraint Manager,** set impedance values for each high-speed net.
  - Use the **Length Tuning** tool to keep trace lengths within acceptable ranges, as reflections are also affected by excessive trace length and mismatched signal paths.

Crosstalk Between Traces

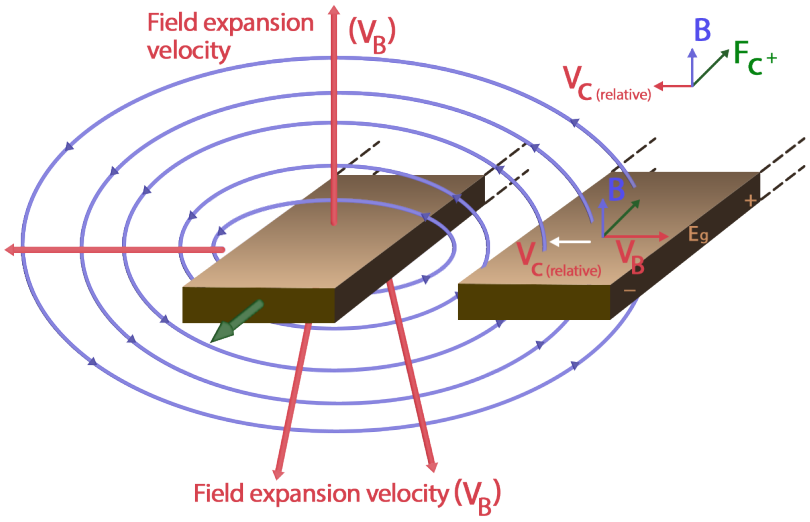


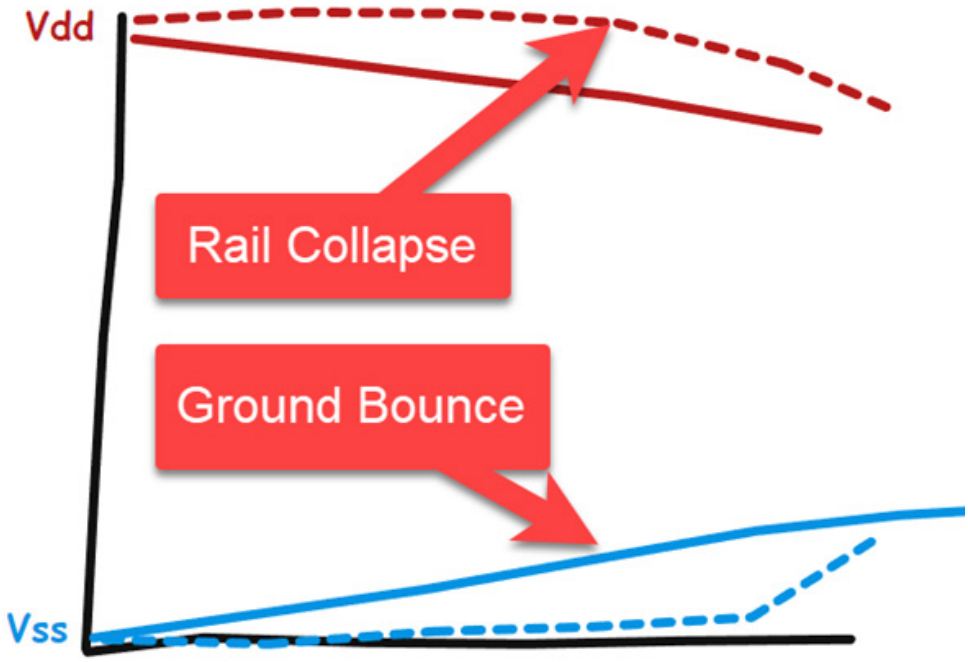
Diagram illustrating crosstalk between two traces running parallel to each other.

- **Problem:** Crosstalk is the unintended coupling of signals between adjacent traces, causing noise and signal interference. This issue is more pronounced in densely packed PCBs with high-frequency signals, as electromagnetic fields from one trace can easily affect another.
- **Solution:** Define trace spacing rules in Constraint Manager to maintain adequate distance between high-speed traces. Additionally, use differential pair routing for noise-sensitive signals, ensuring spacing between pairs is consistent to minimize coupling.
- Implementation Steps:
  - In **Constraint Manager,** set minimum spacing requirements for high-speed nets, especially those prone to crosstalk.
  - For differential pairs, apply consistent spacing and length matching to reduce interference and signal distortion.

Practical Tips for Mitigating Reflections and Crosstalk

- **Use Ground Planes for Shielding:** Place critical high-speed signals adjacent to a continuous ground plane to shield them from interference. Ground planes help contain electromagnetic fields and reduce the risk of coupling.
- **Minimize Stub Lengths:** Stubs, or unused segments of a trace, can act as antennas and introduce reflections. Avoid creating stubs, especially on high-speed nets, or keep them as short as possible.
- **Simulate and Analyze:** Utilize simulation tools to assess the impact of crosstalk and reflections before finalizing the layout. Simulations allow you to visualize potential interference points and validate the effectiveness of spacing and impedance settings.

3. Ground Bounce and Power Distribution Noise (PDN)



Showing how the voltage drops or rises depending on capacitors that were used

- **Problem:** In high-speed designs, rapid switching events cause fluctuations in ground and power planes, known as ground bounce and rail collapse, respectively. This creates power distribution noise, affecting the stability of signals and increasing the risk of data errors.
- **Solution:** See PDN Explanation and Design Steps below (and why it is complicated to calculate)

Designing an optimized Power Distribution Network (PDN) is crucial for ensuring clean and stable power delivery to your circuit, which directly impacts its performance and reliability.

A PDN is essentially the pathway that delivers power from the source to the various components within your circuit. This includes the power and ground traces on your PCB, decoupling capacitors, vias, and any other elements involved in power distribution.

Why PDN Matters:

- **Current flow and impedance:** As current flows through the copper traces on your PCB, the inherent impedance of these traces can cause voltage drops and generate noise.
- **Component sensitivity:** Excessive noise and voltage fluctuations can disrupt the operation of sensitive components and lead to malfunctions or even damage.
- **Signal integrity:** Noise on the power supply can also couple into signal lines, degrading signal integrity and affecting overall circuit performance.

PDN Design is NOT just analysis:

While PDN analysis tools are valuable for identifying potential problem areas, effective PDN design starts at the initial stages of your project. Key aspects include:

1. **Minimizing trace impedance:** Careful selection of trace widths and lengths for power and ground (use wide traces or copper pour wherever possible), along with proper via placement (stitching vias and fanouts), helps to minimize impedance and reduce voltage drops.

2. Decoupling capacitors: Strategic placement of decoupling capacitors provides local energy storage and helps to filter out high-frequency noise.
    a. Decoupling and bypass capacitors must be placed close to their respective voltage sources and device pins to effectively manage power and prevent voltage rail collapse and ground bounce.
    b. Also where possible, use smaller capacitor package types (0402 and 0201 vs 0603 and 0805) because they have smaller leads and therefore lower inductance and impedance.
3. Grounding strategy: A well-designed grounding scheme minimizes ground loops and noise coupling. To achieve proper grounding, you need to create star-based ground connections, so place fanouts to ground and power from each of your parts' pins to allow individual return paths to ground and source paths from power for maximum current carrying capacity.

PDN as a Network of Parasitics:

The PDN can be modeled as a complex network of parasitic capacitors, inductors, and resistors distributed throughout the PCB layout.

By following best practices mentioned in the previous numbered list and applying PDN design principles, you can create a robust power delivery system that ensures the reliable operation of your circuit.

The best way to truly analyze the power distribution network is through simulation and discovery of overall PCB noise when its combined impedances are joined together and multiplied by the currents running through the entire board.

While a precise equation for PDN analysis isn't practical due to the complexity of the interactions (we need multiple equations), a generalized approach can be represented as:

PDN Noise = (Combined Impedance of PDN) × (Currents through the PCB)

Key Points:

- Combined Impedance of PDN: This encompasses the resistance, inductance, and capacitance of all elements within the power distribution network, including planes, traces, vias, and decoupling capacitors.
- Currents through the PCB: These are the currents drawn by all active components on the board.

Impedance Considerations:

- Resistance: Primarily determined by the resistivity of the conductors and the geometry of the traces and planes. Reduce resistance in your conductive material by using smoother materials (speak with your manufacturer) since ragged edges increase resistance through heat and the skin effect.
- Inductance: Influenced by the loop area formed by current paths and the presence of vias. Minimize loop area as much as possible with short, wide traces and large copper pour.
- Capacitance: Affected by the spacing between conductors, dielectric materials, and the presence of decoupling capacitors. Therefore, keep conductive layers of your PCB as close as possible for your manufacturer, to maximize capacitive coupling between traces and their reference planes, and from plane to plane capacitance. Increased capacitance lowers impedance and therefore reduces noise created by current and voltage.

Impedance:

$$Z = R + X_L + X_C$$

Voltage:

$$V = I \times Z$$

Where Z is the impedance of the PCB traces at any given location and over some area, I is the current running through the traces and V is the voltage generated by the current going through said traces and component terminals. This voltage generated applies not only to all your voltages on the PCB but any noise on the 'zero reference' that we usually call 'ground' (it has a voltage, even though it's close to 'zero') as well.

Remember:

This general equation provides a conceptual understanding of PDN behavior. Simulation tools are essential for accurate analysis by way of Maxwell's Equations and optimization of power distribution networks in real-world designs.

- Tips: Use the following to improve your layout:
  - Utilize placement shortcuts like QuickPlace and the ROOM property to efficiently position components and prevent routing issues across split planes.
  - Place decoupling and bypass capacitors adjacent to their intended pins and parts to ensure effective filtering, current delivery, and voltage rail stability.
  - Prioritize capacitor placement close to their associated circuits to optimize their performance in providing necessary filtering and current.

4. Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC)

- Problem: High-speed signals are susceptible to EMI, which can degrade signal integrity and interfere with nearby circuits. Additionally, EMC standards require designs to limit emissions to prevent disruption in other devices.
- Solution: Apply EMI constraints in OrCAD X design rule settings to ensure compliance with EMC standards. Techniques such as controlled impedance, shielding, and optimized ground plane layouts minimize EMI.
- Tips: Use EMI/EMC verification tools to assist in layout practices, including ground plane isolation and proper trace routing techniques, to meet industry & regulatory standards:
  - IEC - International Electrotechnical Commission
  - CISPR - Comité International Spécial des Perturbations Radioélectriques - International Special Committee on Radio Interference
  - FCC - U.S. Federal Communications Commission
  - FAA - U.S. Federal Aviation Administration
  - RTCA - American Radio Technical Commission for Aeronautics
  - UL - Underwriter Laboratories
  - ISO - International Organization for Standardization
  - SAE - Society of Automotive Engineers
  - IEEE - Institute of Electrical and Electronics Engineers
  - MIL-STD 461 - U.S. military set of standards

Managing These Issues with OrCAD X

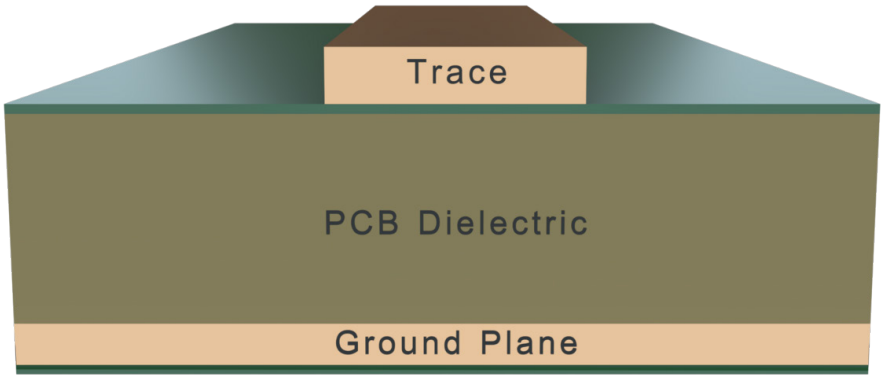
Using constraint-driven tools and having the ability to validate designs in real-time, makes it easy to streamline the process of managing these high-speed design problems. By proactively setting constraints and leveraging the OrCAD X simulation and verification features, designers can tackle high-speed issues upfront, resulting in more reliable designs and fewer prototype iterations.

PCB Transmission Lines and Controlled Impedance

In high-speed PCB designs, controlling impedance is crucial for signal integrity. Transmission lines—specific trace structures on the PCB—help maintain consistent impedance, minimizing signal reflections and preserving signal quality. Here's an overview of common transmission line types and essential factors to consider for impedance control.

Types of Transmission Lines

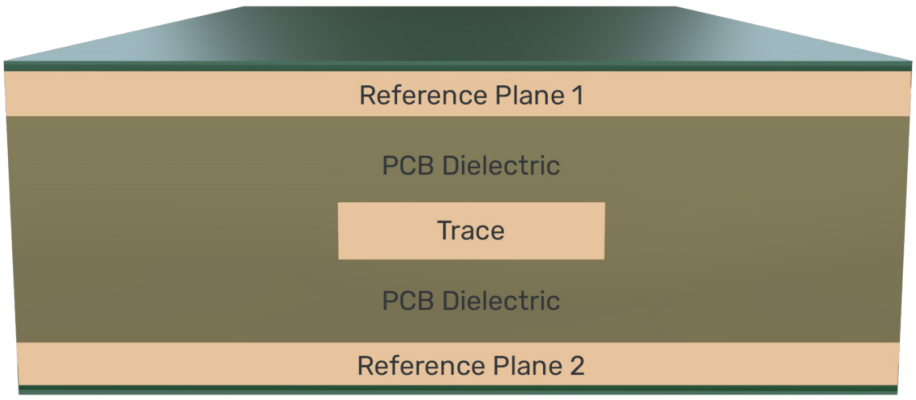
1. **Microstrip:** A single trace routed on an outer layer above a reference ground plane.



Microstrip view on a PCB

- **Application:** Suitable for high-speed signals, often used for signals where surface routing is needed.
- **Impedance Control:** Depends on trace width, height above the ground plane, and PCB material.

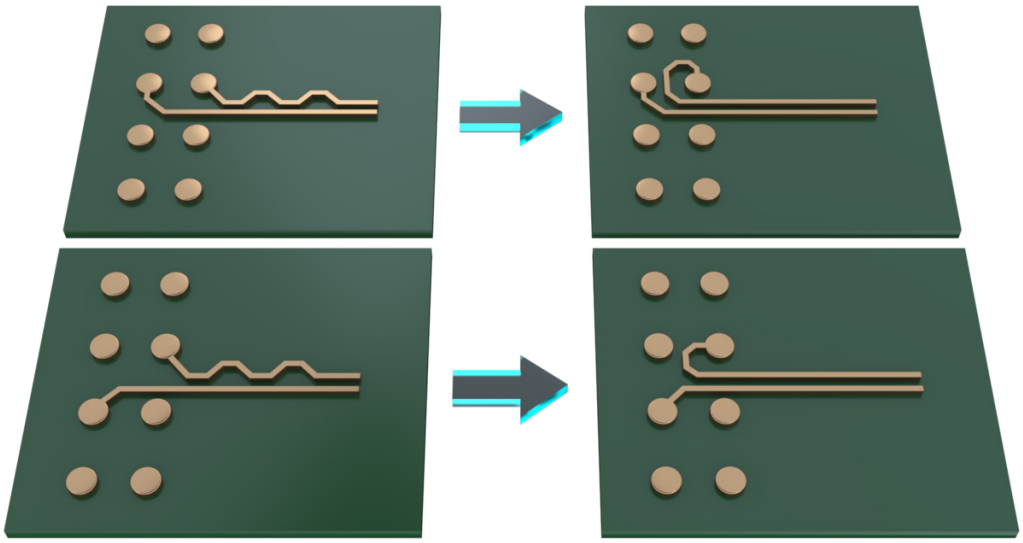
2. **Stripline:** A trace sandwiched between two ground planes within inner layers of the PCB.



Stripline view in a PCB

- **Application:** Provides better isolation from external interference, making it ideal for noise-sensitive signals.
- **Impedance Control:** Controlled by trace width, spacing from ground planes, and dielectric constant of surrounding materials.

3. **Differential Pair:** Two complementary traces (positive and negative) routed close together, used for differential signaling.



Differential Pairs with incorrect (left) and correct (right) tuning

The above images show an important point about differential pairs that sometimes goes overlooked - Differential pairs must be matched in length and symmetry along every millimeter of routing to avoid creating common mode voltage signals, which generate noise and unwanted electromagnetic fields. Delaying both traces by the same amount prevents signal interference. So it is not sufficient to match differential pairs in length only. They must match in the signal phase as well, hence strict adherence to trace symmetry or at least equivalent delay, which is commonly achieved through routing symmetry.

- **Application:** Common in high-speed applications like USB, HDMI, and DDR, as differential pairs are immune to common-mode noise as long as they are routed with proper phase matching.
- **Impedance Control:** Controlled by trace width, spacing between the pairs, and proximity to the ground plane.

Key Factors Affecting Impedance Control

Several factors influence impedance in transmission lines, and controlling them ensures that signals remain within defined impedance thresholds:

- **Trace Width and Thickness:** Wider or thicker traces lower impedance, while narrower traces increase it.
- **Distance to Reference Plane:** The farther a trace is from its reference ground plane, the higher the impedance.
- **Dielectric Constant (Er):** The material between the trace and ground plane affects impedance; materials with lower Er tend to increase impedance.
- **Trace Spacing (for differential pairs):** The distance between differential pair traces affects both their characteristic impedance and coupling strength.

Basics of Routing Differential Pairs and Length Matching

1. **Differential Pair Routing:**
   - Route differential pairs in close proximity to each other with consistent spacing. This maximizes coupling and improves noise immunity.
   - Maintain a consistent gap between the traces across the entire path to control differential impedance.

2. Length Matching:
   - Ensure that each trace in a differential pair is of equal length, so signals arrive at the same time, preventing skew.
   - The **Length Tuning Tool** allows you to fine-tune trace lengths to meet length-matching requirements, ensuring signal timing alignment.

PCB Stackup Design

A well-planned stackup is critical in high-speed PCB design, as it directly impacts signal integrity, power distribution, and EMI/EMC performance. In high-speed applications, stackup decisions determine how effectively signals are transmitted across the board and how well the design manages interference and noise.

High-Level Overview of Stackup for High-Speed Designs

A typical high-speed PCB stackup includes multiple layers to support signal routing, power distribution, and grounding. Common high-speed stackups are designed to optimize impedance control and minimize signal distortion. Here's an example of a basic configuration used for high-speed designs:

OrCAD X Cross-section Editor displaying an 8-layer stackup configuration

1. Top Layer (Signal):
   - Used for high-speed signals and critical components.
   - Directly above a ground plane to ensure controlled impedance.
2. Ground Plane:
   - Placed directly beneath the top signal layer for shielding and to provide a stable reference for impedance.
   - Essential for reducing EMI and crosstalk.
3. Internal Signal Layer1:
   - Used for routing additional high-speed signals.
   - Sandwiched between ground or power planes to form stripline structures, which enhance signal integrity.

4. Power Plane 1:

- Provides a low-impedance path for power distribution.
- Paired with ground planes to create decoupling capacitance, improving power integrity and reducing noise.

5. Ground Layer 2:

- This acts as a reference layer for signals on the bottom of the PCB and for the power plane below it
- Stronger capacitive coupling between this layer and the power plane below.

6. Internal Signal Layer 2:

- Convenient for routing high-speed signals to manage EMI and shield from outside EMI.

7. Power Layer 2:

- Great coupling between this layer and Ground Layer 2, as opposed to Ground Layer 1
- Placed here avoids introducing EMI effects from signal propagation, say from Layer 1 through this Layer.

8. Bottom Layer (Signal or Power):

- May be used for additional signal routing or as an additional power/ground plane, depending on design requirements.
- Typically reserved for less critical signals if used for routing.

Material Selection Considerations

Material choice is a crucial part of stackup design, especially for high-speed PCBs, as it affects signal speed, impedance, and loss characteristics. Here are the main considerations for selecting PCB materials:

1. Dielectric Constant ('Er' or 'Dk'):

- A lower dielectric constant (Er) reduces signal delay, which is beneficial in high-speed designs.
- Materials with stable Er over the board's operating frequency range ensure predictable signal behavior, such as certain high-performance laminates (e.g., Rogers, Isola).

2. Loss Tangent (Df):

- The loss tangent measures how much signal energy is lost as heat. Lower Df values are preferable for high-speed designs to minimize signal loss.
- Common materials with low Df include high-frequency laminates like FR-408 and Megtron 6.

3. Thermal Stability:

- High-speed PCBs can generate significant heat, so materials must have good thermal stability to prevent warping or dielectric breakdown.
- Look for materials with high glass transition temperature (Tg) and thermal conductivity, ensuring the board performs reliably under operating conditions.

4. Cost Considerations:

- High-performance materials can be more expensive, so it's essential to balance performance needs with cost constraints.
- A good compromise is using an FR4 core for most layers while adding specialized low-loss materials for the high-speed signal layers.

Practical Tips for Stackup Design

- Keep High-Speed Signals Adjacent to Ground Planes: Placing high-speed layers next to ground planes helps control impedance and minimize EMI.
- Minimize Layer Transitions: Limit the number of vias and layer transitions in high-speed signals to reduce impedance mismatches and signal reflections.
- Use Symmetric Stackup Design: A symmetrical stackup helps reduce mechanical stress during manufacturing and prevents warping, contributing to a more reliable design.

Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC)

As frequencies and data rates increase in high-speed PCB designs, controlling electromagnetic interference (EMI) and ensuring electromagnetic compatibility (EMC) become crucial. EMI can degrade the performance of nearby circuits and, if not controlled, may cause the device to fail regulatory EMC standards. Managing EMI/EMC effectively requires careful design practices and layout strategies.

Electromagnetic Interference (EMI)

- Problem: EMI arises when high-speed signals radiate unwanted electromagnetic waves that can interfere with neighboring circuits or external devices. High-speed traces and components with rapid switching, such as microprocessors and memory modules, are common sources of EMI.
- Solution: Set EMI constraints in the Constraint Manager and employ techniques like shielding and controlled impedance to minimize radiation. OrCAD X also has simulation tools to evaluate potential EMI issues before the final layout.
- Implementation Steps:
  - Define trace width and spacing constraints in Constraint Manager to control impedance and reduce radiated emissions.
  - Use ground planes and shielding to contain EMI, especially around high-frequency traces and sensitive components.

Electromagnetic Compatibility (EMC)

- Problem: EMC ensures that the device can operate without interference from or with other electronic devices. Devices need to meet EMC regulatory standards, such as FCC or CE certification, which place limits on emissions.
- Solution: Define EMC compliance constraints, ensuring that layout practices minimize emissions and comply with regulatory standards.
- Capabilities in OrCAD X Presto:
  - You may use Presto PCB Editor to place shielding and define enclosure grounding points, creating barriers that prevent interference from escaping the device.
  - Set up trace clearance and spacing rules in Constraint Manager to ensure sensitive signals are isolated from potential EMI sources.
  - Check for some level of EMC compliance using the Impedance or Coupling analyses tools that are integrated, allowing for early detection of areas needing shielding or rerouting.

Practical Tips for Managing EMI and EMC in High-Speed Designs

- Minimize Trace Loops: EMI is often generated by looped traces that act like antennas. Keep trace loops as short and compact as possible, especially for power and high-speed signals.
- Use Solid Ground Planes: Continuous ground planes adjacent to high-speed signals reduce EMI by absorbing and containing electromagnetic fields.
- Run Differential Pairs for High-Speed Signals: Differential pairs help balance the electromagnetic fields between traces, reducing radiated emissions. The constraint settings and parameters for differential pair routing help maintain consistent spacing and length, in the Electrical and Physical rule sets within the Constraint Manager, even for extended nets.
- Shield Sensitive Components: Physically shield components that are prone to or produce EMI. Use metal shielding enclosures in the design for critical areas and ground them properly.

Power Integrity

In high-speed PCB designs, maintaining power integrity is essential to ensure stable and noise-free power delivery across the board. An effective Power Distribution Network (PDN) design minimizes fluctuations, reduces noise, and maintains voltage stability, allowing high-speed components to function optimally.

Overview of Power Distribution Network (PDN) Design

The PDN supplies stable voltage levels to all active components while managing power noise and minimizing impedance across the board. A well-designed PDN provides a low-impedance path from the power source to each component, ensuring smooth and consistent power flow, even during high-speed switching events. Typical PDN design elements include:

- **Power and Ground Planes:** Dedicated planes in the PCB stackup for power and ground reduce impedance and provide an effective path for current flow.
- **Decoupling Capacitors:** Placed strategically near high-speed ICs, decoupling capacitors filter high-frequency noise, stabilizing voltage levels.
- **Stitching Vias:** Connecting power and ground planes across layers helps reduce ground bounce and ensures even voltage distribution.

Key Causes of PDN Noise

PDN noise can arise from several factors, particularly in high-speed applications where rapid switching causes voltage fluctuations. Here are some common sources:

- **Ground Bounce:** When multiple ICs switch simultaneously, it creates fluctuations in the ground potential, leading to noise in the PDN.
- **Simultaneous Switching Noise (SSN):** High-speed digital signals, such as clock signals or data lines, can introduce noise due to large numbers of transistors switching at once, affecting power stability.
- **Inductive Effects:** Vias, connectors, and power planes introduce inductance into the PDN. This can cause voltage spikes or drops, particularly during high-speed operation.

Simplified Design and Analysis Methods

To ensure power integrity, designers use a combination of target impedance strategies, careful decoupling capacitor placement, and PDN analysis tools. Here's a simplified approach to PDN design and analysis:

1. Target Impedance:

- **Definition:** Target impedance is the maximum PDN impedance allowed for a specific frequency range to prevent voltage fluctuations.
- **Implementation:** Calculate the target impedance based on current requirements and acceptable voltage ripple for the design. A lower target impedance supports higher power stability, especially in high-speed designs.

2. Decoupling Capacitors:

- **Purpose:** Decoupling capacitors act as local energy reservoirs, filtering out high-frequency noise and stabilizing voltage levels near high-speed components.
- **Placement Strategy:**
  - Place capacitors as close as possible to the power pins of ICs, with smaller-value capacitors closest to the pins to filter higher frequencies.
  - Use a combination of different capacitance values (e.g., 0.01 µF, 0.1 µF, and 10 µF) to cover a broad frequency range.
- **Practical Tip:** The room property for components allows you to optimize capacitor placement, ensuring effective noise reduction. For full power solutions, consider Cadence Celsius PowerDC.

Practical Tips for PDN Design

- **Use Multiple Ground Planes:** Dedicated ground planes in the stackup help contain noise and provide a stable reference voltage for high-speed components.
- **Optimize Via Placement:** Placing stitching vias near high-speed ICs reduces ground bounce and ensures even power distribution.
- **Simulate Early and Often:** Perform PDN analysis as part of the design process to catch potential issues early, making it easier to adjust the layout and capacitor placement as needed.

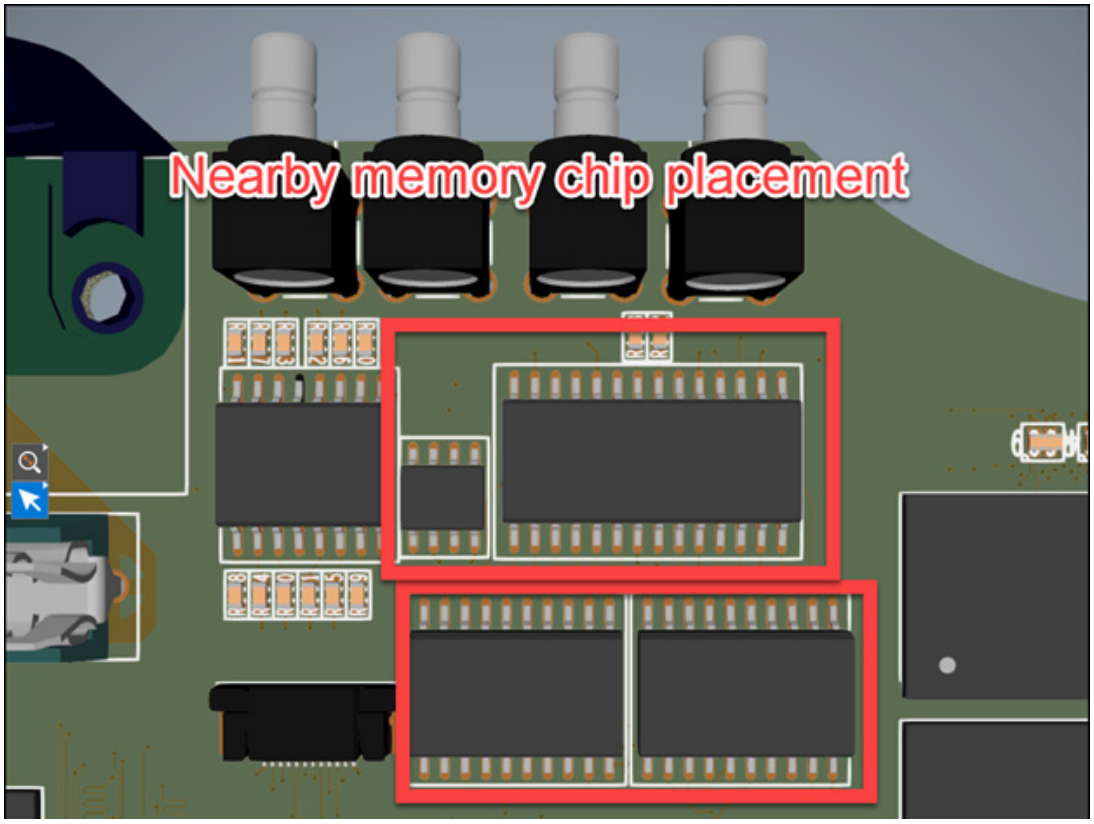
High-Speed PCB Layout Design

Effective layout design is essential in high-speed PCBs, as it directly impacts signal integrity, EMI, and power stability. Key layout considerations include strategic component placement, high-level routing techniques, and careful management of signal return paths and vias.

Key Component Placement Strategies

In high-speed designs, component placement affects signal paths, noise coupling, and power distribution. Placing components strategically minimizes signal integrity issues and optimizes performance.

1. Position High-Speed Components Near Their Connections:



- Place critical components like microcontrollers, memory modules (e.g., DDR), and interfaces (e.g., HDMI) close to each other to reduce trace lengths and avoid unnecessary signal paths.
- **Example:** Place the processor near memory components to minimize delay and simplify routing for data and clock lines.

2. Isolate Sensitive Components:

- Analog and digital components often require different routing strategies. Isolate sensitive analog components from high-speed digital signals to reduce interference.
- Use ground planes or shielding to separate noisy sections, such as switching regulators, from high-speed data lines.

3. Minimize Crosstalk with Component Spacing:

- Maintain adequate spacing between components with high-speed signals, reducing the risk of signal interference and crosstalk.
- Consider arranging components in functional blocks for easier routing and reduced noise.

High-Level Routing Techniques

Routing high-speed signals requires attention to proximity rules, differential pair routing, and controlled impedance. These techniques help maintain signal quality and minimize reflections.

1. Signal Proximity Rules:

- **Purpose:** High-speed signals routed too closely to other signals can induce crosstalk. Maintain a consistent distance between high-speed traces to minimize coupling.
- **Implementation:** Define minimum spacing constraints within the Constraint Manager to ensure critical traces are isolated from each other.

2. Differential Pair Routing:

- **Purpose:** Differential pairs are commonly used for high-speed signals, such as USB and Ethernet, because they reduce susceptibility to noise.
- **Implementation:**
  - Route differential pairs with consistent trace width and spacing to maintain impedance.
  - Keep pairs as close as possible along their entire route and avoid sudden changes in spacing or width that could introduce reflections.
  - Set up constraints to help maintain spacing and length matching for improved signal integrity.

3. Controlled Impedance Routing:

- Purpose: High-speed signals require consistent impedance to reduce signal reflections and maintain signal integrity.
- Implementation:
  - Define impedance values in Constraint Manager for critical nets and use routing tools to ensure these values are met throughout the design.
  - Avoid abrupt changes in trace width or layer transitions, as these can disrupt impedance control.

Signal Return Paths and Via Design

Signal return paths and via design are key considerations in high-speed layouts. Proper return path management and via design prevent noise, signal distortion, and EMI issues.

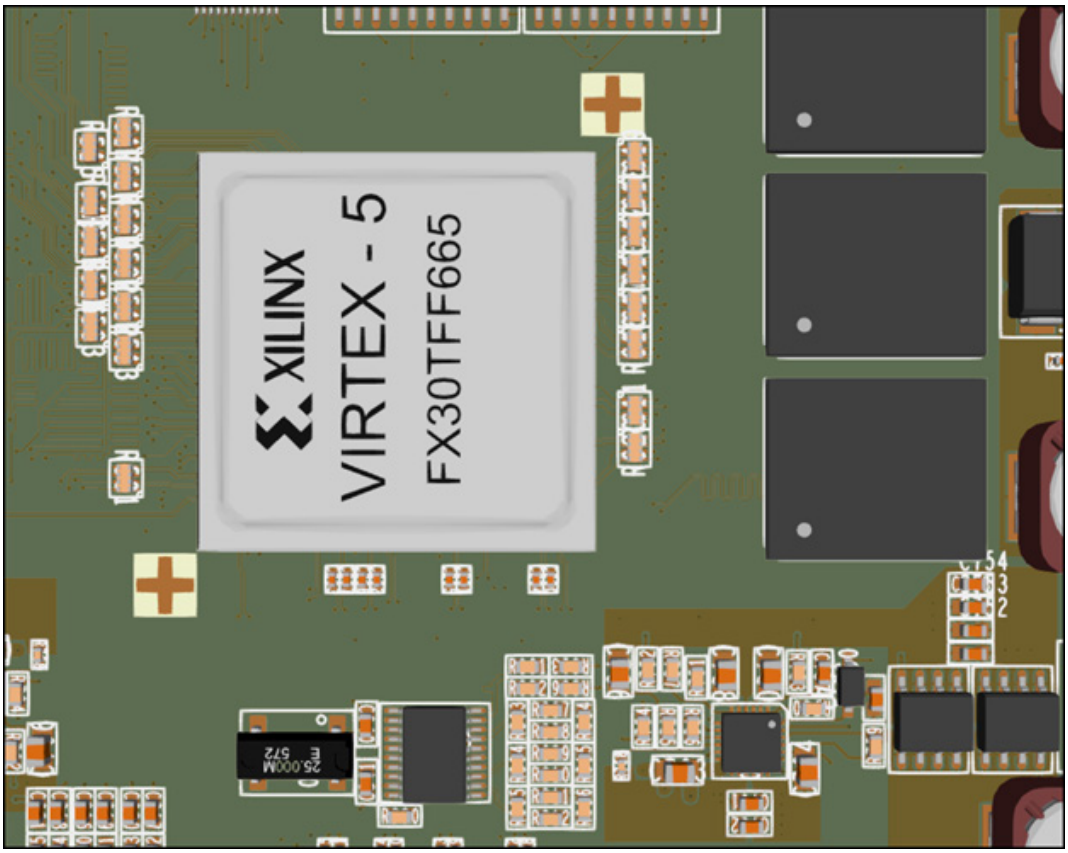
1. Signal Return Paths:

- **Purpose:** High-speed signals should have a clear, continuous return path to minimize loop area and reduce electromagnetic interference.
- **Implementation:**
  - Place high-speed signal traces over a solid ground plane to provide a low impedance return path, reducing potential EMI and crosstalk.
  - Avoid routing high-speed signals over split planes, as this can disrupt the return path and introduce impedance variations.

2. Via Design:

- **Purpose:** Vias used for layer transitions can introduce impedance discontinuities, affecting signal quality in high-speed designs.
- Implementation:
  - Use controlled impedance vias for high-speed signals, defining via geometry (drill size, pad size) in Constraint Manager.
  - Keep high-speed vias as short as possible in the Z axis (whether using back-drilling or blind and buried vias) and avoid unnecessary vias on high-speed signal paths.
  - For differential pairs, use closely spaced vias to preserve coupling and impedance consistency.

Practical Tips for High-Speed Layout



Layout with proper component placement, routing and via placement

- **Use Ground Planes for Shielding:** Ground planes reduce EMI and provide a stable return path for high-speed signals.
- **Limit Layer Transitions for High-Speed Signals:** Each transition introduces potential impedance mismatches; minimize transitions to maintain signal integrity.
- **Simulate Routing Choices Early:** Run pre-layout simulations to test high-speed routing strategies, making adjustments to placement and routing before finalizing the layout.

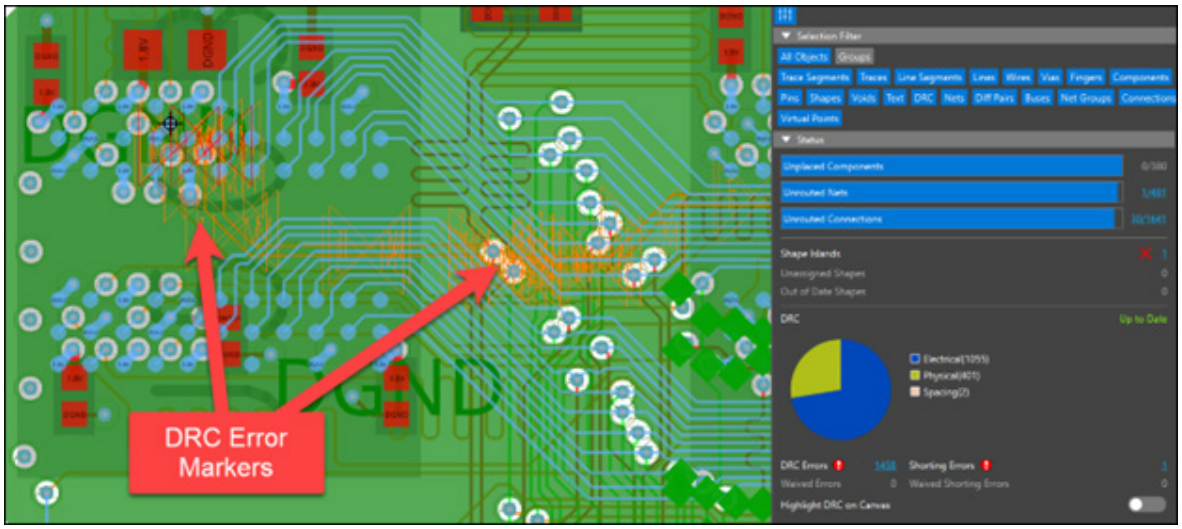
Post-Route Verification and Analysis

Design Rule Checks and Post-Layout Analysis

In high-speed PCB design, verifying that your layout adheres to the defined constraints and is optimized for signal integrity is crucial. Design Rule Checks (DRCs) and post-layout analysis provide a final opportunity to catch issues before manufacturing, ensuring that your design performs reliably under real-world conditions.

Design Rule Checks (DRC)

The DRC tool in OrCAD X continuously monitors the layout, ensuring that all defined constraints are met as you route traces and place components. The DRC flags any violations of spacing, impedance, and length constraints, enabling real-time adjustments and corrections.



- **Purpose:** DRCs validate that every constraint defined in Constraint Manager is enforced, identifying impedance mismatches, spacing issues, length mismatches, and other rule violations.
- Key Features:
  - **Real-Time Monitoring:** As you work, the DRC actively checks against all design rules, providing immediate feedback for faster iteration.
  - **Customizable Reports:** The DRC generates detailed reports that pinpoint exact locations of violations, making it easy to review and adjust design elements.

Signal Integrity Analysis

Sigrity X Aurora integrated within OrCAD X offers in-depth signal integrity analysis, particularly valuable for high-speed designs where even small layout changes can affect performance. It provides an integrated simulation environment that enables designers to evaluate and address signal integrity (SI) issues.

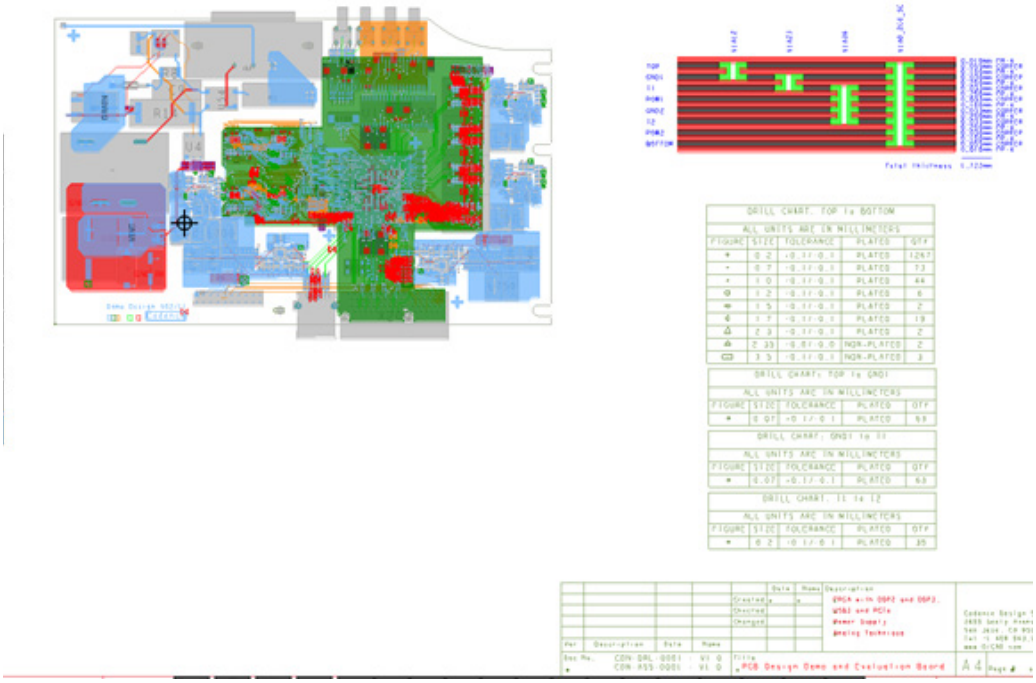
- **Purpose:** Signal integrity simulations help designers visualize signal quality, analyzing issues like reflections, crosstalk, and timing mismatches in critical nets.

Key Features:

- **Reflection and Crosstalk Analysis:** Sigrity X Aurora simulates high-speed signals, showing reflections and crosstalk across adjacent traces, allowing designers to adjust trace spacing, widths, and routing as necessary.
- **Eye Diagram Visualization:** Sigrity X Aurora generates eye diagrams for differential pairs and clock lines, providing a visual representation of signal quality and timing. This is particularly useful for verifying that high-speed signals remain clear and distortion-free.

- How to Use:
  - Run signal integrity simulations on critical nets, focusing on differential pairs, clock lines, and data lines. Review eye diagrams, then make routing adjustments in Presto PCB Editor.
  - Identify sources of reflections or crosstalk in Sigrity X Aurora, using simulation results to refine trace placement and spacing.

Practical Tips for Manufacturing Handoff



- **Communicate High-Speed Constraints:** Include a summary of high-speed requirements with the manufacturing files, such as trace width tolerances and controlled impedance specifications.
- **Review Gerber Files with the Manufacturer:** Coordinate with your manufacturer to review the Gerber files and ensure that all high-speed requirements and DFM/DFA adjustments are understood and achievable with their equipment.
- **Document Assembly Guidelines:** For DFA, include notes on component orientation, assembly order, and any special instructions for placing high-speed components like BGAs or connectors.