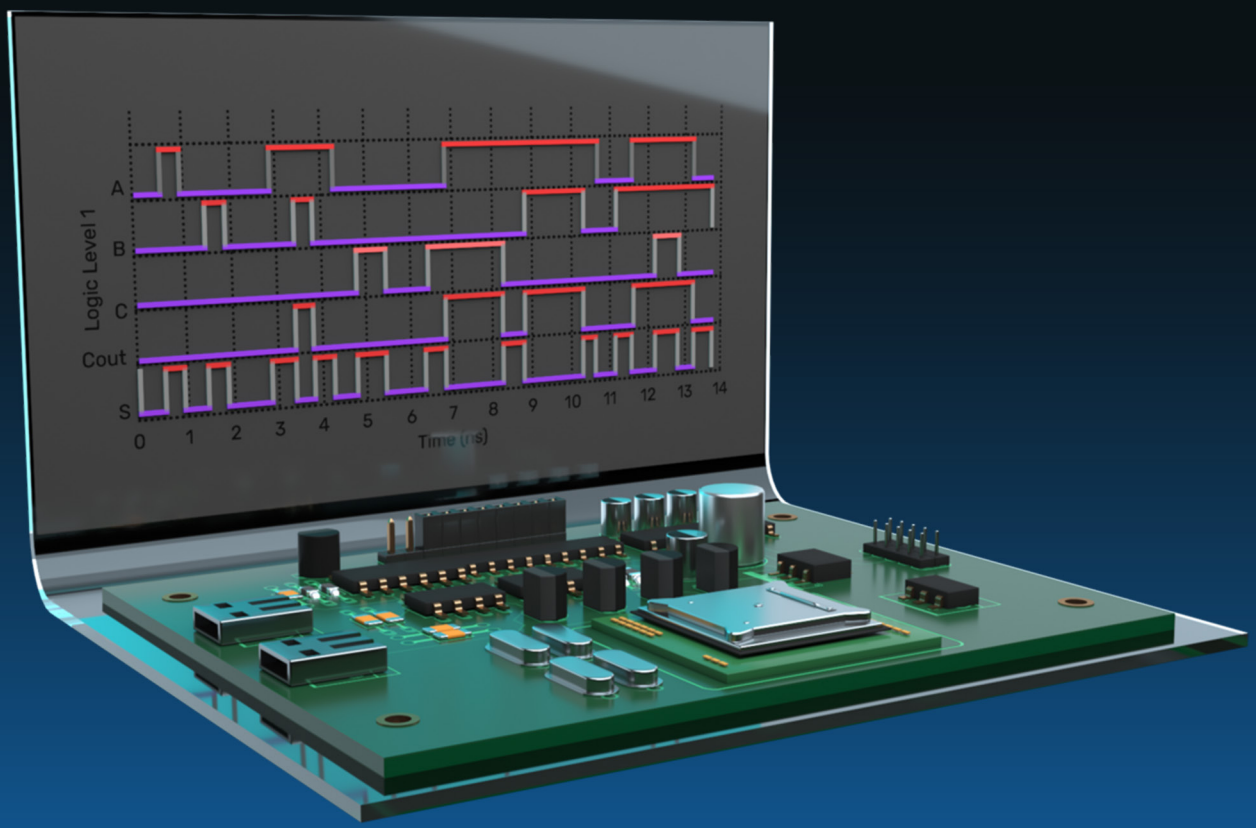
DESIGN **GUIDE**

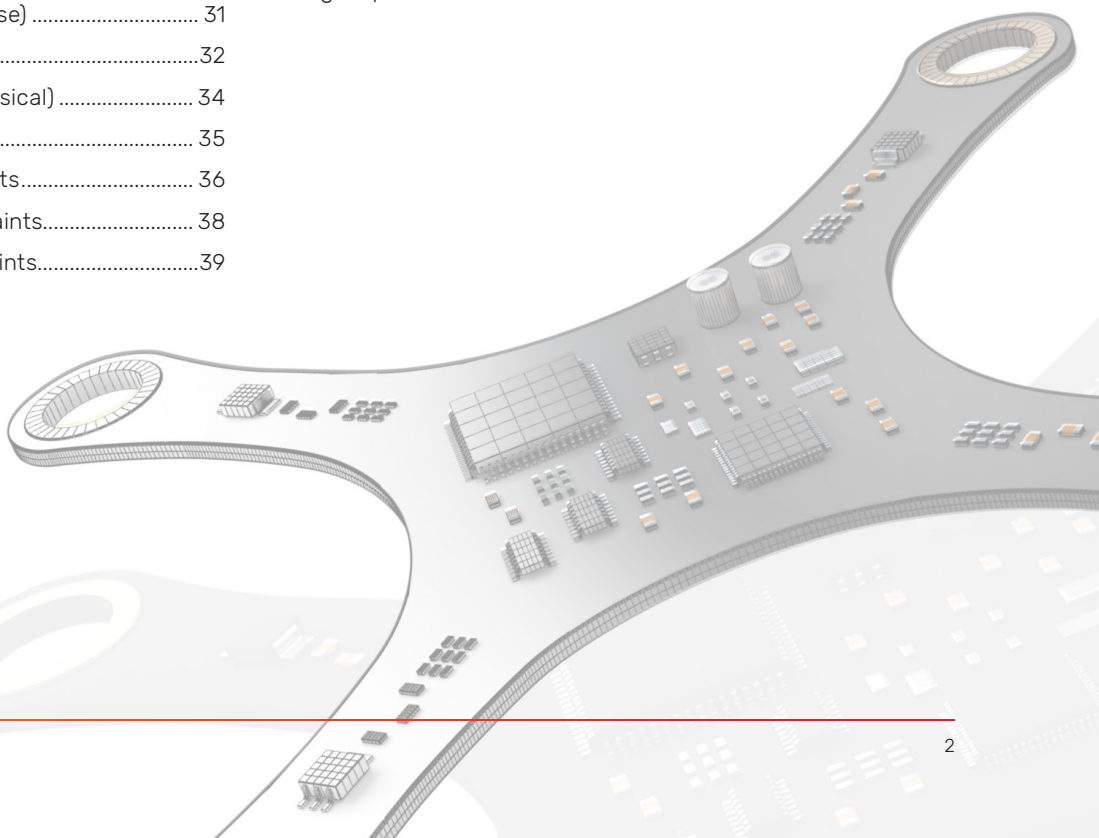
cadence®

OrCAD X High-Speed Digital Design Guide

Part 2 of 3: Practical Example – Constraint Management



Contents



Part 2: Practical Example - Constraint Management for High-Speed Designs

Welcome to the second part of this high-speed digital design guide. To solve common high-speed issues in printed circuit boards we have general rules and recommendations, but the most important aspect is practical application.

Use Part 1 of the guide as a reference and reminder for what you can do to reduce problems in high-speed PCB.

In this guide, we will show you how to implement high-speed constraints in a practical design. The guide will focus on application, specifically for high-speed timing considerations, with references to signal integrity, EMI, power integrity, the power distribution network and more relevant topics for creating a successful PCB layout.

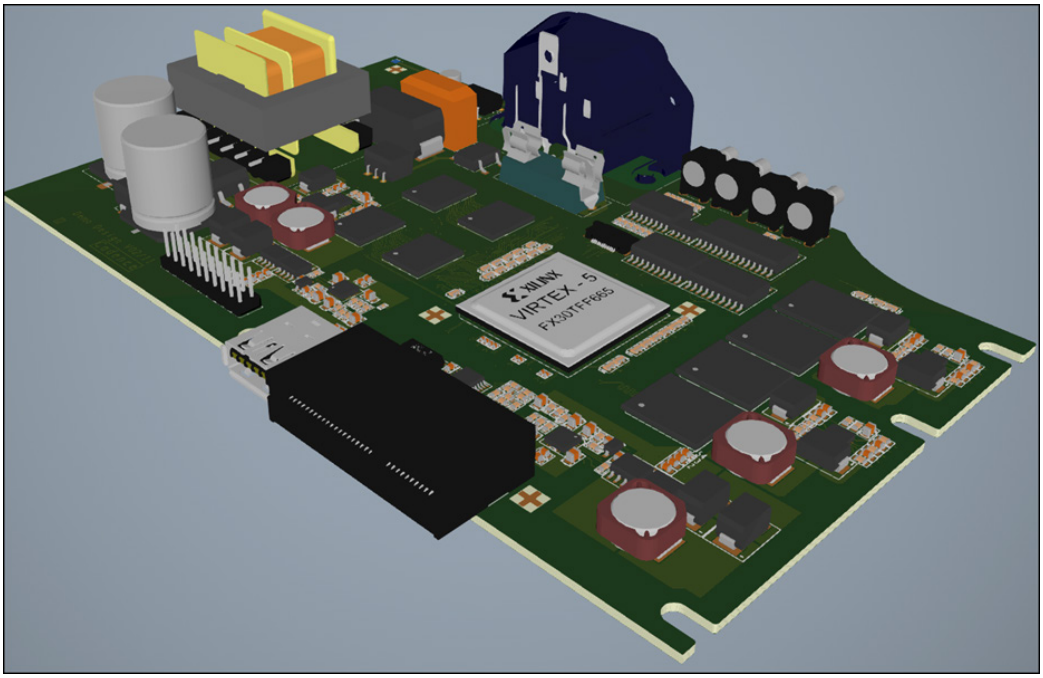
We will not cover every signal but just enough to explain how to implement the critical steps for a high-speed PCB layout. The entirety of the design is left as an exercise for the reader.

To access the project files used in this guide click this link: HSD_FPGA.zip

Project Overview

This high-speed design project centers around an FPGA interfacing with DDR memory, specifically:

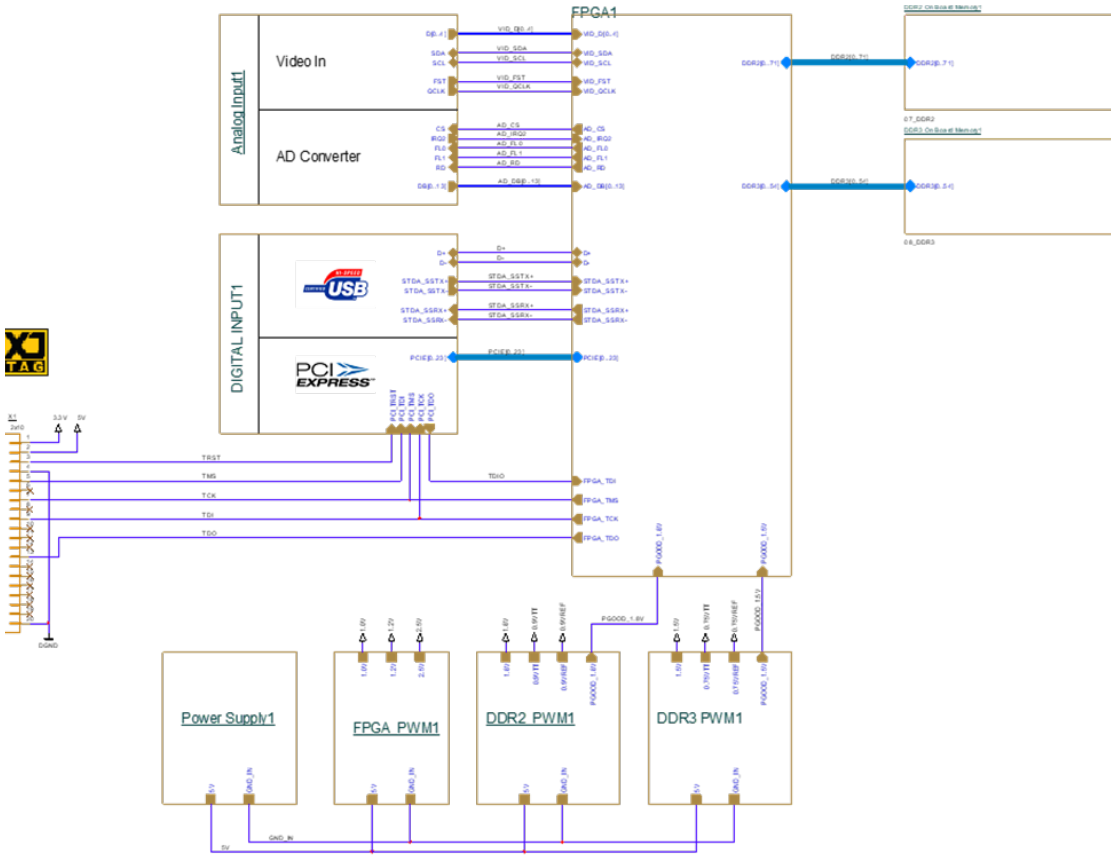
- FPGA: XC6SLX25-3FTG256I
- DDR3 Devices:
  - UPD431000AGW-B15
  - MT41J512M4JE-15E:A



Key Design Parameters

- DDR Interface: 300-800 MHz
- Crosstalk Limit: 8% for critical signals
- Manufacturing Capabilities:
  - High-speed traces: 4 mil minimum
  - Standard traces: 6 mil minimum

Schematic Capture



High-level view of the schematic for our Hardware Project

Constraint Definition (Schematic Side)

In high-speed PCB design, constraint definition is a critical step that sets the foundation for a successful layout. For our FPGA with DDR2 and DDR3 memory project, properly defined constraints ensure signal integrity, help manage electromagnetic interference and facilitate manufacturing processes.

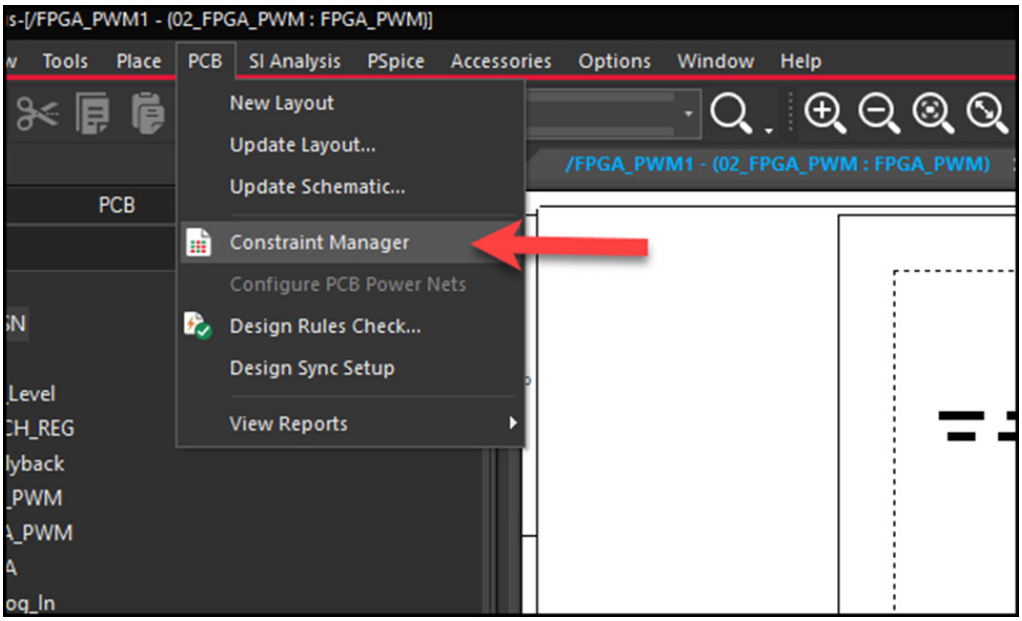
General Solution

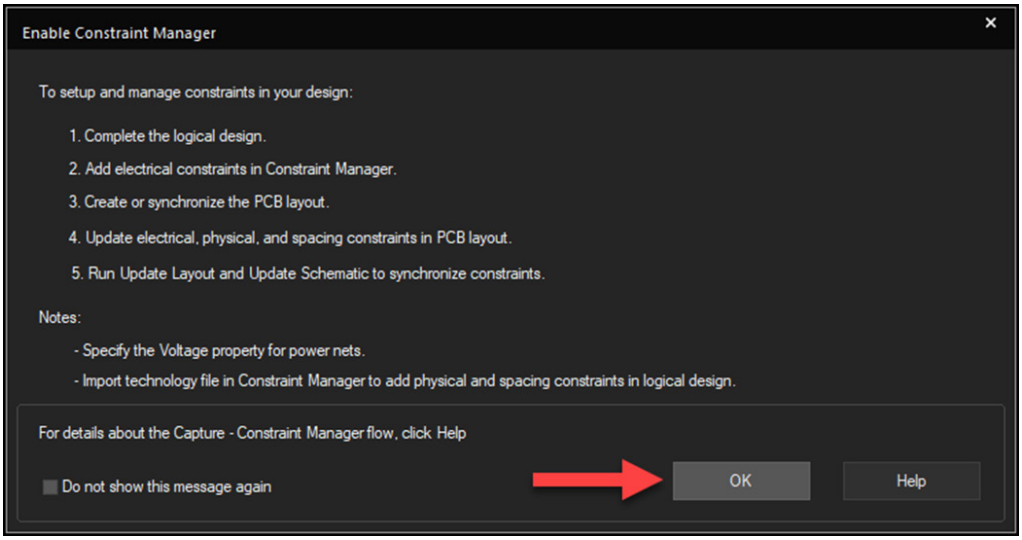
Effective constraint definition involves creating a comprehensive set of rules that govern electrical, physical, spacing, and manufacturing aspects of the PCB design. This approach helps prevent issues early in the design process and ensures that the final product meets performance and reliability requirements.

Specific Application in OrCAD X Capture:

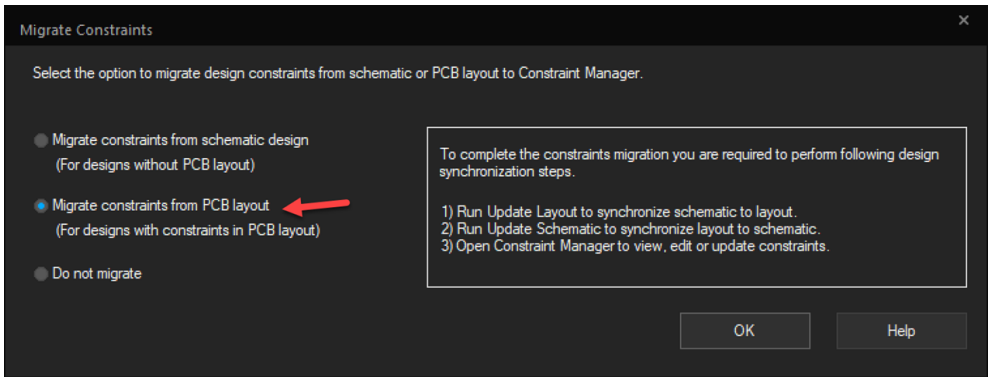
1. Open the Constraint Manager:

a. From the toolbar, go to **PCB > Constraint Manager**, when a dialog window appears, click OK.



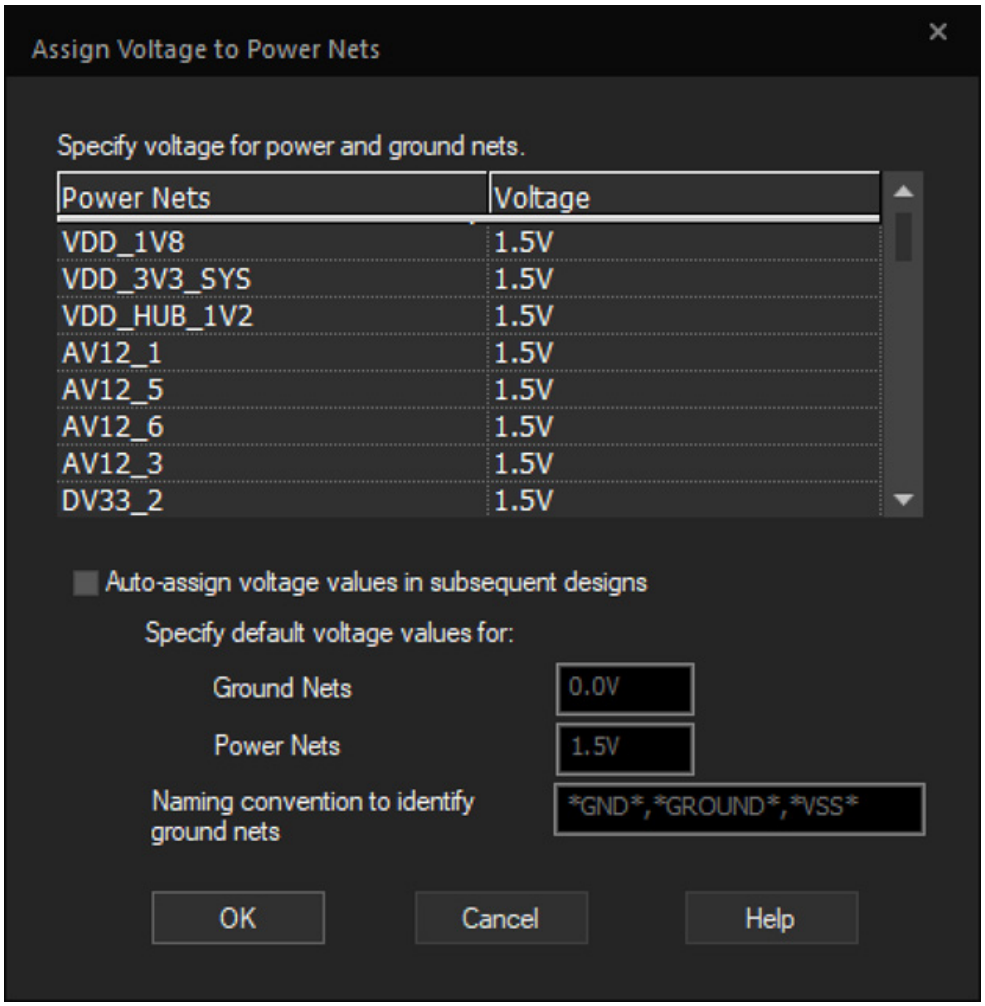


Capture may open a new window stating that you should perform an engineering change order, where you synchronize the schematic to the PCB layout, then synchronize the PCB layout file to the schematic.

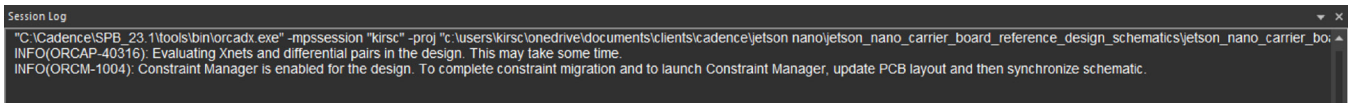


Follow the second option in those instructions so that the design becomes synchronized, then click OK.

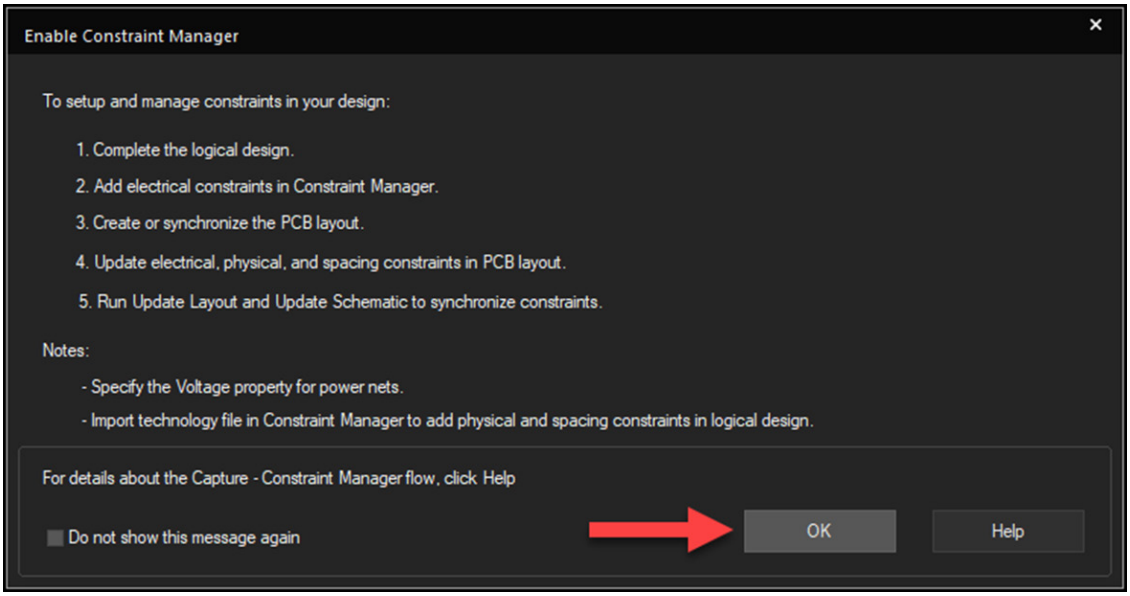
1. We selected **Migrate constraints from PCB layout**, so we have some more steps to perform as listed in the previous window.
2. You may be prompted to assign voltage to Power Nets.



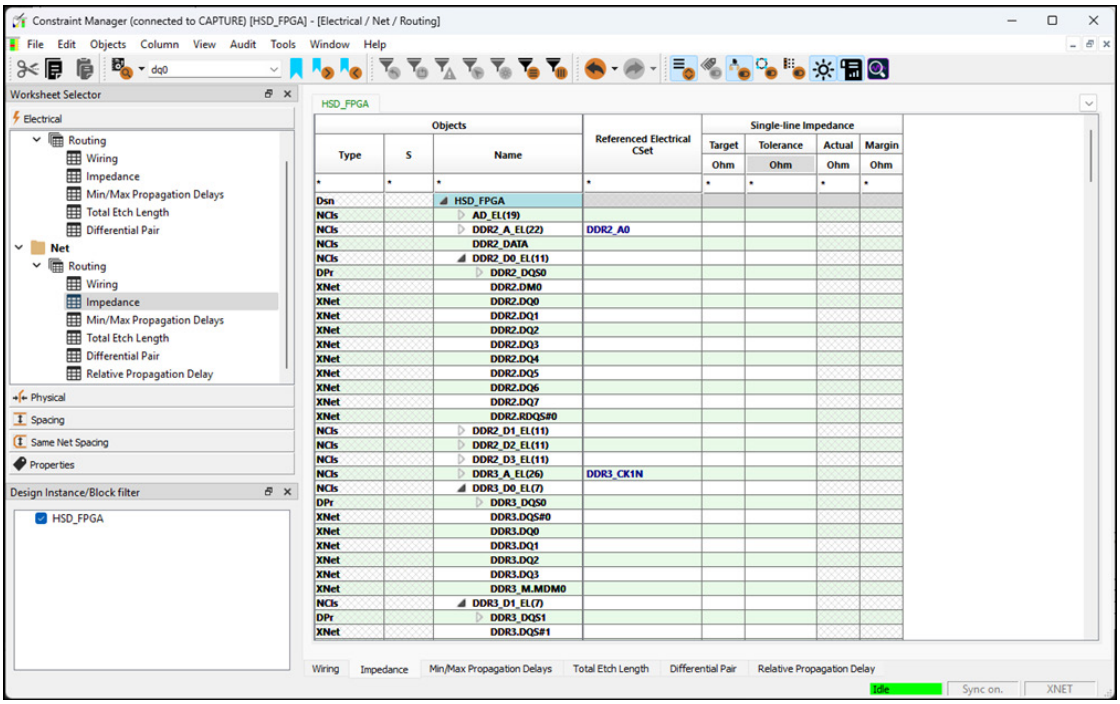
3. You can choose to Auto-assign voltage values in subsequent designs if you want, but we will leave it blank for now. Click OK.
4. Nothing will appear to happen, but if you go to the Capture menu and choose View > Session Log, it will display background processing information in the panel at the bottom of the tool.



5. The session log also reminds us of the next steps to fully activate and synchronize the Constraint Manager.
6. Once finished, go back to the menu PCB > Constraints option, then the **Enable Constraint Manager** window will appear again.

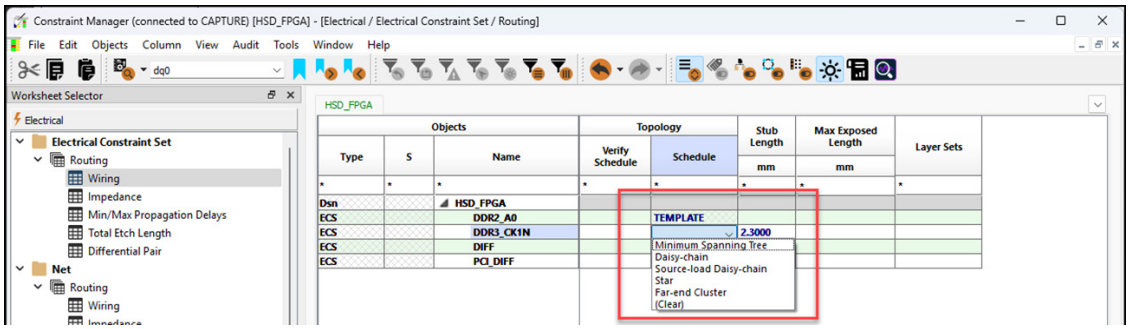


7. Once it does, click OK. Here you will see the constraints listed inside the Constraint Manager as shown below.



Electrical Constraints

For any high-speed design, first go to the **Worksheet Selector** on the left, then set up electrical constraints. Navigate to **Electrical Constraint Set > Routing > Wiring.**



We can control the Topology, Stub Length and Max Exposed Length of traces, but first set those values as rules. Those rules (Electrical Constraint Sets) can be applied to the desired traces.

We will go through each rule and set them within the Constraint Manager on the schematic side.

Electrical Wiring Topology

Set specific routing paths for technologies like DDR3 and T-branch to minimize signal attenuation due to PCB material properties. Or Daisy Chain or star topologies.

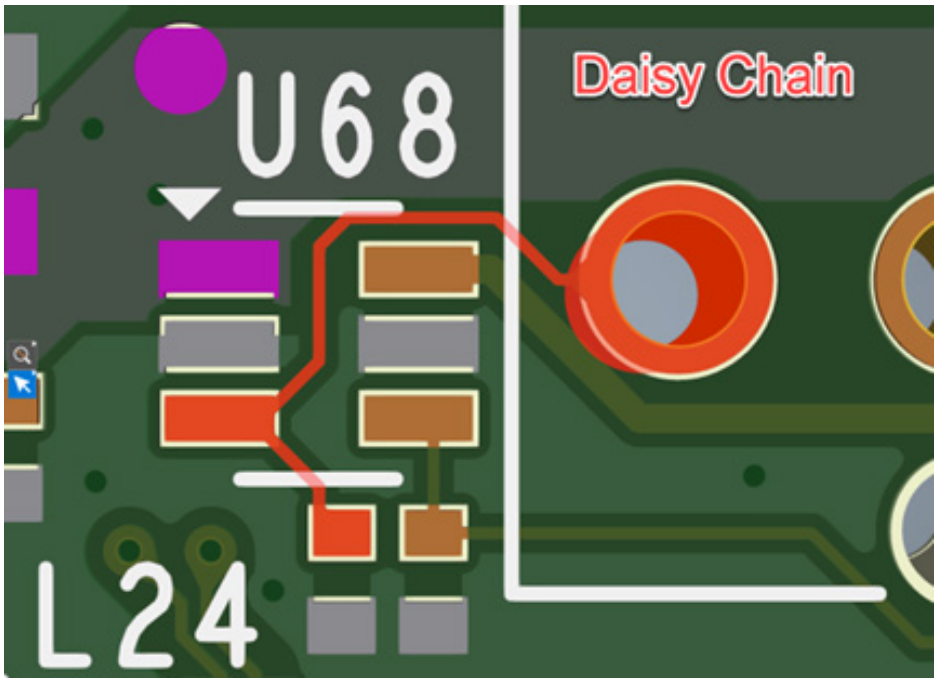


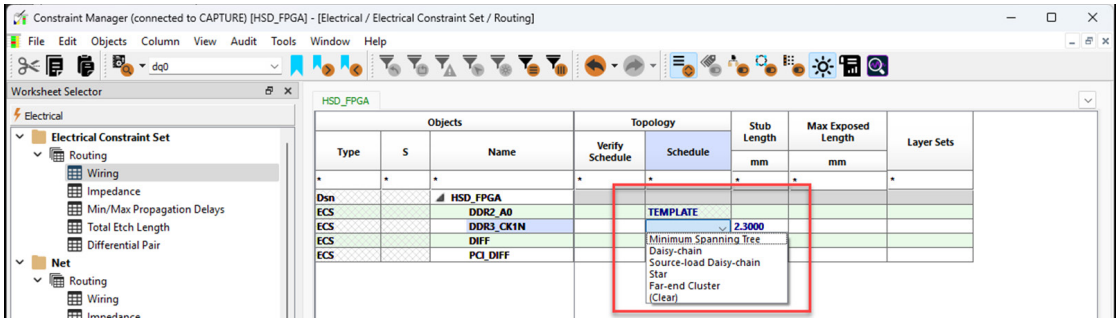
Diagram showing the prioritized routing of critical nets on a PCB

Definition: Wiring topology involves organizing the connections between different nets on a PCB to achieve a certain outcome, such as minimizing signal reflections, signal attenuation or voltage drops.

Example: Let's ensure that a DDR3 Command or Address net follows a daisy-chain topology.

Steps:

1. Open the Constraint Manager, then go to the **Electrical > Routing > Wiring** spreadsheet.
2. In the Schedule column, you can right click your Dsn cell, create a new Electrical Constraint Set (ECS). Notice in the image below, we have multiple ECSets already declared.
3. Select one of the cells within the **Schedule** column and you can choose your net topology from the drop-down menu that appears.

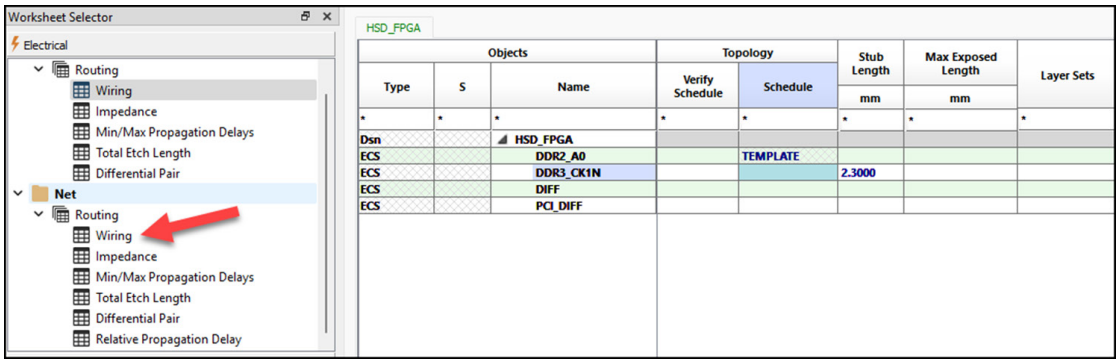


These are the net topology options that are available:

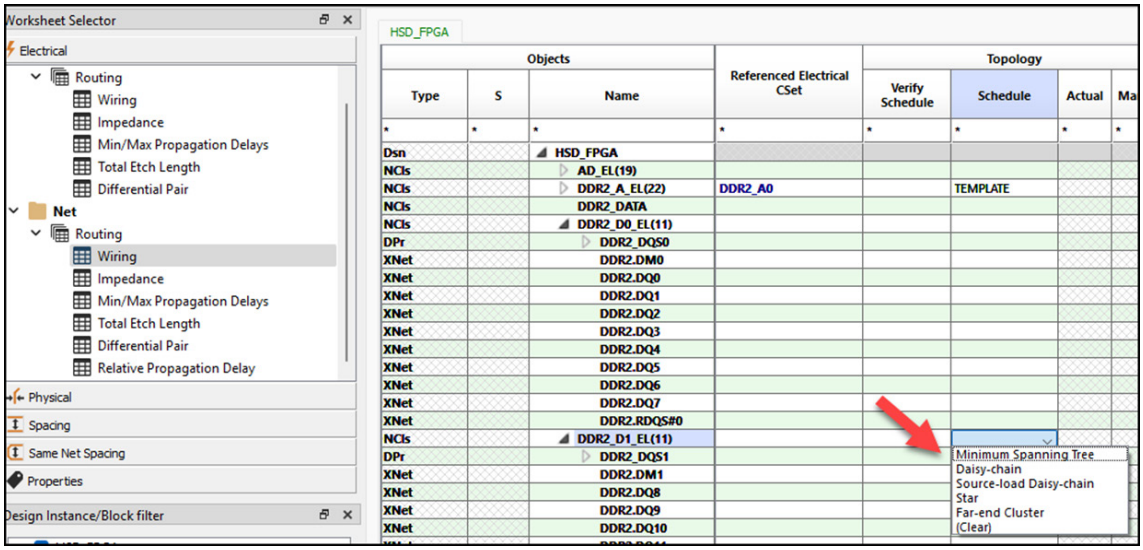
- Minimum Spanning Tree
- Daisy-chain
- Source-load Daisy-chain
- Star
- Far-end Cluster
- (Clear)

Each topology has its own benefits, depending on the application. Apply the type to your Electrical Constraint Set (ECS) as needed for your design.

4. Once you have set the topology for that ECSet, you can apply it to the appropriate nets found in the spreadsheet under **Electrical Constraint Set > Net > Routing > Wiring.**



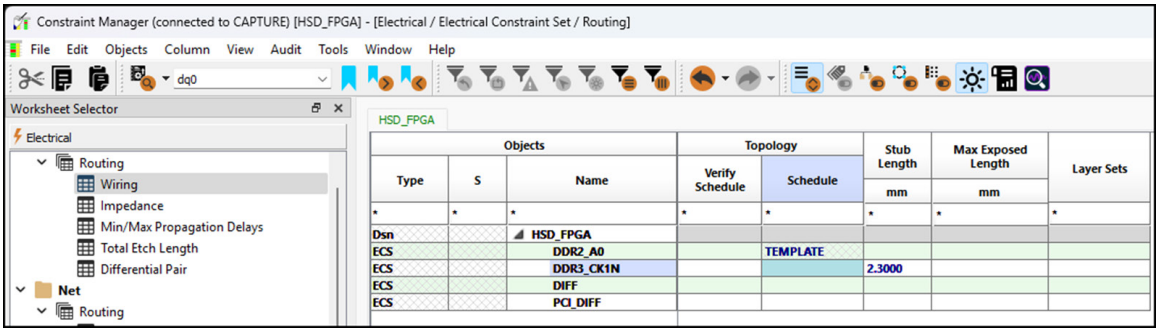
5. In this example, however, you can also directly apply a net schedule (see below).



Note: Depending on your use case, you can use either constraint sets or a specific rule application as needed, like in this example. However, please use constraint sets as often as possible to catch the majority of cases first before applying net-specific one-off rules. Using constraint sets modularizes and streamlines your PCB design constraint process and makes you more efficient. The constraint set method also reduces the likelihood of errors and forgotten constraints.

Benefit: Improves signal integrity and timing by ensuring critical connections are made efficiently.

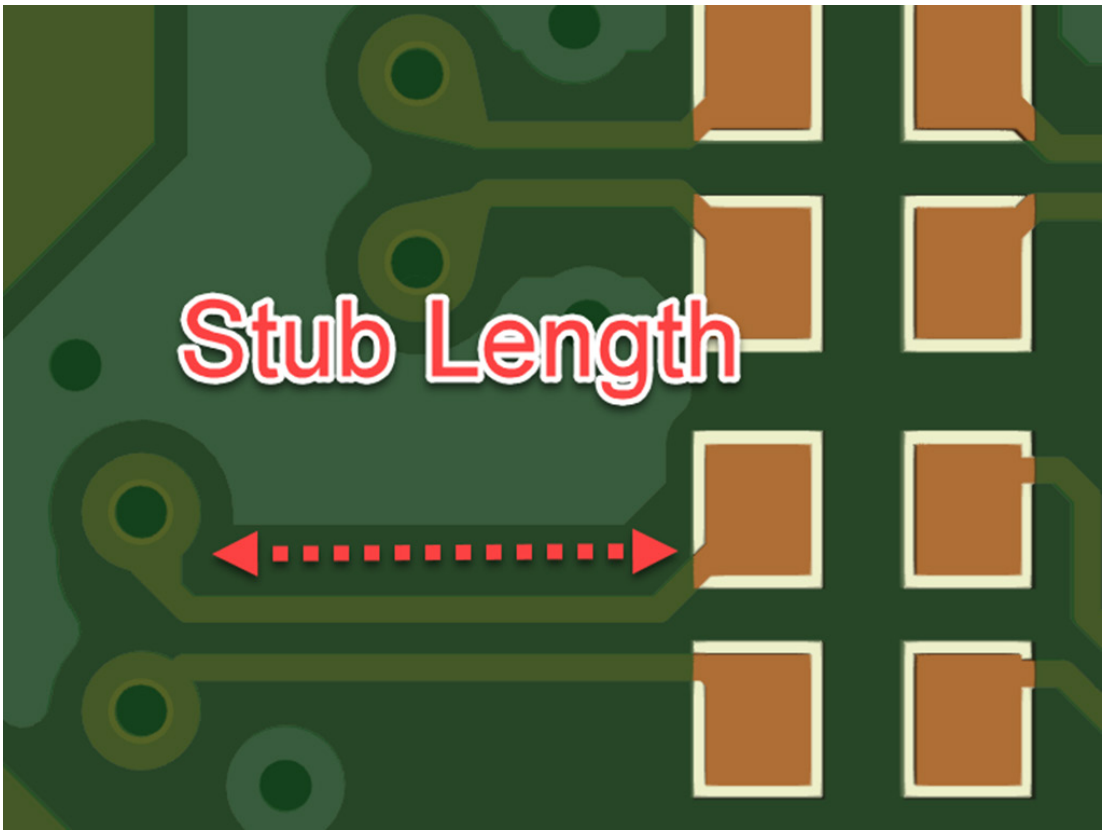
Let's return to the Electrical rules where we can set the constraint sets (see below).



At this point, you want to set your rules for parameters like Stub Length, Max Exposed Length, choose any Layer Sets you may have imported into the Constraint Manager from other engineers/designers, and choose to Verify Schedule.

Stub Limits (Stub Length)

For stub length, you want to set it to whatever your signal integrity engineers have modeled, say, during the schematic phase, or if you've done some signal integrity analysis in the schematic phase, then you will have an idea of allowed stub lengths.



Top view of PCB displaying trace stub length

Maximum Stub Length

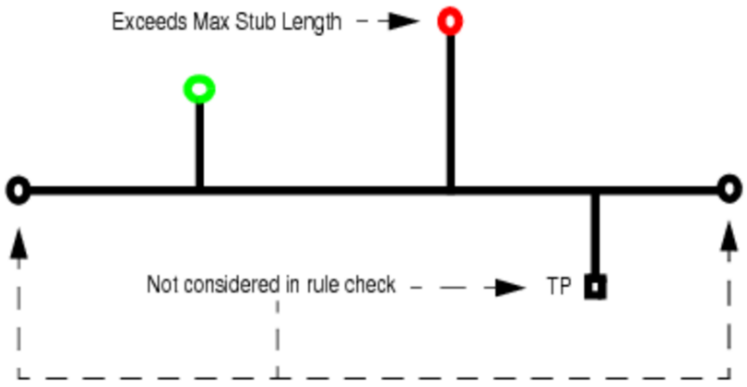
Checks the maximum stub length in design units for daisy chain routing.

Note: When a pin is routed to a connect line, the stub is the line of etch between the pin and the connect line.

The stub length constraint is validated only if NET_SCHEDULE is enabled and RATSNEST_SCHEDULE is set to either MIN_DAISY_CHAIN or MIN_SOURCE_LOAD_DAISY.

>

This check ignores pins at the end of clines, dangling clines, and test points. The chosen net schedule impacts the rule check.



Legal Values: Design Units
DRC Code: ES
Applicable Objects: Xnet, Net, ElectricalCSet, NetClass, DiffPair, Bus, NetGroup
Attribute Name: STUB_LENGTH

A stub as defined in OrCAD X Presto PCB Editor

Purpose of Stub Length Limits: To restrict the length of a copper stub connecting to a trace's vias or on a net wiring topology to reduce signal reflections and maintain signal integrity. For high-speed designs, aim for zero or minimal stub lengths, keeping them as short as possible.

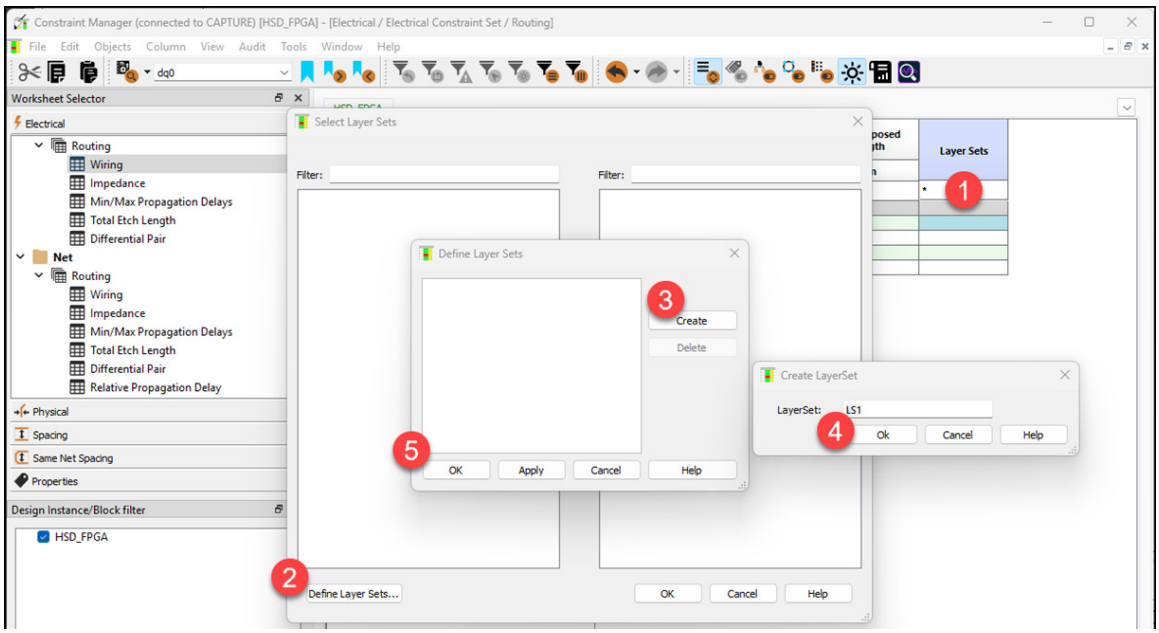
Applies to: USB, HDMI, and any other high-speed interfaces that need minimal fanouts or stubs to operate efficiently.

Max Exposed Length

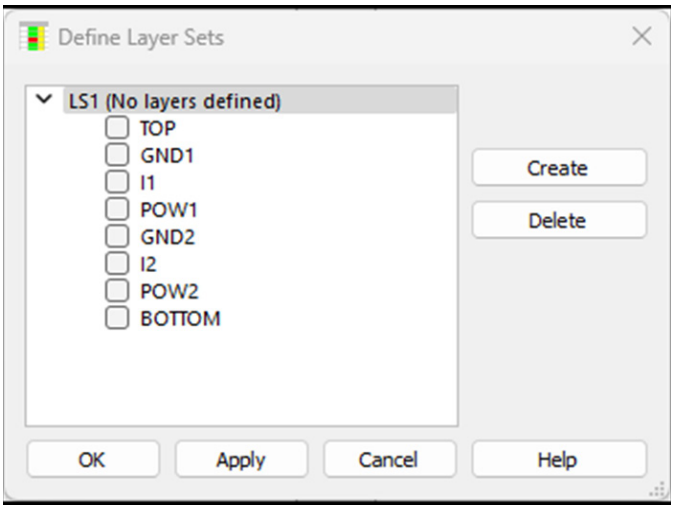
Refers to the amount of exposed copper that extends out from the soldermask on your PCB. It's part of the stub shown earlier. We recommend setting this as small as you can if this is a very important setting for your PCB. Otherwise, you can leave it blank for now.

Layer Sets

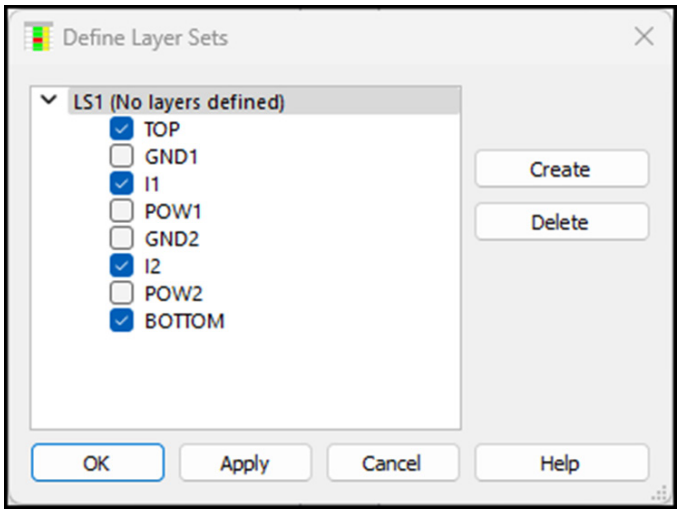
You can limit the layers that nets are allowed to be routed to/through by using Layer Sets. Follow the steps shown below to create a Layer set.



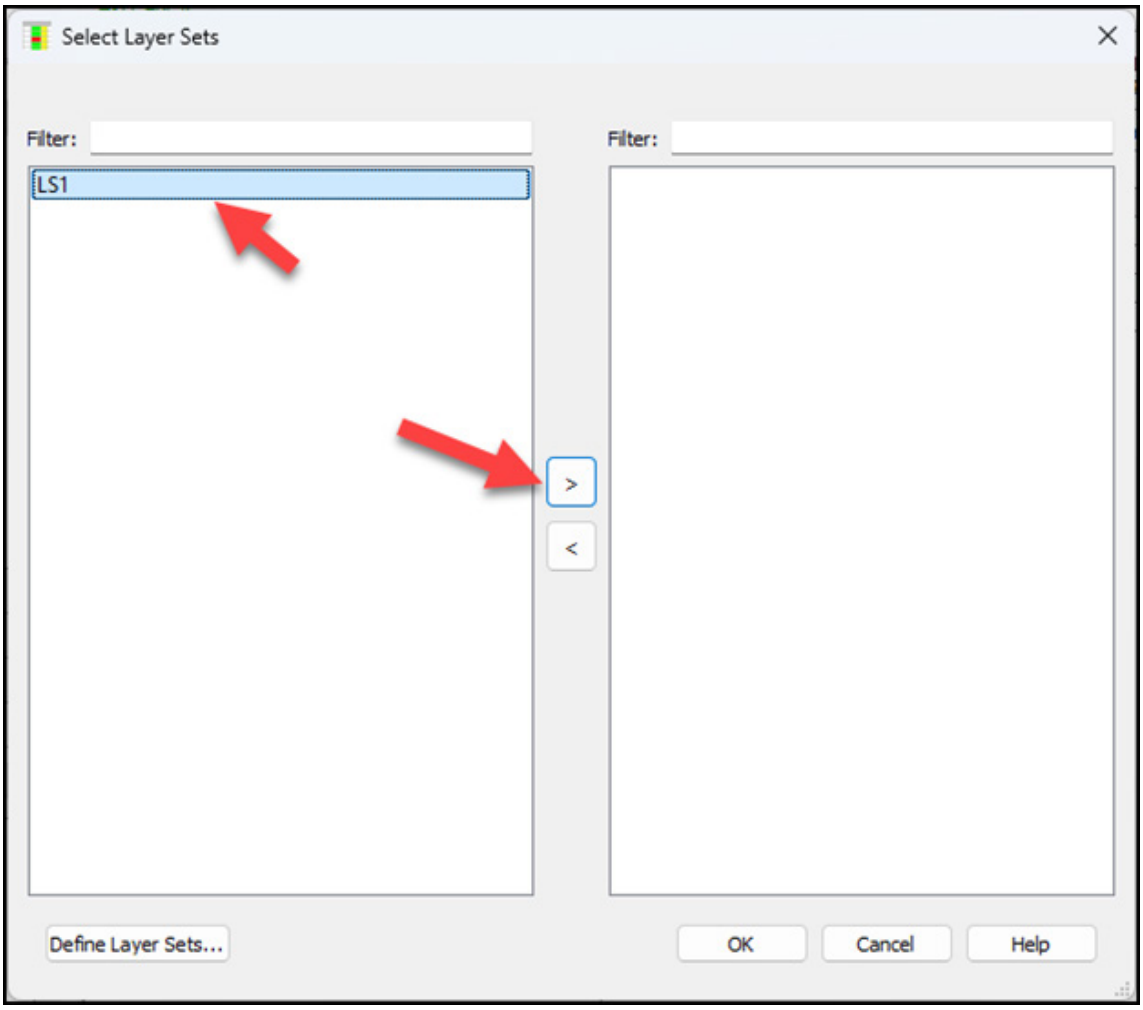
We'll call this LS1 (for Layer Set 1). Once it's created you can click the carrot next to the LS1 row, then you will get your layer options:



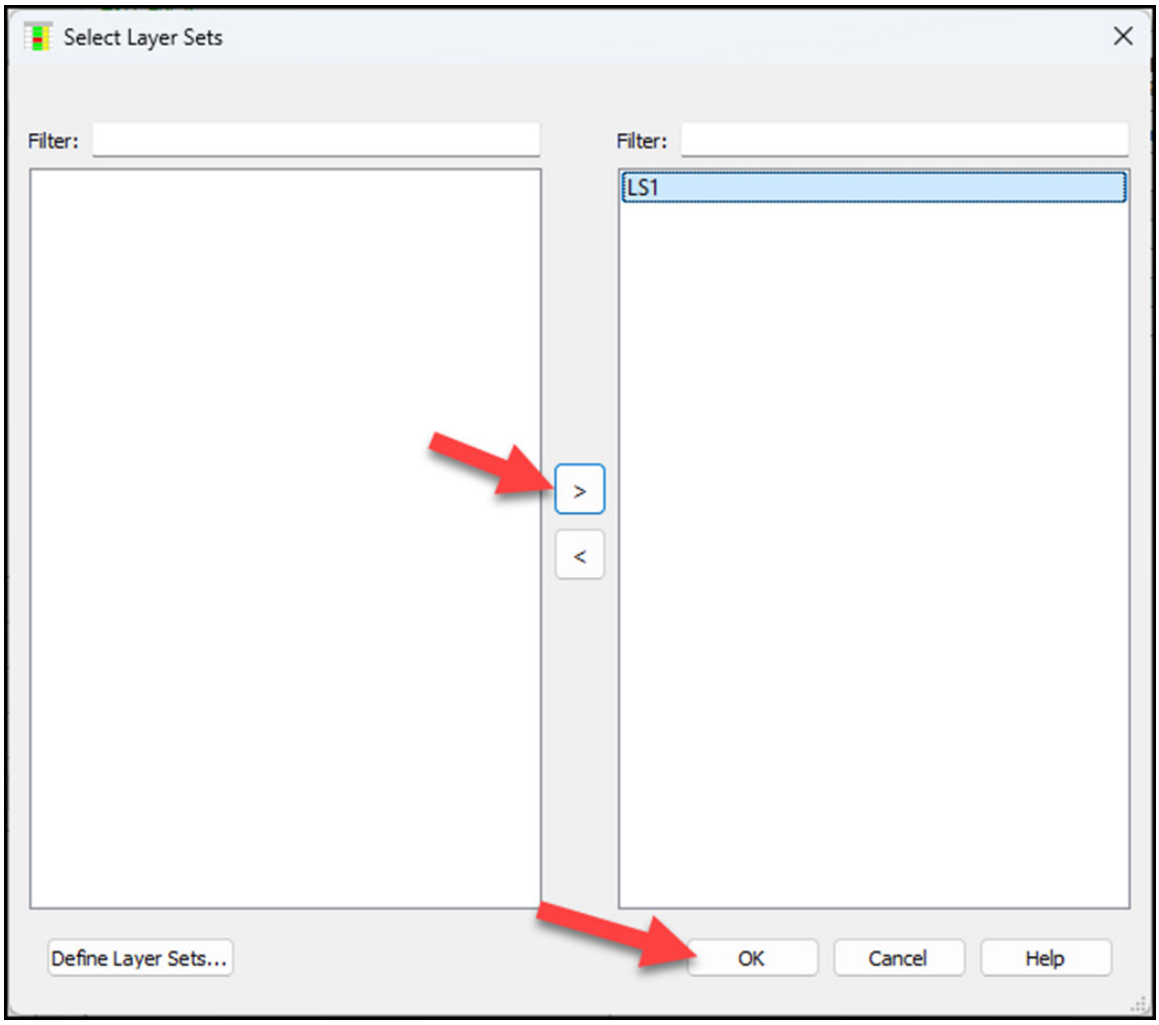
Some signals will need to be routed only on the TOP, L1, L2 and BOTTOM layers, or other layers, depending on their net. However, layer sets are typically needed for critical nets, while other nets can be routed on all layers for convenience.



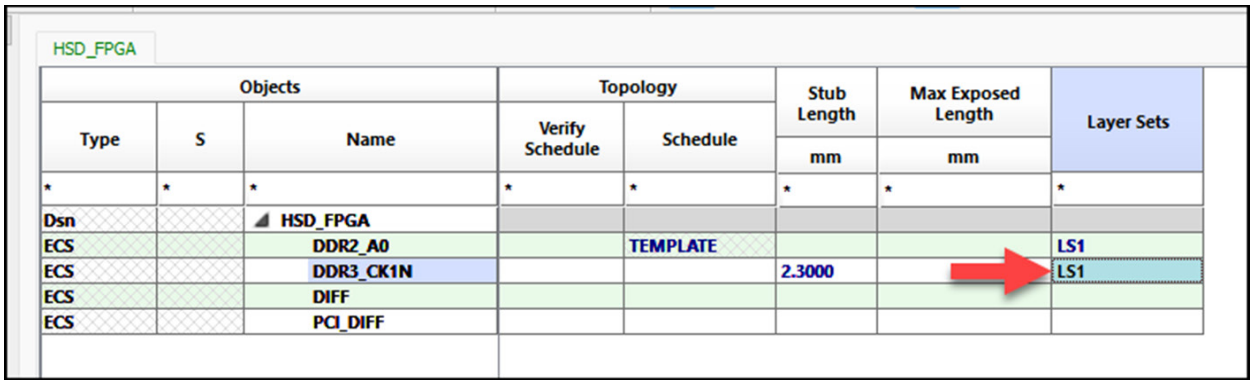
Click OK to define that layer set shown above. You will get the window below.



Click the right arrow button as shown above and that will place the layer set on the right.



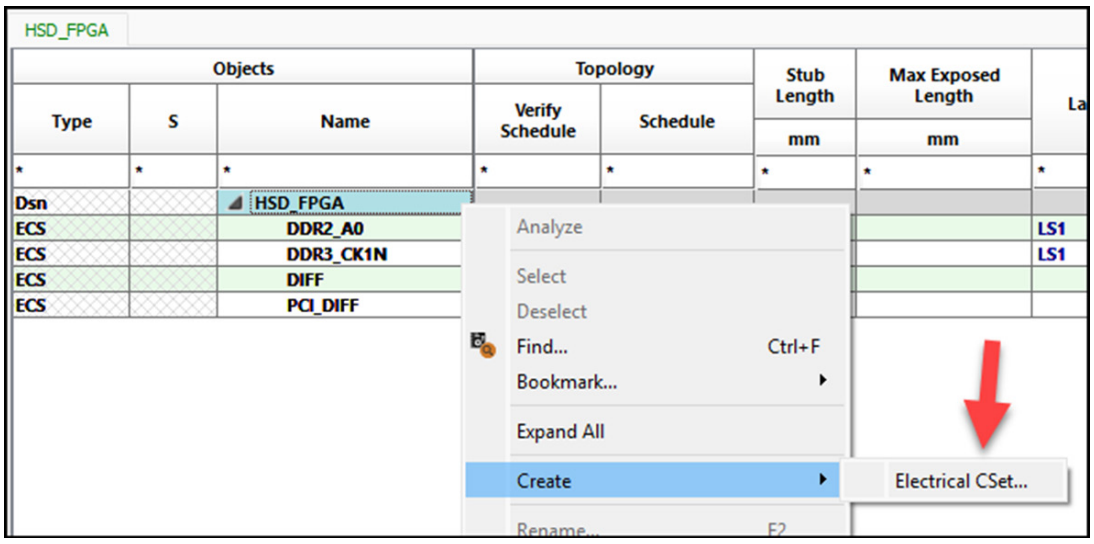
Once finished, you get the LS1 added to the allowed layer sets for that Electrical Constraint Set (ECS). Clocks are sensitive signals, so you can set the DDR3_CK1N constraint set to use that LS1 layer set as well (see below).



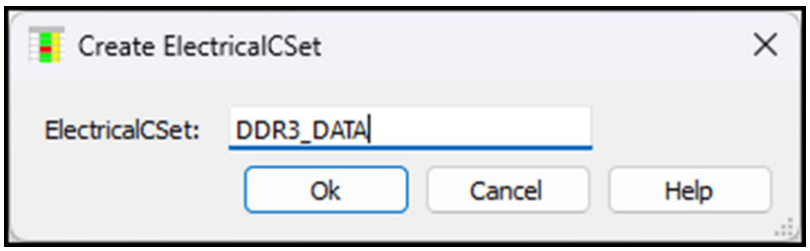
Notice in the image above that our ECS which is named DDR2_A0 already has a Schedule assigned to it. This is possible if you import or manually define a Schedule, but that is outside the scope of this document. We will define a new ECS of our own for the DDR3 signals.

Creating an Electrical Constraint Set for DDR3 signals:

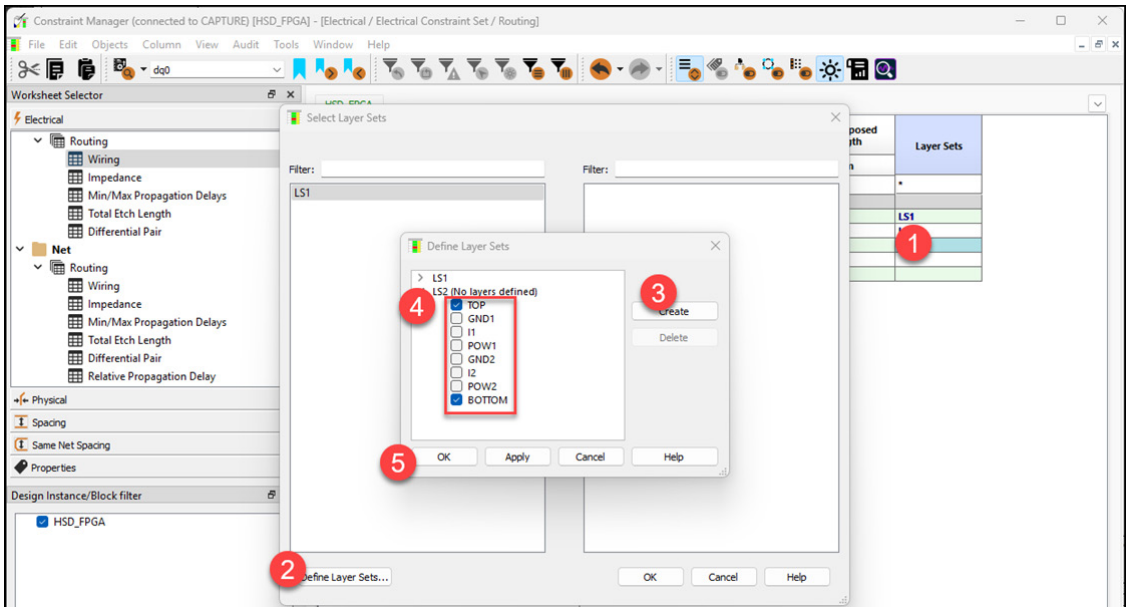
1. Right click on the **Dsn** element named **HSD_FPGA.**
2. Choose Create > Electrical CSet…



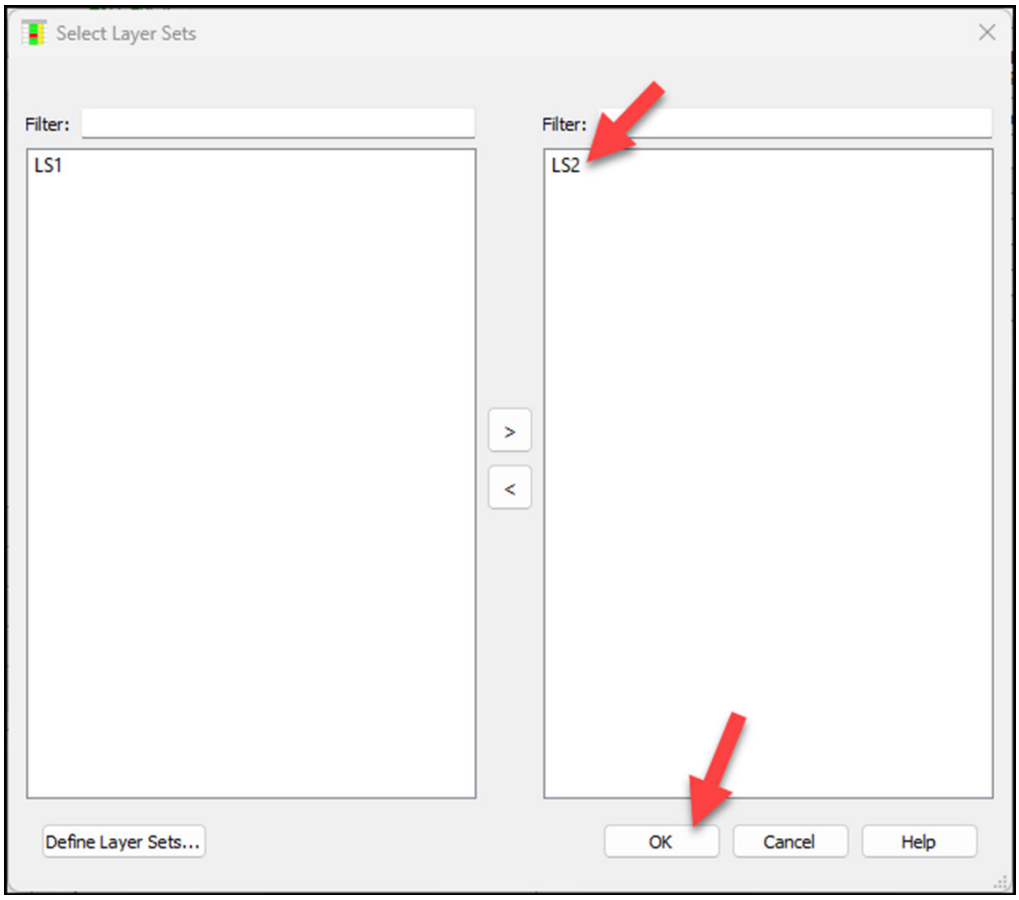
3. Name it DDR3_DATA.



4. Set the following columns in the worksheet to:
    a. Schedule = blank
    b. Stub Length = 0.127 mm (when really it should not have stubs ideally)
    c. Max Exposed Length = 0.1 mm (for solder mask clearance purposes)
    d. Layer Sets = LS2, where you would create a layer set and choose only the Top and Bottom layers (as shown)



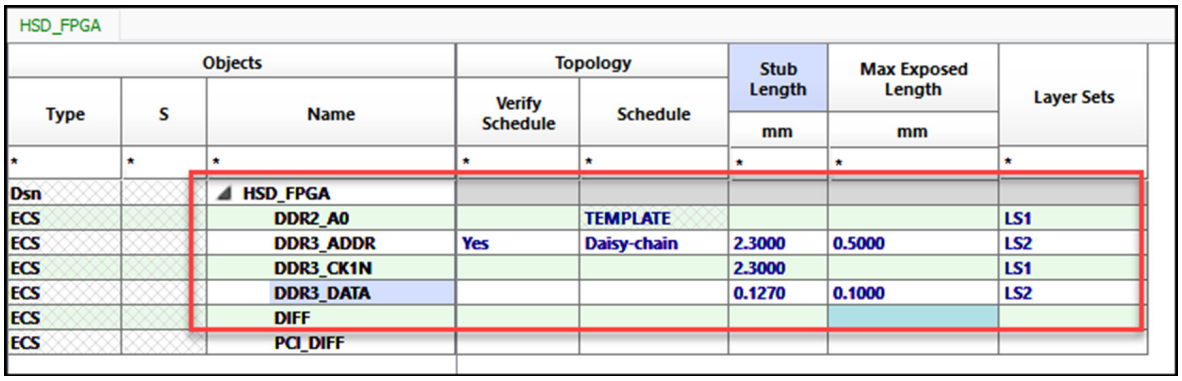
e. Then double-click on the L2 layer set or select it, then use the > button to move it over to the right column and click OK.



5. Once Layer sets are created, you will get what looks like below for the DDR3_DATA Electrical CSet.
6. For nets that need a topology, such as address and command nets, apply the Daisy Chain Schedule and choose Verify Schedule to the Electrical CSet (seen below).

Exercise

As an exercise, now that you know how to create Electrical Csets and add the appropriate settings for them, let's set the DDR_ADDR Electrical Constraint Set.



HSD_FPGA

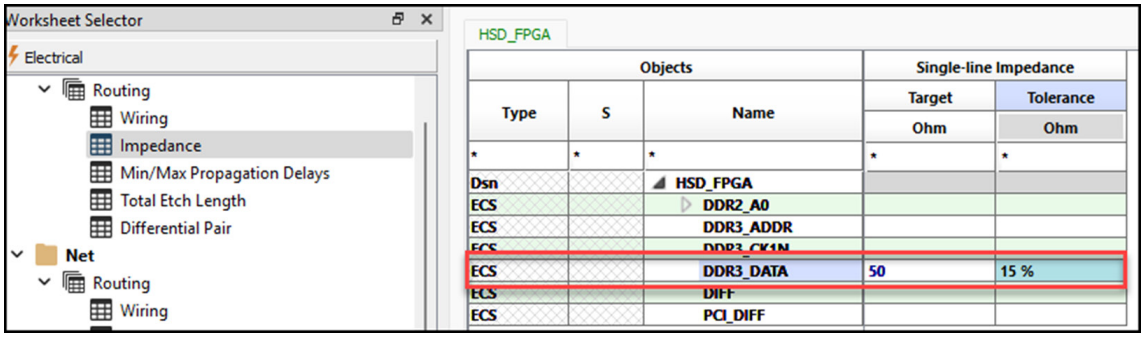
Objects			Topology		Stub Length	Max Exposed Length	Layer Sets
Type	S	Name	Verify Schedule	Schedule	mm	mm	
*	*	*	*	*	*	*	*
Dsn		HSD_FPGA					
ECS		DDR2_A0		TEMPLATE			LS1
ECS		DDR3_ADDR	Yes	Daisy-chain	2.3000	0.5000	LS2
ECS		DDR3_CK1N			2.3000		LS1
ECS		DDR3_DATA			0.1270	0.1000	LS2
ECS		DIFF					
ECS		PCI_DIFF					

Once finished, your Electrical CSet will look like the one above.

Set Impedance Targets

The next step in any high-speed design is to define your impedance targets (e.g., 50Ω for single-ended, 100Ω for differential). To do that:

1. In the Constraint Manager, go to Electrical > Routing > Impedance (as shown below):



2. Set your value under the **Target** column for the row, DDR3_DATA to 50 Ohms and Tolerance to 15% as most manufacturers can accommodate this level of precision. However, choose whatever tolerance your specific manufacturer tells you to.
3. To set an impedance target for your differential pairs, say, 100 Ohms, you still set the single-ended impedance for now to half that differential (100/2 = 50 Ohms) and at 15%

Important Note: If possible, avoid using **Ohm** as the **Tolerance**. Constraint Manager can take **%** or **Ohm**. However, we want it to automatically calculate the right tolerance for us instead of a hard-set value.

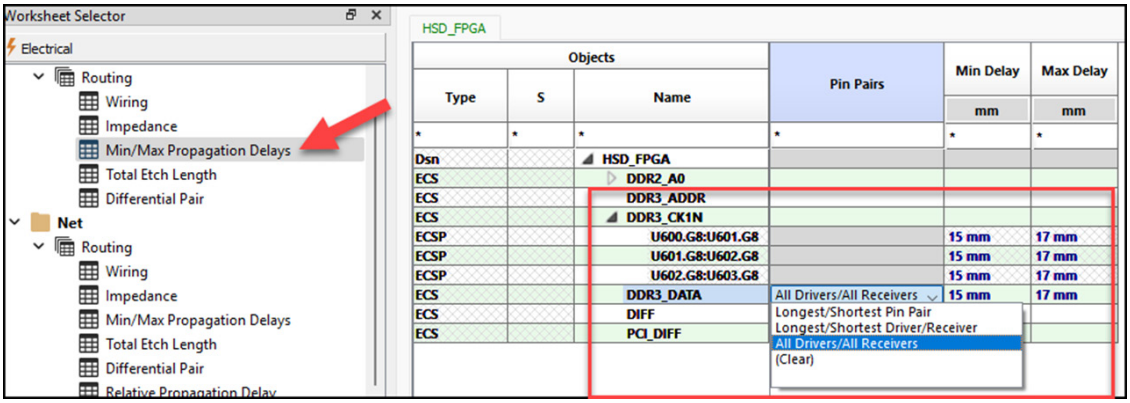
Jitter

If your license allows it, set maximum allowed jitter (e.g., 5-8% of the clock period), depending on the version of the software. This setting is not available in the version used for this guide.

Set Minimum and Maximum Propagation Delays

In high-speed digital boards, the pins inside a package tend to have propagation delay. That translates to the nets as well. If we know the package and part information (usually from the IBIS models) we can set these numbers.

1. In the Constraint Manager, go to Electrical > Routing > Min/Max Propagation Delays. Note how some are already set for the DDR3_CK1N ECSet.
2. We can manually set delays for our ECSet like the DDR3_DATA set if we know the propagation delay on the DDR3 chip they connect to. Set them as shown below:
   a. Min Delay = 15 mm
   b. Max Delay = 17 mm
   c. Pin Pairs = All Drivers/All Receivers



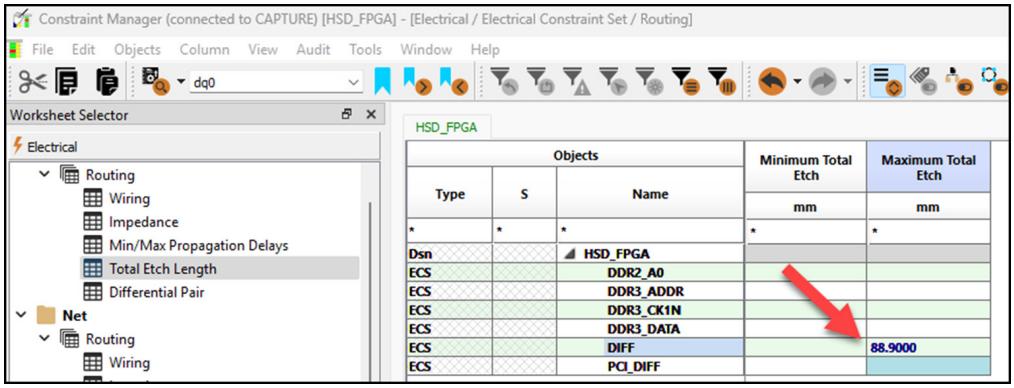
Note: These propagation delays set us up for length matching later.

Total Etch Length

Traces have critical lengths necessary to avoid signal reflections on the PCB. There are different rules of thumb, such as 1/20th or 1/6th of a wavelength, but sometimes these are overly conservative or too lenient. The only way to know is through simulation. But for now, you can use the manufacturer's data sheet information for the protocol implemented by their specific chip or family of chips. Let's set the Total Etch Length for an ECSet.

Steps:

1. In Constraint Manager, go to **Electrical > Routing > Total Etch Length.**
2. For the DIFF ECSet, set the **Maximum Total Etch** value to 3500 mil (when you hit Enter on your keyboard, Constraint Manager will automatically convert it to the target units, which is mm in our case).



For DDR3 data lines, you would set a minimum and maximum Total Etch according to your design guide. For example, from a design guide for DDR3 you may get values like 4500 mils from the controller.

Note: Why set DIFF to 3500 mils? That's a rough estimate given for USB 3.1 as a critical length allowed by some semiconductor manufacturing companies for their chips. We cannot know the critical length in truth until we simulate the differential pair signals in a PCB. To do that, you may use a tool like TopXplorer for signal integrity analysis. Set the other **Electrical Constraint Sets to Maximum Total Etch Lengths** (critical lengths) according to what signal integrity analysis engineers determined from simulation or is mentioned by manufacturing documentation.

Differential Pair Constraints (Electrical)

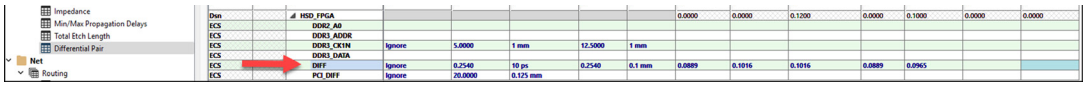
Let's set rules for differential pairs in general. To do that:

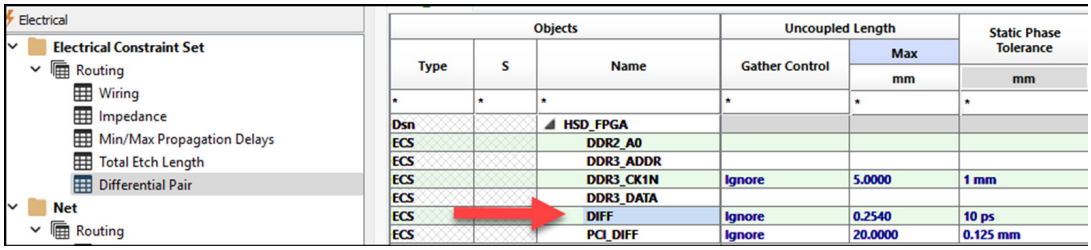
1. Go to the Constraint Manager, Electrical Constraint Set > Routing > Differential Pair worksheet.
2. Choose the following parameters and values for the DIFF ECSet.
    a. Uncoupled Length:
        i. Gather Control = Ignore
        ii. Max = 0.254 mm (10 mils)
    b. Static Phase Tolerance = 10 ps (picoseconds)
    c. Dynamic Phase:
        i. Max Length = 0.2540 mm (10 mils)
        ii. Tolerance = 0.1 mm (3.937 mils)
    d. Min Line Spacing = 0.0889 mm (3.5 mils)
    e. Primary Gap = 0.1016 mm (4 mils)
    f. Primary Width = 0.1016 mm (4 mils)
    g. Neck Gap = 0.0889 mm (3.5 mils)

h. Neck Width = 0.0965 mm (3.8 mils)

i. (+)Tolerance = blank

j. (-)Tolerance = blank





Objects			Uncoupled Length		Static Phase Tolerance
Type	S	Name	Gather Control	Max	
				mm	mm
*	*	*	*	*	*
Dsn		HSD_FPGA			
ECS		DDR2_A0			
ECS		DDR3_ADDR			
ECS		DDR3_CK1N	Ignore	5.0000	1 mm
ECS		DDR3_DATA			
ECS		DIFF	Ignore	0.2540	10 ps
ECS		PCI_DIFF	Ignore	20.0000	0.125 mm

Dynamic Phase		Min Line Spacing	Coupling Parameters					
Max Length	Tolerance		Primary Gap	Primary Width	Neck Gap	Neck Width	(+)Tolerance	(-)Tolerance
mm	mm	mm	mm	mm	mm	mm	mm	mm
*	*	*	*	*	*	*	*	*
		0.0000	0.0000	0.1200	0.0000	0.1000	0.0000	0.0000
12.5000	1 mm							
0.2540	0.1 mm	0.0889	0.1016	0.1016	0.0889	0.0965		

You may set your desired Tolerances at the end, but ensure that the (-)Tolerance value does not cause the **Neck Gap** spacing to be less than the **Min Line Spacing** setting, else you will get an error message.

Notes:

1. Static phase is used to manage the skew on a set of differential pairs.
2. Dynamic phase controls how much we allow the differential pair signals to be out of phase in real-time, to avoid common mode voltage and the noise it creates.
3. Primary gap is the edge-to-edge distance between two differential traces in unrestricted routing conditions.
4. Neck gap is the edge-to-edge distance between the two differential pair traces but when 'necking down' on the PCB; it's usually to get through tight areas.

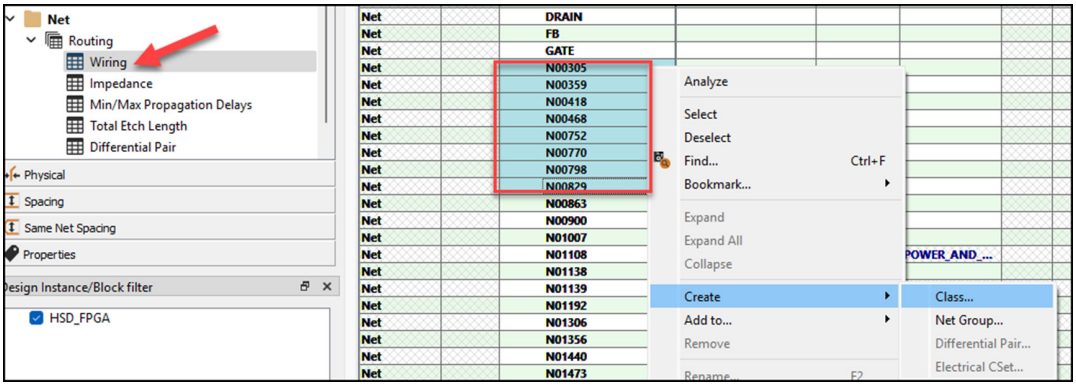
As with any ECSet, you can create your own Differential Pair Classes and fill in their properties as necessary.

We have created our electrical constraints, now it's time to create net classes to apply those electrical properties to.

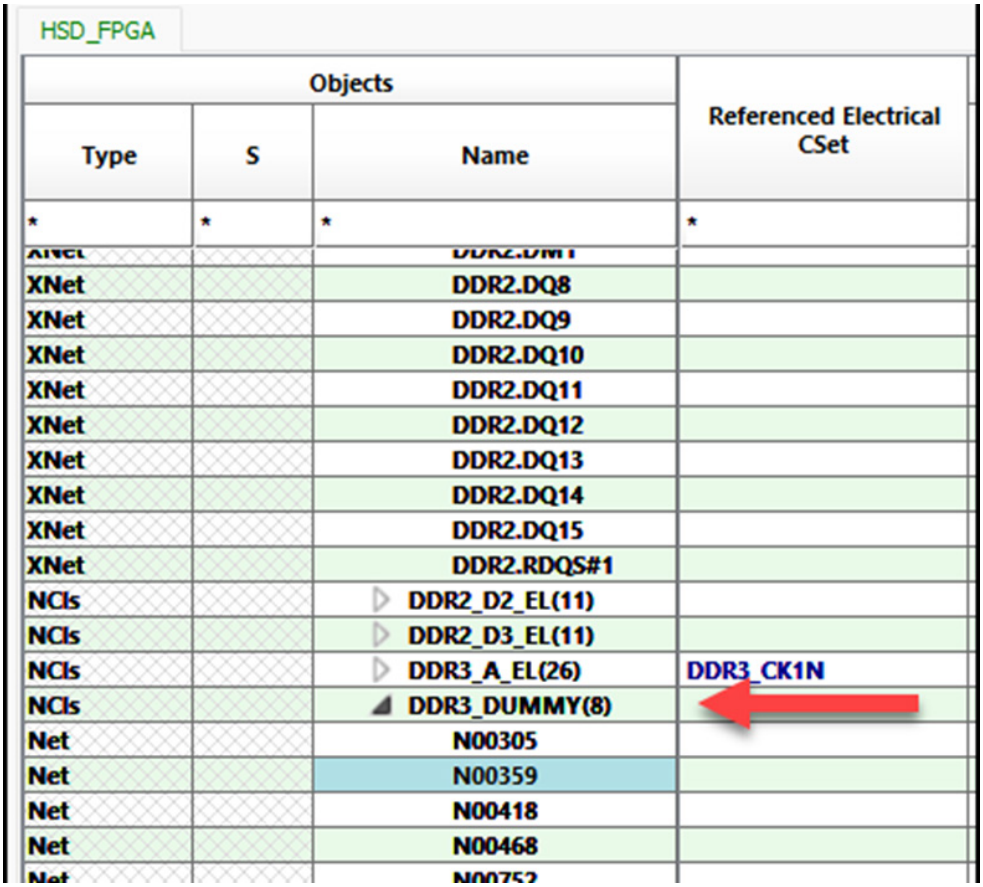
Create Net Classes

We'll set a net class for our DDR3_DATA interface as an example:

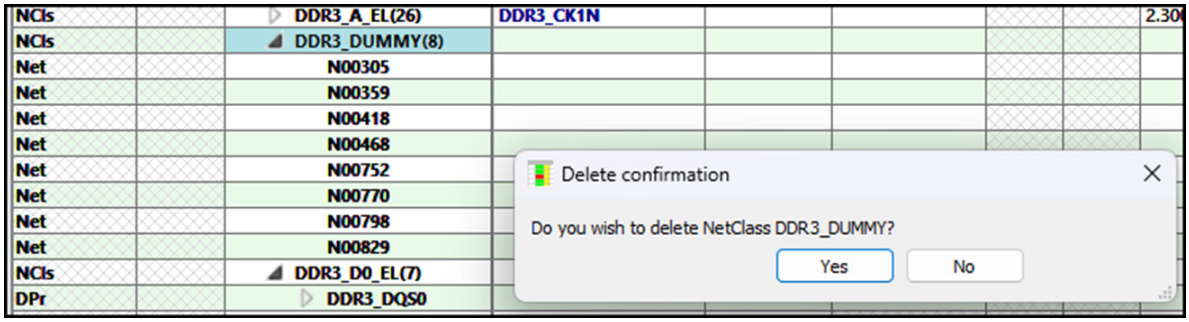
1. In the **Electrical > Net > Routing > Wiring** worksheet, highlight any number of arbitrary nets, like shown below (click and drag the left mouse button across various nets so they're highlighted).
2. Right click any of the highlighted net names. Choose Create, Class.



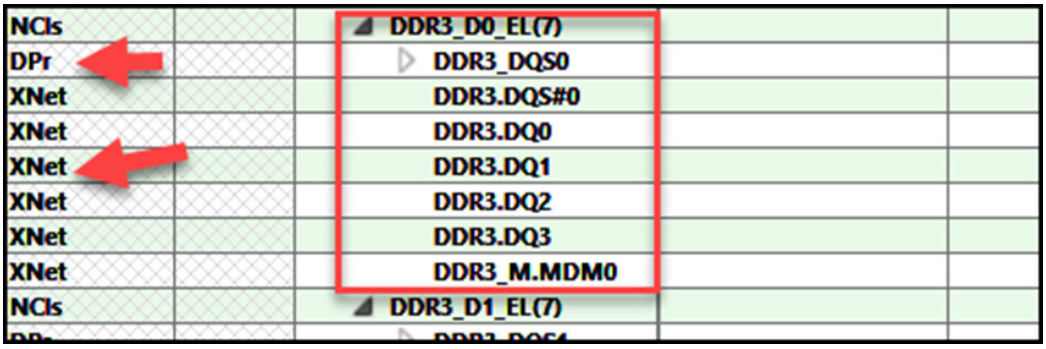
3. The Create NetClass window appears. Name the class DDR3_DUMMY. Then click OK. Now the list of nets shows the DDR3_DUMMY net class.



4. Now we don't need this net class, because we have a DDR3_D1 class already for a data class. So right click the DDR3_DUMMY(8) net class and choose Delete.
5. When asked if you wish to delete NetClass DDR3_DUMMY, click Yes (see below).



6. The net class disappears. In the same worksheet, scroll up to the DDR3_D0_EL net class. See how it has already been set in the design and has a Differential Pair (DPr) in it (as DDR3_DQS0, the data strobe) and Extended Nets (XNet) as well.

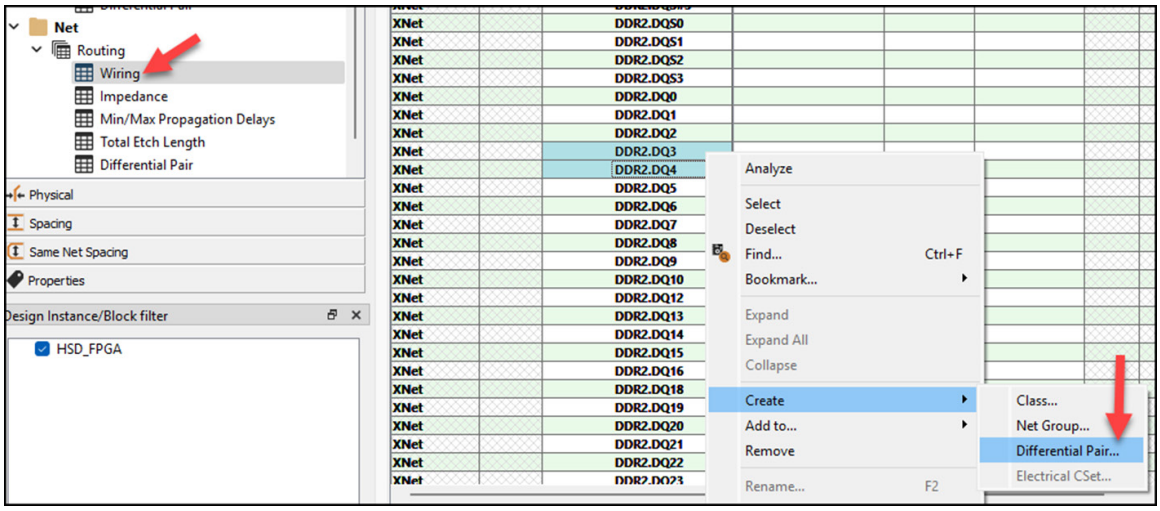


Next let's define differential pairs.

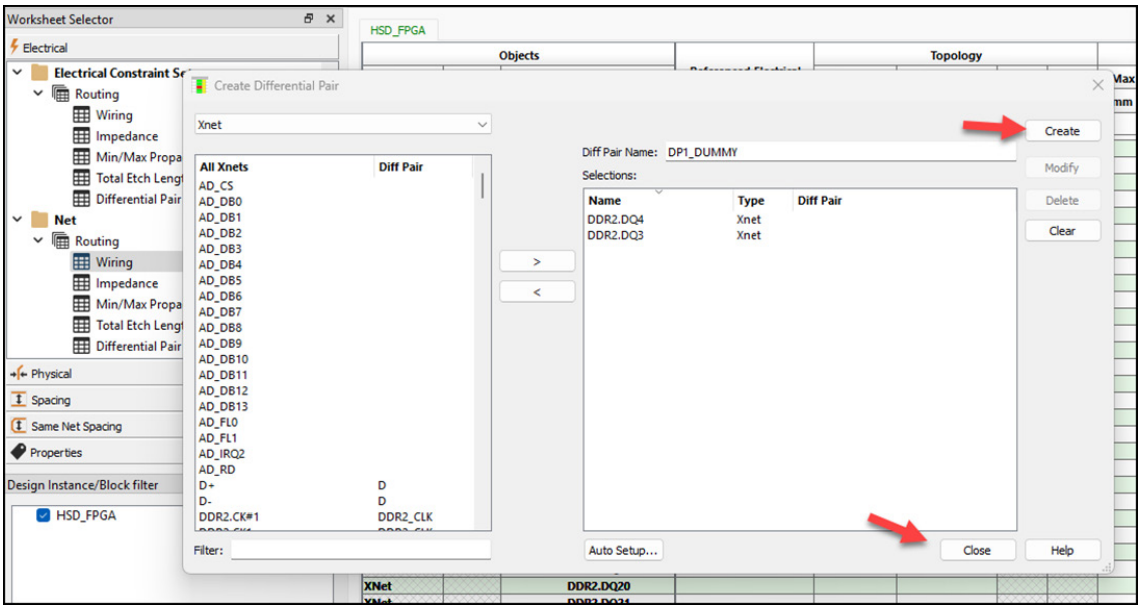
Define Differential Pairs

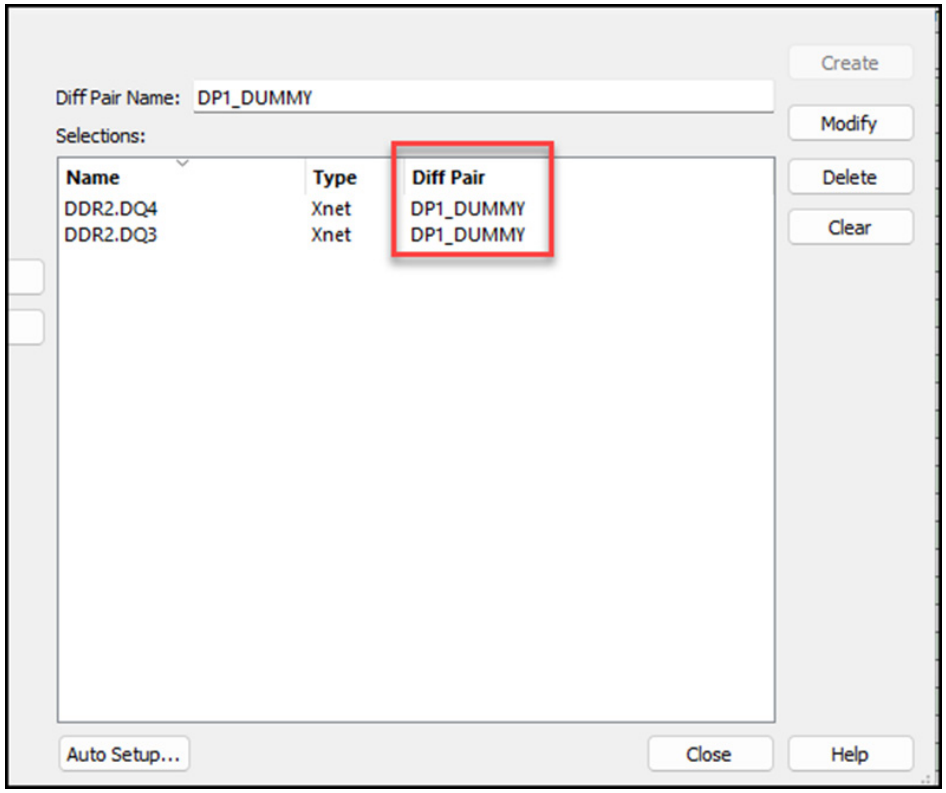
To set up differential pairs in OrCAD X Capture, have the Constraint Manager open:

1. Go to the Electrical > Net > Routing > Wiring worksheet.
2. Select any two signals, like DDR2.DQ3 and DDR2.DQ4 (click, drag and select or use the Ctrl Key + select to choose multiple), then right click and choose Create > Differential Pair….



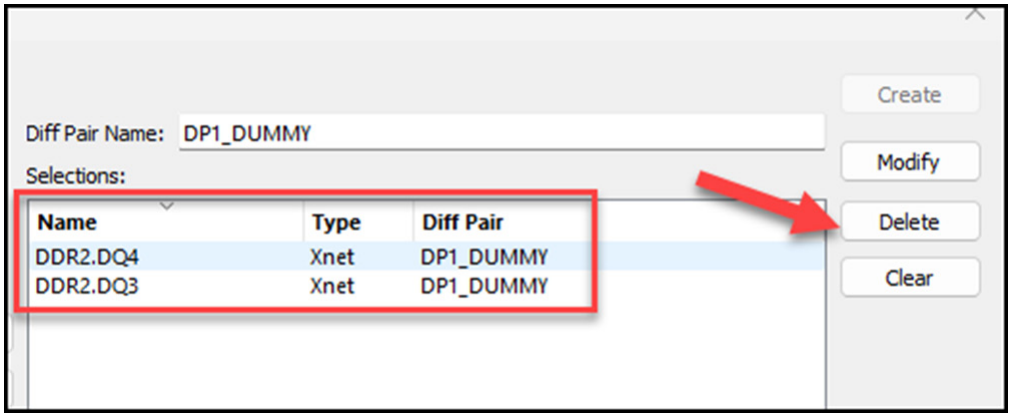
3. Name it whatever you want, then click on Create, then Close.

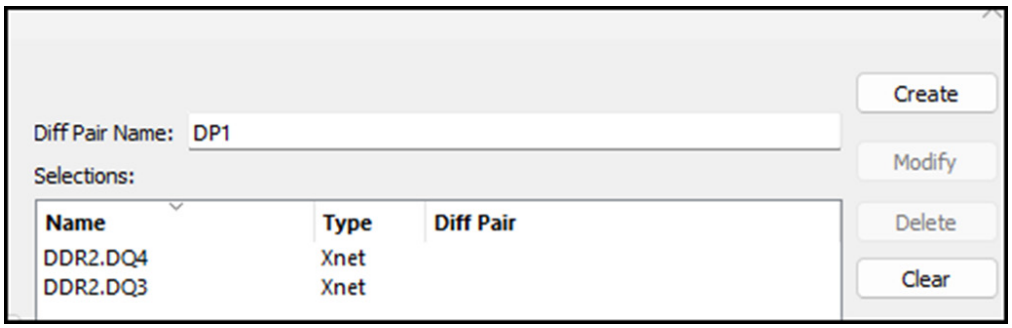




Notice how the **Diff Pair** column shows the name of the differential pair we just created (DP1_DUMMY).

4. Now, since we don't need these set as a differential pair, click the Delete button. Those differential pair names (DP1_DUMMY) will be cleared (see below).





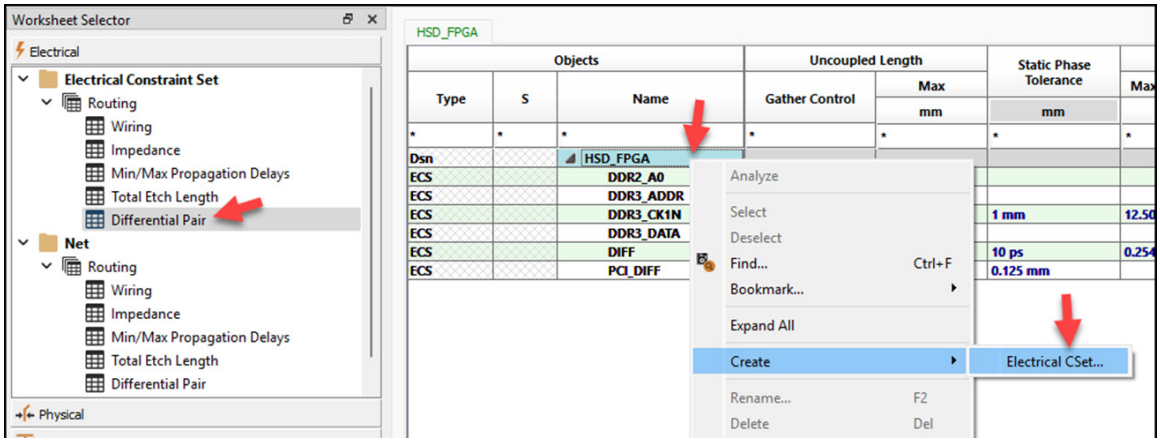
5. Click the Close button at the bottom of the Create Differential Pair window. You will return to the worksheet from where you created the differential pairs.
6. Scroll up to DDR2_DQS0, then click the arrow button to expand the list, which shows the differential pair nets, DDR2.DQS#0 and DDR2.DQS0, which are strobe signals for the data group (DDR2.DQ0 through DDR2.DQ7)

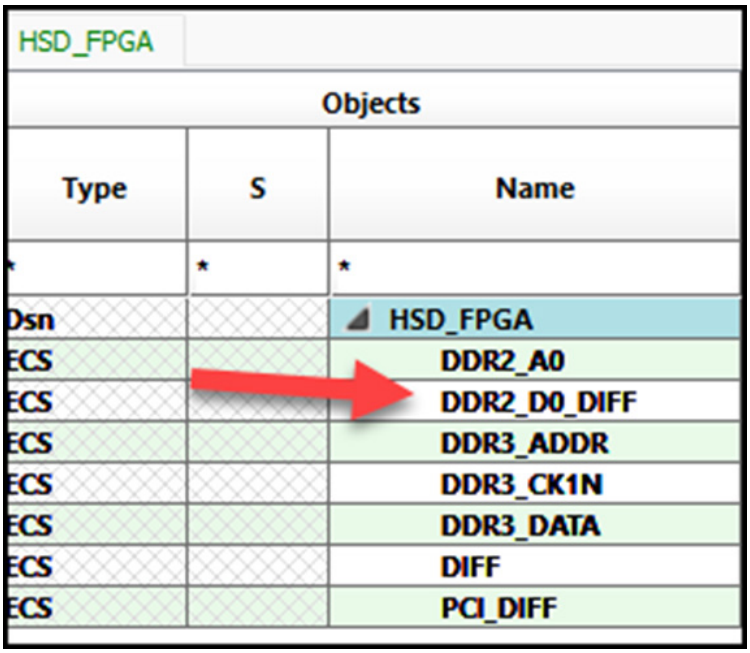
Copying Constraint Sets

Now that we have differential pairs already, we need some rules. You can simply copy a differential pair constraint set (right click, then copy and them from existing constraint sets and confirm. Rename the ECSet as needed), then apply those rules to the appropriate differential pair.

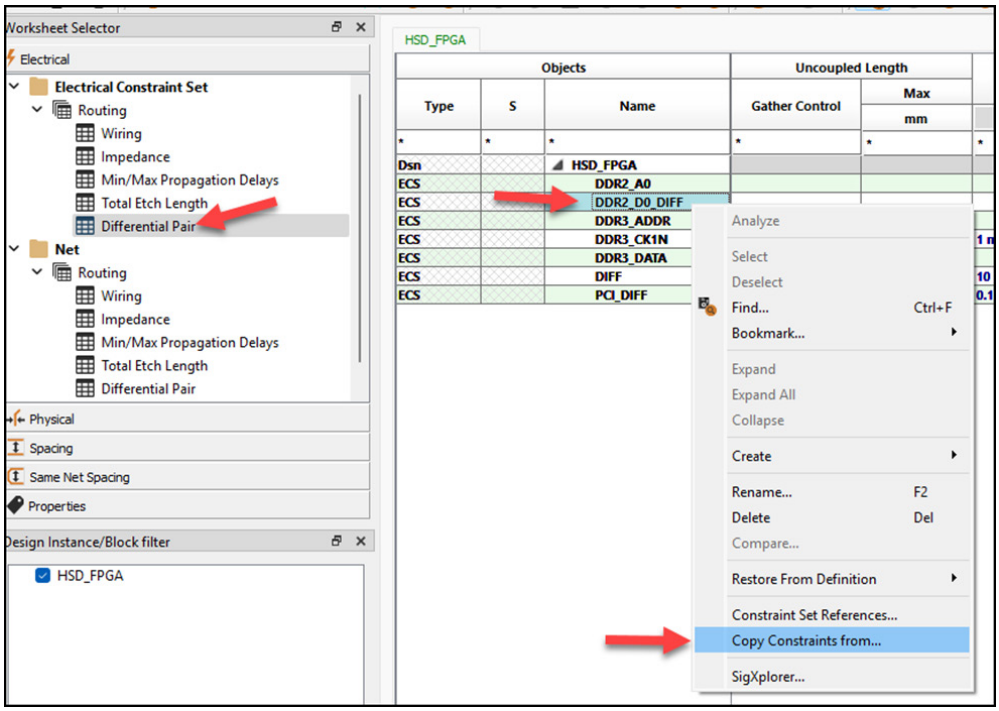
For example, in the Constraint Manager:

1. Go to the **Electrical Constraint Set > Routing > Differential Pair** worksheet.
2. Right click on the Dsn element called HSD_FPGA, then create a new Electrical Constraint Set named **DDR2_D0_DIFF** as shown below.





3. Once created, we will copy existing constraints from DIFF into this new ECSet we just made (DDR2_D0_DIFF). Right click on the DDR2_D0_DIFF ECSet, then choose Copy Constraints From (shown below).



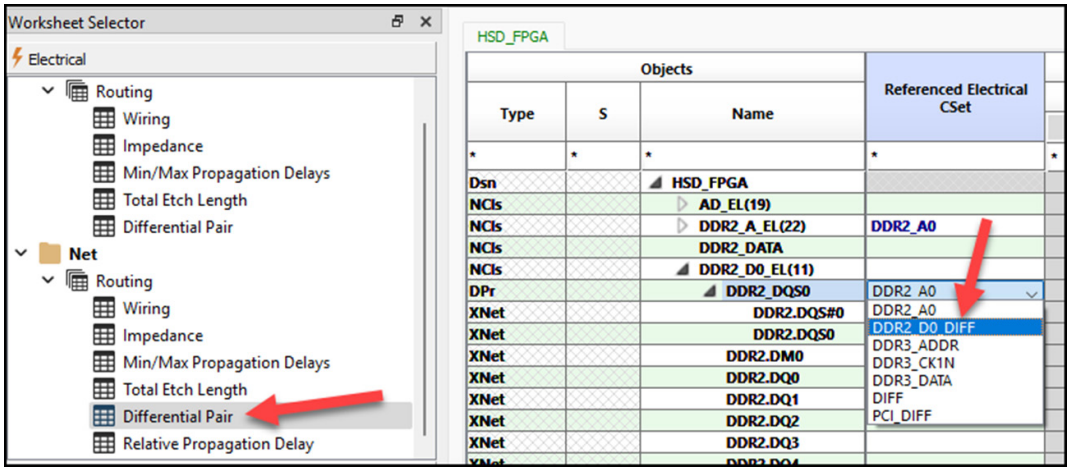
4. You get a new Select Object window. Choose the DIFF constraint set to copy the constraint values from, then click Ok.
5. Notice the values are populated immediately afterward for DDR2_D0_DIFF.

Exercise: Modify the constraint values as required for your ECSet, based on your design guidelines.

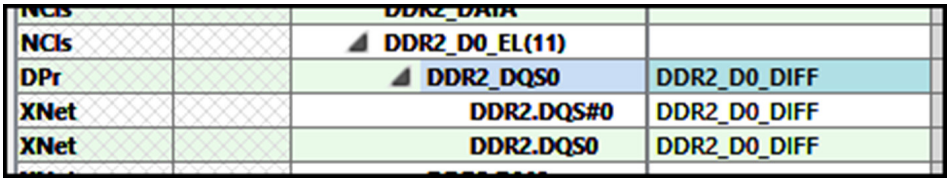
Applying Electrical Constraints

Creating constraints isn't enough. We must apply them to specific nets or net classes. Let's apply the DDR2_D0_DIFF constraint set to the DDR2_DQS0 differential pair. To do that:

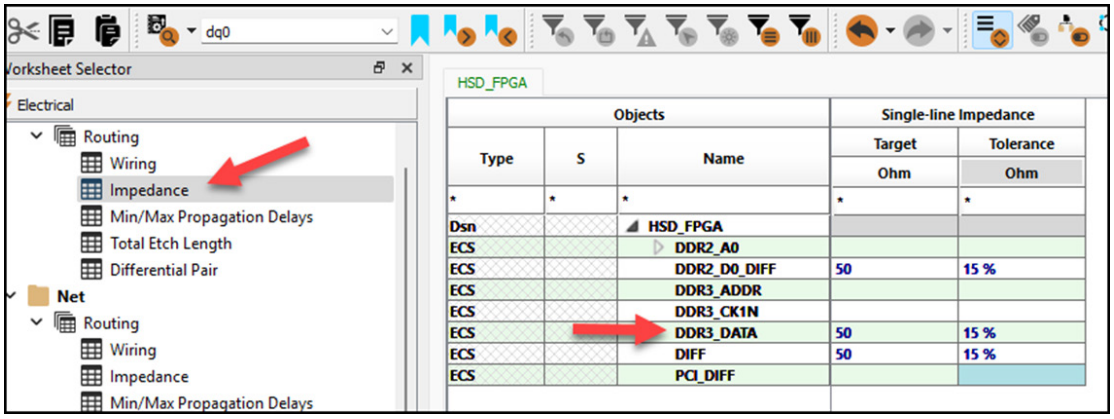
1. Select the Electrical > Net > Routing > Differential Pair worksheet.
2. Go to the Referenced Electrical CSet column for the DDR2_DQS0 differential pair (DPr).
3. Click the dropdown item then select that DDR2_D0_DIFF we created earlier.



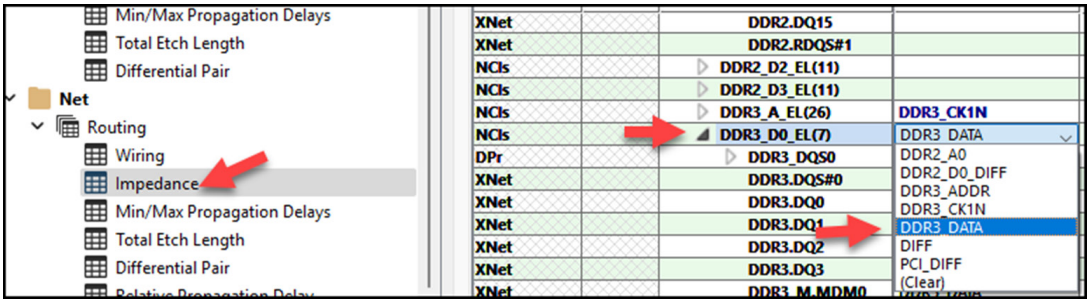
4. You will know that the constraint set was applied when all three rows are populated with the "DDR2_D0_DIFF" constraint set name.

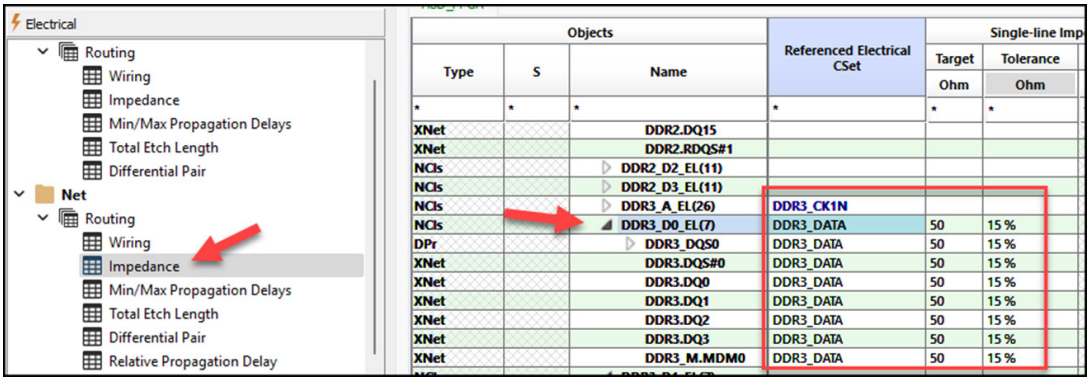


5. For Impedance, apply the 50 Ohm impedance Constraint set to nets within the Impedance worksheet. To do this, go to Electrical > Routing > Impedance > DDR3_DATA (50Ω at 15 %). We will apply this to all our DDR3 Data nets.



6. Now to use this, go to Electrical > Net > Routing > Impedance and select the DDR3_D0_EL(7) cell (that's a Net Class or NCIs Element), then set its entire Referenced Electrical CSet to DDR3_DATA by selecting the dropdown.





7. With that complete, you know how to apply any ECSet to any net or group of nets.

Exercise: Apply a Min/Max Propagation Delays ECSet to a group of Data bit lines (any DDR3.DQ1, DQ2, etc.).

Net Groups

Sometimes we need a group of nets that perform a specific function but may have different (or the same) electrical and physical properties. We call these Net Groups in hardware design.

Net groups can serve various purposes, but for our design, we will use it to match the signal timing for the nets in the same data group DDR3.DQ0 - DDR3.DQ3.

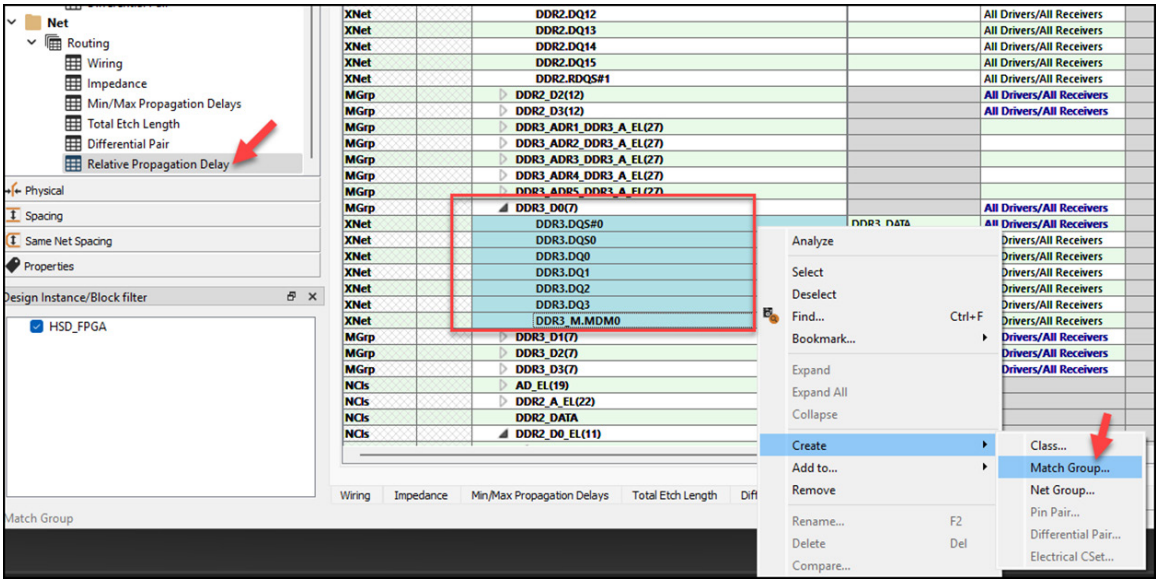
To achieve the same timing for signals, we create a **Matched Group** in the Constraint Manager.

Setting Up Length Matching

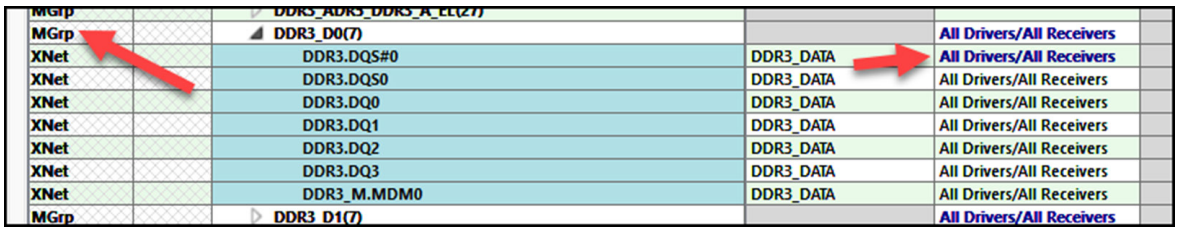
Length Matching requires choosing the correct pin settings within a Matched Group in the Constraint Manager.

To create a Matched Group:

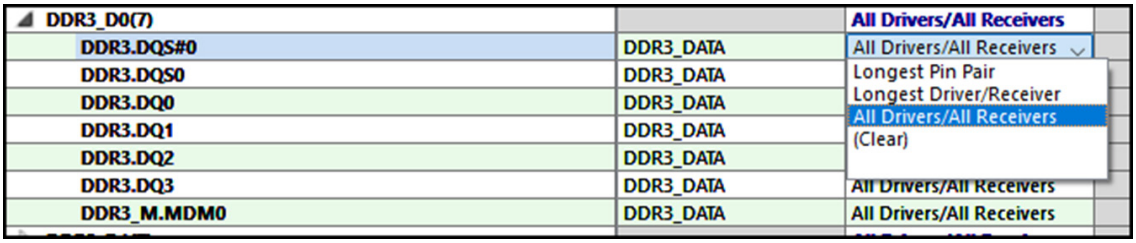
1. Highlight any group of nets that you need to match in timing. Then you can right click and select Create > Match Group…



2. In the new window, Create Match Group, name the match group according to whatever works for your organization's naming conventions, but in this case, click on Cancel.
3. We already have those nets in a Match Group in the worksheet (indicated by MGrp) in the **Type** column on the left-most column of the worksheet.

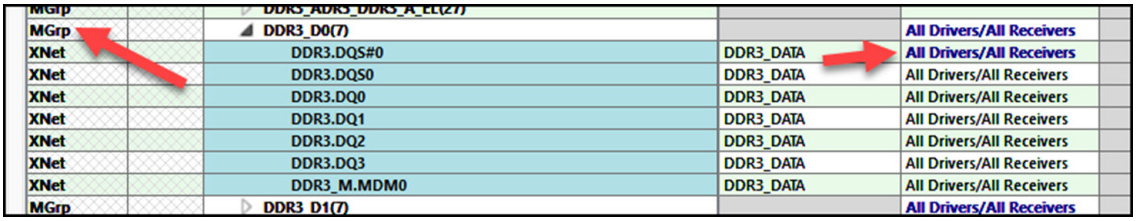


4. We can change the types of Pin Pair combinations that determine how OrCAD X evaluates timing for length matching. Choose the correct option accordingly.



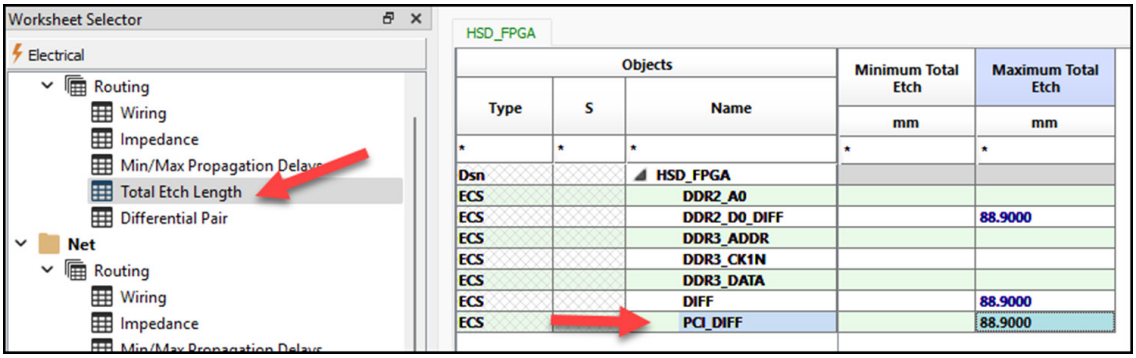
The Longest Pin Pair option will make the longest connection in that group dictate the length matching limits. The Longest Driver/Receiver makes the decision based on the longest driver and receiver pin pairs (pin from the transmitter chip to the pin of the receiver chip) as explained. The All Drivers/Receivers option is the typical safe default. This automatically adjusts the limits as necessary.

5. Choose the **All Drivers/All Receivers** for the Match Group, DDR3_D0(7).

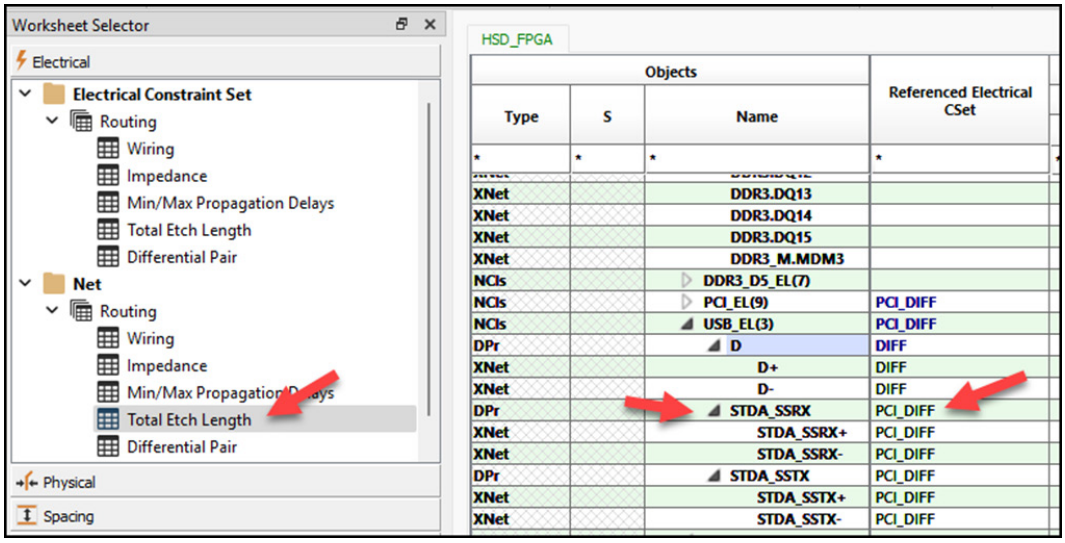


For final Electrical constraint set assignments, do the following:

1. Go to the **Electrical Constraint Set > Routing > Total Etch Length** worksheet. Select the **PCI_DIFF** (set value to 3500 mils = 88.900 mm).



2. Then assign this constraint set by going to the **Net > Routing > Total Etch Length** worksheet.
3. Then assign the constraint, **PCI_DIFF**, on the **STDA_SSRX** Differential Pair object as shown below.



Electrical Constraints Conclusion

By meticulously defining constraints within the Constraint Manager, we've established a robust framework for our high-speed FPGA design.

These constraints will guide the PCB layout process, ensuring that critical signals meet their performance requirements and that the design adheres to manufacturing standards.

In the next section, we'll explore how to apply these constraints effectively during the PCB layout phase, translating our defined rules into a physical design that meets our high-speed requirements.

Physical Constraints (Schematic Phase)

First, we'll create a physical constraint set for our DDR3 interface using the Constraint Manager. The physical constraints for the PCB are set by current carrying capacity, board density, manufacturable capabilities of your manufacturer, and impedance abilities of the selected materials for your PCB stack-up. For our design we have the following constraints as examples.

Trace Width Rules:

- Minimum width: 4 mils (high-speed signals)
- Standard width: 6 mils
- Neck Mode: 3.5 mils (BGA escape)

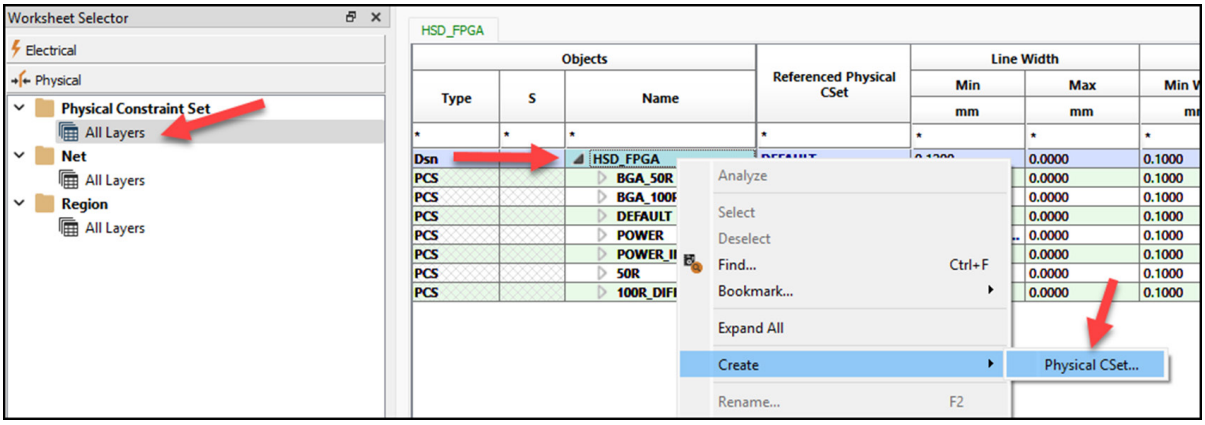
Differential Pairs:

- Min Line Spacing: 3.5 mils
- Trace Width: 4 mils
- Gap Width: 3.8 mils
- Max Uncoupled: 100 mils

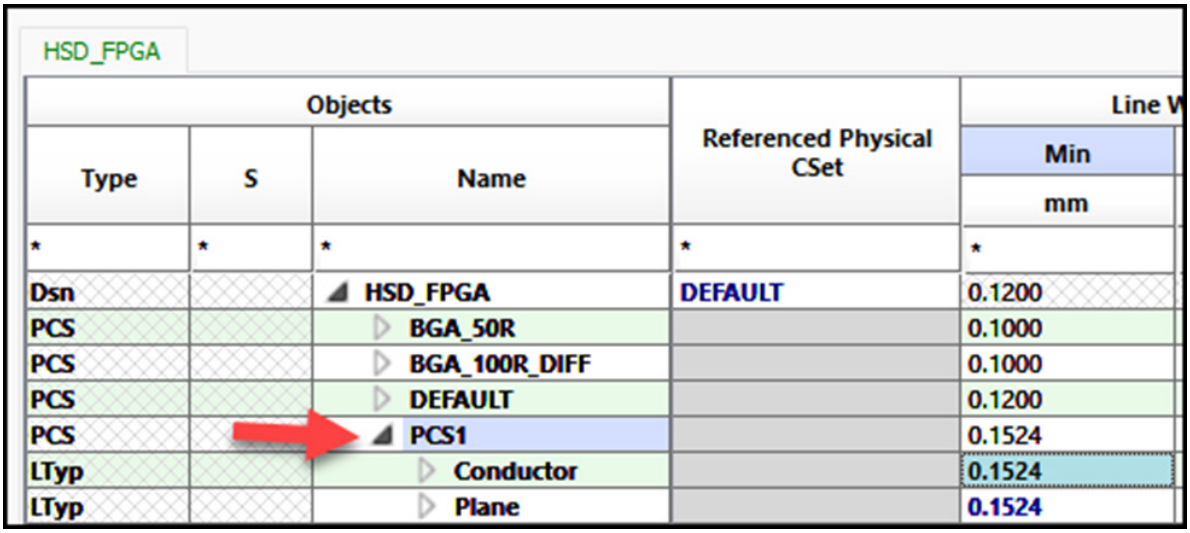
Trace Width Constraints

To set constraints for trace widths, open OrCAD X Capture Constraint Manager by going to PCB > Constraint Manager.

1. Go to the Physical section on the left of the Constraint Manager window, then go to **Physical Constraint Set > All Layers**. Notice we have physical constraints already set. For an exercise, let's say we want 6 mil (0.1524 mm) traces as a standard routing setting for normal traces, then for high-speed signal traces that need impedance control, let's use 4 mils.
2. Right click the **HSD_FPGA** element then select Create > Physical CSet…



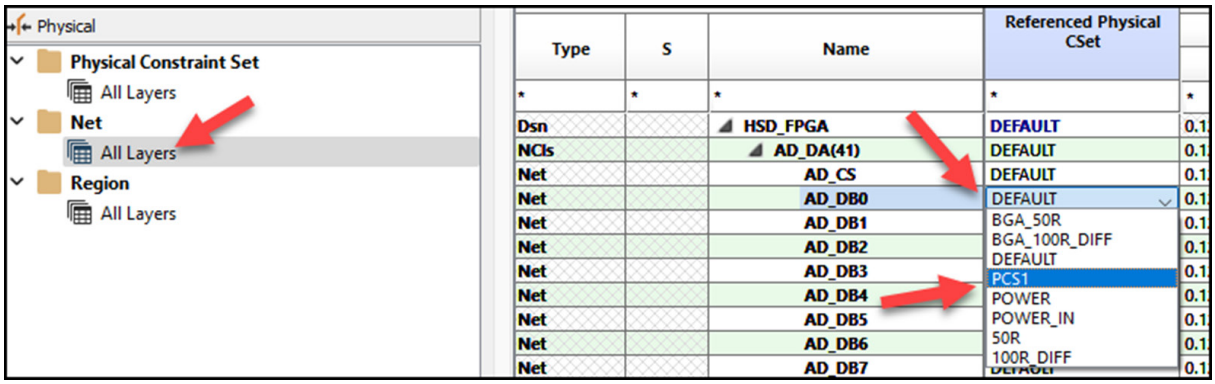
3. Name the Electrical Constraint Set as **PCS1**. It gets created (see below).



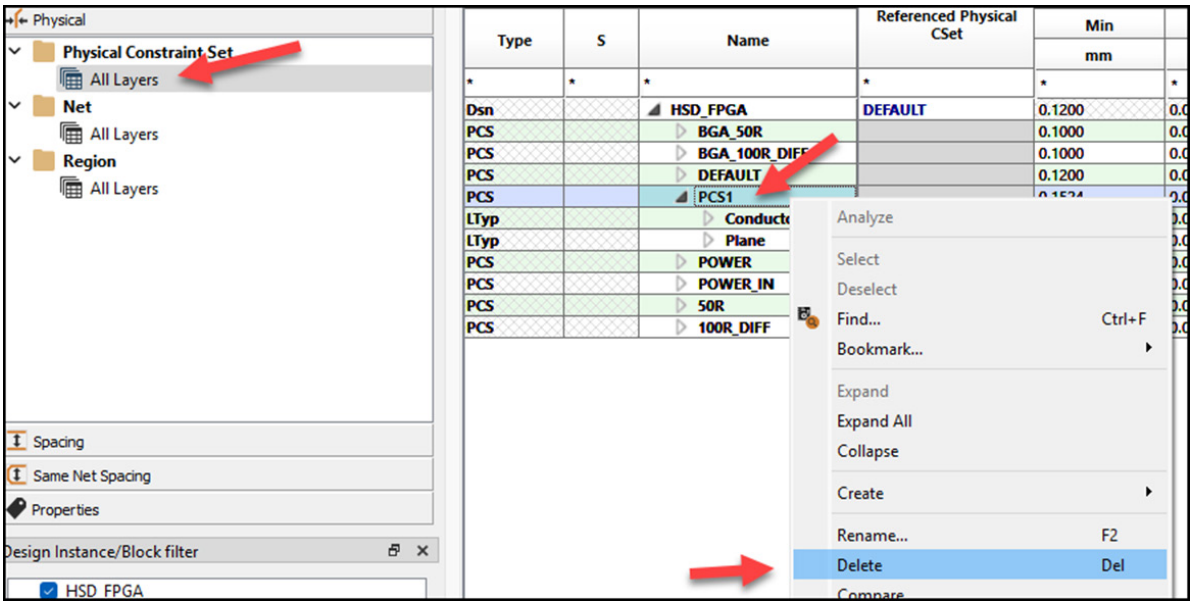
4. We created an arbitrary Physical Constraint Set named PCS1.
5. Set the Line Width to 6 mils (0.1524 mm).

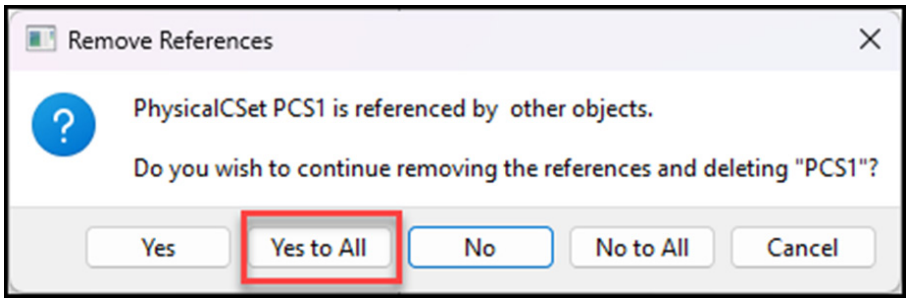
We can use this constraint set to apply it to any nets that don't need 4 mil widths for impedance control or don't need to be as narrow as 4 mils. However, note that 6 mil traces give you fewer routing options on a densely populated PCB. It may just be best to go with 4 mils for every trace if that won't affect cost more than having such narrow traces normally would.

To apply the physical constraint set, simply go to the **Physical > Net > All Layers worksheet**. Then select a net, net group or net class, then apply the physical constraint set to that/those nets (as shown below). In our case, **AD_DB0**.

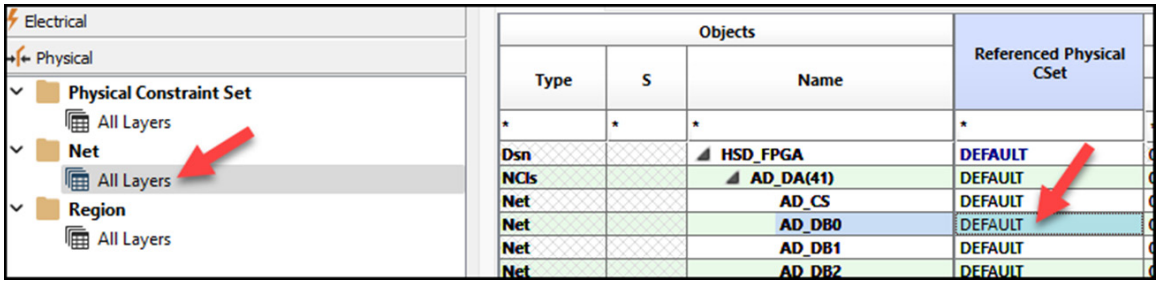


Exercise: This constraint assignment is unnecessary, so let's delete it by right clicking the original Physical Constraint Set worksheet (in Physical Constraint Set > All Layers), then choosing the constraint "PCS1", right clicking it, then choosing Delete. You will be asked if you're sure. Say Yes/Ok. Then you'll be asked if you wish to continue removing the references and deleting "PCS1"? Choose Yes to All (see below).





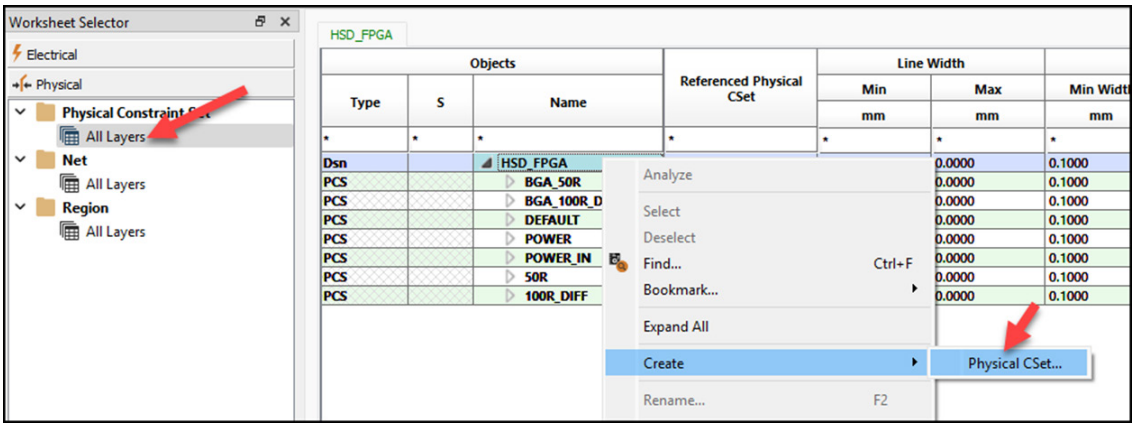
Once deleted, go back to the **Physical > Net > All Layers** worksheet. Notice for **AD_DB0** how the Referenced Physical CSet changed back to DEFAULT and no longer has PCS1.



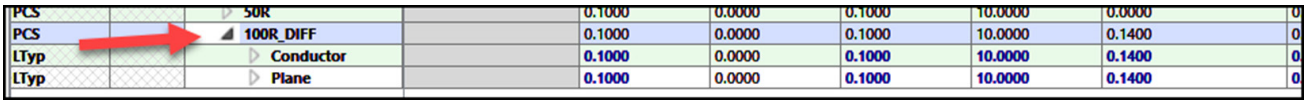
Differential Pair Constraints (Physical)

Constraint Manager has two ways to manage differential pair constraints, electrical and physical. The physical constraints are implemented the same way as the electrical constraints. However, the physical constraints for differential pairs specify allowing **Etch** (copper) or **Ts**, while the electrical constraints for differential pairs do not have those options.

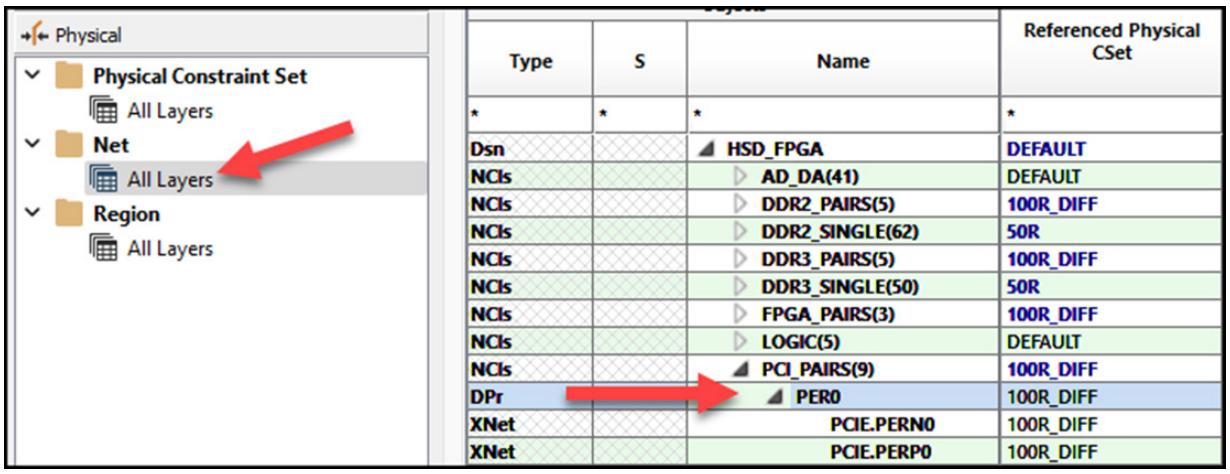
Follow similar instructions to set a differential pair constraint set and you can apply them to any differential pair within the **Net > All Layers** worksheet. See images below to see the constraint and application.



That's to create a differential pair. But let's delete it, we will use the existing differential pair physical constraint set named **100R_DIFF**.



Then apply it to the appropriate differential pairs in the **Net > All Layers** worksheet. Expand the **PCI_PAIRS** Net Class (shown below), then apply it to any of the differential pairs within that class, like **PER0.** Notice that the rule is applied to all the differential pairs within that class already.



Spacing Constraints

We can even set spacing constraints at the schematic phase. Proper spacing is critical to avoid crosstalk in PCB design. The general most conservative rule of thumb is to make the trace edges at least 3 times the width of any particular trace. In some cases, it can be less than or more than that. The details are left up to your discretion from design guides, datasheets and EMC specialists.

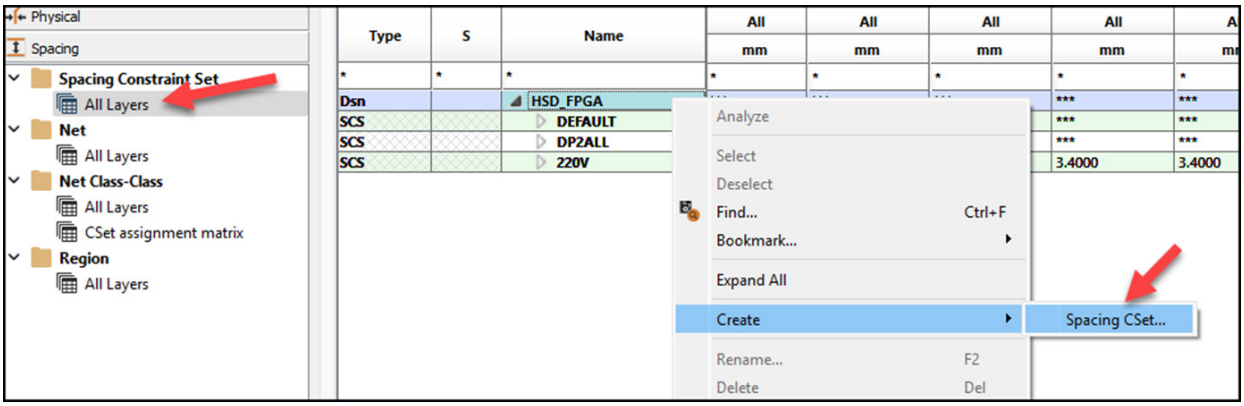
To separate the standard traces from each other and maintain minimal coupling in general, we create the following:

1. Critical Signal Spacing:
    a. CLK to other signals: 3x trace width
    b. DATA to DATA: 2x trace width
    c. ADDR to ADDR: 1.5x trace width
2. BGA Region Specific:
    a. Trace to Trace: 4 mils
    b. Pad to Trace: 5 mils
    c. Via to Via: 8 mils
3. Differential Pair Spacing:
    a. Intra-pair spacing
    b. Inter-pair spacing

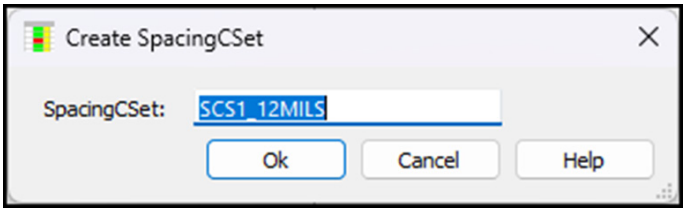
Critical Signal Spacing Constraints

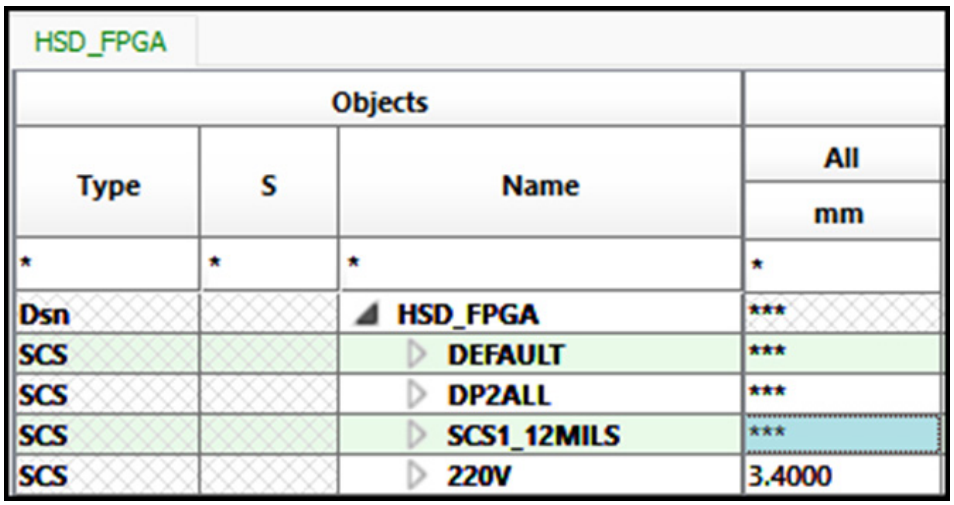
For critical traces, create a new spacing constraint set (SCS) by doing the following:

1. Navigate to the Spacing > Spacing Constraint Set > All Layers worksheet.
2. Right click the HSD_FPGA object.
3. Choose Create > Spacing CSet…

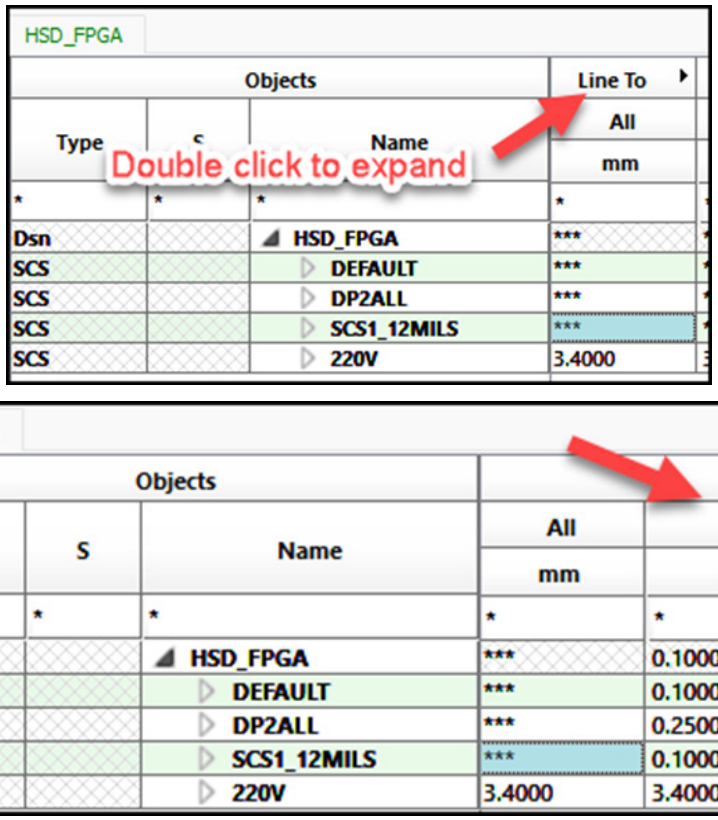


4. Name the constraint set something that indicates the spacing, like 12 mils (3x trace width, so 3x4 mils = 12 mils), so name it SCS1_12MILS. Then it will populate the list as shown below.

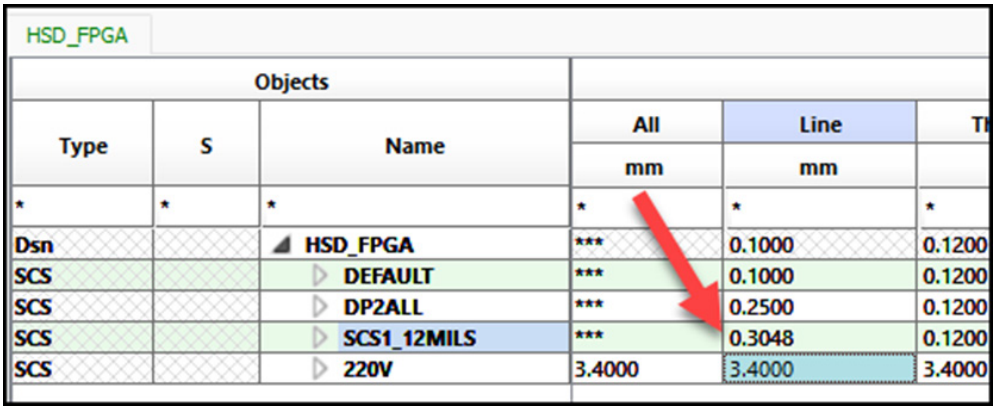




5. We have a lot of spacing constraints, but we only care about trace-to-trace spacing right now (line-to-line). Double-click the column that says **Line To** at the top. That expands our Line-to-Object options (e.g. Line to Line, Line to Thru Pin, Line to SMD Pin, etc.).



6. We care about line to line spacing. Set the value to 12 mils = 0.3048 mm (you can type it in as 12 mils and it will automatically convert it to mm or vice versa).



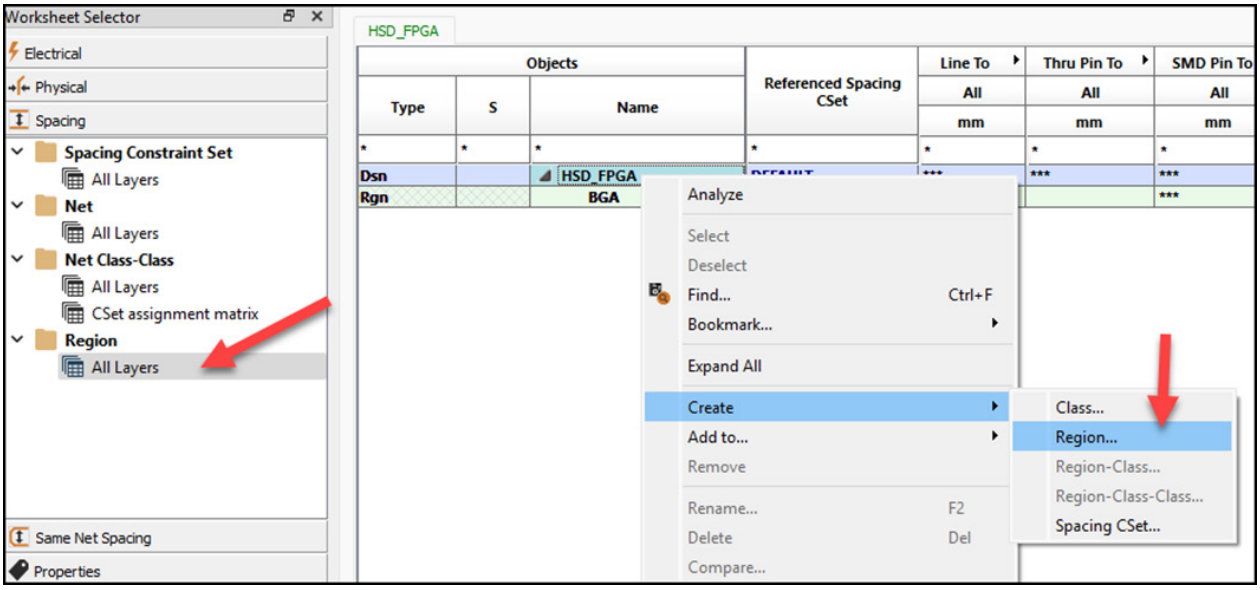
7. Now let's apply the constraint to a critical net, like Clock.
8. Notice the 220V Spacing Constraint Set as well. Its traces are set to be at least 3.400 mm (133.858 mils) away from all other traces.

This is nice but what about regions that need tighter spacing?

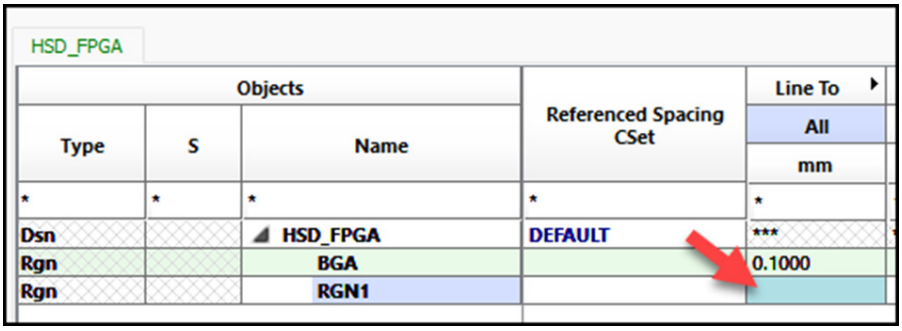
Region-Specific Spacing Constraints

Constraint Manager can set entire regions to have different spacing constraints.

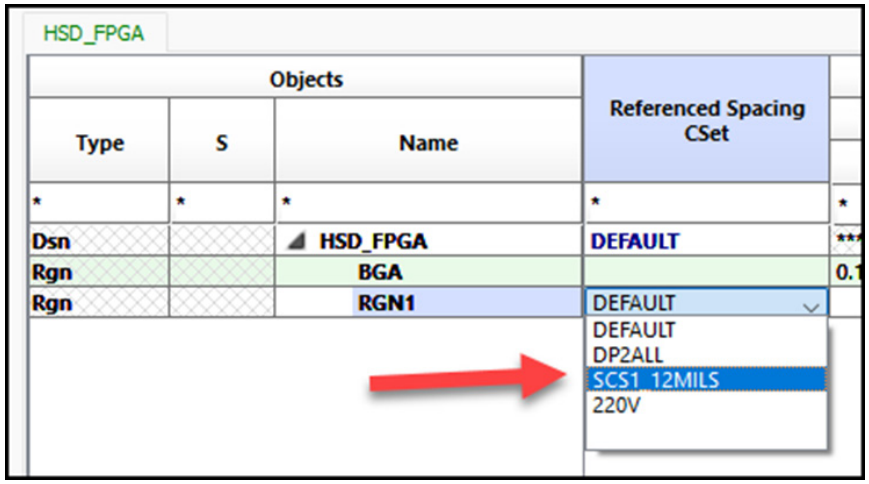
1. Select the **Spacing > Region > All Layers** worksheet.
2. Right click the HSD_FPGA design name.
3. Choose Create > Region….



4. In the new window, name the region the default and click OK. Then you have the region created as RGN1 (see below), where you can set the Line To (any object) spacing.



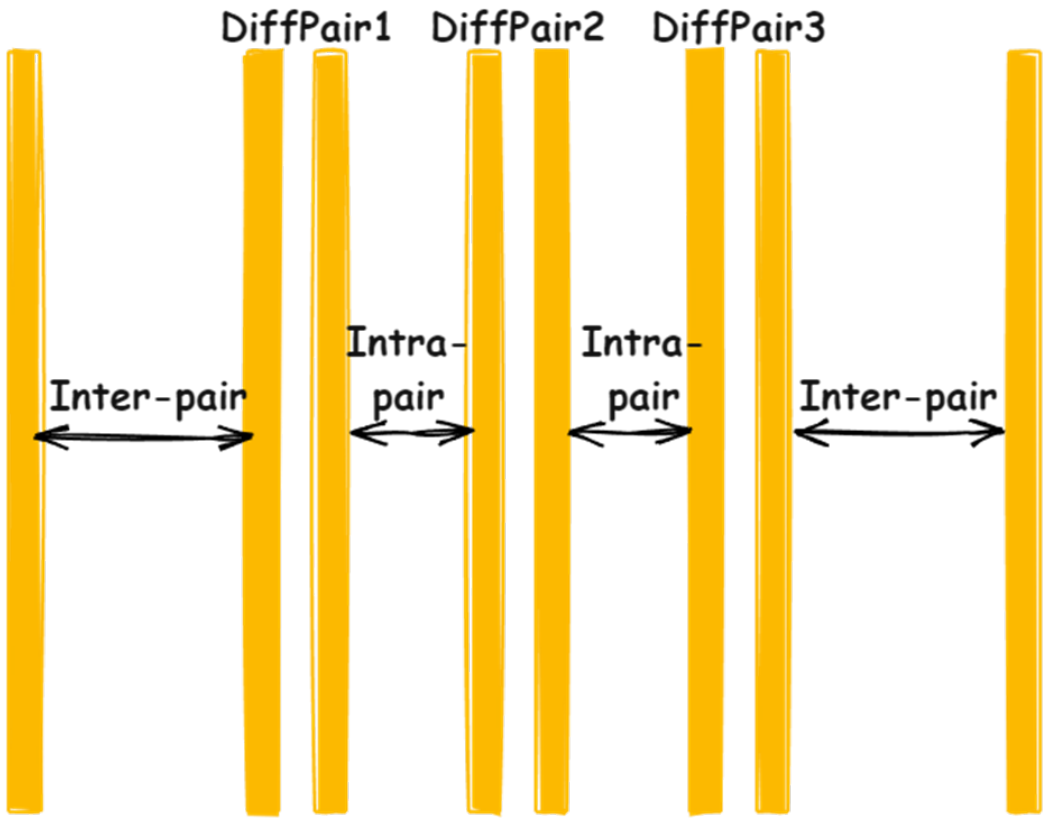
5. The best option is to apply a spacing constraint set that's already created, so click the Referenced Spacing CSet column option, then select the SCS1_12MILS CSet we created earlier.



Now that you've learned how to set constraints for traces, let's look at Class-to-Class spacing, as we need it for differential pairs.

Differential Pair Spacing Constraints

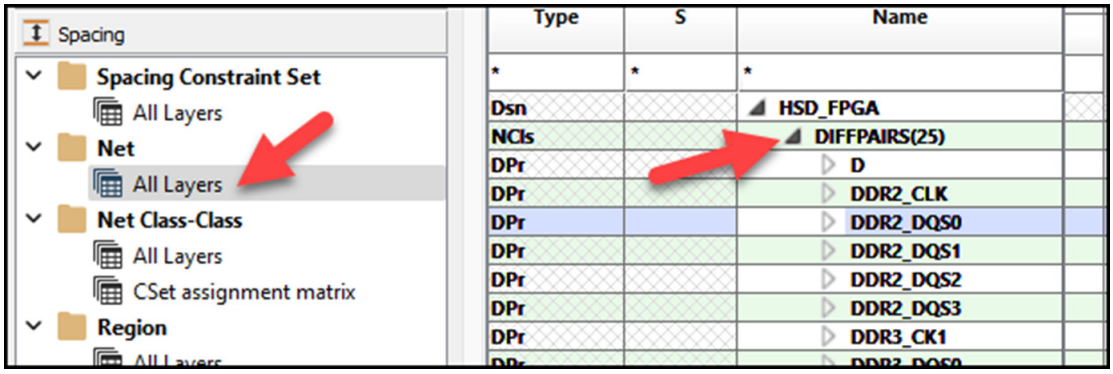
For differential pairs we need to create class-to-class spacing. You already know how to make net classes, so we will show how to set differential pairs to have the right intra-pair spacing (edge to edge, differential pair to differential pair) and inter-pair spacing (differential pair to any other non-differential pair).



Differential pairs indicating inter-pair and intra-pair spacing

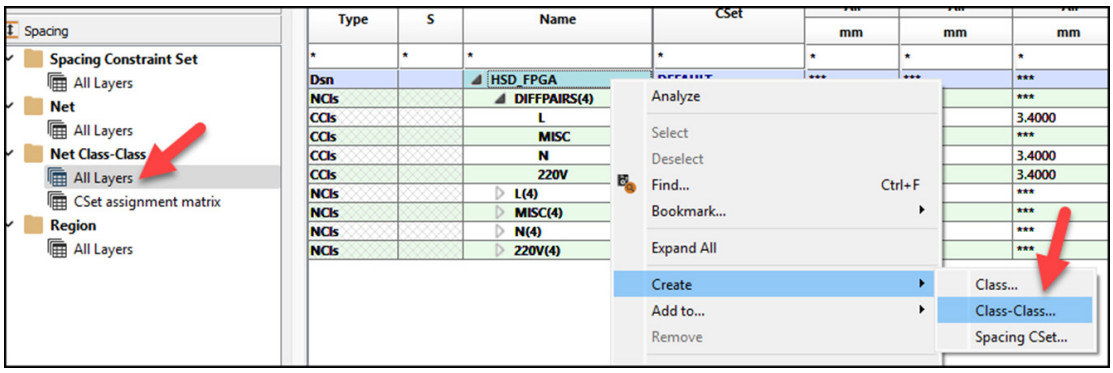
To set the differential pair spacings as shown above, do the following within the Constraint Manager:

1. Go to **Spacing > Net > All Layers**. Notice the Net Class (NCIs) named DIFFPAIRS(25).



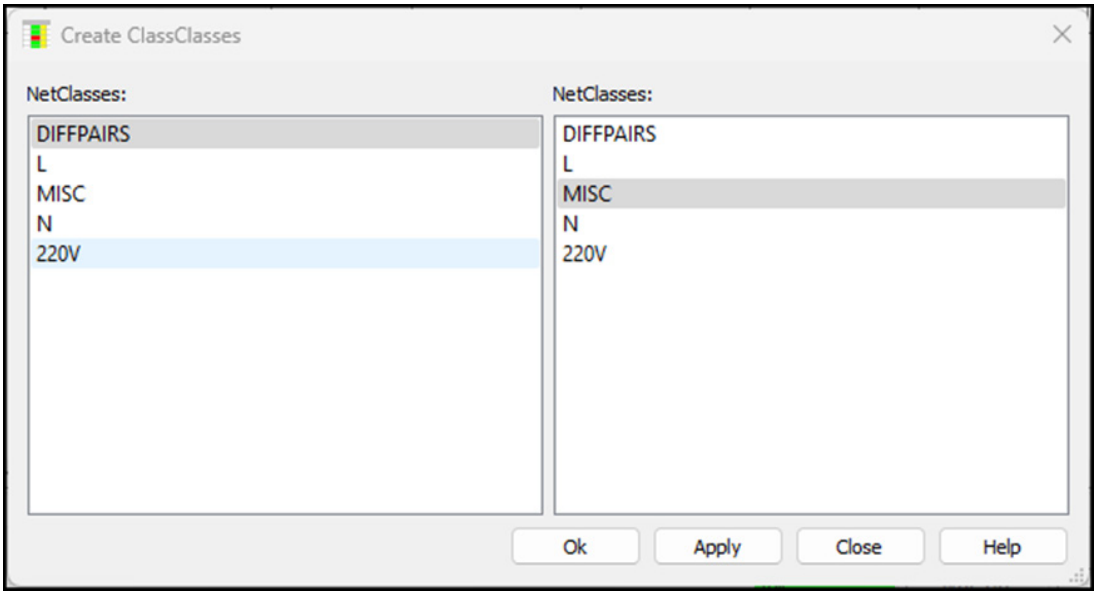
2. We'll make a class-to-class rule that says any differential pair to another differential pair will have a certain spacing (intra-pair), and any differential pair to any other class of nets will have other kinds of spacing (inter-pair)

3. Go to the **Net Class-Class > All Layers** worksheet.

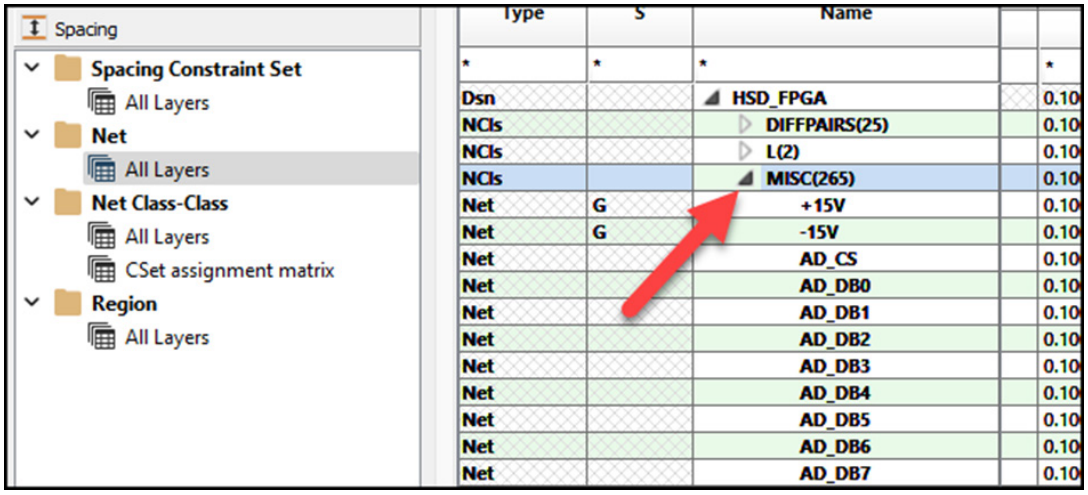


4. A new window, Create ClassClasses, appears. Under the NetClasses sections on the left and the right, select DIFFPAIRS for each, then click Apply. The list will populate with that class-to-class spacing for intra-pair spacing.

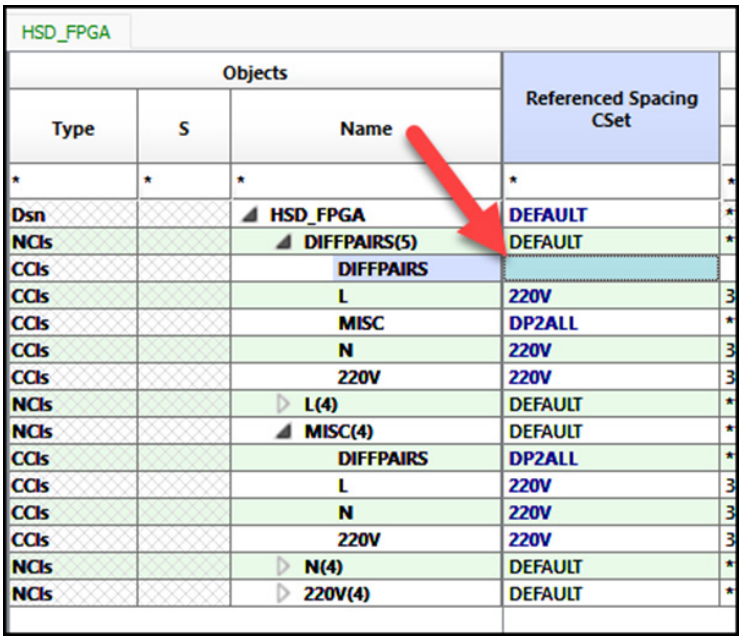
5. For the inter-pair spacing (diff pairs to all other net classes), select DIFFPAIRS in the left column and MISC in the right column.



6. MISC is all other nets from what we have defined in the Net Classes already (see below).



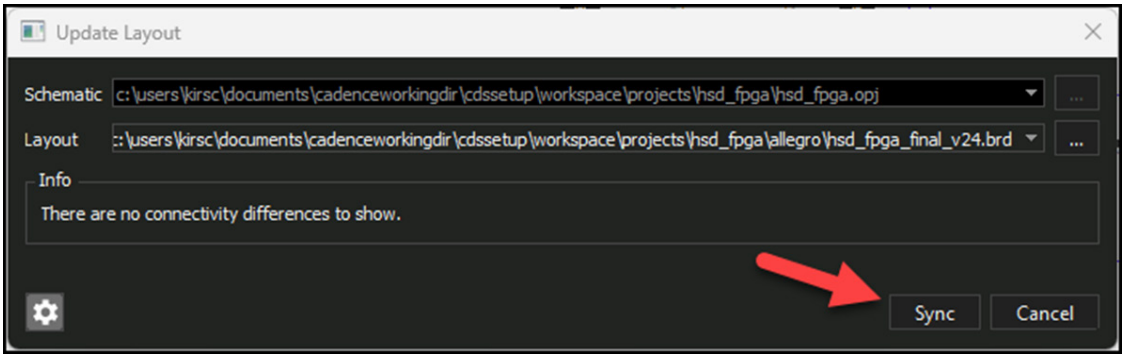
7. Now you can set the spacing for DIFFPAIR to DIFFPAIR (intra-pair) to whatever you wish, but choose it from a Spacing Constraint Set (you can pick anyone, but given the current values, you should create one, say 20 mils).



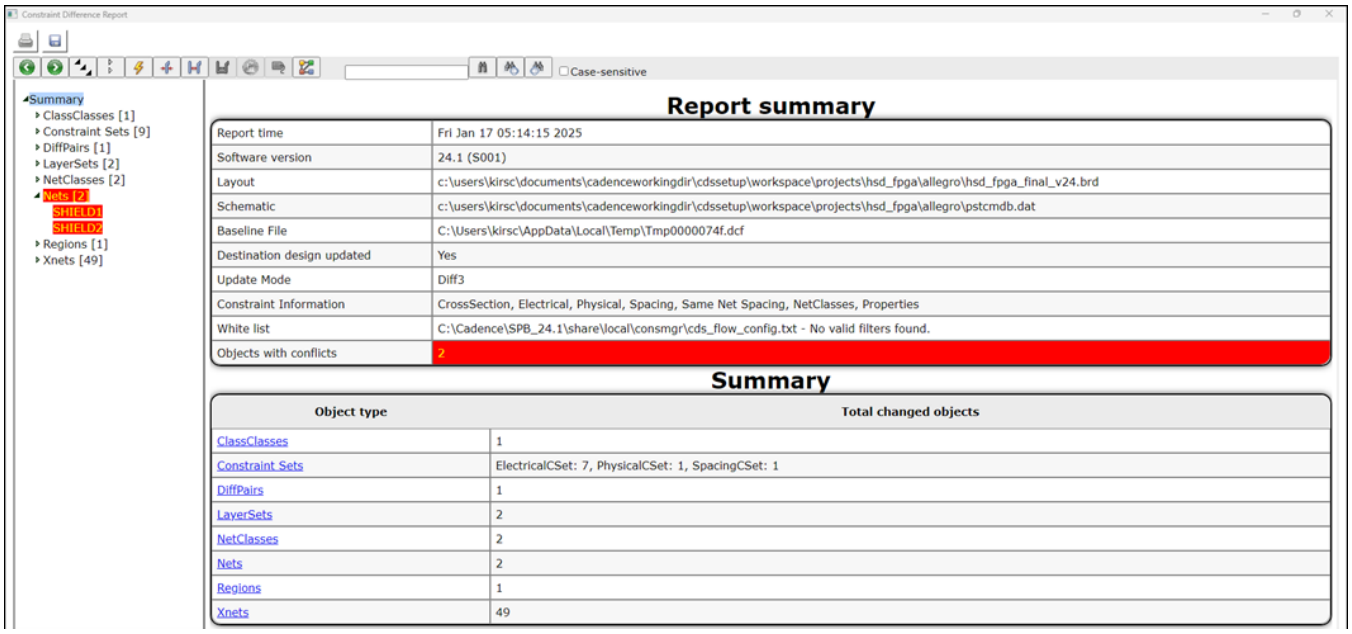
Exercise: Create a spacing constraint set that sets line to line spacing at 20 mils and name if DIFFTODIFF. Then assign that spacing constraint set (SCS) to the DIFFPAIRS to DIFFPAIRS class-to-class spacing from the previous step.

This ends the schematic-enabled constraint settings you can create in OrCAD X Capture.

In OrCAD X Capture, go to **PCB > Update Layout** in the toolbar menu. The Update Layout window will appear. Click on the Sync button as shown.



It generates a Constraints Difference Report as shown below:



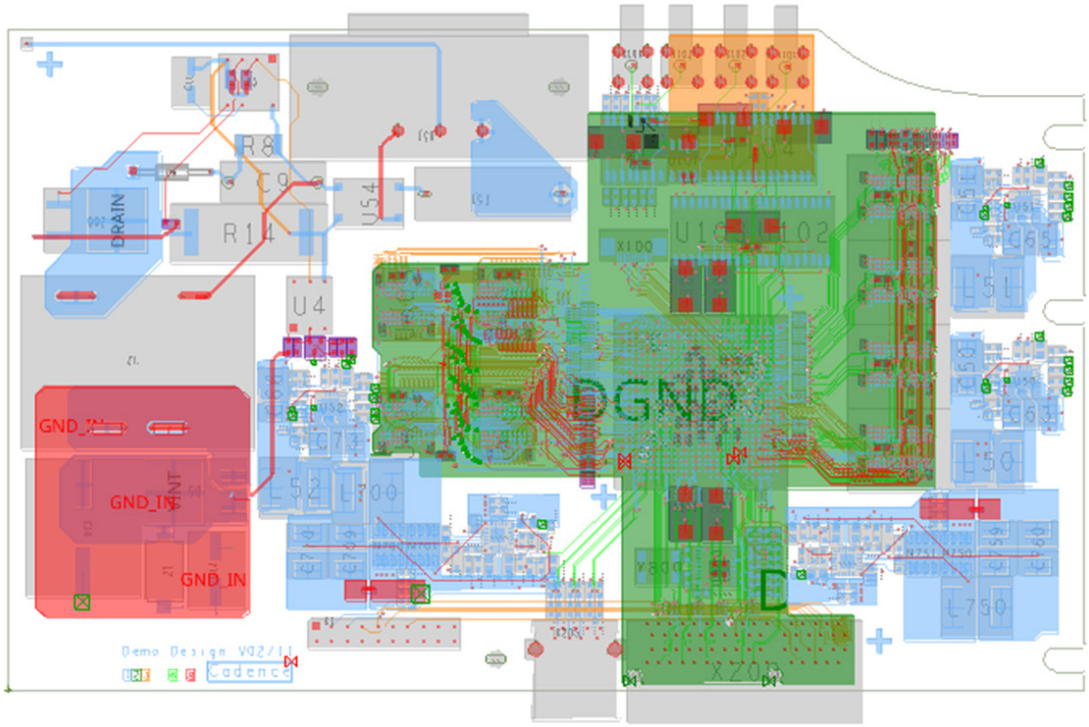
For now, ignore the warnings/error messages and open OrCAD X Presto PCB Editor.

PCB Layout

Introduction

PCB layout is a critical phase in high-speed design, where the schematic and constraints are transformed into a physical board. For our FPGA with DDR memory project, careful attention to component placement, stackup definition, and routing is essential to maintain signal integrity and meet performance requirements.

This project has a completed PCB layout. We will analyze the critical parts of the design that need to be created for a successful high-speed layout. Not every net will be covered in this design. We will explain just enough of the nets and rules to implement so you know how to apply them to most any situation. The rest of the net or entire design is left as an exercise for the reader.



Top view of a completed PCB Layout.

Here are the devices we will focus on:

- FPGA
  - Manufacturer Part Number: XC6SLX25-3FTG256I
- 2 DDR3 interfaces
  - Manufacturer Part Number: UPD431000AGW-B15
  - Manufacturer Part Number: MT41J512M4JE-15E:A

The operating frequency for DDR interface is 300–800 MHz, maximum allowed jitter could be whatever is reasonable, crosstalk coupling limit 8% for critical signals like clock, target impedance for power distribution network, and a FCC class - whichever one is more lenient.

Manufacturing capabilities specify a minimum trace width of 4 mils for high-speed signals. Standard non-high-speed signals are maybe 6 mils. There is a lot going on in the design, but we will start with the most essential high-speed signals and steps in general that need to be covered.

General Solution

Effective PCB layout involves defining an appropriate stackup, strategically placing components, and routing traces according to the defined constraints. This approach ensures optimal signal performance, minimizes electromagnetic interference, and facilitates proper power distribution.

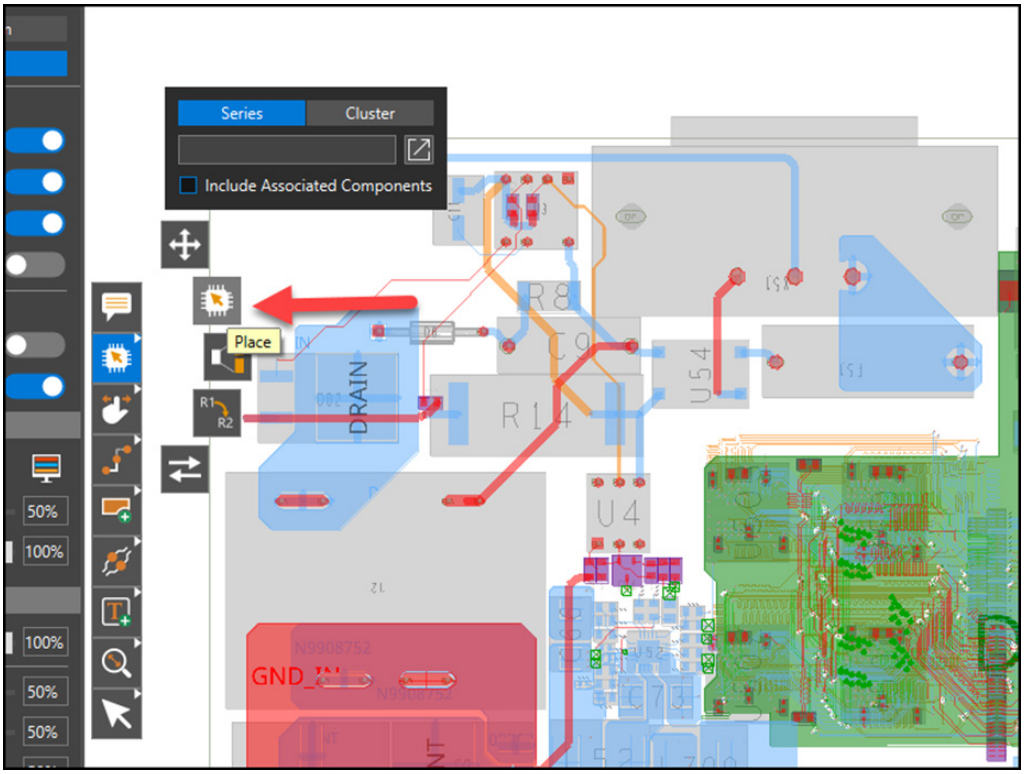
Application in OrCAD X Presto:

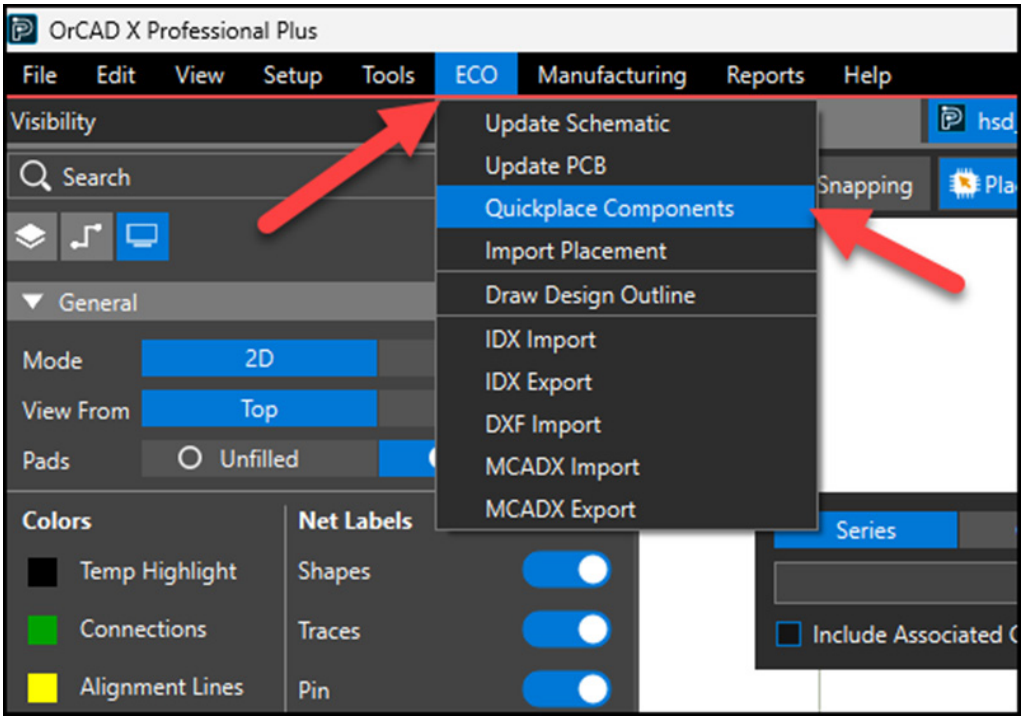
1. Define the PCB stackup:
    a. Go to Tools > Cross Section
    b. We have an 8-layer stackup with dedicated power and ground planes:
        i. Top Layer (Signal)
        ii. Ground Plane (GND1)
        iii. Signal Layer 1 (L1)
        iv. Power Plane (POW1)
        v. Ground Plane 2 (GND2)
        vi. Signal Layer 2 (L2)
        vii. Power Plane 2 (POW2)
        viii. Bottom Layer (Signal) (BOTTOM)

Primary

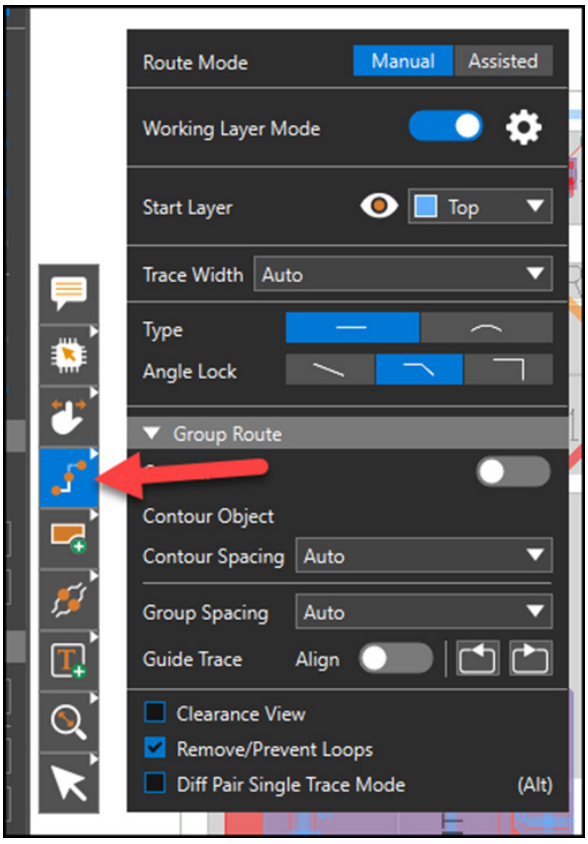
OBJECTS		TYPES				THICKNESS	
#	NAME	LAYER	LAYER FUNCTION	MANUFACTURE	CONSTRAINT	VALUE	(+)TOL.
*	*	*	*	*	*	*	*
		Surface					
		Dielectric	Dielectric			0.01	0
1	TOP	Conductor	Conductor			0.055	0
		Dielectric	Dielectric			0.15	0
2	GND1	Plane	Plane			0.03	0
		Dielectric	Dielectric			0.25	0
3	I1	Conductor	Conductor			0.033	0
		Dielectric	Dielectric			0.25	0
4	POW1	Plane	Plane			0.033	0
		Dielectric	Dielectric			0.1	0
5	GND2	Plane	Plane			0.033	0
		Dielectric	Dielectric			0.25	0
6	I2	Conductor	Conductor			0.033	0
		Dielectric	Dielectric			0.25	0
7	POW2	Plane	Plane			0.03	0
		Dielectric	Dielectric			0.15	0
8	BOTTOM	Conductor	Conductor			0.055	0
		Dielectric	Dielectric			0.01	0
		Surface					

2. Place your components:
    a. Use the “Place Component” tool from the floating toolbar
    b. For critical components like FPGA and DDR3 memories:
        i. Go to ECO > Quickplace Components
        ii. Set placement priorities and spacing requirements

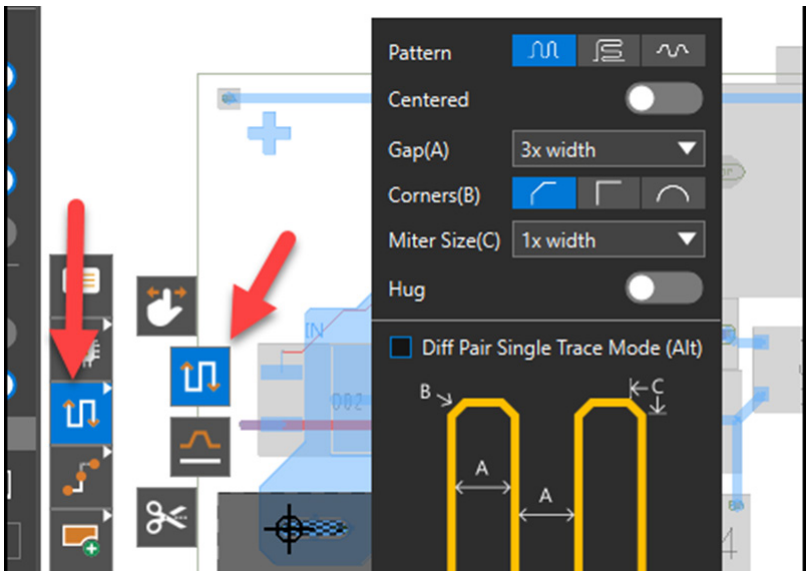




3. Route critical nets:
    a. Use the routing icon on the floating toolbar for manual routing of high-speed signals
    b. For differential pairs, you can use the same tool and click a diff pair to start routing

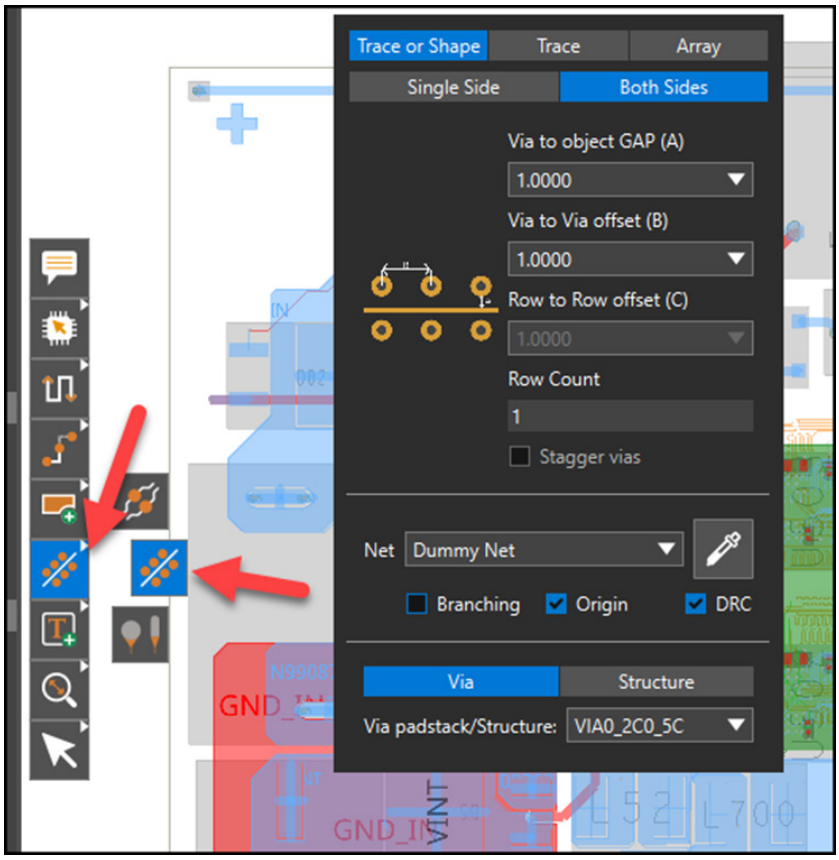


4. Perform length and phase tuning:
    a. Select the delay tune command from the floating toolbar as shown below
    b. Select from the various options and adjust existing traces through length tuning and phase tuning



5. Add stitching vias:

    a. Select the via structure menu option to add via structures



    b. Set parameters for via spacing (e.g., every 500 mils)

These are some of the most important options for getting your PCB placed, routing and ready for manufacturing. Now let's take a look at constraints for high-speed PCBs.

Constraints for Signal Integrity

Advanced constraints include rules for high-speed complex printed circuit boards. Standard PCBs are usually 300 components or fewer, where the primary concern is designing for manufacturing, fabrication, assembly, and test, then maybe differential pairs and single-ended impedances depending on the protocols in your design.

Complex high-speed PCBs however need considerations for impedance control, differential pairs, inter-pair and intra-pair skew, a limit on the number of vias and other such factors that manage signal integrity and electromagnetic interference.

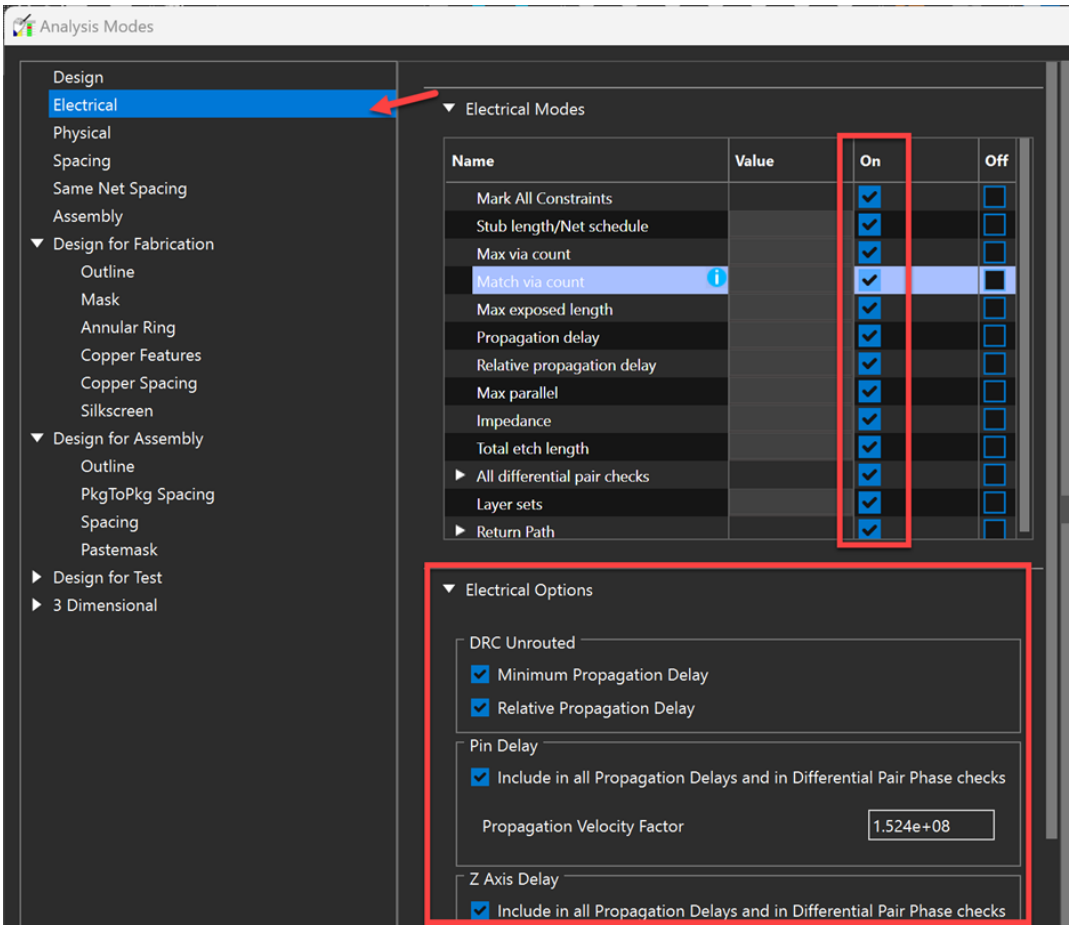
Advanced Constraints also account for typical high-density interconnect boards, military grade PCBs and rigid-flex or flex PCBs. Anything outside the normal DFM considerations would be considered advanced constraints for a printed circuit board.

Now that we understand the difference between regular and advanced constraints, let's look at ways to turn on or off the kinds of constraints we should enforce in the Constraint Modes section.

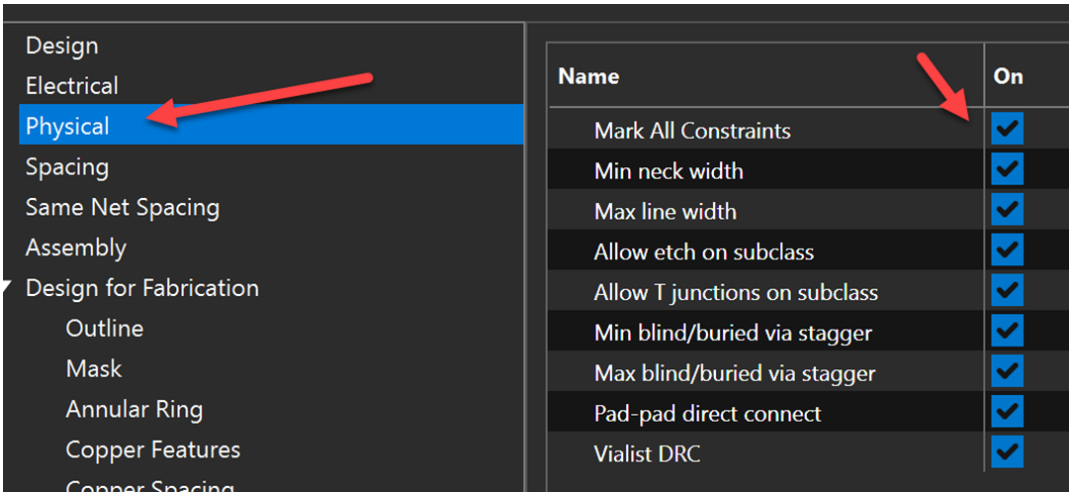
Constraint Modes

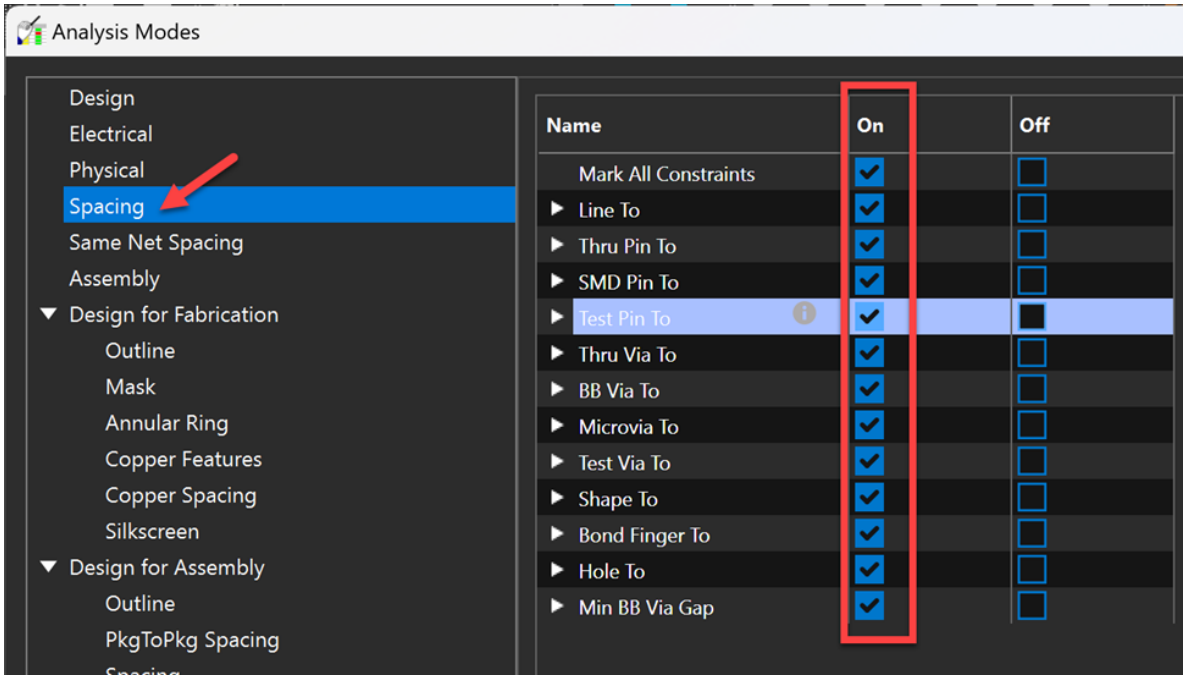
Implementing USB constraints in OrCAD X Presto.

1. Open Constraint Manager by clicking on **Tools > Constraint Manager** in the toolbar menu.
2. Then within the Constraint Manager toolbar menu click on **Analyze > Analysis Mode.**
3. Check all options in the **Electrical Modes** and **Electrical Options** sections (see below).



4. Also enable all checks in the Physical and Spacing Categories as well.





In general, you want to enable all Electrical, Physical and Spacing Constraints when working with high-speed constraints and boards. Note that these can affect performance if routing large complex boards with many layers.

Signal Integrity

In this section we will address the most common rules you should set for signal integrity in the PCB. We are using a different reference design for the PCB Layout, but the principles are the same.

Impedance Control: Specification for controlled impedance traces for high-speed signals

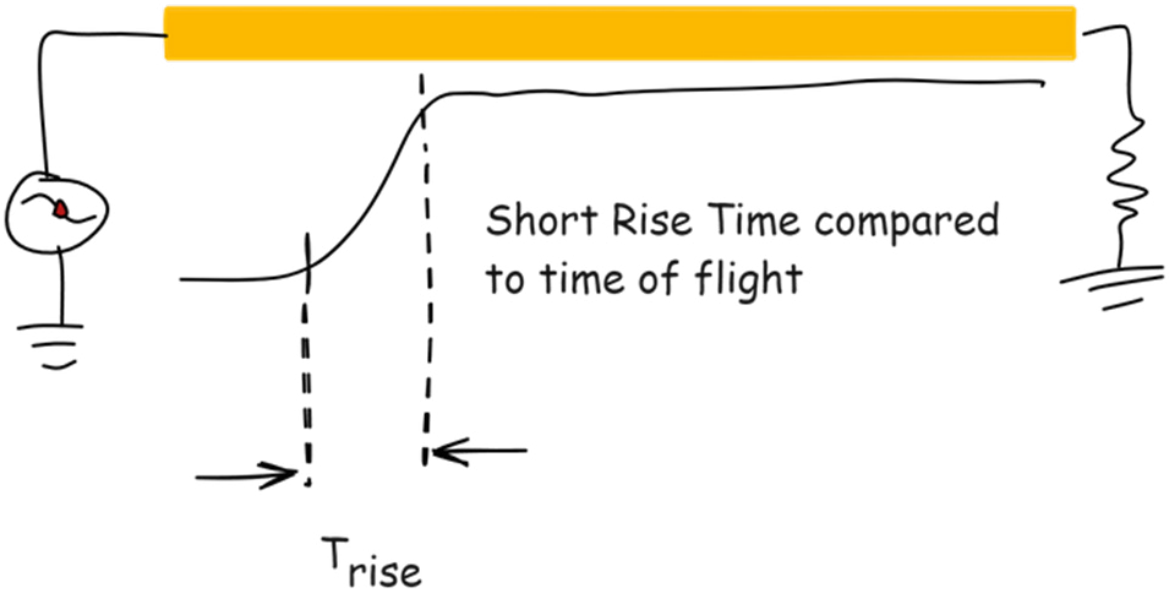
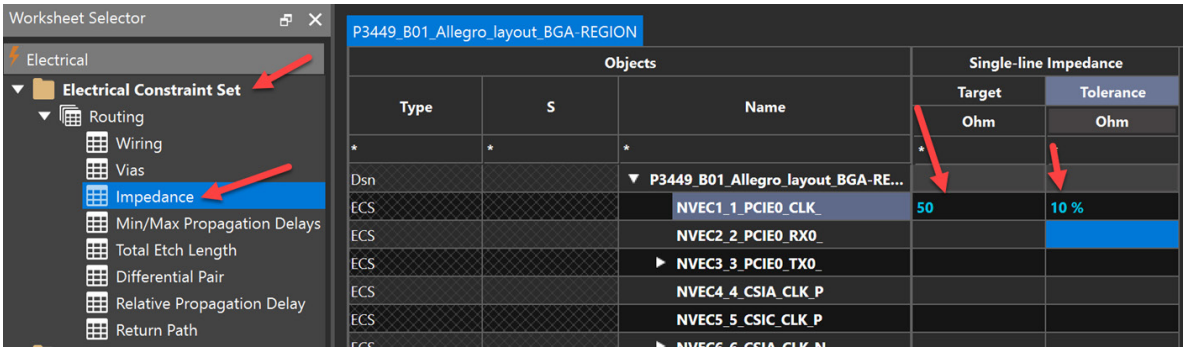


Diagram showing a PCB copper wire with signal propagation

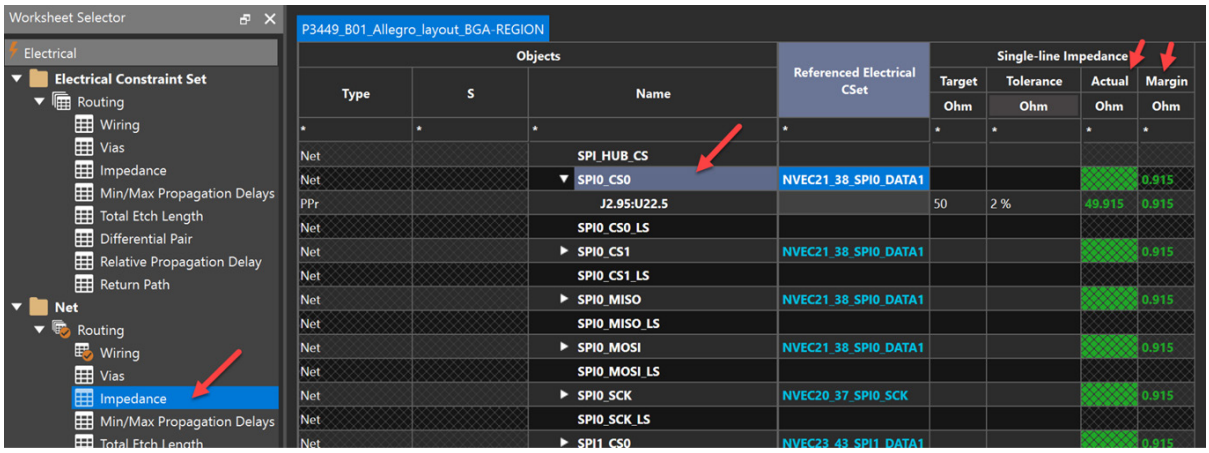
Purpose: Impedance control is used to specify and maintain consistent characteristic impedance for high-speed signal traces throughout the PCB.

Steps to Execute Constraint for Impedance Control:

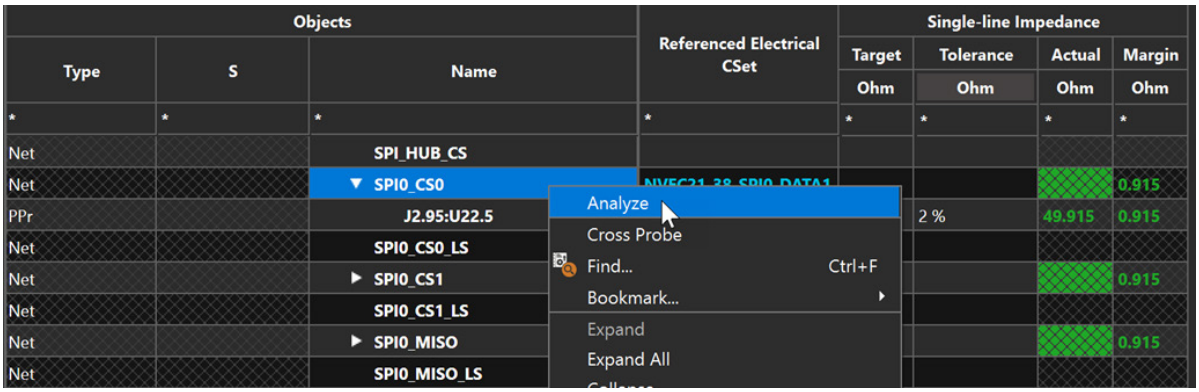
1. Open the Constraint Manager.
2. Navigate to the **Electrical > Electrical Constraint Set > Impedance** worksheet.
3. Define target impedance values for different trace types (e.g., single-ended).



4. You can then go to the **Electrical > Net > Routing > Impedance** worksheet and apply the constraint to any net, net class, or net group.



5. Then you can determine whether the nets are adhering to the rules inside the constraint set by right clicking a net name and selecting Analyze.



6. The analysis will show red, yellow or green for whether your net complies with the Single line impedance constraint.
7. It lets you know the target impedance, the tolerance, actual impedance of the trace and margin (how much off you are in terms of impedance).

Note: The behavior of the trace will be such that when you're routing it, the trace thickness will change to maintain the impedance, or at least a DRC error will appear if your trace falls outside the target impedance range.

Reason: Controlled impedance is crucial for maintaining signal integrity in high-speed circuits. It helps minimize signal reflections, reduce crosstalk, and ensure proper signal transmission. Specify target impedance values (e.g., 50Ω for single-ended traces, 100Ω for differential pairs) to minimize reflections and ensure compatibility with specific communication protocols. This involves controlling trace width, spacing, and dielectric properties.

Impact on the Board:

- Improves signal quality and reduces distortion in high-speed signals (by reducing reflections)
- Enhances overall system performance and reliability
- May require specific PCB materials and manufacturing processes to achieve desired impedance values
- Can influence trace routing and layer stack-up decisions

By implementing proper impedance control constraints, designers can ensure that high-speed signals maintain their integrity throughout the PCB, leading to more reliable and higher-performing electronic products.

Crosstalk Mitigation: Maximum parallel trace length

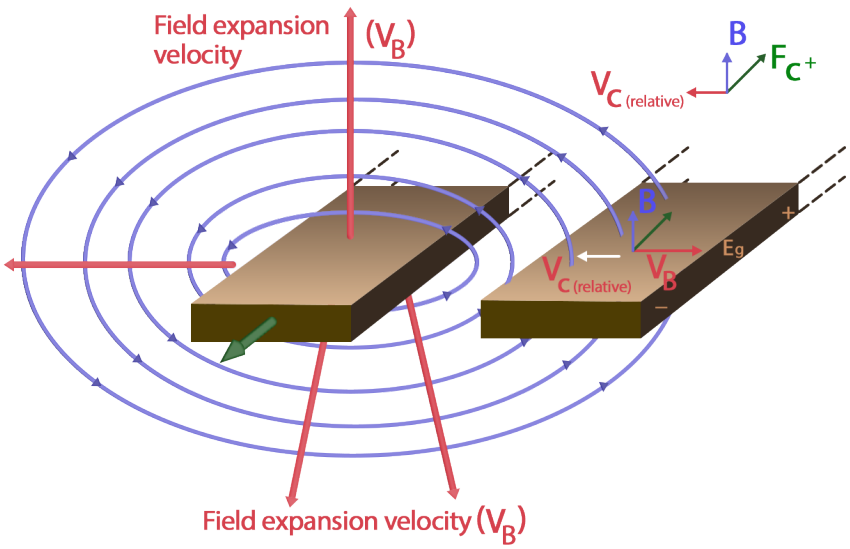


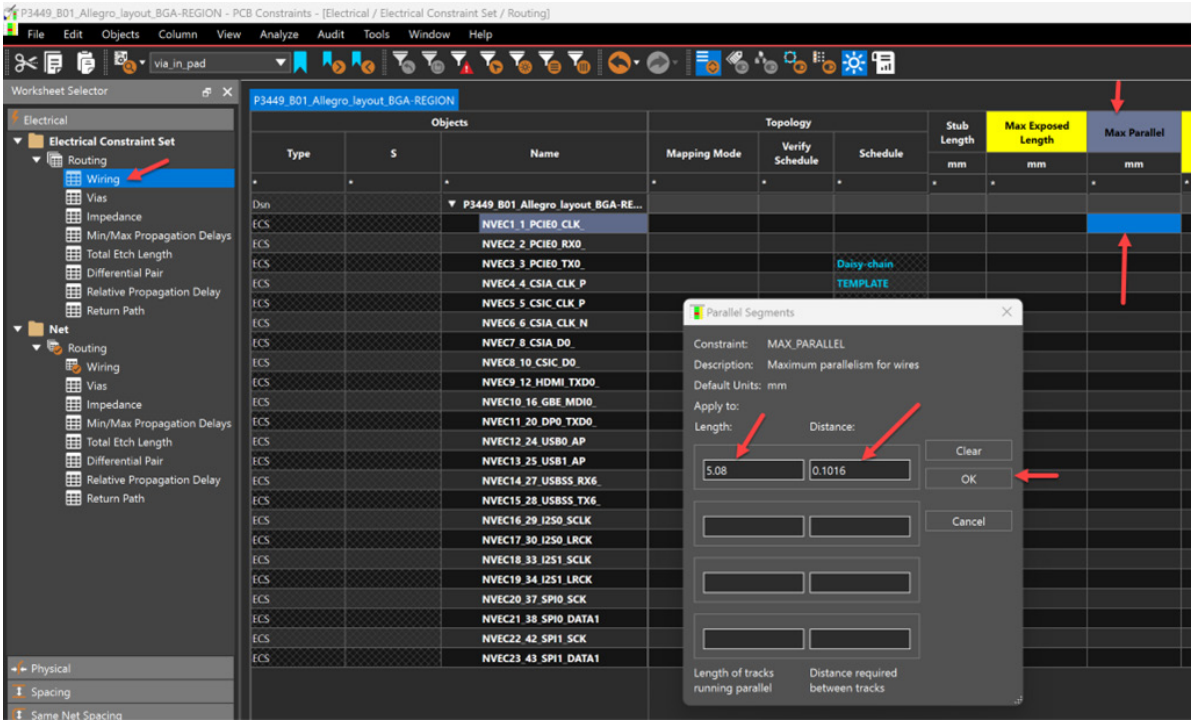
Diagram illustrating crosstalk between two traces running parallel to each other.

Purpose: Limit the length that signal traces run parallel to each other to reduce coupling and crosstalk. This is especially crucial for high-speed differential pairs. The acceptable length depends on factors like trace spacing, layer stack-up, and signal frequency.

In this example, you will learn how the Constraint Manager prevents excessive coupling among traces.

Steps to Execute Constraints:

1. Navigate to the **Electrical > Electrical Constraint Set > Routing > Wiring** worksheet.
2. Scroll horizontally to the Max Parallel column, then in that same column, select the cell for any of the Electrical Constraint sets shown below. Then a Parallel Segments window will appear.



3. Enter some values that would work for your design calculations (e.g. not allowing traces that are 0.1016 mm / 4 mils apart to traverse more than 5.08 mm / 200 mils together). Click Ok.
4. With the constraint set values set, apply the constraint set by going to the **Electrical > Net > Routing > Wiring** worksheet.
5. Click one of the applicable nets (e.g. **PCIE0_CLKREQ**) then apply the constraint set (in this case **NVEC1_1_PCIE0_CLK_**)

Reason: Signal integrity constraints are crucial for maintaining data integrity, especially in high-speed designs where signals are more susceptible to degradation and interference.

Impact on the Board:

- Reduces signal distortion and data errors
- Improves overall system reliability and performance
- May influence trace routing, layer stack-up, and component placement decisions
- Can lead to more complex design rules and potentially increased PCB manufacturing costs

By implementing proper signal integrity constraints, designers can ensure that their PCBs maintain signal quality and minimize interference, resulting in more reliable and higher-performing electronic products.

EMC and EMI

Electromagnetic compatibility (EMC) is a crucial aspect of high-speed PCB design, ensuring that the device operates reliably without causing or being affected by electromagnetic interference (EMI). Implementing effective EMC design techniques is essential to maintain signal integrity and compliance with regulatory standards.

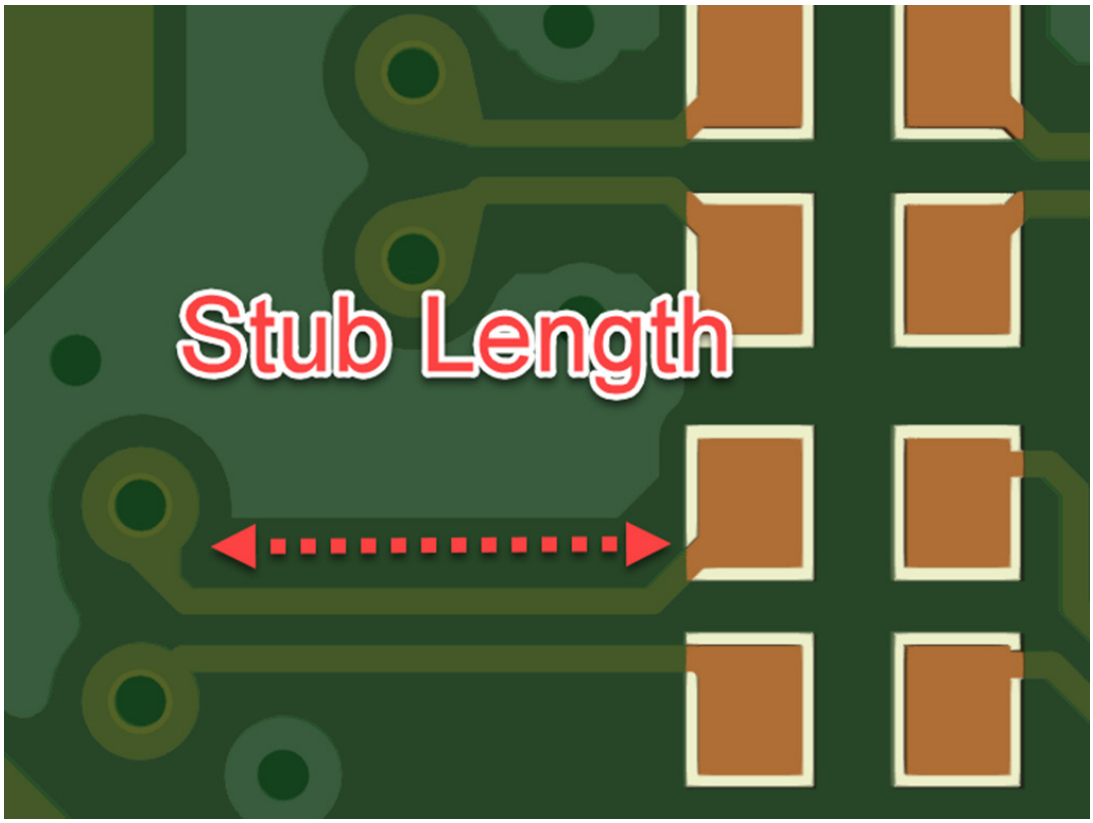
General Solution:

To achieve EMC compliance, the design should incorporate strategies such as proper PCB stack up, proper grounding, shielding, and trace routing. These techniques help minimize EMI emissions and susceptibility, ensuring the device operates effectively in its intended environment.

Application in OrCAD X Presto:

1. Implement ground planes:
    a. Go to Setup > Cross Section
    b. Ensure dedicated ground planes are included in the stackup for effective return paths
2. Use guard traces:
    a. Use Route > Add Dynamic Shape to create guard traces around sensitive signals like DDR3 clocks
    b. Connect guard traces to ground at regular intervals using stitching vias
3. Add stitching vias:
    a. Use Place > Via and select a predefined via definition
    b. For automatic stitching, use Tools > Add Stitching
    c. Set parameters for via spacing (e.g., every 500 mils) to enhance grounding
4. Route high-speed signals on inner layers:
    a. Use Route > Interactive Routing and select inner layers for critical high-speed nets
    b. This reduces EMI by shielding signals with adjacent ground planes
5. Minimize loop areas:
    a. Ensure power and ground traces run parallel to minimize loop areas
    b. Use Route > Power Planes to define power distribution areas that overlap with ground planes
6. Stub Length Control

Stub Length



Top view of PCB displaying trace stub length

Maximum Stub Length

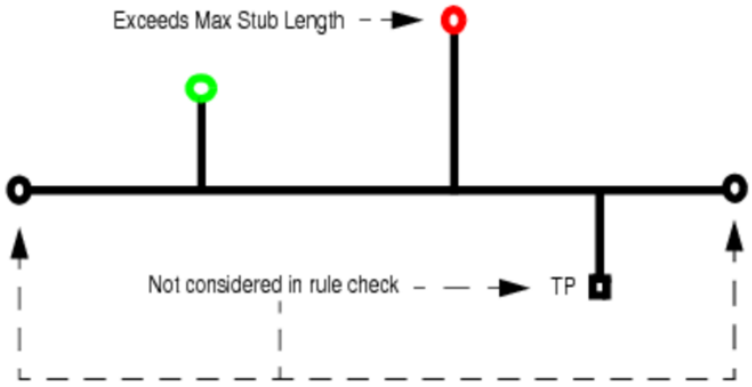
Checks the maximum stub length in design units for daisy chain routing.

Note: When a pin is routed to a connect line, the stub is the line of etch between the pin and the connect line.

The stub length constraint is validated only if NET_SCHEDULE is enabled and RATSNEST_SCHEDULE is set to either MIN_DAISY_CHAIN or MIN_SOURCE_LOAD_DAISY.

>

This check ignores pins at the end of clines, dangling clines, and test points. The chosen net schedule impacts the rule check.



Legal Values: Design Units
DRC Code: ES
Applicable Objects: Xnet, Net, ElectricalCSet, NetClass, DiffPair, Bus, NetGroup
Attribute Name: STUB_LENGTH

A stub as defined in OrCAD X Presto PCB Editor

Purpose: To restrict the length of the stubs extending from a trace on a net to reduce signal reflections and maintain signal integrity. For high-speed designs, aim for zero or minimal stubs. When stubs are unavoidable, keep them as short as possible.

Applies to: USB, HDMI, and any other high-speed interfaces that need minimal fanouts or stubs to operate efficiently.

Importance: Affects current-carrying capacity and signal integrity

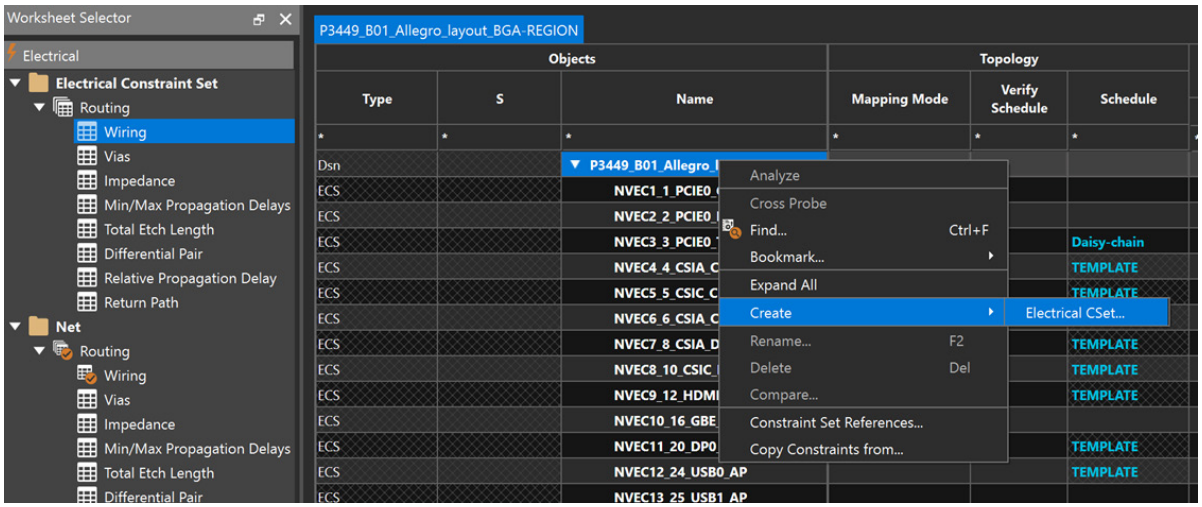
Application: High-speed signals, electromagnetic compliance (avoiding antennae) Steps:

Steps:

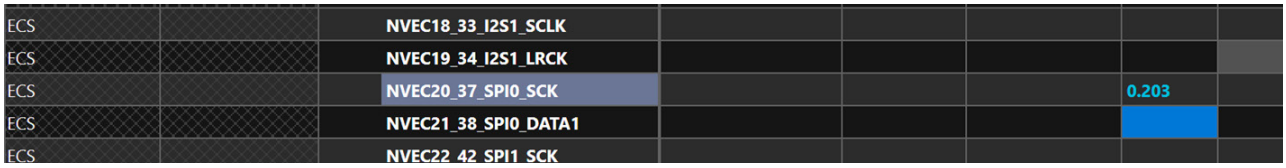
1. In OrCAD X Presto PCB Editor, open the Constraint Manager using **Tools - Constraint Manager.**

Tip: As usual we will make a constraint set that holds the rules/constraints, then we apply that constraint set to a net, class, group or region.

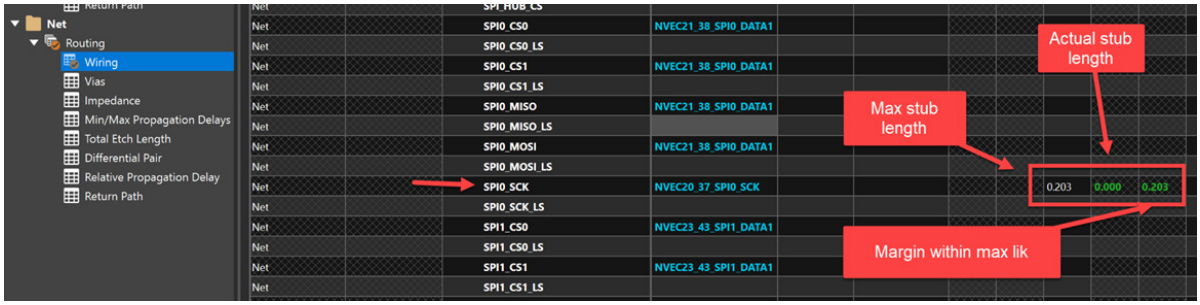
2. Create an electrical constraint set under **Electrical > Electrical Constraint Set > Routing > Wiring**, and right click on the project name for DSn.
3. Choose **Create > Electrical CSet…**



4. Give the ECSet a name and it will be added to the spreadsheet.
5. Once added, enter a desired maximum stub length for the ECSet.
6. For example, let's say you want your stubs to be no more than 8 mils (0.203 mm), so you enter '8 mils' in the rule shown below for the SPI0_SCK signal constraint set.



7. Now you go to the following location to apply that constraint and stub rule it has.
8. Go to the **Net > Routing > Wiring** worksheet.
9. Choose from the **Referenced Electrical CSet** column to set it to your desired net.
10. Notice how the stub length rule applies to the net, with added details like Max, Actual and Margin.



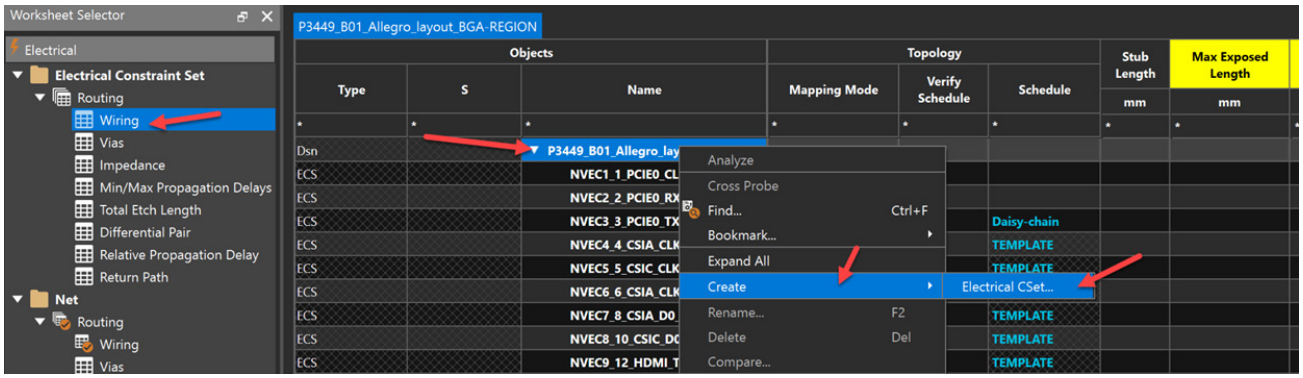
Tip: Use to ensure tight signal integrity, and minimal reflections and antennas.

Maximum Stub Exposed Length

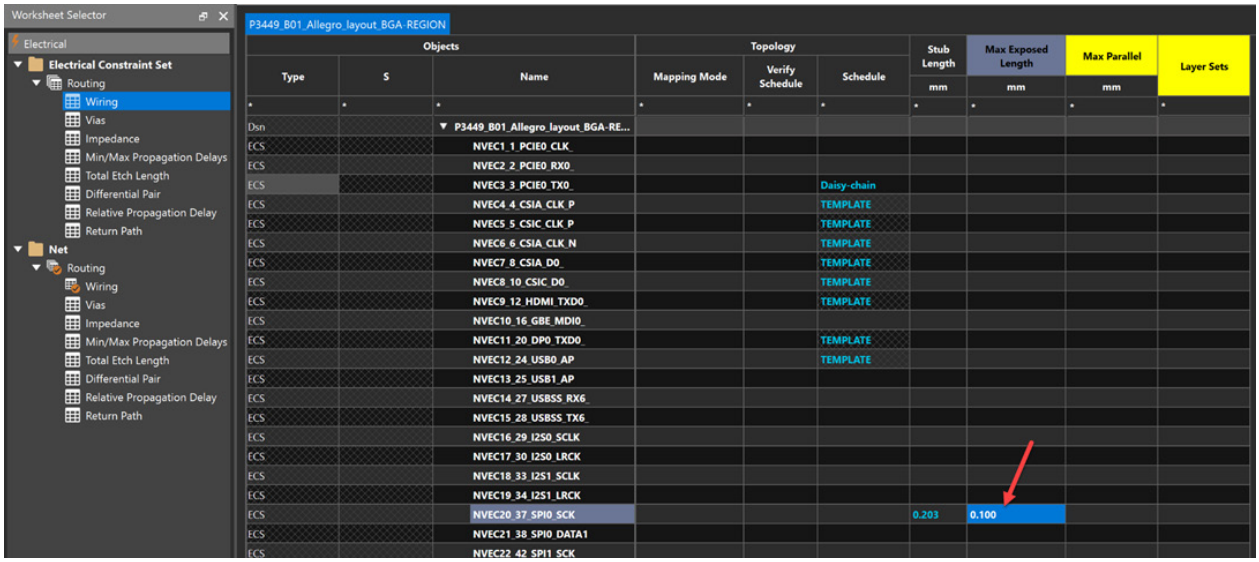
Set a maximum length for exposed stubs to prevent unintentional antenna effects. This is particularly important for high-frequency signals where wavelengths are shorter. A general rule of thumb is to keep stub lengths below 1/20th of the signal's wavelength.

Steps:

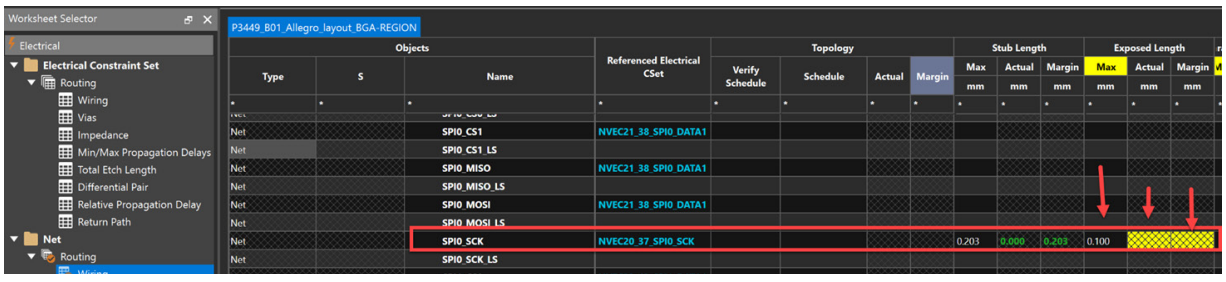
1. Similar to the stub length rule application, open the Constraint Manager.
2. Create an electrical CSet in the **Electrical Constraint Set > Routing > Wiring** worksheet.



3. Once created, scroll horizontally and fill in a max exposed trace length (ideally below 1/20th of signal wavelength) in the **Max Exposed Length** field in the row of your desired ECSet.



4. Finally, go to the **Electrical Constraint Set > Net > Routing > Wiring** worksheet.
5. Click and apply the appropriate ECSet onto the desired net by selecting the ECSet from the Referenced Electrical CSet column. The rule is automatically applied to that net.

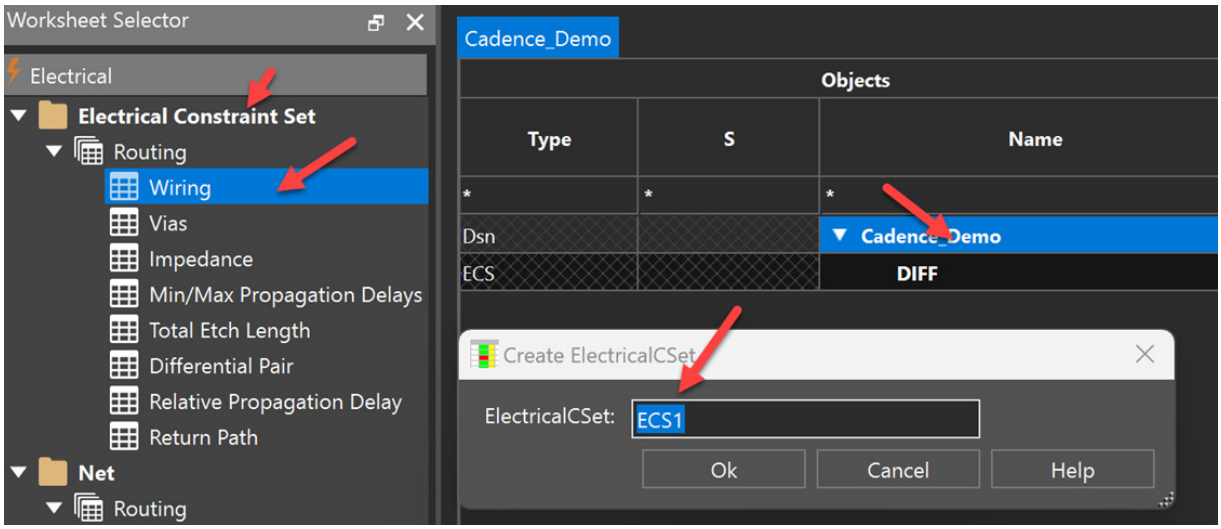


Layer Restrictions

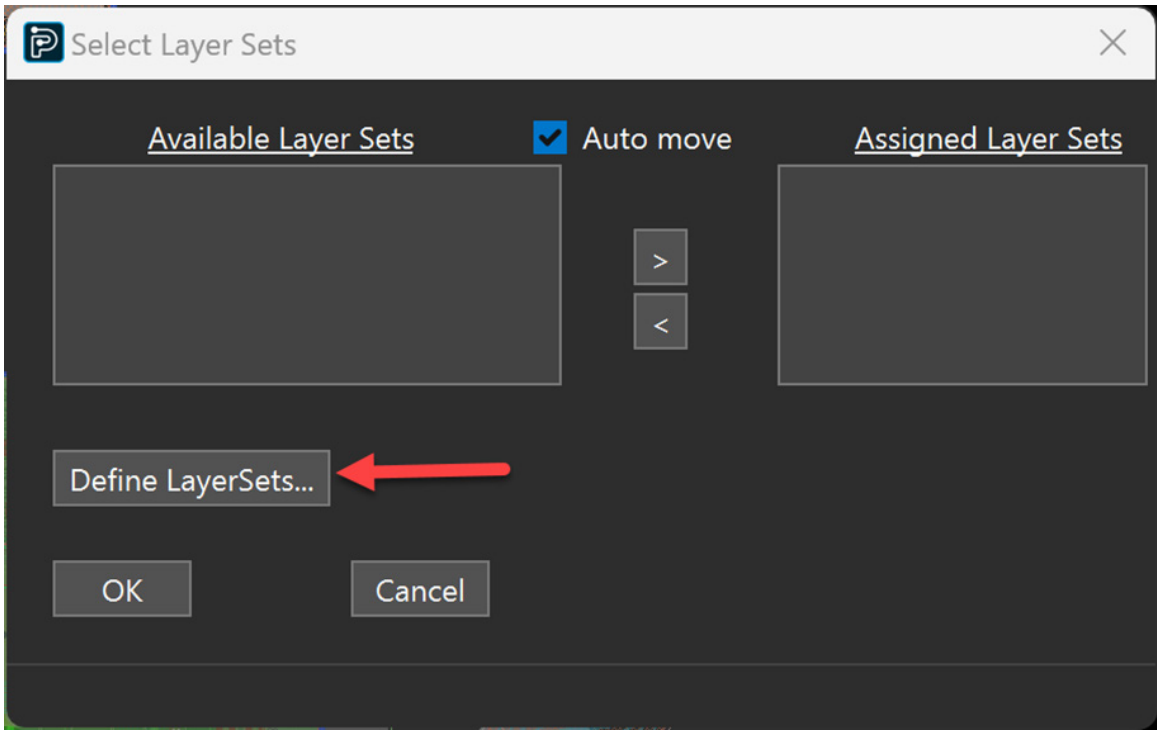
Purpose: Control EMI by limiting the layers through which a trace can be routed. For example, keep high-speed signals on internal layers sandwiched between ground planes for better shielding.

Example:

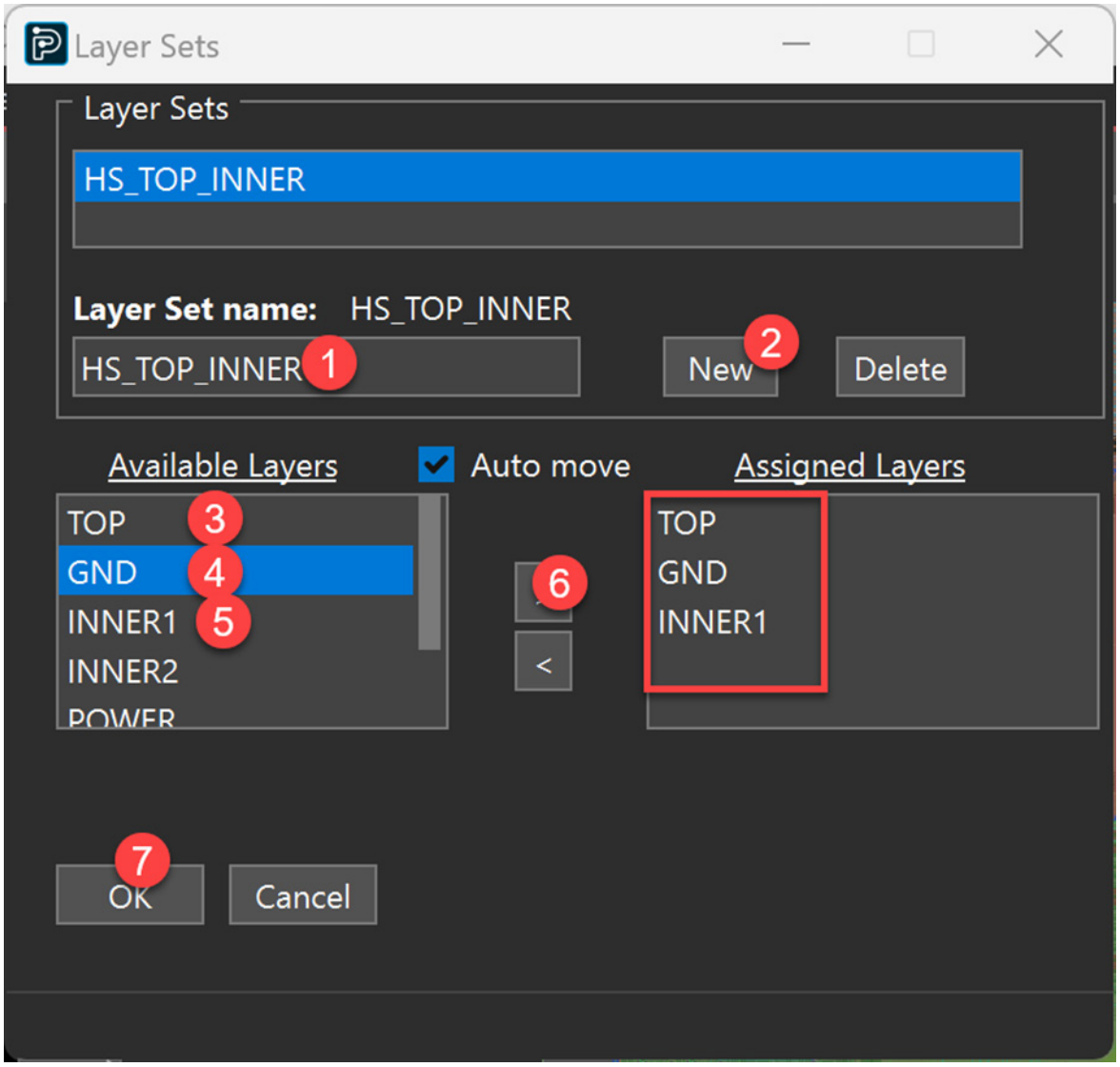
1. Within the Constraint Manager, go to the **Electrical Constraint Set > Routing > Wiring** worksheet.
2. Create an electrical constraint set and give it a name (e.g. ECS1) shown below.



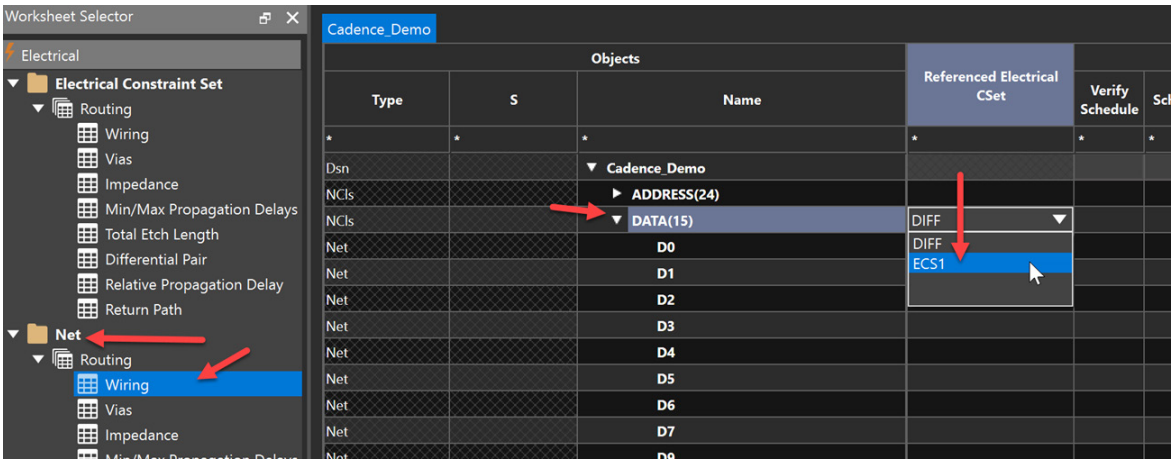
3. Click the cell under the Layer Sets column that is in the same row as your ECS1 row. The Select Layer Sets window appears.



4. There aren't any layer sets defined yet, so click the Define LayerSets… button.
5. Enter a name for the Layer Set: HS_TOP_INNER, then hit New. That creates the layer set.
6. Next, depending on your application, choose which layers you want this rule to apply to. For example, we would prefer high-speed signals to be routed on the top of the PCB and the inner layer and in some cases the GND layer, but no traces are allowed on the bottom half of the PCB (to control for Capacitive plane couple, controlling the EM signals in the Z-axis, etc.).



7. Click OK. This brings you back to the Select Layer Sets window.
8. Click the HS_TOP_INNER from the Available Layer Sets list. It will move over to the Assigned Layer Sets section. Click OK.
9. Finally we will apply this ECSet (ECS1) to the DATA(15) Net Class as an example, as shown below.



10. Scroll horizontally to the final column named Layer Sets.
11. Some nets in the Net Class will pass or fail the Name within the layer set, because not all the nets are routed on the TOP, GND or INNER1 layers. It is working as intended.

Impact: The layers a signal goes through vertically affect how much coupling and EMI is passed through the PCB. Utilize the constraint manager to avoid unnecessary EMC issues in PCB Design.

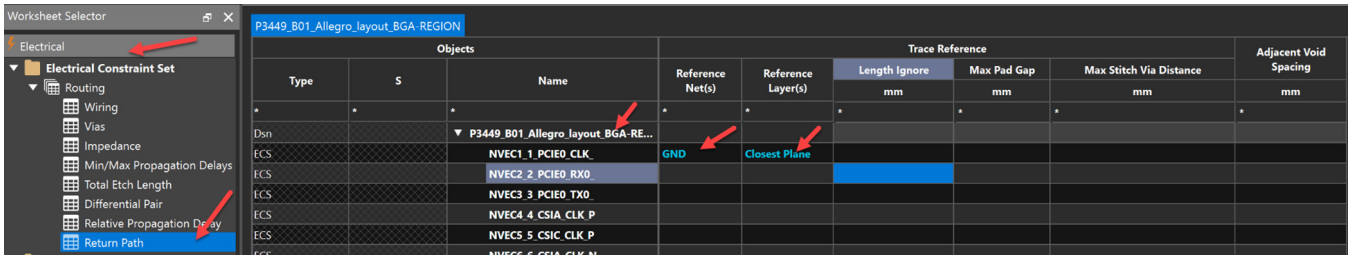
Return Path

Purpose: Reduce electromagnetic interference by checking that signals are following a proper return path.

OrCAD X Constraints support return path checking for Impedance and EMI.

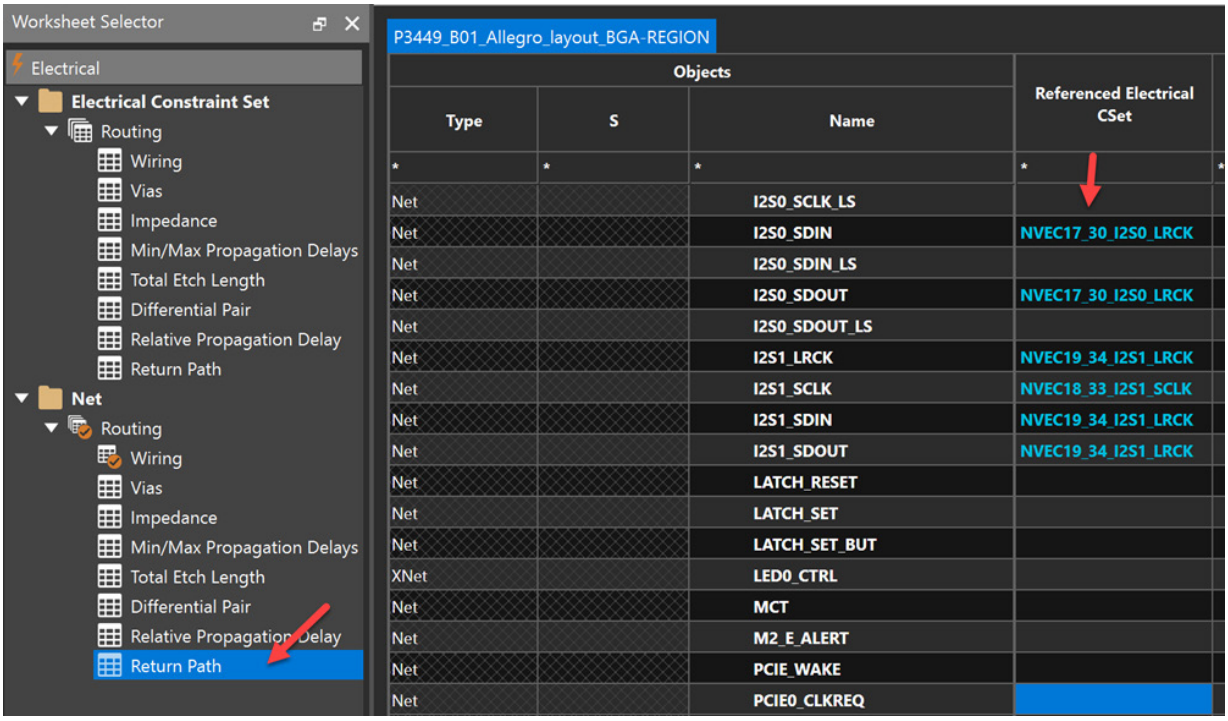
Steps to implement return path checks in OrCAD X Presto PCB Editor:

1. Within the Constraint Manager, go to the **Electrical > Electrical Constraint Set > Routing > Return Path** worksheet.
2. Right click on the Dsn cell name (P3449_B01…) create an Electrical CSet, give it a name, then it will add itself to your list of ECSets (see below).
3. Whether you create an ECSet or use an existing one, you have multiple options available for return path checks.



4. You can set the right reference Nets and layers for your signals.

5. After such, to apply the rules, go to **Electrical** > **Net** > **Routing** > **Return Path**, choose the net you want to apply your ECSet to, and that's it.



Impact on the Board:

- Improves overall reliability and performance of the PCB in various electromagnetic environments
- Ensures compliance with regulatory standards, which is essential for product certification and market entry
- May influence component placement, routing strategies, and layer stack-up decisions
- Can lead to the inclusion of additional shielding or filtering components
- Might require changes in trace routing to minimize crosstalk and emissions

By implementing proper EMC and EMI constraints like return path checking, designers can create PCBs that not only function well but also meet the stringent electromagnetic compatibility requirements of modern electronic devices.

High Speed Constraints:

Note: The content in this section is also contained in Part 3 of our Constraint Management Guide.

Min/Max Relative Propagation Delay: Controlling Signal Timing

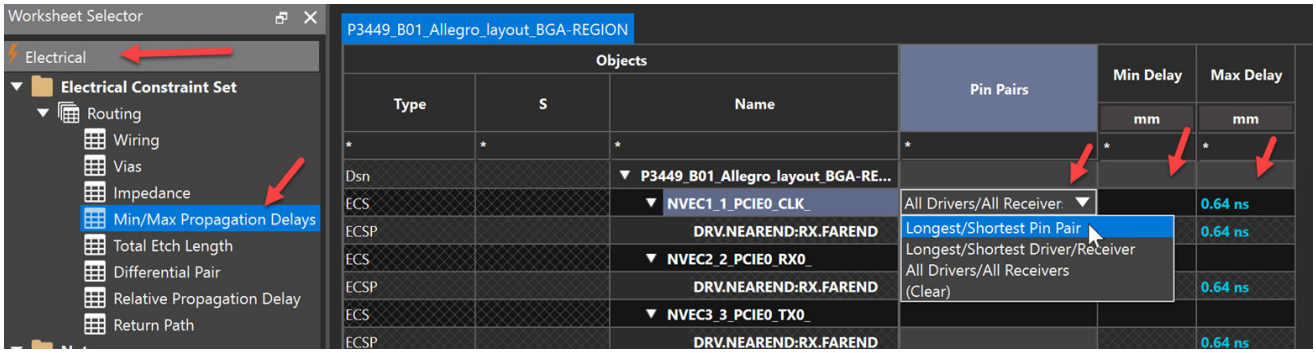
Definition: Managing the propagation delay of signals to ensure they arrive at their destination at the correct time.

Example: Ensuring that critical signals have minimal delay to synchronize with other signals.

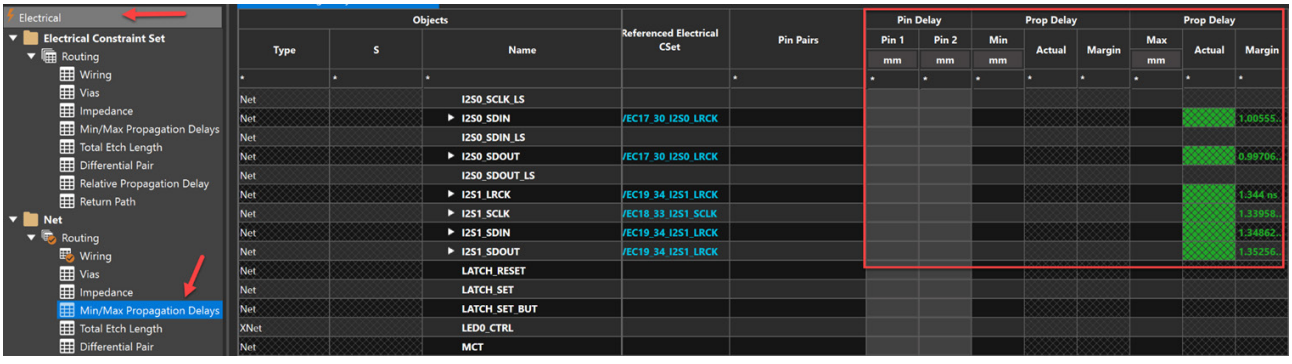
Steps:

To set the signal propagation delay:

1. Go to the following worksheet: **Electrical > Routing > Min/Max Propagation Delays.**
2. You can create your desired constraint set, but let's look at the existing ones shown below.

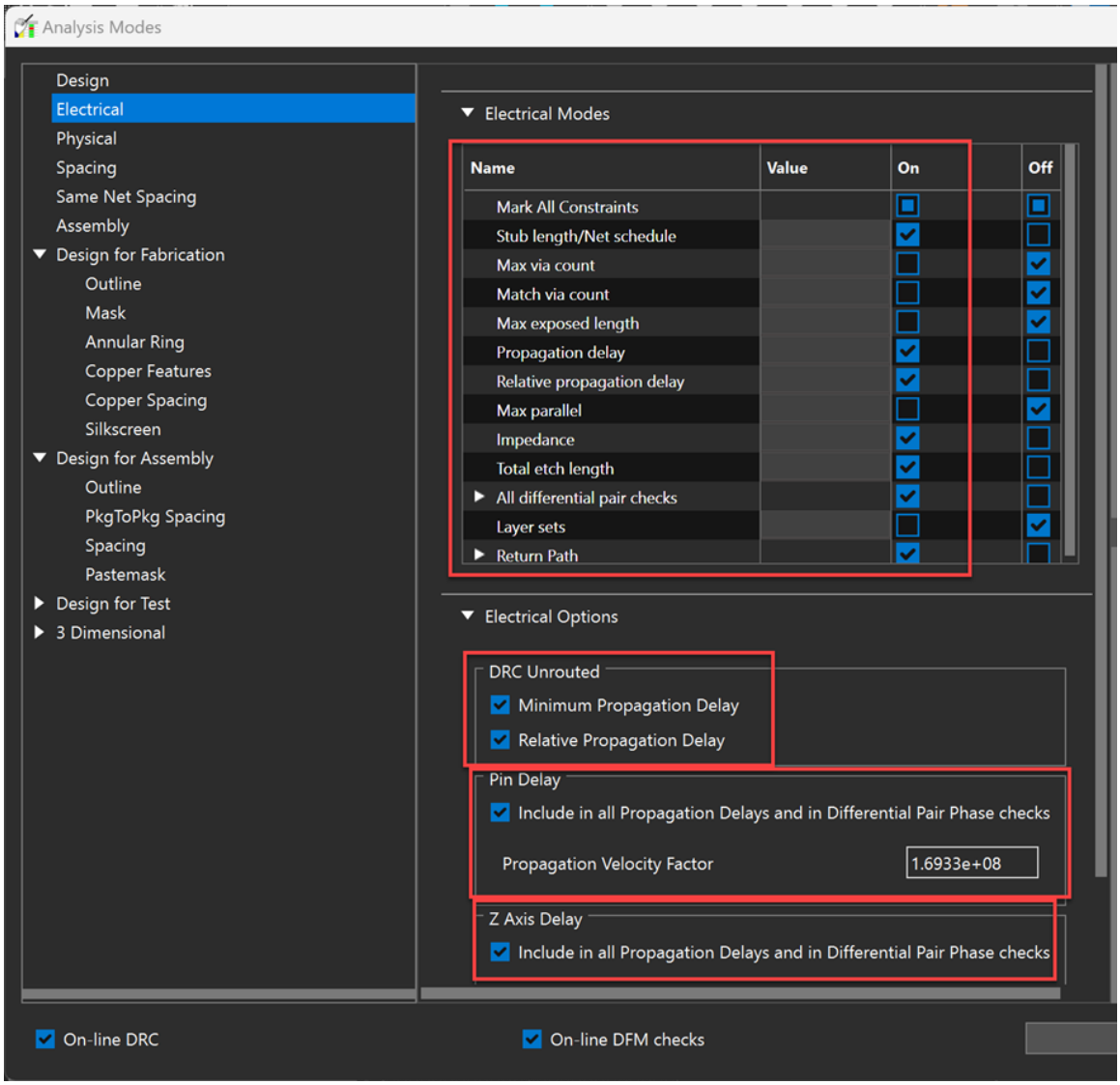


3. You can choose the pin pairs (transmitter and receiver) that will be on either side of the signal being propagated through the respective trace.
4. Choose the Pin Pairs based on your design criteria.
5. Next you can apply the constraint in the worksheet called **Net > Routing > Min/Max Propagation Delays**



6. Notice that once you apply your constraint set, you can right click on the nets of interest, then choose Analyze, then the constraint manager will let you know in the Prop Delay columns whether those nets have the actual propagation delays you need in the board.

IMPORTANT: Please note that you must enable Analysis Mode in Constraint Manager. To ensure this, go to the menu at the top, Analyze - Analysis Modes. The Analysis Modes window will appear.



Check all the electrical modes you want analyzed and include the checked items shown in the image above.

Click Ok, then the Constraint Manager will be able to analyze the relevant constraints.

Benefit of Propagation Delay: Improves timing accuracy and reduces the risk of data errors. Assess this pre- and post-routing layout. This built-in high-speed analysis feature greatly reduces risk of errors in the PCB design. It is still recommended to analyze the signal integrity and timing analysis using post layout software, but these features are extremely powerful within OrCAD X Presto PCB Editor.

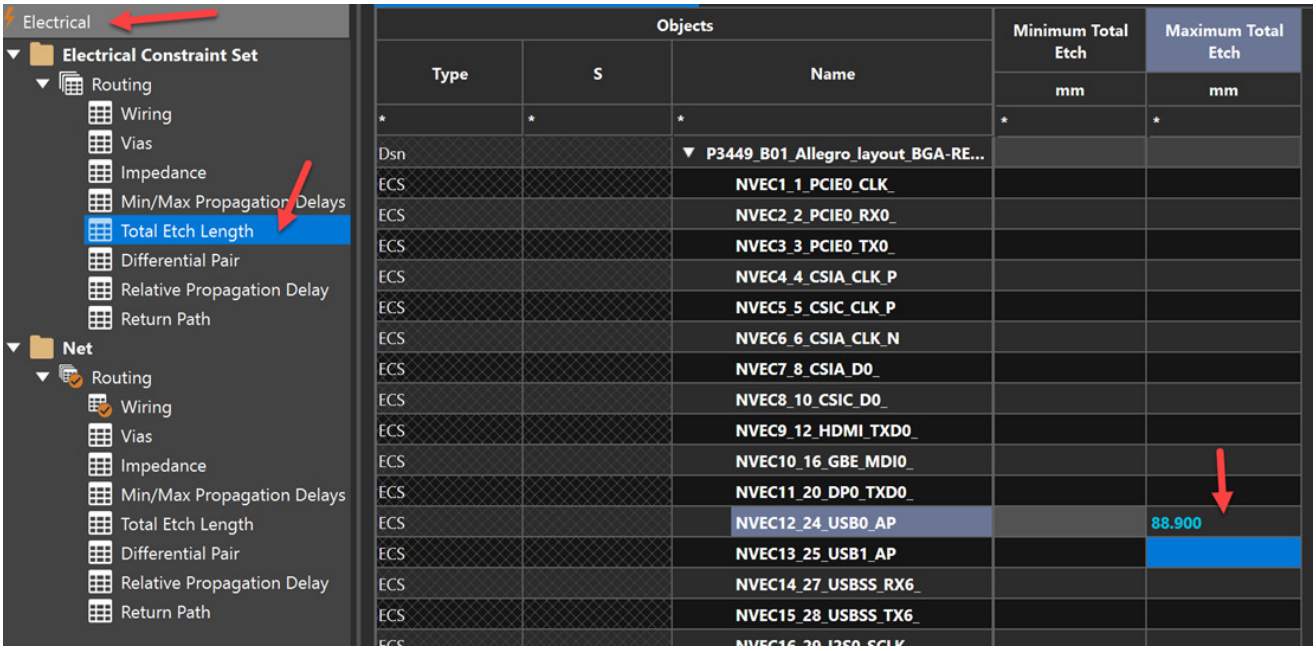
Create accurate models of signal propagation delays to account for potential signal degradation during operation. This helps in timing analysis and ensuring proper synchronization in high-speed designs.

Critical Trace Length

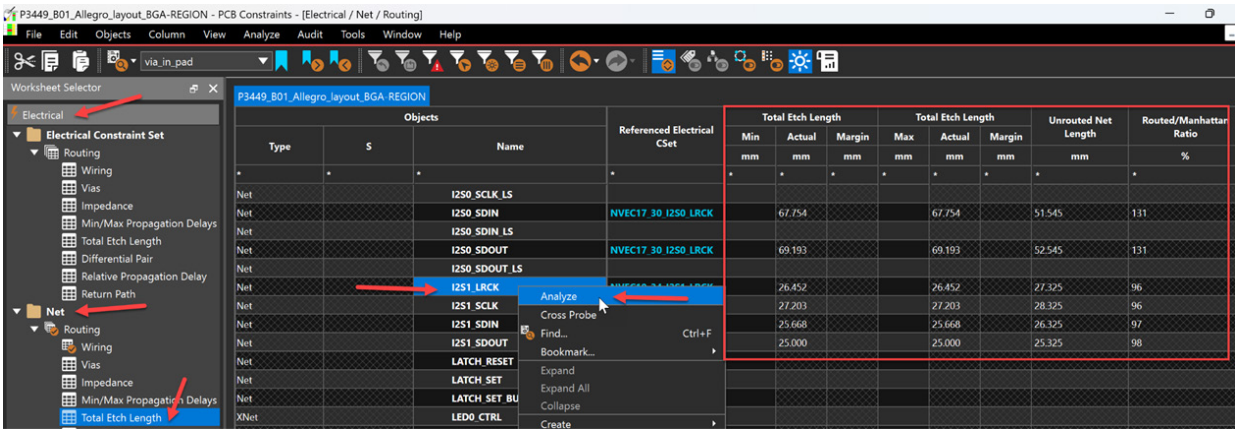
Definition: Critical trace length is the length of a trace or transmission line that would cause the signal to reflect if it's too long electrically.

Steps:

1. Navigate to the **Electrical > Routing > Total Etch Length** worksheet.
2. We have existing Constraint Sets but feel free to make a new one.
3. For an electrical constraint set in the list, set the Maximum Total Etch. For example, USB 2.0 operating at 480 Mbps, may consider any traces longer than 3500 mils (88.90 mm) to be electrically long. So we set the max total etch to that value (shown below).



4. Recall that this is just the constraint set. It must be applied to nets in the design. Navigate to the **Electrical > Net > Routing > Total Etch Length** worksheet.
5. Next right-click on the nets you want to analyze then choose **Analyze**. You will see the results below.



6. The Constraint Manager shows what the total etch length of the traces are in real-time, including the length of the unrouted parts and even the percent of the routed net over the Manhattan distance (orthogonal position and distance if only routing at 90-degree angles).

Impact: Manufacturers have significantly reduced the rise times of chip signal transmissions, and we may not always have enough space on a PCB to slow these signals down. Fortunately, we can shorten trace lengths, which helps create a more compact PCB layout. This reduction minimizes the chances of signal reflections, preserving signal integrity and ensuring effective communication between devices for optimal PCB functionality. It's essential to set maximum trace lengths to avoid critical timing issues and signal degradation, especially for high-speed signals, as longer traces can lead to increased attenuation and skew.

Length Matching

Purpose: Ensuring that traces carrying related signals are of equal length. Matching the lengths of data lines in a memory interface to ensure synchronized data transfer.

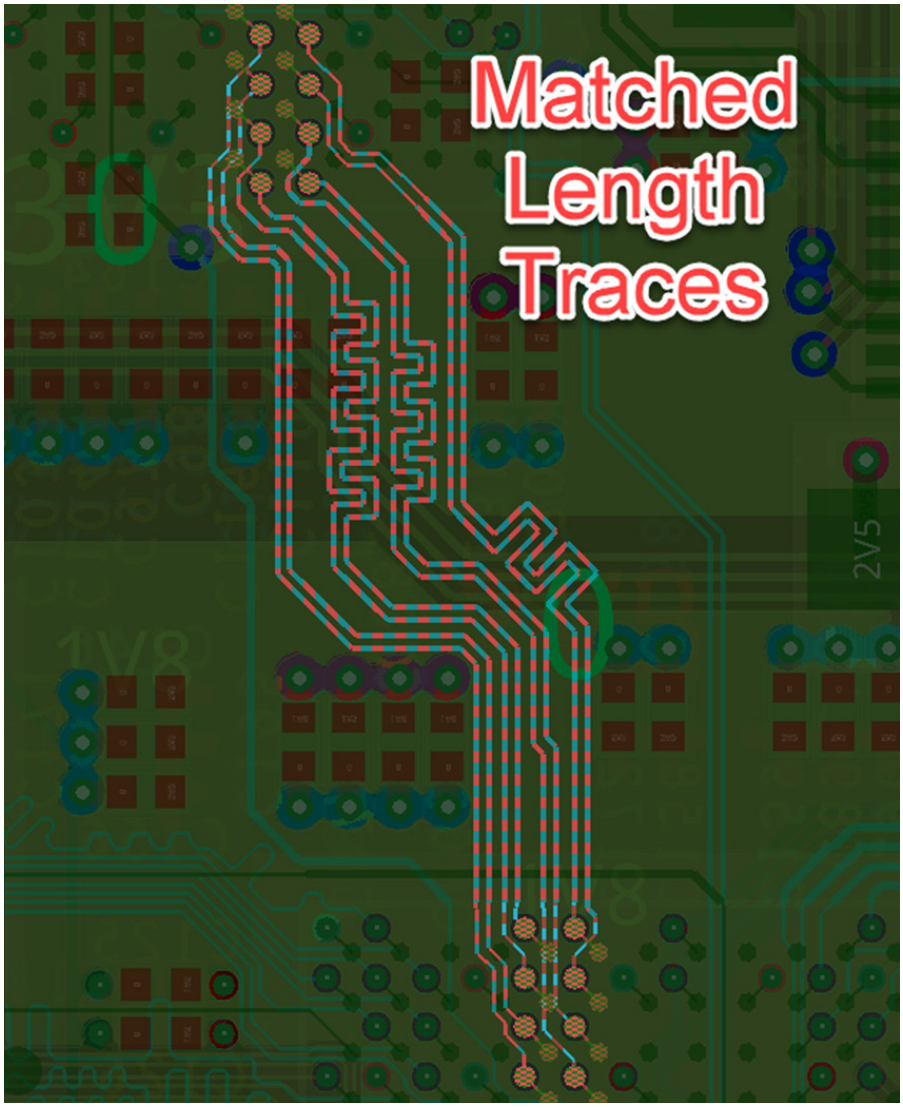
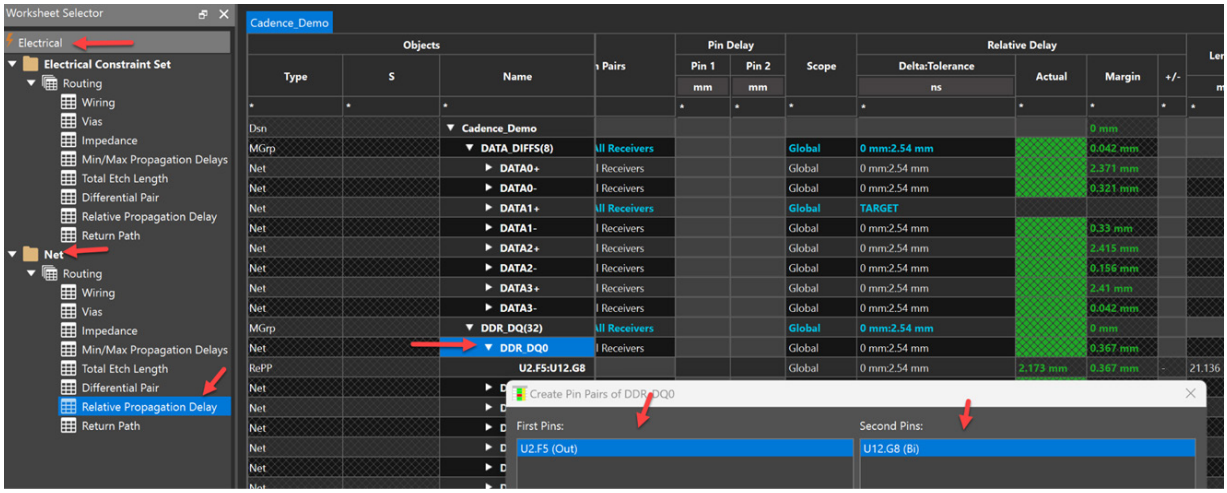


Diagram showing matched-length traces on a PCB.

Steps/Example:

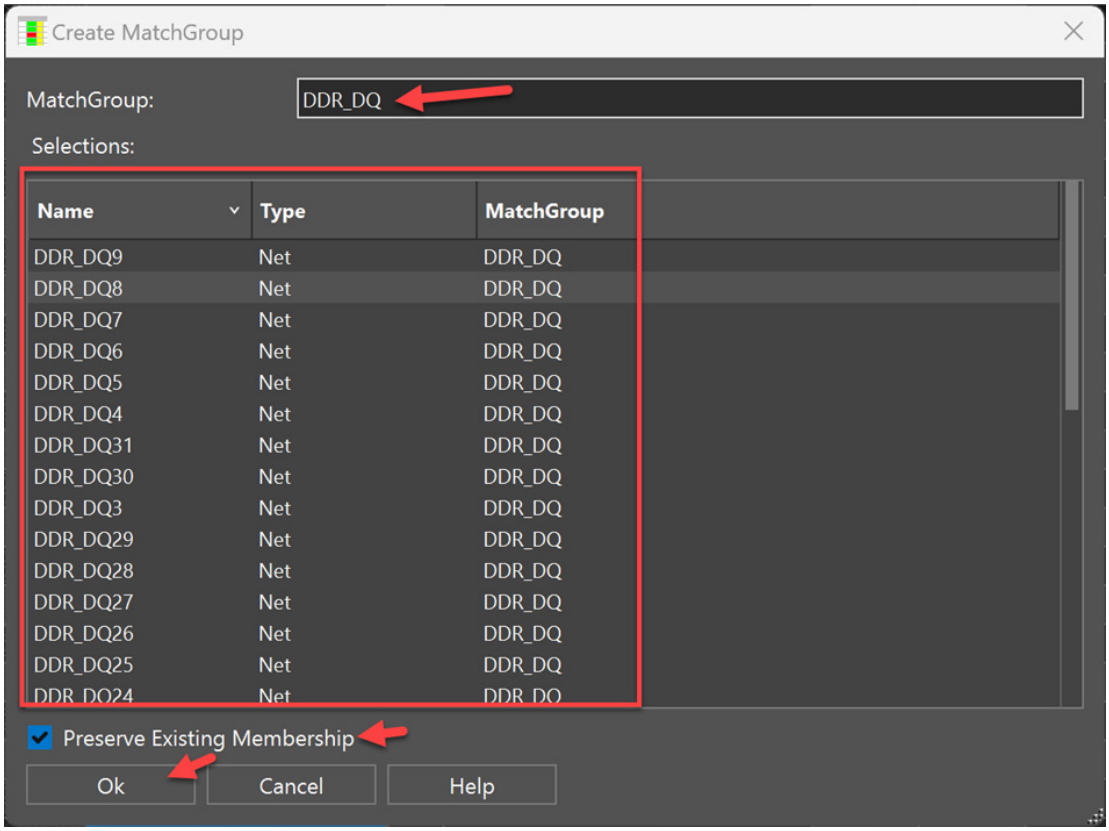
1. Open the Constraint Manager.
2. First, ensure that the Constraint Manager is analyzing all the electrical constraints, pin delays, etc., with Analysis Mode enabled (from the menu select **Analyze > Analysis Mode,** choose all options in Electrical then click Apply and Okay).
3. Then navigate to this worksheet: **Electrical > Net > Relative Propagation Delay.**
4. In your design you will need to create a matched group for nets that are carrying parallel signals, like in the image below where **DDR_DQ(32)** has 32 nets.
5. But first, make a pin pair for all the nets you want to put into a matched group. For example, let's say you didn't have the DDR_DQ# signals in a match group yet. You would select something like the DDR_DQ0, right click it - **Create > Pin Pair…**, click **Ok** when presented with the pin options.



6. Once done, that will create the pin pair underneath the signal in the worksheet (shown below).

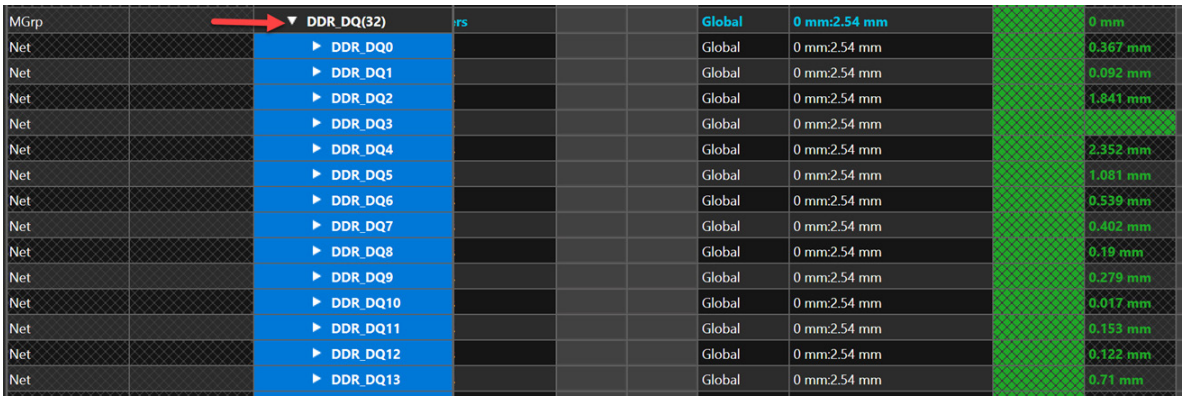
7. Where it says **All Driver/All Receivers**, you can change the pin pair relationships to other options such as:
   a. Longest Pin Pair
   b. Longest Driver/Receiver
   c. All Drivers/All Receivers
   d. (Clear)
8. For this example, we selected **All Drivers/All Receivers**. After that, you repeat the previous steps to create more pin paired nets, then to put your nets into a matched group.

9. To put nets into a matched group, click, then hold and drag the mouse to highlight all the nets of interest (DDR_DQ0 through DDR_DQ31 in this case). After that right click any of the selected nets and choose **Create > Match Group**. A new window appears.



10. Give the match group a name, like DDR_DQ, then click Ok (Ensure that the **Preserve Existing Membership** checkbox is enabled).

11. The group gets created and is shown in the worksheet.



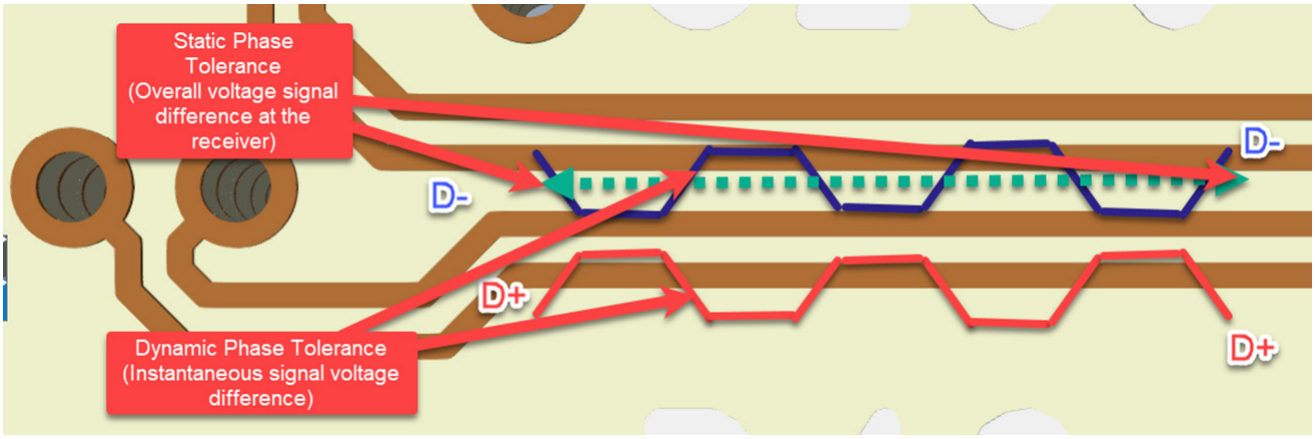
12. To see the analysis of the routed traces with respect to their pin delays and Relative Delays, right click on the Match Group that was just created (DDR_DQ(32)), then choose Analyze.

13. There will be color codes (yellow if not in range, green if fully in range, red if problematic) to show you which traces are within tolerance of the longest Driver Receiver pair.

Impact: Prevents timing issues and ensures reliable data transmission for parallel signal communication (e.g. DDR3).

Differential Pairs (High-Speed)

Definition: Rules for routing differential pairs, which are pairs of traces that carry equal and opposite signals.



Differential pairs showing signal propagation with Static Phase vs. Dynamic Phase.

This blog on our website explains two important concepts for differential pairs, inter pair skew and intra pair skew:

"Ideally, synchronized signals need to arrive at their destination simultaneously to ensure there is no loss of data arising from timing issues. In reality, however, differences (even minute) in the propagation paths mean no two signals will ever arrive at the same time. For greater ease of use, components are forgiving and allow for some timing mismatch – known as clock skew – within tolerable limits.

Timing mismatches are most heavily reliant on the length of the traces, resulting in two variations:

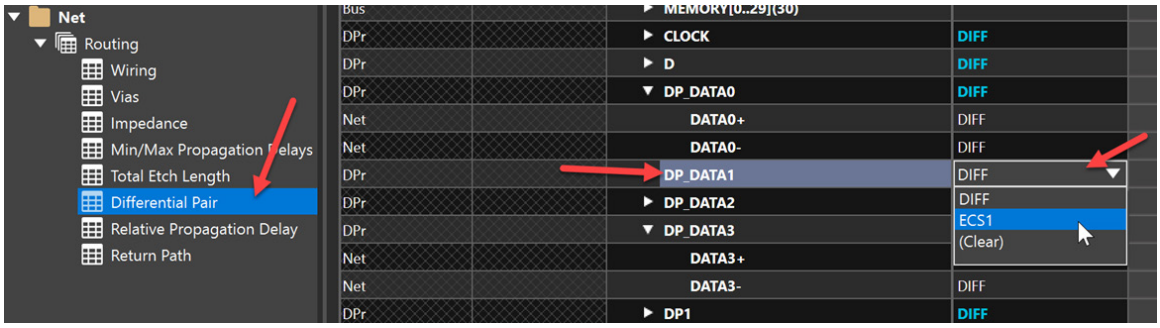
- Intra pair skew between two lines of a differential pair, which indicates the timing difference between the positive and negative signal lines. Keeping the mismatch low between the two differential signals allows for more headroom and better noise protection in balanced lines.
- Inter pair skew indicates the timing difference between signals used in data formats that do not have an embedded clock signal. Inter-pair skew can cover both single-ended and differential pairs within a data format, making some signals doubly constrained by skew."

Example: For this example, we will use Constraint manager to ensure differential pairs are routed together with consistent spacing to maintain signal integrity for dynamic signals and for overall length matching.

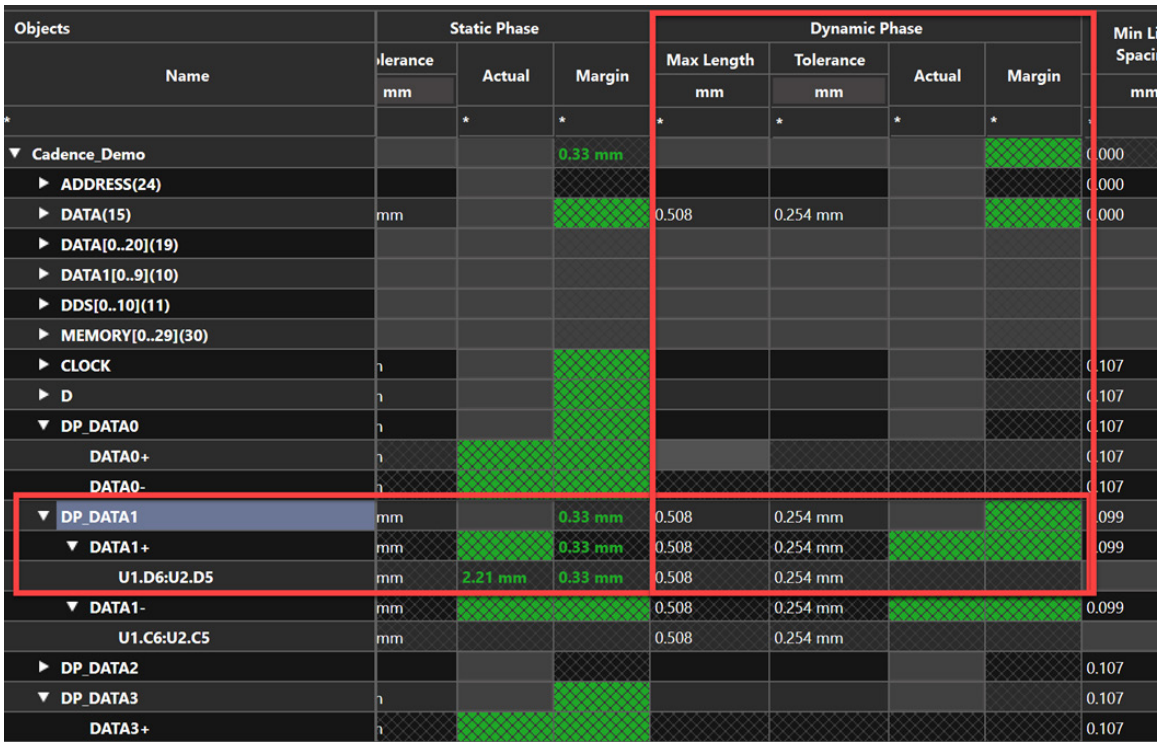
1. Within the Constraint Manager, go to the **Electrical > Electrical Constraint Set > Routing > Differential Pair** worksheet.
2. Create a constraint set (e.g. ECS1).
3. Fill in values for Static Phase Tolerance and Dynamic Phase Tolerance as shown below.

Name	Uncoupled Length		Static Phase Tolerance	Dynamic Phase	
	r Control	Max		Max Length	Tolerance
		mm	mm	mm	mm
		*	*	*	*
Cadence_Demo					
DIFF		2.000	6 mm		
ECS1		2.000	2.54 mm	0.508	0.254 mm

4. You should already have values populated for the other parameters. Now apply the constraint set to any relevant diff pairs by going to the worksheet **Electrical > Net > Differential Pair.**
5. Choose the ECS1 Constraint Set we recently made and apply it to any differential pair, say to the DP_DATA1 diff pair.



6. Then the values will appear on the relevant columns (see below).



7. Notice that from the analysis (you can right click the DP_DATA1 field then choose Analyze) that our traces are within target tolerances.

Meaning of the Parameters:

Implement specific rules for differential pairs to ensure optimal signal propagation. This includes:

- **Dynamic phase tolerance:** Allow for slight variations in differential pair length matching to account for manufacturing tolerances. Ensuring that this remains as close to 0 as possible, reduces the common mode voltage that can be created by slightly mismatched signals - intra pair skew.
- **Static phase control:** Set strict length matching requirements to minimize skew between the positive and negative signals. Some signals do not have to be matched instantaneously, but their data must arrive at the receiver at the same time.
- **Maximum uncoupled length:** Specify the maximum length that differential pair traces can be routed separately before recoupling. Being uncoupled allows for the introduction of unevenly distributed noise among diff pair traces, which can cause the differential receiver to have a harder time canceling the signal noise.

Impact:

The signals propagating through the differential pairs are in sync in real time and at the receiver. Proper control over the traces for in sync signal behavior reduces noise created from common mode voltages and improves signal timing for high-speed data transmission.

Other High-Speed Constraints

Wiring Topology

Set specific routing paths for technologies such as DDR3 to optimize for their signal and power needs. Common topologies include Daisy Chain, Star, and T-branch.

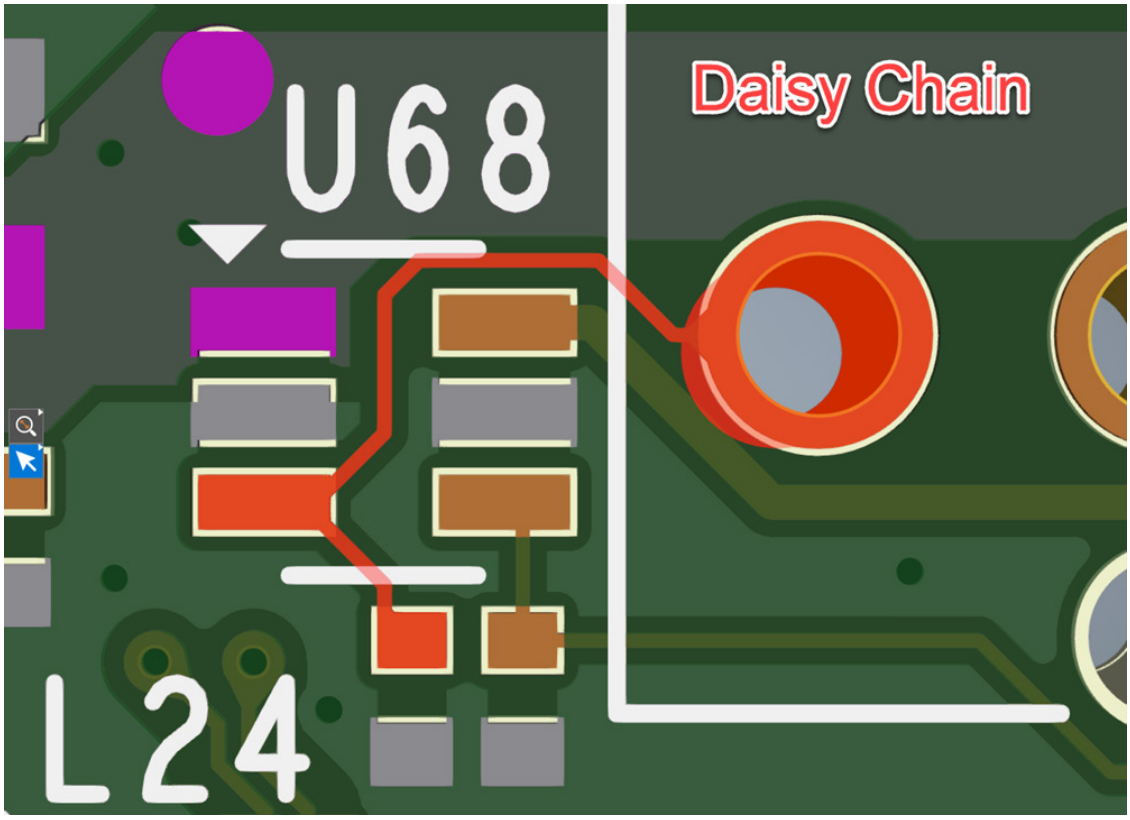


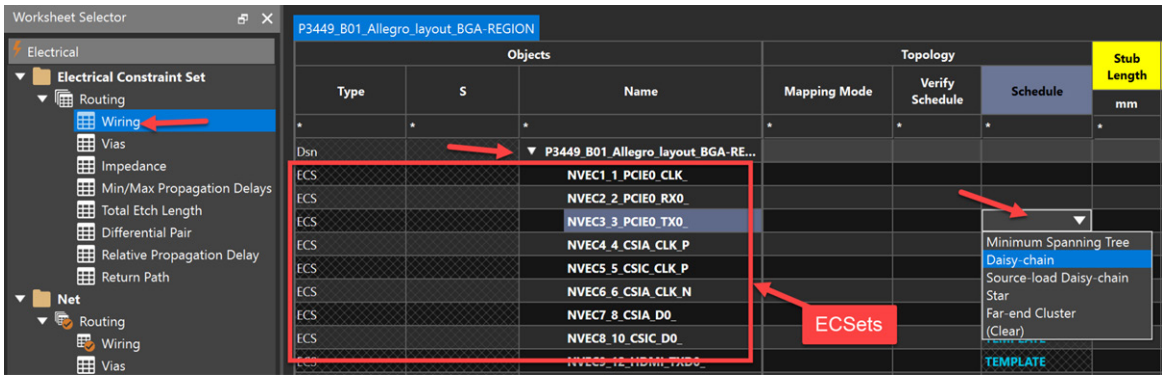
Diagram showing the prioritized routing of critical nets on a PCB.

Definition: Wiring topology involves organizing the connections between different nets on a PCB to achieve a certain outcome, such as minimizing signal reflections, signal attenuation or voltage drops.

Example: Let's ensure that a pulse-width modulated net follows a daisy-chain topology.

Steps:

1. Within the Constraint Manager, go to the **Electrical > Routing > Wiring** worksheet.
2. In the Schedule column, you can right click your Dsn cell and create a new Electrical Constraint Set (ECS). Notice in the image below, we have multiple ECSets already declared.
3. Select the drop-down in one of the cells in the Schedule column and you can choose your net topology.

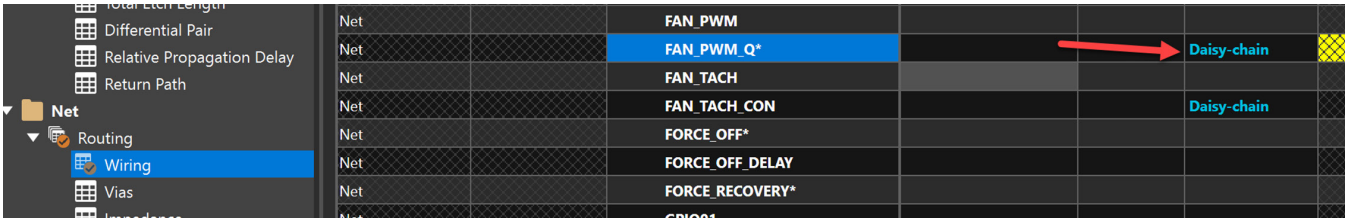


These are the net topology options that are available:

- Minimum Spanning Tree
- Daisy-chain
- Source-load Daisy-chain
- Star
- Far-end Cluster
- (Clear)

Each topology has its own benefits, depending on the application.

4. Once you have set the topology for that ECSet, you can apply it to the appropriate nets found in the spreadsheet under Electrical Constraint Set > Net > Routing > Wiring.
5. In this example, however, you can also directly apply a net schedule (see below).



Note: Depending on your use case, you can use either constraint sets or a specific rule application as needed, as seen in this example. However, please use constraint sets as much as possible to catch the majority of cases first before applying net-specific one-off rules. Using constraint sets modularizes and streamlines your PCB design constraint process and makes designing more efficient. The constraint set method also reduces the likelihood of errors and forgotten constraints.

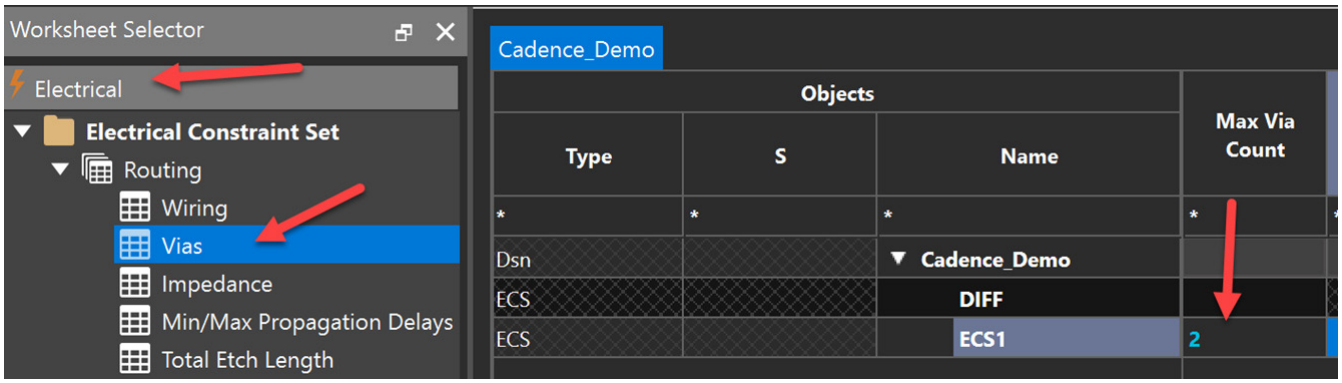
Benefit: Improves signal integrity and timing by ensuring critical connections are made efficiently.

Maximum Via Count

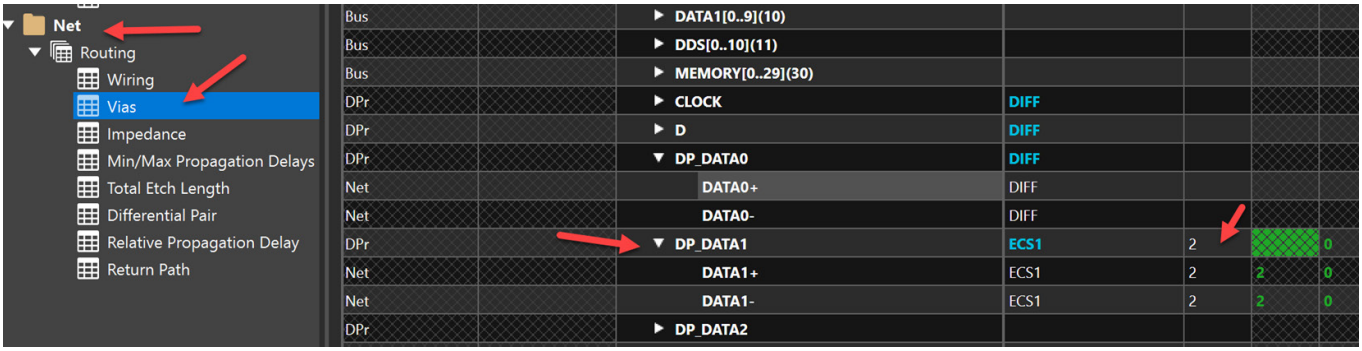
Purpose: Set the maximum number of vias for a trace or net to maintain impedance control and minimize parasitic capacitance. Each via introduces discontinuities and can degrade signal integrity, especially at high frequencies.

Steps:

1. Within the Constraint Manager, navigate to the **Electrical > Electrical Constraint Set > Routing > Vias worksheet**.
2. Then either by creating a constraint set or using an existing one (like the ECS1 below), set the Max Via Count to 2.



3. Now you can apply this constraint set to specific differential pairs or nets by going to the Electrical > Net > Routing > Vias worksheet.



4. In our case, the DP_DATA1 has the ECS1 Constraint set and the via limits applied. Notice how the actual number of vias on the DP_DATA1 differential pair are within the acceptable limit of vias established in the Electrical Constraint Set (ECS1).

Impact: It is easy to forget so many important factors in PCB design that are all crucial for high-speed designs. For instance, for USB 3.2, it's strongly recommended to use no vias or layer transitions. However, if transitions (vias) are needed, to use no more than two per differential pair (i.e. one via per trace).

Constraining the number of vias ensures that we do not inadvertently introduce errors into our board because of forgetting the via limits. Let the constraint manager do the remembering for you as a designer.

High-Speed and Advanced Constraints Conclusion

Now that we've carefully translated our schematic and constraints into a physical design optimized for high-speed performance, this layout forms the foundation for successful signal integrity and power distribution in our FPGA and DDR memory design. In Part 3 of the guide, we'll explore how to verify our design through signal integrity analysis, ensuring that our layout meets the stringent requirements of high-speed digital circuits.