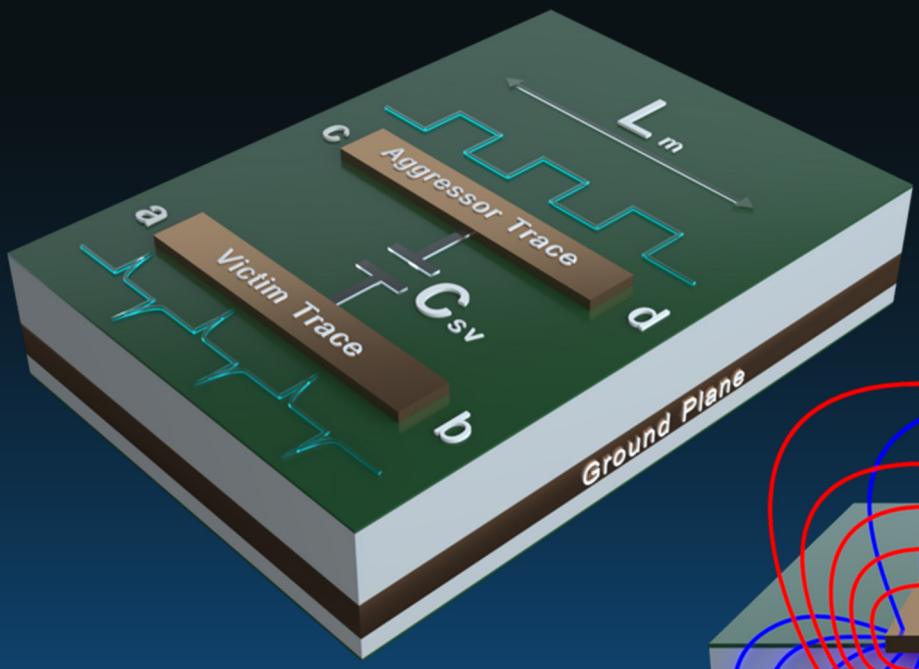
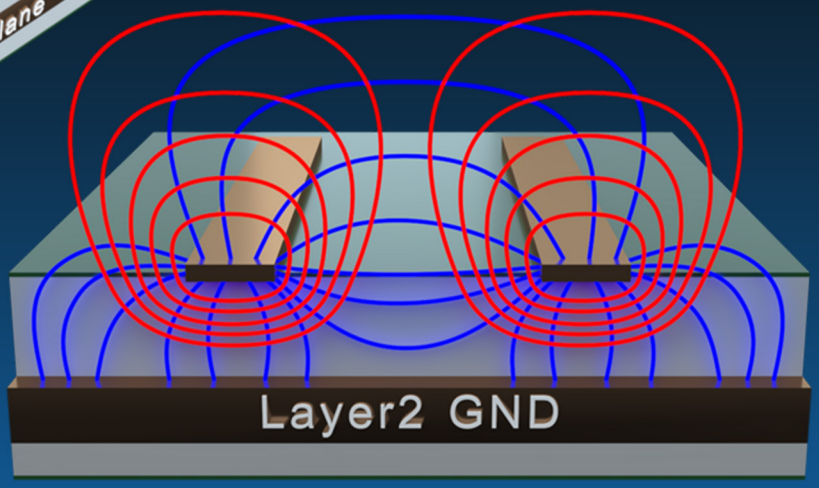
DESIGN **GUIDE**

cadence®

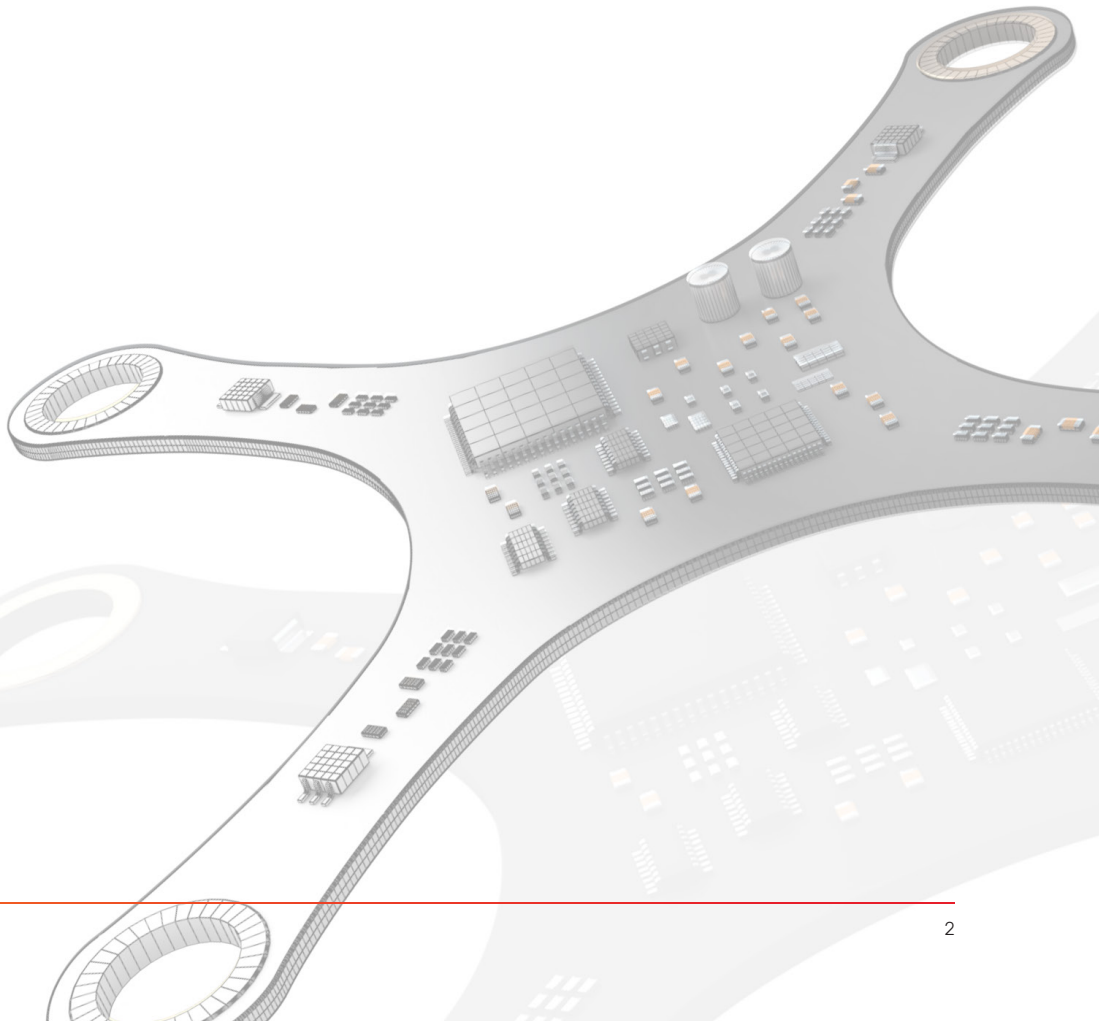
OrCAD X High-Speed Digital Design Guide

Part 3 of 3: Simulation, Analysis, and Verification





Contents



Part 3: Simulation, Analysis, and Verification

After setting constraints and routing, we need to verify the signals in a design. Typically, you want to do the following kinds of analyses: signal integrity, electromagnetic compatibility, high-speed signal timing, and power integrity.

Signal Integrity Analysis

Signal integrity (SI) is a cornerstone of high-speed PCB design, ensuring that signals are transmitted without distortion or degradation. For our FPGA with DDR2 and DDR3 memory project, maintaining SI is critical for avoiding timing errors, data corruption, and performance issues. Proper SI analysis helps identify and mitigate issues such as reflections, crosstalk, and impedance mismatches.

General Solution

Signal integrity analysis involves both pre-layout and post-layout simulations. Pre-layout analysis helps define constraints such as impedance targets and trace lengths, while post-layout analysis verifies that the implemented design meets these constraints. Tools like OrCAD X Presto provide integrated workflows for identifying and resolving SI issues.

Signal Integrity Analysis Conditions:

1. DDR3 Parameters:

- Rise time: 200ps
- Operating frequency: 800 MHz
- Voltage swing: 1.5V

2. Critical Analysis Points:

Clock Analysis:

- Clock to DQS skew
- Clock tree delay
- Crosstalk on CLK pairs

Data Group Analysis:

- Setup/hold margins
- Reflection analysis
- Crosstalk analysis

Impedance Analysis

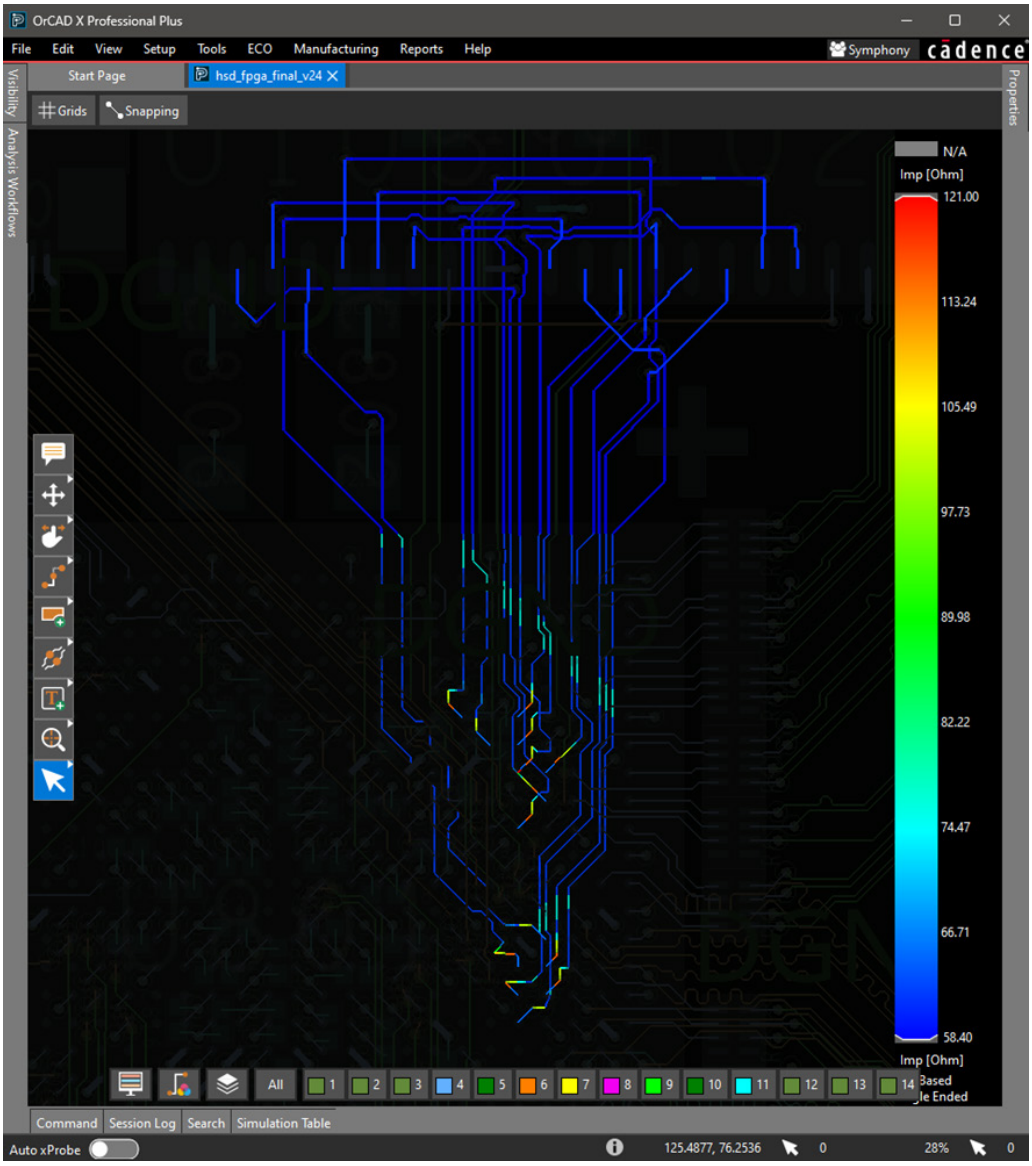
The lowest hanging fruit to simulate for is trace impedance.

First, ensure you have the appropriate version of Sigrity X Aurora installed on the computer. For example, if you're using OrCAD X version 24.1, then you must use Sigrity X Aurora 24.1, and not some other version like 23.1 or 24.0.1.

Once installed, you're ready to run analyses on your PCB.

To analyze impedance on your board in OrCAD X Presto PCB Editor, do the following:

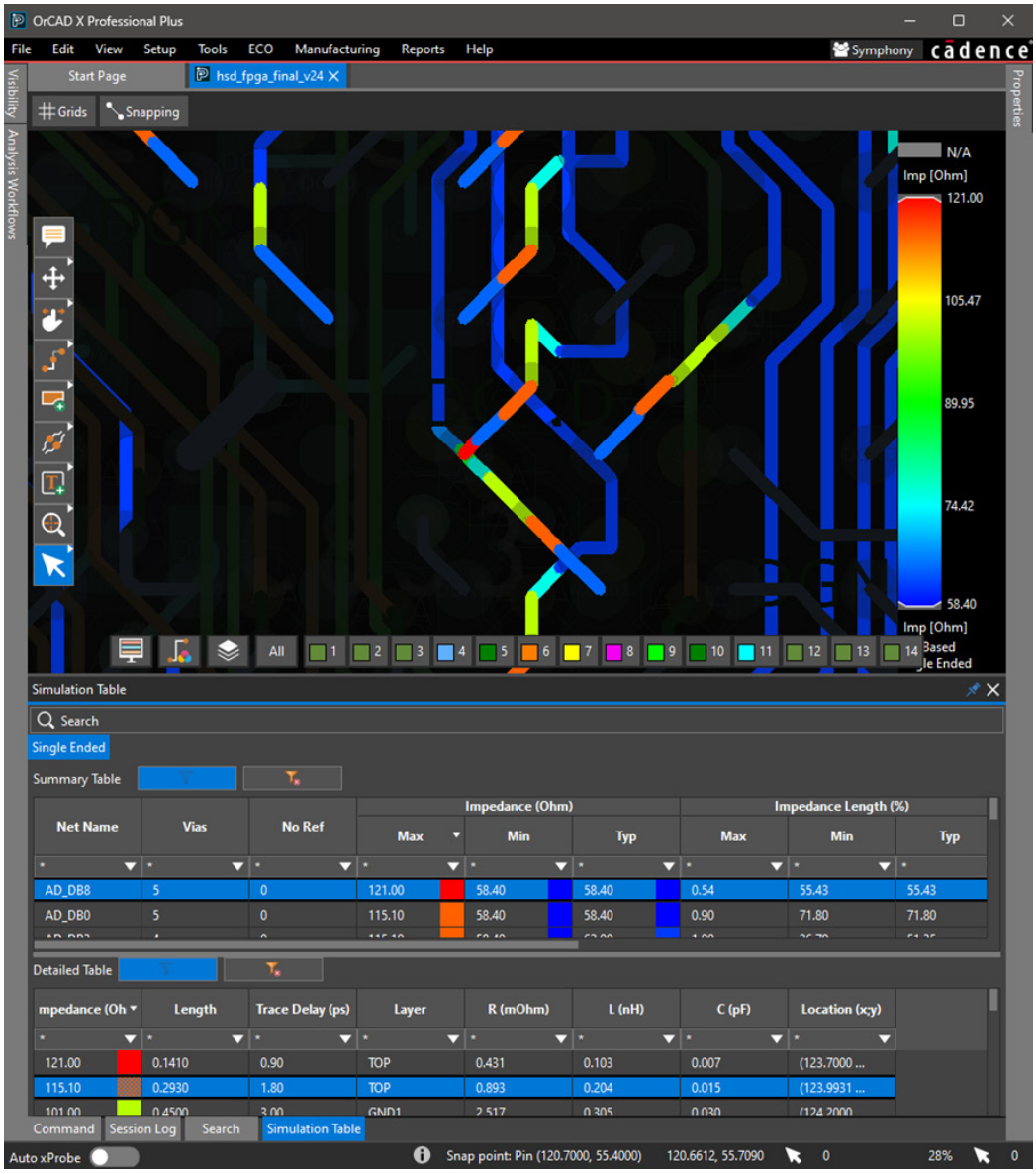
1. Go to **View > Panels > Analysis Workflows.**
2. From the drop down within the Analysis Workflows panel make sure Impedance Workflow is selected.
3. Under Analysis Set Up, keep Analysis Modes as Net Based, then choose Select Nets.
4. Select all the nets for analysis then click apply and OK.
5. Next, select Set Up Analysis Options. This opens the IDA Compliance Analysis Parameters Setup.
6. Turn everything on that you would want to analyze, then click Apply and OK.
7. Next, click Start Analysis. The software will analyze the design, showing a progress bar to let you know when it is finished.
8. Once the design has been analyzed, select **View Impedance Visions** to see a color-coded view of the analyzed nets.



The design will visually show you the impedances of every trace you added for analysis. We see that most traces fall within the 58 Ohm to 75 Ohm impedance range while some traces are in the 110+ Ohm range.

It is up to the designer and layout standards for those protocols to decide what impedances are acceptable vs. not acceptable.

9. For more detailed impedance measurements, click the View Impedance Tables option. This option provides data in a tabular form that can be exported for analysis.

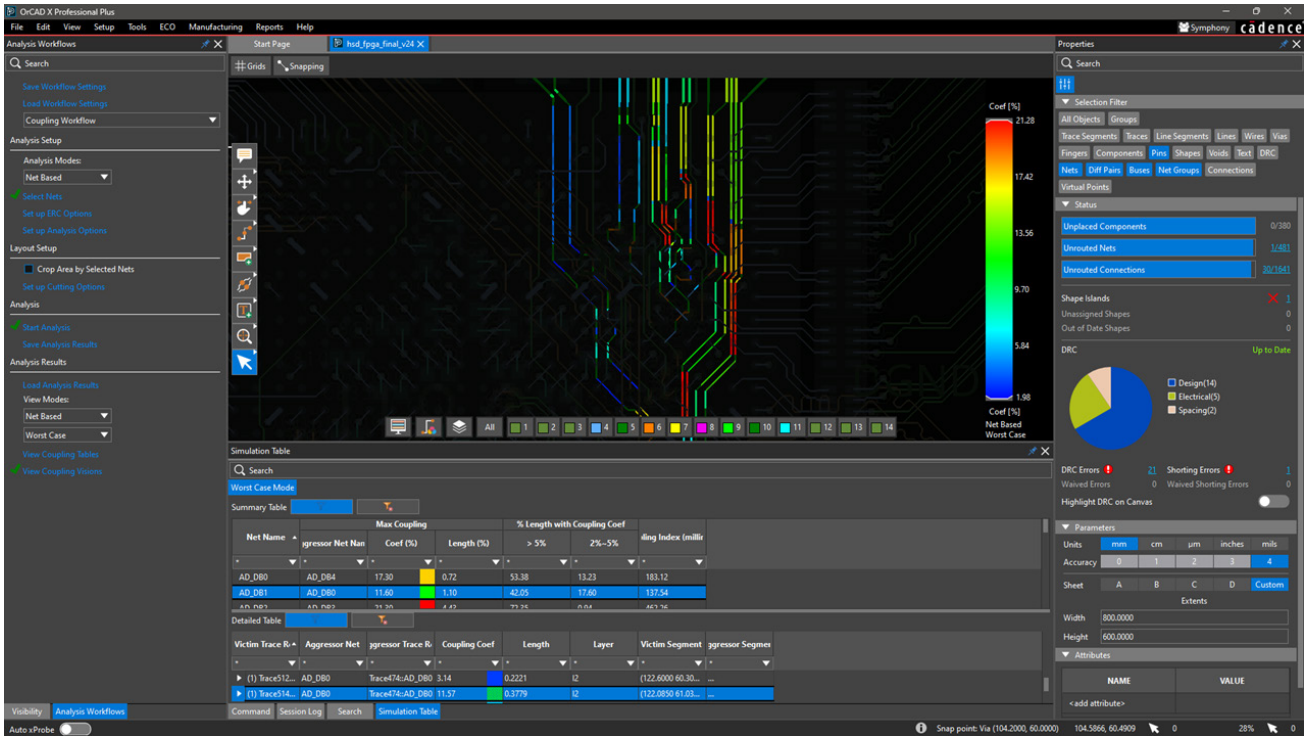


10. You can also save the simulation results below the Analysis Setup menu in the image above (Pin or move the table to see it).

Coupling Analysis

Another major enemy of working designs is signal coupling. OrCAD X Presto PCB Editor addresses this concern as well through simulation. To run this analysis, do the following:

1. Go to **View > Panels > Analysis Workflows**.
2. From the drop down within the Analysis Workflows panel select Coupling Workflow.
3. Under Analysis Modes, Choose Net Based, then click Select Nets
4. Add all nets to the right column for analysis, then click Apply and OK.
5. As before, you can Set Up Analysis Options and check any options that interest you.
6. After that, click Start Analysis. The software will perform its analysis, then generate results in visual form as an option and tabular form through **View Coupling Visions** and **View Coupling Tables**, respectively.



You would check the analysis results then save them as needed.

As an example, you would have certain criteria that need to be met in order to know whether the results above are suitable.

Examples of Signal Integrity Limits:

1. Timing Requirements:

Clock Skew:

- Pass: < ±50ps
- Warning: 50-75ps
- Fail: > 75ps

Setup/Hold Times:

- Pass: > 125ps setup, > 100ps hold
- Fail: Below these limits

2. Crosstalk Limits:

Clock Signals:

- Acceptable: < 8% coupling
- Warning: 8-10%
- Critical: > 10%

Data Signals:

- Acceptable: < 10%
- Warning: 10-15%
- Critical: > 15%

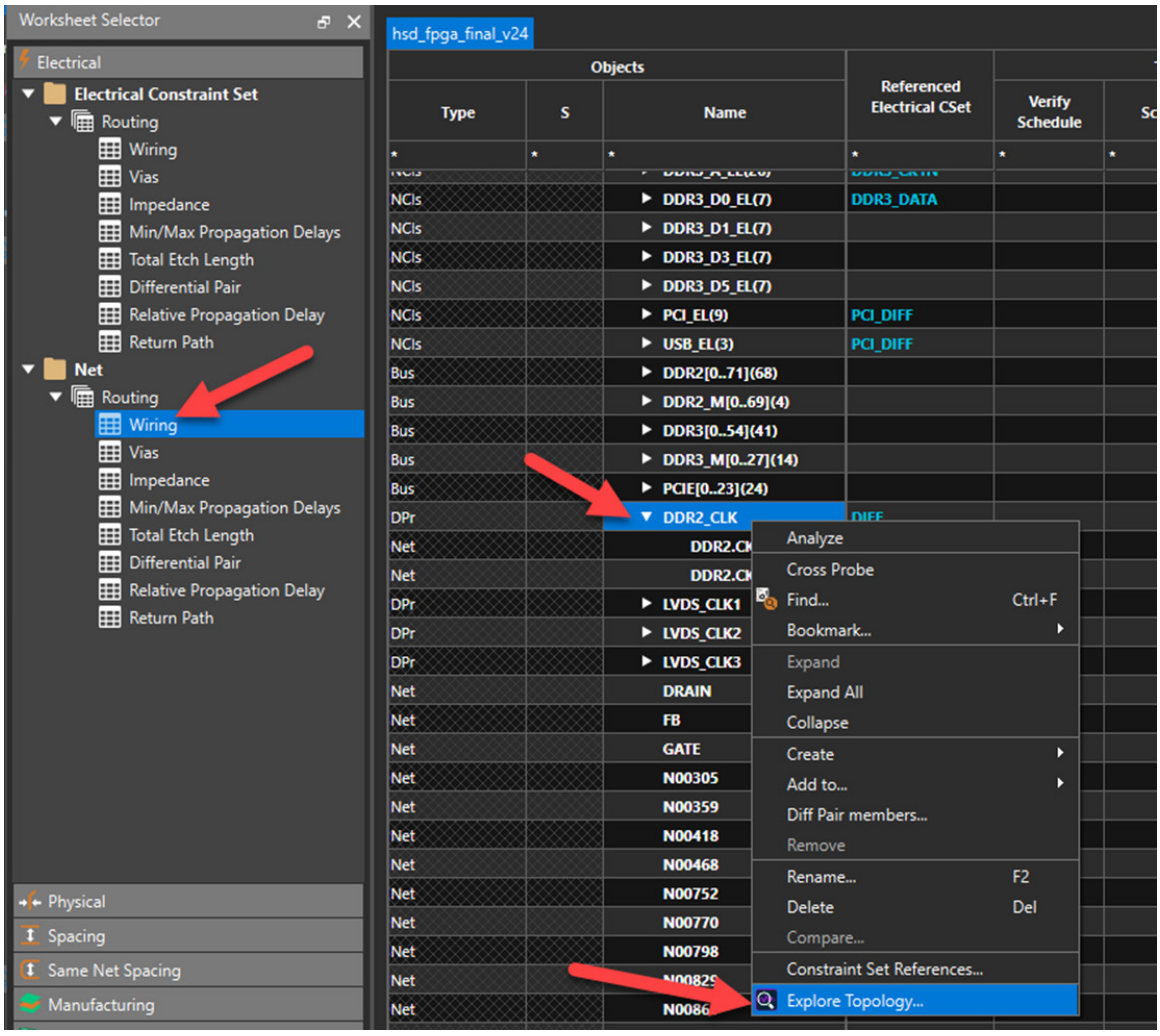
High-Speed Simulation and Verification

While understanding that coupling and impedance are valuable, we need to know if certain signals genuinely pose a problem in the current layout. To find out, we must see the signal behavior on traces of interest. The best way is through transmission line simulation and eye diagram analysis. We will show you how to verify signal behavior with special tools in OrCAD X.

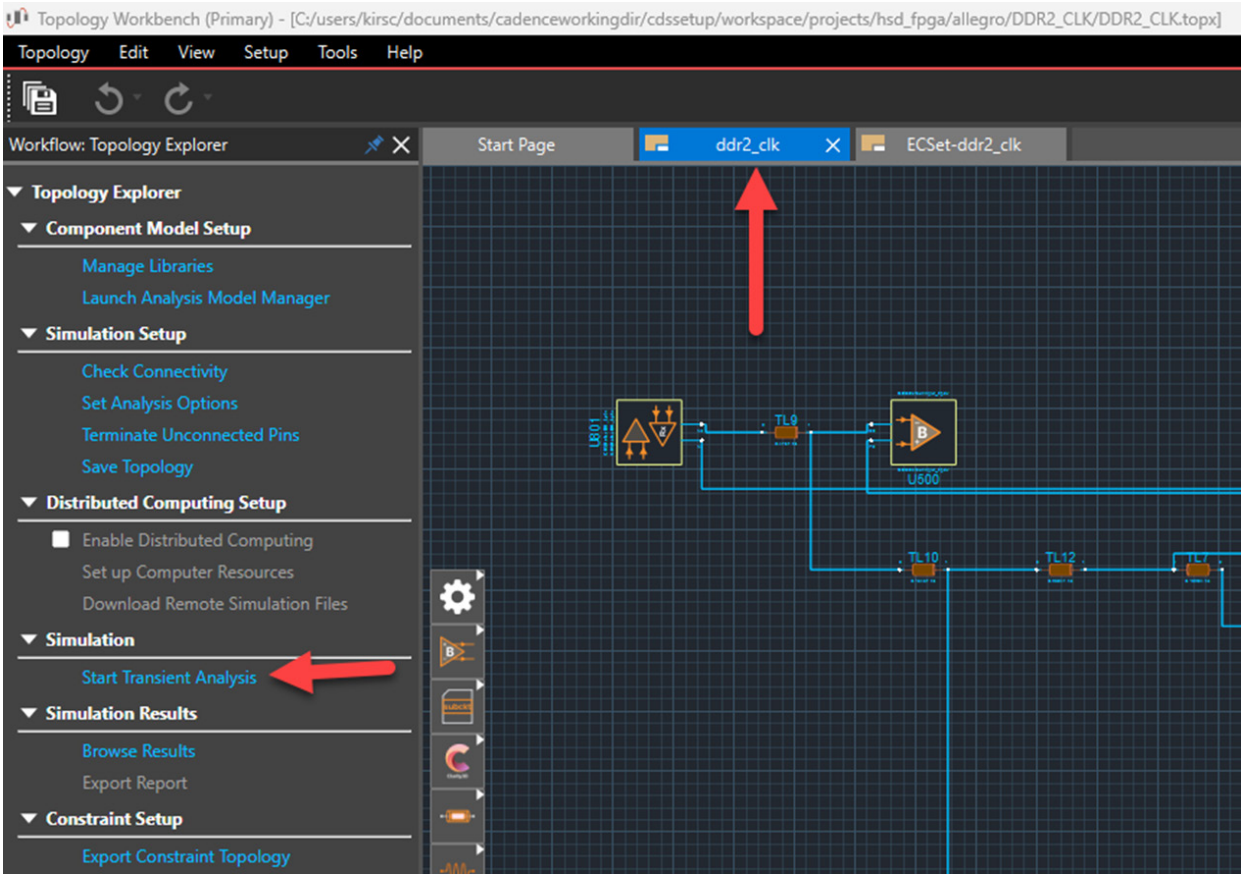
Signal Reflection Analysis

Let's check a clock signal to see if it has issues:

1. Go to **Tools > Constraint Manager.**
2. Select a clock net from within the **Electrical > Electrical Constraint Set > Vias worksheet**, then right click and select Explore Topology. Alternatively, you can highlight the net, then while highlighted (in blue) click the Constraint Manager's menu **Tools > Explore Topology.**

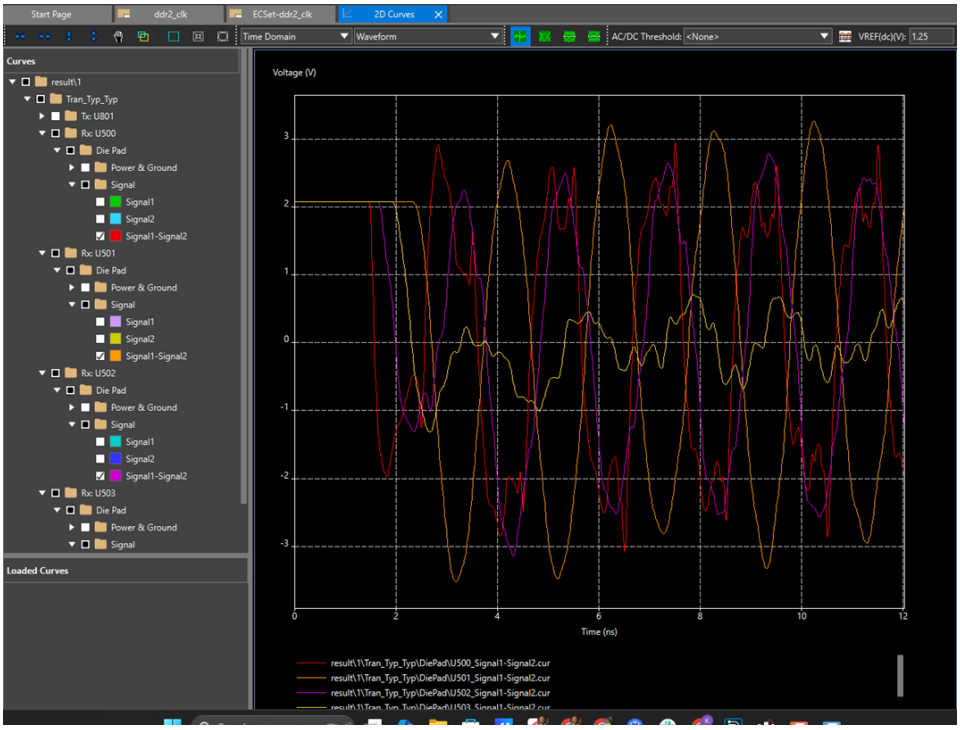


3. **Topology Workbench** will open.
4. Click the DDR2_CLK tab or whichever tab that has a view of buffers and transmission lines, like the ones shown below.

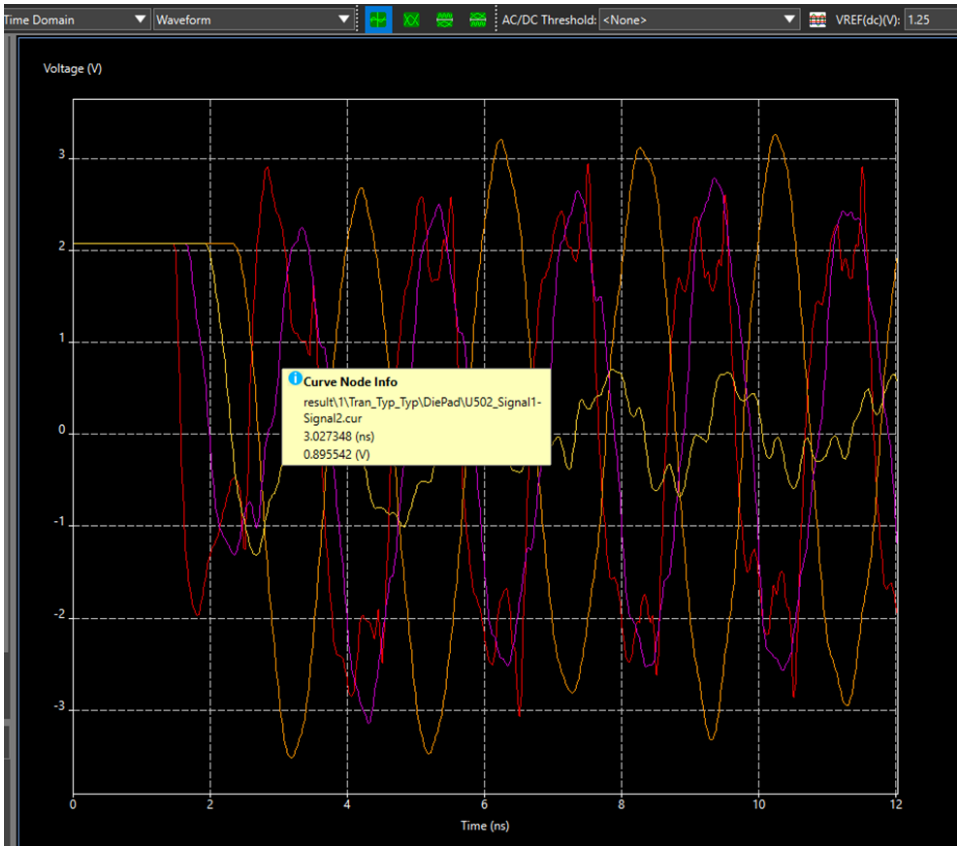


5. Click on **Start Transient Analysis** to perform signal simulation on the circuit and see the waveform.
6. However, you may get a window pop up that says your IO (IBIS) blocks are of Receiver type. You can choose to continue the simulation. Choose **No**.
7. Set the left-most device, U801 to Transmitter instead of Receiver by clicking on U801, then on the right panel, find the Type filed under the Name column.
8. Where it says Receiver, double-click that word, then get the dropdown and change it to Transmitter. Now our circuit should be set up to see how well our traces are carrying the high-speed signals.
9. Go back to the Topology Explorer Panel and under the **Simulation** section, click **Start Transient Analysis**.

10. A new tab named 2D Curves pops up and shows the waveforms for the signals (see below).



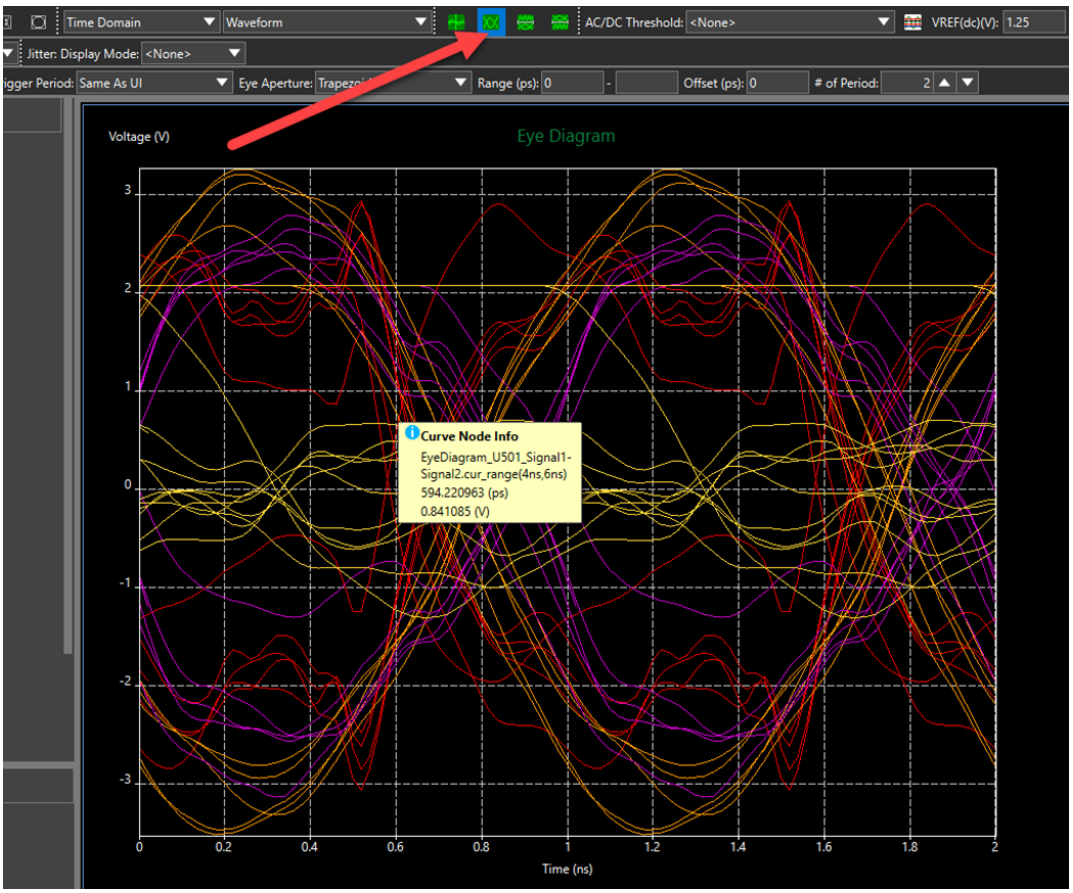
11. It shows you how the clock signals will appear once they travel through the trace for those nets.



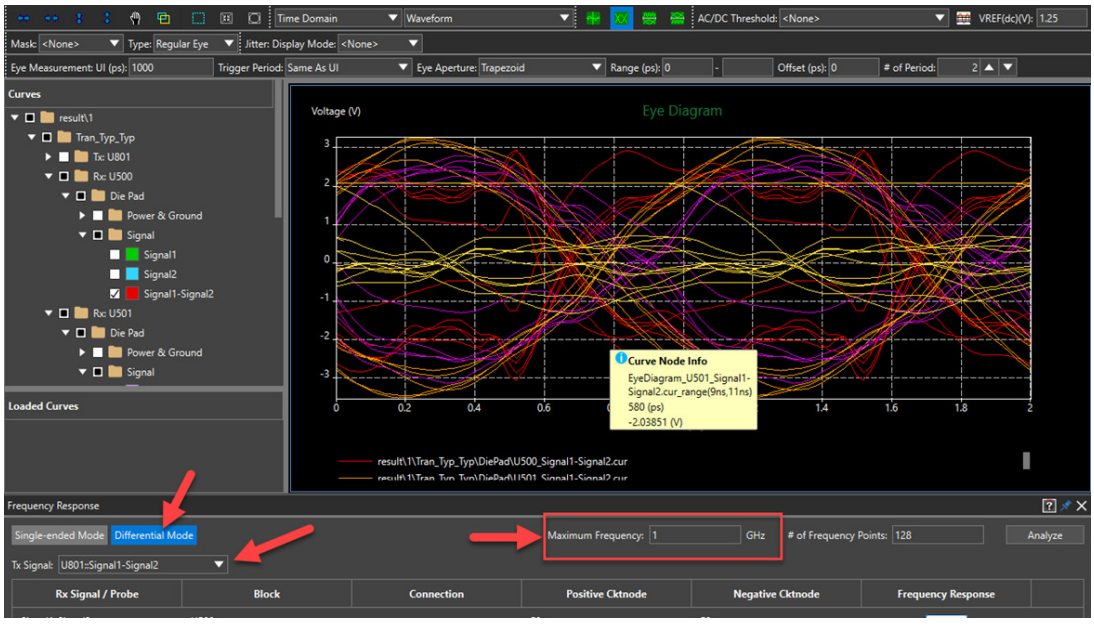
Eye Diagram Analysis

While in Topology Workbench and viewing the waveform, you can adjust the view for eye diagram performance.

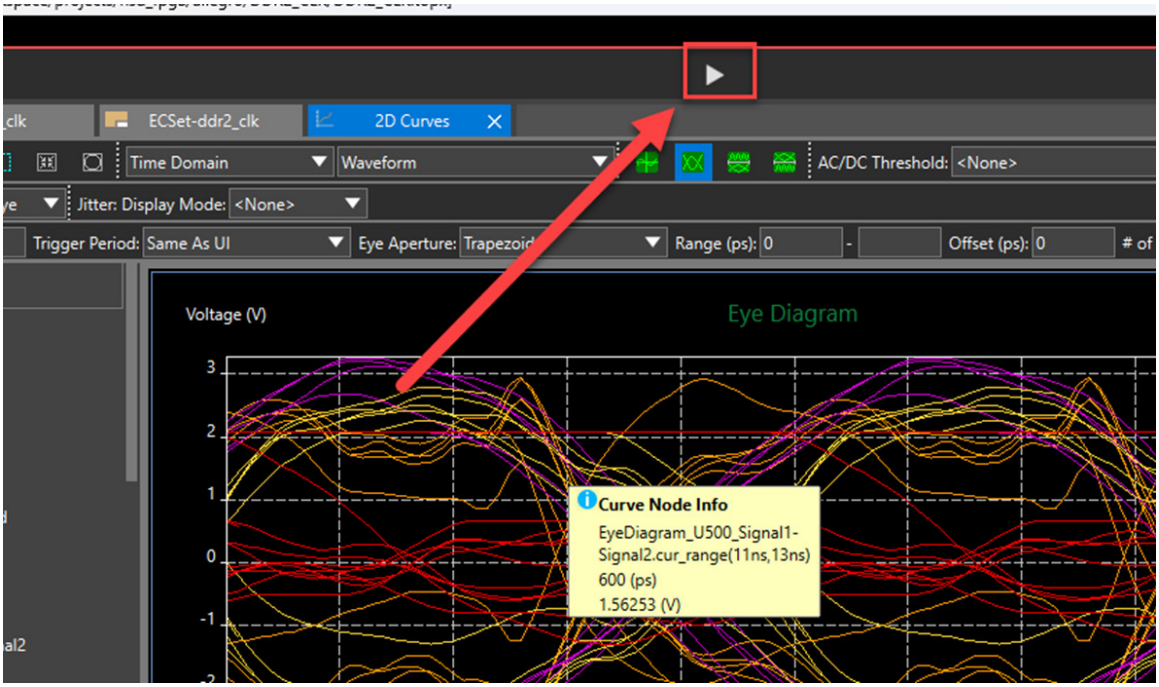
1. Within the 2D Curves tab, click on the Eye Diagram icon within the toolbar. As you'll see, a number of these eyes have collapsed, so our parameters and values may need tweaking, or the routing is not well done



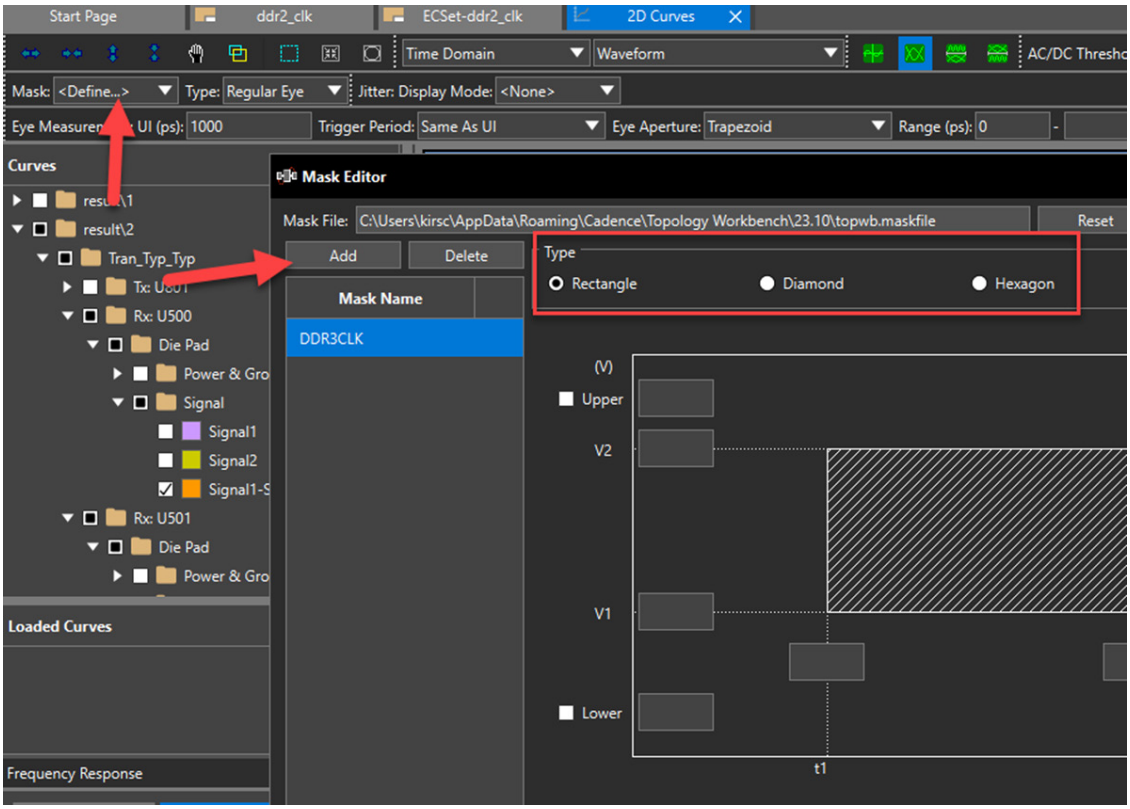
2. Set the analysis to the appropriate frequency for the device you're analyzing - in this case DDR3 at 800 MHz (up to 1 GHz is also fine).



3. Then run the simulation by clicking the Play button at the top of the screen and see how the eye looks.



If the eye mask you're using from your design requirements fits, then the layout is sufficient for signal performance. See the eye diagram options you can select in the image below by clicking the menu *Mask - Define* options, then when the Mask Editor window appears, click the **Add** button to start adding your own mask shapes for high-speed eye diagram signal verification. As highlighted in the image below, you can select different Types (shapes) for the mask as well:



As you work within the Topology Workbench you will discover that you can vary the information, bits and pulses sent through the transmitter for the signal in that net as well, thus being able to test and search for any specific bit patterns that can come from the clock signal that can ruin the design.

Depending on your findings from simulation, you can also back-propagate the appropriate constraints that would meet optimal signal perforce from the simulation. Then use those new constraints in OrCAD X Presto PCB Editor Constraint Manager to properly constrain the traces and PCB layout in a way that would comply with the desired simulation outcome. This is results driven and constraints driven PCB Design.

For more information on how to use the Topology Workbench, refer to Cadence documentation and design guides.

Power Integrity Considerations

Power integrity (PI) is essential in high-speed PCB design, ensuring that power is delivered consistently and cleanly to all components. For our FPGA with DDR2 and DDR3 memory project, maintaining PI is critical to avoid voltage fluctuations and ensure stable operation.

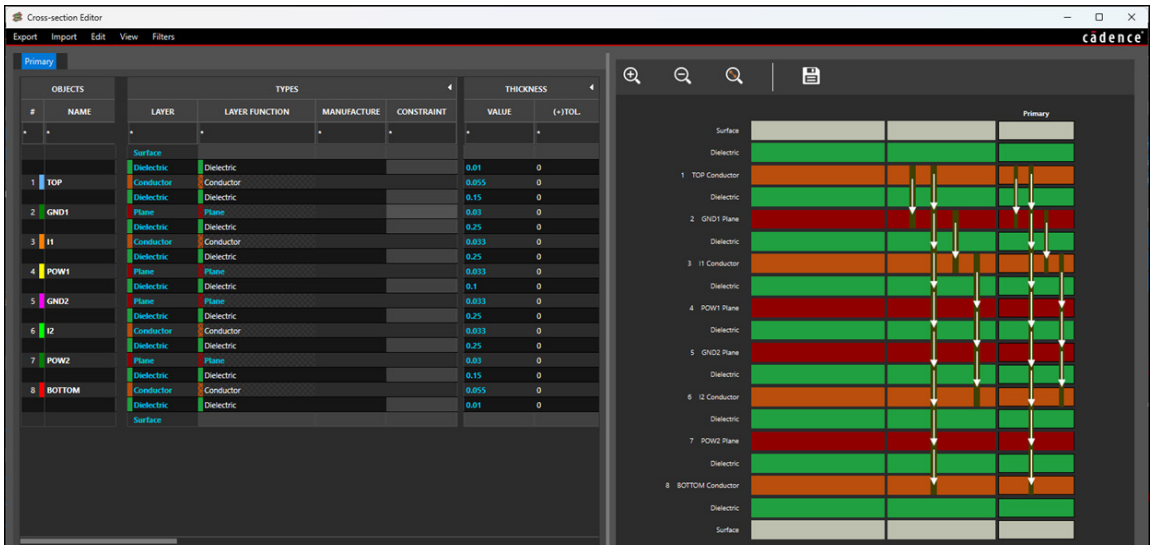
Proper PI considerations help prevent issues such as power noise and voltage drop, which can affect signal integrity and overall device performance.

General Solution:

Effective power integrity management involves designing a robust power distribution network (PDN), strategically placing decoupling capacitors, and minimizing inductance in power delivery paths. These practices help maintain a stable voltage supply across the board, even under dynamic load conditions.

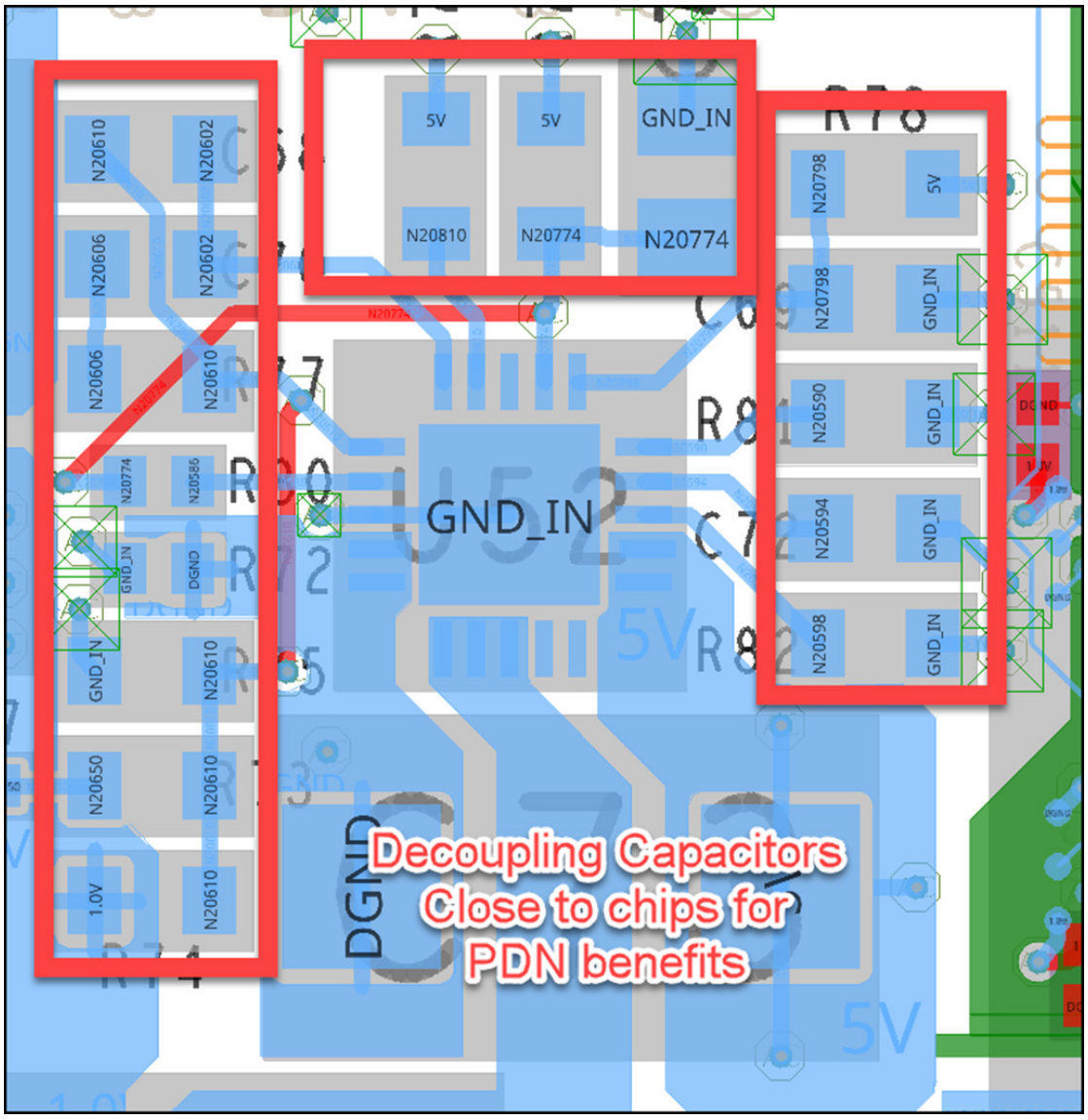
Application in OrCAD X Presto:

1. Design the Power Distribution Network (PDN):
    a. Go to Tools > Cross Section to define power planes
    b. Ensure dedicated power planes are included for core, I/O, and DDR3 voltages
    c. Set power planes within the stack-up to create low-impedance paths for power delivery. See the stack up below



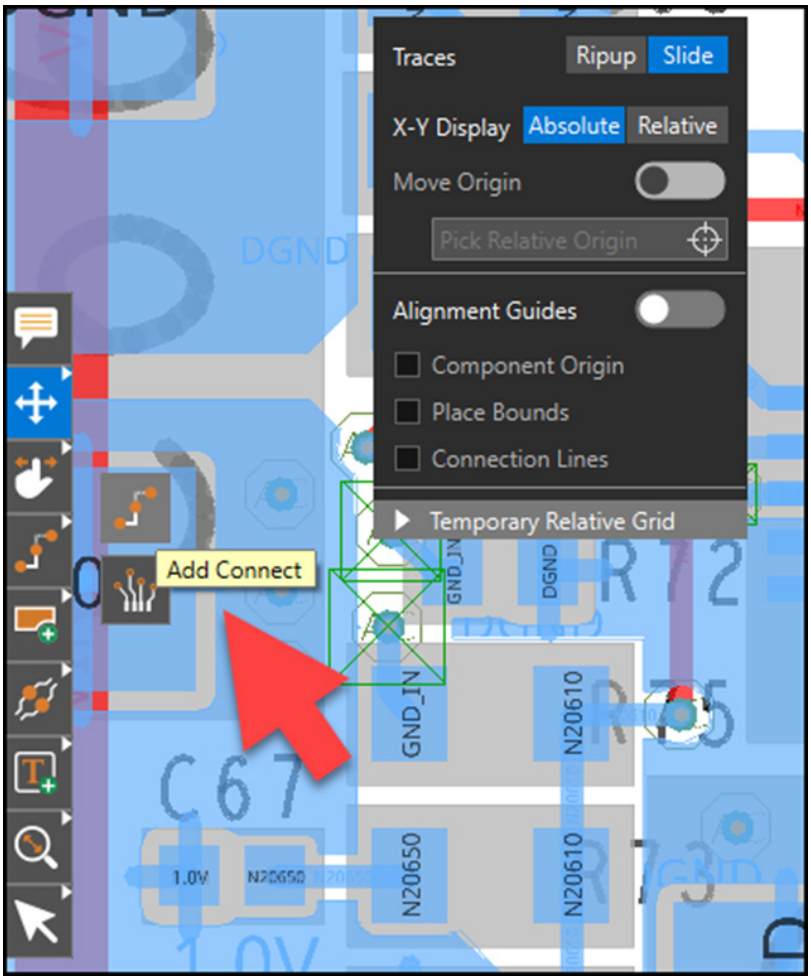
2. Placing Decoupling Capacitors:
    a. You can use the place icon in the toolbar to add decoupling capacitors near each IC power pin
    b. Place a combination of 0.01µF, 0.1µF, and 10µF capacitors for broad frequency coverage
    c. In Presto PCB Editor go to **ECO > Quickplace Components** for automatic placement of capacitors near their chips if organized by room

Placing capacitors by room makes it easier to place them right next to their respective chip pins, like what is shown in the image below.



Screenshot showing the placement of decoupling capacitors around a DDR Memory chip

3. Minimize Inductance:
    a. Route power traces with minimal loop area by keeping them parallel to ground traces
    b. Use multiple vias for power connections to reduce inductance
    c. Ensure short and wide traces for power delivery



4. Perform Power Integrity Analysis:
    a. Use a power integrity analysis tool such as Celsius PowerDC to analyze the power distribution on a PCB

Example of Power Distribution Acceptance Criteria:

Core Power (1.2V):

- Good: < 3% drop (< 36mV)
- Marginal: 3-5% drop
- Unacceptable: > 5% drop

DDR3 Power (1.5V):

- Good: < 4% drop (< 60mV)
- Marginal: 4-6% drop
- Unacceptable: > 6% drop

Power Integrity Analysis Conclusion

By implementing robust power integrity strategies in OrCAD X Presto, we've ensured stable power delivery across our high-speed PCB design. This step minimizes risks of voltage fluctuations like rail collapse and ground bounce and enhances overall device reliability.

PCB Simulation and Verification Conclusion

The only true way to know if your design will work is if you test it, but simulation is just as good of a solution for a fraction of the time and cost. Where possible, simulate. It always beats rules of thumb, but only if you have time. If simulation is too much to set up, then quick impedance and coupling workflows with rules of thumb are a quick compromise. But considering how easy it is to simulate using OrCAD X, there is not a strong case to skip this step any longer in the hardware design process.

Lessons Learned and Best Practices

Here are key takeaways for successful high-speed digital PCB design:

1. Constraints-Driven Design Approach:
    a. Define clear design constraints early
    b. Use simulation and analysis tools proactively
    c. Iterate design based on simulation results
2. Signal Integrity Considerations:
    a. Minimize trace lengths
    b. Use inner layers for critical signals
    c. Implement proper termination strategies
    d. Maintain consistent impedance
3. Power Integrity Techniques:
    a. Use multiple decoupling capacitors
    b. Design low-impedance power distribution networks
    c. Consider power plane segmentation
    d. Minimize power and ground loop areas
4. EMC Design Strategies:
    a. Implement ground planes
    b. Use guard traces
    c. Add stitching vias
    d. Route high-speed signals on inner layers
5. Continuous Learning:
    a. Stay updated with latest high-speed design techniques
    b. Attend technical conferences
    c. Read industry publications
    d. Experiment with new design methodologies

Conclusion

Mastering high-speed digital PCB design requires a holistic approach combining theoretical knowledge, practical skills, and advanced tools. By understanding signal integrity, power integrity, and electromagnetic compatibility, you can create robust, high-performance electronic systems.

The constraints-driven methodology outlined in this guide provides a systematic approach to tackling the complexities of modern high-speed digital design that meet design outcomes. Remember that each design is unique, and continuous learning, good tools and iteration are key to success.

As technology advances, the principles of careful design, thorough analysis, and rigorous testing will remain fundamental to creating reliable, high-performance electronic hardware.