WHITE **PAPER**

cadence®

Accelerating SI/PI Signoff: A Shift-Left Approach to High-Speed PCB Design

Introduction

In modern PCB design, addressing signal integrity (SI) and power integrity (PI) issues early in the design cycle is critical for cost efficiency and product reliability. Transitioning designs from schematic to layout and signoff is a complex process for PCB design engineers, often involving multiple teams and iterative workflows to meet performance expectations.

This white paper examines the challenges that PCB design engineers encounter during the signoff process and provides detailed guidance on addressing these issues through in-design analysis using Cadence tools. It outlines how Cadence enables engineers to implement a "shift-left" approach, allowing for the early identification and resolution of SI and PI challenges. By incorporating these advanced tools into the design workflow, engineers can reduce the risk of costly late-stage design iterations, ensure adherence to performance specifications, and enhance overall design confidence and efficiency.

Contents

The Importance of Early SI/PI Analysis

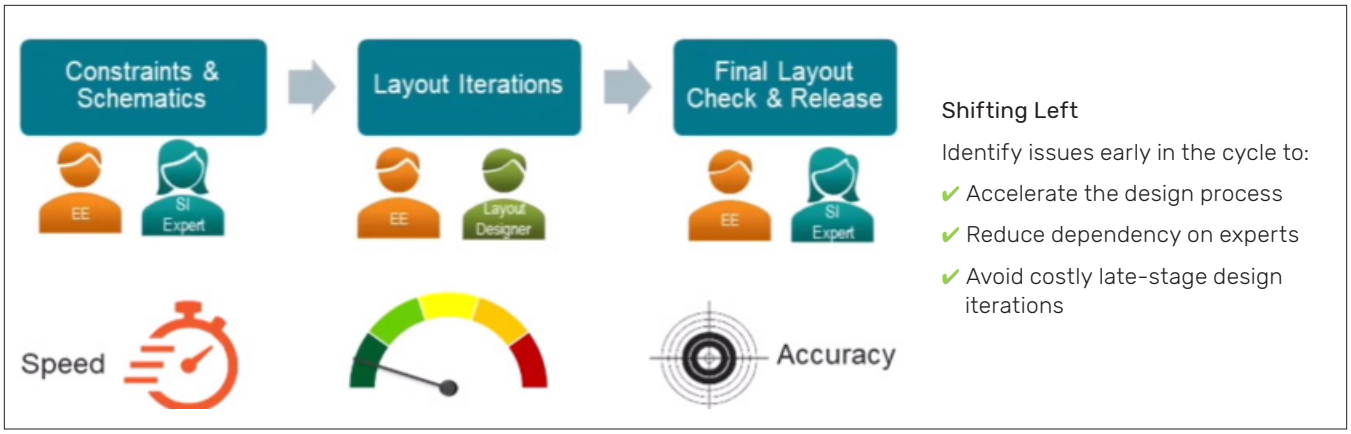
The concept of "shift left" focuses on identifying and resolving design challenges as early as possible in the development process. Early intervention reduces the cost and effort of corrections and prevents cascading issues that could arise in later stages. At Cadence, we equip electrical engineers with the tools to identify and resolve SI/PI issues, reducing dependency on experts, and accelerating the design process.

The PCB Design Cycle and Signoff

Schematic > Layout > Post Layout > Signoff

The traditional PCB design cycle involves distinct phases, each presenting unique challenges:

- **Schematic Phase:** Focus on determining design constraints, fundamental "rules of thumb," and SI/PI basics.
- **Layout Phase:** Collaboration between electrical engineers (EE) and layout designers ensures high-speed nets meet design criteria.
- **Post-Layout and Signoff:** Validation of the design against protocol specifications and SI/PI standards.



By integrating **in-design analysis tools** into this timeline, engineers can **address potential errors**, such as SI and PI issues, **early and with greater accuracy.**

"The earlier you catch issues, including power and signal integrity, the better, as they are usually easier and cheaper to fix. At Cadence, we empower electrical engineers to shift left and identify major issues as early as possible in the design cycle."

Patrick Davis, Product Management Director

Enhancing Collaboration Across Teams

Seamless collaboration between schematic designers, signal integrity engineers, and layout designers is critical. Our solutions aim to:

- Enable EEs to define high-speed constraints at the schematic stage with minimal reliance on signal integrity experts.
- Provide layout designers with intuitive visualization tools to address SI/PI issues directly in the layout environment.
- Facilitate efficient handoffs and iterative improvements through in-tool feedback mechanisms.

Balancing Speed and Accuracy

In the early design stages, engineers prioritize quick, ballpark answers to identify potential problems. As the design matures, the need shifts toward high accuracy to meet compliance standards and secure final sign-off. Our approach includes:

- **Targeted Simulations:** Focus on specific components or network segments early in the process to gain quick, meaningful insights.
- **Parallel Processing:** Use distributed computing to run detailed simulations efficiently, maintaining both speed and accuracy.
- **Protocol Compliance Checks:** Continuously check designs against protocol standards to ensure full compliance before production.

Challenges in Ensuring Seamless Signoff

1. Power Integrity Challenges

1.1. Power Delivery Network Visualization

Understanding the power structure of a PCB is fundamental to achieving a reliable and efficient design. Cadence's Power Tree tool provides a detailed visualization of power sources, sinks, and connections, helping engineers identify issues like unnatural resistance drops or bad connections.

1.2. DC and AC Power Analysis

DC Power Analysis

DC power analysis focuses on understanding how direct current flows through a PCB's power distribution network (PDN). The primary concern in DC analysis is voltage drop, also called IR drop, which results from the finite resistance of copper traces, vias, and planes. If excessive voltage drop occurs, critical components may not receive sufficient power, leading to malfunction or degraded performance.

Key considerations in DC power analysis include:

- **IR Drop Analysis:** Evaluating voltage drops across power planes and traces to ensure they remain within defined tolerances, maintaining system integrity and performance.
- **Current Density Analysis:** Mapping regions of elevated current density to identify areas at risk for excessive thermal buildup or electromigration-related failures.
- **Copper Weight and Thickness Optimization:** Calculating and verifying appropriate copper thickness to reduce resistive losses and enhance overall power delivery efficiency.

Cadence's tools provide detailed resistance and voltage drop simulations to help engineers calculate whether these voltage drops remain within acceptable limits.

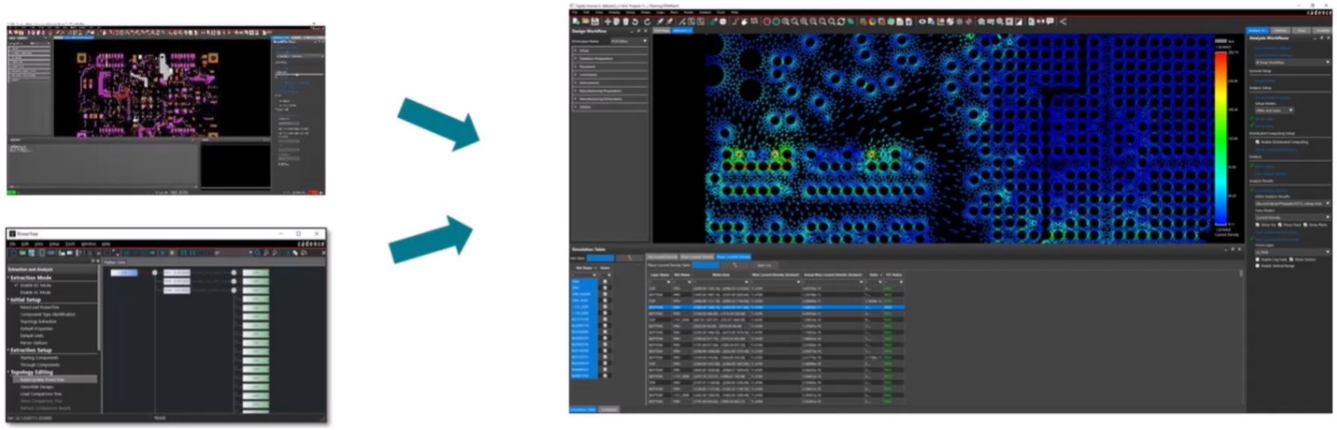


Figure 1: Power workflow for DC drop analysis identifies IR drops, currents, current density, and via currents to avoid bottlenecks.

AC Power Analysis

AC power analysis is essential for understanding how a PCB reacts to transient and high-frequency switching currents. Each time the logic switches, millions of integrated circuits (ICs) will toggle simultaneously, demanding instant current. This high-frequency activity causes PCB inductance. Unlike DC analysis, which deals with steady-state conditions, AC analysis examines dynamic behaviors that can impact system performance, such as power noise, impedance mismatches, and inductive effects. Identifying high-inductance capacitors and minimizing inductance is key to ensuring proper power delivery.

Key factors in AC power analysis include:

- **Decoupling Capacitor Placement:** Ensuring proper capacitor selection and placement to provide instantaneous current to ICs during switching events.
- **Power Integrity in High-Frequency Domains:** Evaluating the effectiveness of bypass capacitors and power planes in reducing power noise.
- **Impedance Analysis:** Measuring and controlling power plane impedance to maintain stable voltage delivery across a wide frequency range.
- **Inductive Effects:** Addressing unwanted inductance, which can cause voltage fluctuations and noise, particularly in fast-switching logic circuits.
- **Simultaneous Switching Noise (SSN):** Analyzing the impact of multiple ICs switching at the same time, which can generate unwanted noise and voltage ripples on the PDN.

Cadence's AC power analysis tools simulate transient responses, power noise, and impedance profiles to ensure that high-speed components receive clean and stable power. These insights help engineers mitigate issues such as excessive noise, unwanted resonances, and transient voltage fluctuations, ensuring overall power integrity.

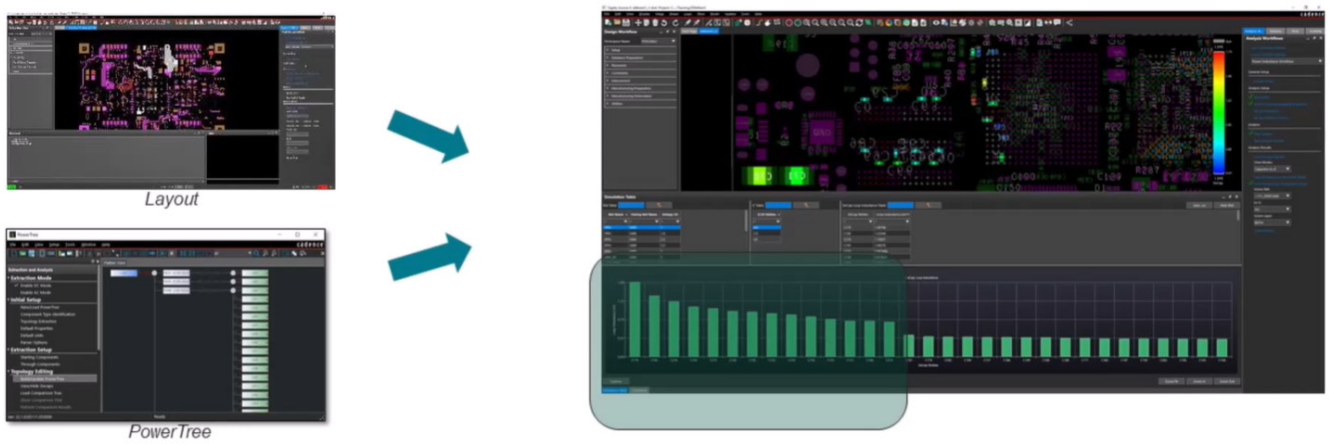


Figure 2: Power workflow for decoupling cap placement enables quick identification of outliers in loop induction.

By combining DC and AC power analysis, Cadence tools provide engineers with comprehensive solutions to optimize PDN performance, reduce power-related failures, and ensure seamless signoff for complex PCB designs.

2. SerDes Design Challenges

Serializer/Deserializer (SerDes) interfaces operate at extremely high speeds, often multi-gigabit rates in applications such as PCIe, Ethernet, USB, and UCIe. Designing for SerDes presents unique design challenges due to the extreme sensitivity of signals to channel losses, via effects, and specification compliance.

2.1. Vias and their Impact on Signal Integrity

Vias play a critical role in high-speed PCB design, but they introduce unwanted discontinuities, impedance mismatches, and signal degradation, especially in SerDes channels. Key via-related challenges include:

- Unwanted inductive and capacitive effects, causing reflections and degraded signal quality
- Stub resonance caused by unused portions of vias
- Return path discontinuity, increasing noise and electromagnetic interference (EMI)

Using the Cadence Aurora Via Wizard, engineers can design, easily visualize and validate via structures early in the cycle—part of our shift-left mentality—reducing dependency on signal integrity experts.

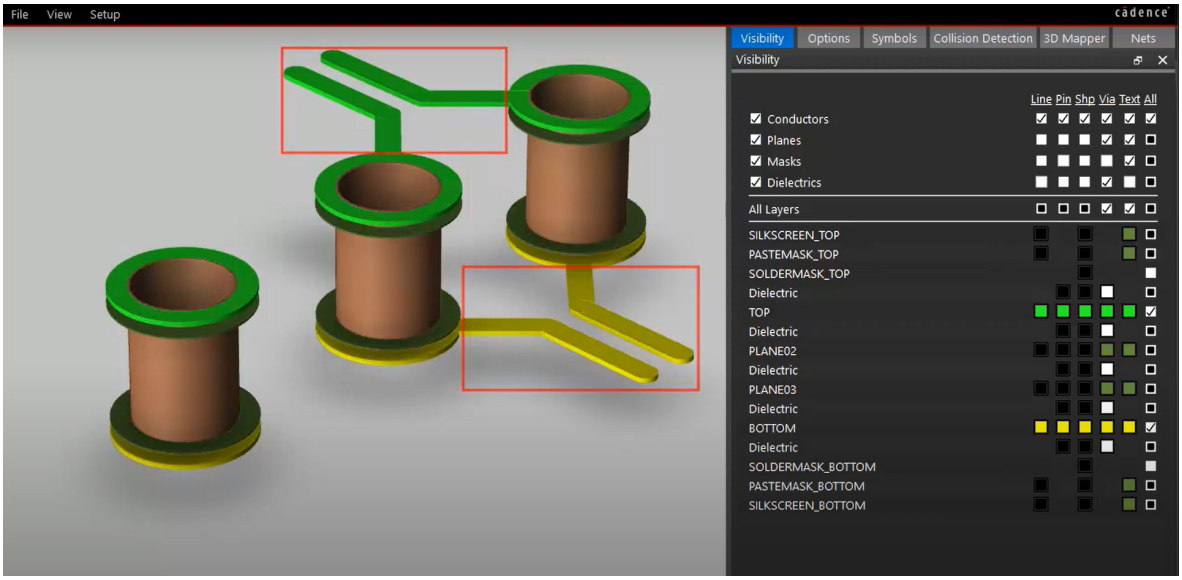


Figure 3: Aurora Via Wizard

2.2. Channel Losses and Material Selection

At high frequencies, PCB materials like FR4 have a significant impact on signal integrity due to losses introduced by conductor resistance, dielectric absorption, and roughness of copper traces. Choosing the right materials and physical design constraints is essential to reducing losses.

Primary Loss Mechanisms:

- **Conductor Loss (Skin Effect):** At SerDes frequencies, current density shifts toward the outer surface of traces, increasing effective resistance and signal attenuation.
- **Dielectric Loss (Dissipation Factor, Df):** High-frequency signals lose energy within the PCB substrate, degrading signal amplitude over long traces.
- **Copper Surface Roughness:** Rougher copper surfaces increase resistance, leading to higher insertion loss and signal degradation.

Material and Design Considerations:

- **Dielectric Selection:** Choosing low-loss materials such as MEGTRON 6, Rogers 4000 series, or Isola Tachyon for better high-frequency performance.
- **Optimized Trace Geometry:** Adjusting trace width and spacing to control impedance and minimize signal loss.
- **Reference Plane Considerations:** Maintaining a continuous ground plane beneath signal traces to ensure stable impedance and reduce unwanted reflections.

Cadence's Sigrity™ X Topology Explorer Workbench enables engineers to easily simulate different dielectric materials to compare loss characteristics and determine design constraints such as trace spacing and reference plane height to minimize insertion and return losses.

2.3. Specification Requirements and Protocol-Specific Requirements

SerDes interfaces must comply with strict industry standards, each defined by specific electrical performance and compliance criteria. Some of the most common protocols include PCIe, USB, and UCIe. By integrating compliance analysis directly into the design tool chain, engineers can iteratively refine designs to meet these stringent specifications.

SerDes interfaces push PCB design to its limits, demanding precise control over vias, signal integrity, and compliance requirements. Cadence's suite of design tools—including Aurora Via Wizard, Sigrity X Topology Explorer Workbench, and Compliance Analysis Tools—empower engineers to validate designs early, optimize signal paths, and ensure adherence to protocol specifications. These capabilities reduce the need for design iterations and increase the likelihood of achieving first-pass design success.

3. DDR Memory Challenges and Solutions

Double Data Rate (DDR) memory is widely used in high-performance computing, networking, and consumer electronics. While DDR speeds are lower than SerDes, they pose unique design challenges due to their high net counts, stringent timing requirements, and mixed-signal requirements. Modern DDR interfaces, such as DDR5, now operate at multi-gigabit speeds, approaching those of lower-end SerDes devices.

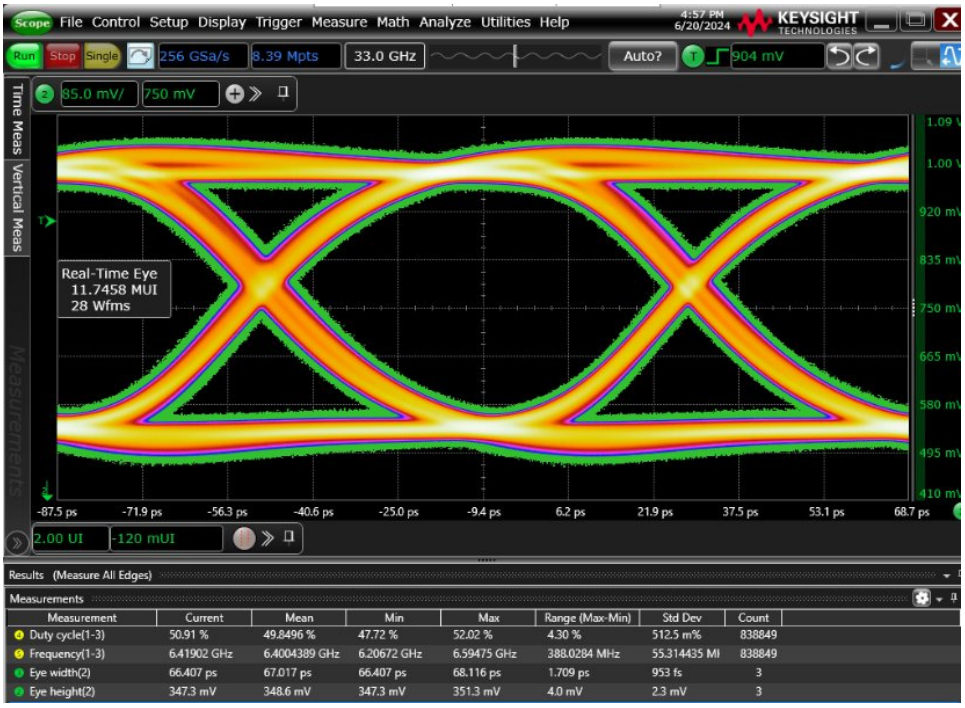


Figure 4: Cadence's 3nm silicon write eye diagram for DDR5 MRDIMM IP running at 12.8Gbps

3.1. Schematics and Constraints

DDR interfaces require precise timing alignment and impedance control to prevent data corruption. Incorrect termination, poor routing topologies, or uncontrolled impedance discontinuities can lead to ringing, overshoot, undershoot, and reflections. Timing margins are shrinking as DDR speeds increase, making setup and hold time violations more common.

The Solution: Cadence's Sigrity X Topology Explorer Workbench facilitates parameter sweeps, enabling engineers to evaluate multiple constraints and termination configurations. This capability facilitates the identification of optimal routing solutions and the early detection of timing violations, streamlining the design process and minimizing unnecessary iterations.

3.2. Signal Integrity Checks in Layout

DDR memory buses contain dozens or even hundreds of signals, including data, address, and control lines, all of which must meet strict impedance and crosstalk requirements. Layout errors can cause signal degradation, resulting in read/write failures or intermittent data corruption.

The Solution: Sigrity X Aurora streamlines DDR signal integrity verification through automated processes, including:

- **Impedance Validation:** Ensuring trace widths and reference plane configurations meet target impedance specifications.
- **Crosstalk Analysis:** Detecting high-risk trace interactions and recommending routing adjustments to mitigate interference.
- **Return Path Optimization:** Ensuring that signal traces have continuous, low inductance return paths to reduce ground bounce and enhance signal integrity.

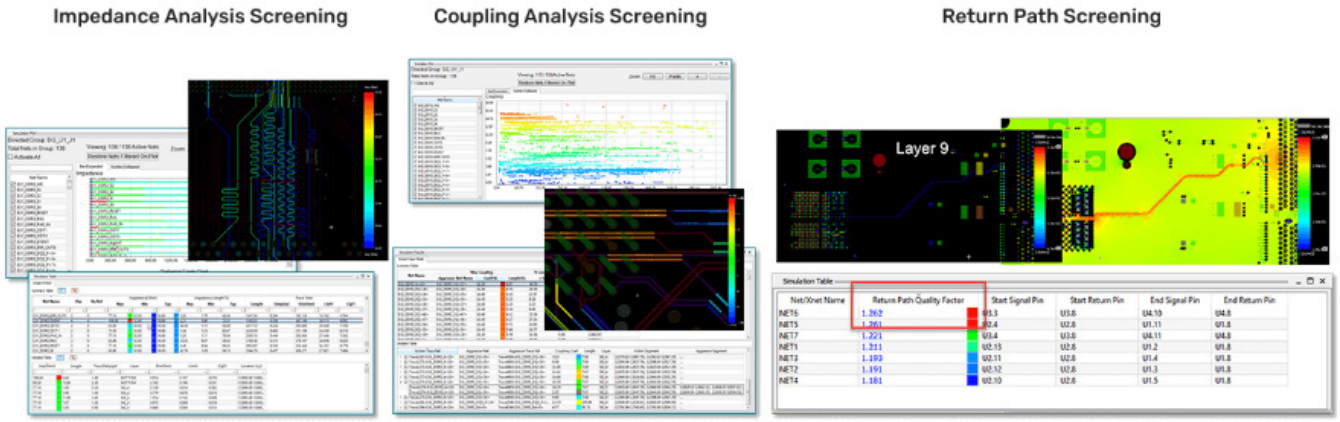


Figure 5: Signal quality in-design analysis

By integrating these verification checks directly into the layout process, Cadence's tools facilitate seamless communication between schematic and layout teams, minimizing reliance on manual debugging and iterative back-and-forth adjustments, streamlining the overall design workflow.

3.3. Simultaneous Switching Noise

When multiple DDR signals switch simultaneously—e.g., during a burst read/write operation—, the sudden demand for current can cause voltage fluctuations in the PDN. This effect, known as simultaneous switching noise (SSN) or ground bounce, can result in unstable reference voltages, increased jitter and timing violations, and degraded DDR performance at higher speeds.

The Solution: Cadence's power-aware IBIS and advanced PDN analysis tools, help engineers systematically identify vulnerabilities within the power delivery network, optimize decoupling capacitator placement for minimal power noise, and accurately simulate SSN effects. This comprehensive, power-aware methodology ensures reliable DDR memory performance, even in high-density, high-speed designs, by addressing critical power integrity challenges under real-world operating conditions.

3.4. Via-to-Via Crosstalk

High-speed DDR signals often require multiple layer transitions through vias, which can result in electromagnetic coupling between adjacent vias. This phenomenon, known as via-to-via crosstalk, can:

- Inject noise into neighboring signals, degrading read/write integrity.
- Reduce DDR timing margins, leading to errors.
- Create ground loop issues, increasing EMI susceptibility.

The Solution: Cadence's 2.5D and 3D analysis options provide precise via modeling, ensuring electromagnetic coupling effects are accounted for, design recommendations, such as via shielding techniques and optimized layer transitions, and stub reduction strategies, such as back drilling, to minimize unwanted resonances.

By incorporating 3D field solvers and crosstalk simulations, Cadence ensures that via-related interference is mitigated.

DDR memory design is becoming increasingly complex, with challenges related to timing, layout, power integrity, and crosstalk. Cadence's suite of Sigrity X Topology Explorer Workbench, signal integrity checks, power-aware IBIS modeling, and 3D crosstalk analysis tools empower engineers to:

- Identify signal integrity risks early, avoiding expensive post-layout modifications.
- Optimize PDN performance, ensuring consistent and reliable power delivery under high DDR load conditions.
- Minimize crosstalk and EMI issues, enhancing DDR system robustness and overall reliability.

Best Practices for PCB Design Engineers

To harness the full potential of in-design analysis, consider these actionable best practices:

- **Apply shift-left methodologies** to address SI/PI concerns in the schematic stage.
- **Leverage advanced visualization tools to analyze power delivery networks and identify critical issue**s such as voltage drops and excessive inductance.
- **Perform regular parameter sweeps** during the pre-layout stage to define robust design constraints that will guide the entire development process.
- Ensure high-speed interface designs, such as SerDes and DDR, meet performance standards by conducting **protocol-specific compliance checks** to validate and optimize functionality.

The Cadence Advantage

Cadence offers a unified suite of tools that integrate seamlessly into the PCB design flow, from schematic to signoff:

- **Allegro® X Design Platform** for layout design with integrated SI/PI checks
- **Sigrity X Platform** for distributed computing and advanced power analysis
- **Sigrity X Aurora Via Wizard** and **Sigrity X Topology Explorer Workbench** for parameter sweeps and optimization
- **Clarity™ 3D** Solver for detailed electromagnetic analysis

Cadence equips engineers with practical, efficient solutions to tackle SI/PI challenges and achieve faster, more reliable signoff.

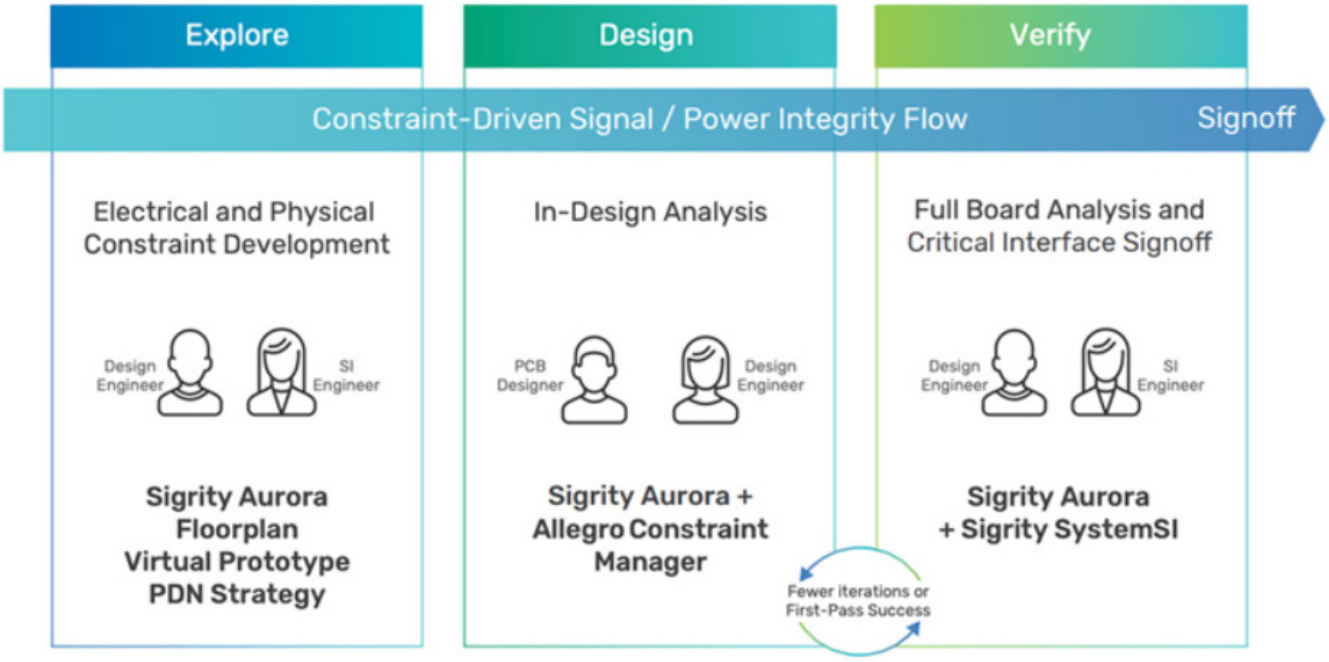


Figure 6: Seamless integration of Sigrity and Allegro environments enables engineers to identify and fix signal and power issues in real-time, reducing costly re-spins.

Conclusion

Signal integrity and power integrity are no longer afterthoughts to be addressed at signoff; they are critical aspects of the entire PCB design process. Cadence's in-design analysis tools empower PCB design engineers to take charge of SI and PI challenges early.

By shifting left, leveraging distributed computing, and simplifying complex concepts, electrical engineers can achieve faster, more accurate designs while reducing dependency on other experts. By shifting left, leveraging distributed computing, and simplifying complex concepts, electrical engineers can achieve faster, more accurate designs while reducing dependency on other experts. Our solutions bridge the gap between speed and accuracy, ensuring seamless SI/PI signoff for PCB designs.

To find out how Cadence's solutions can streamline your PCB design process with unmatched speed and accuracy *request a free trial here.*

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