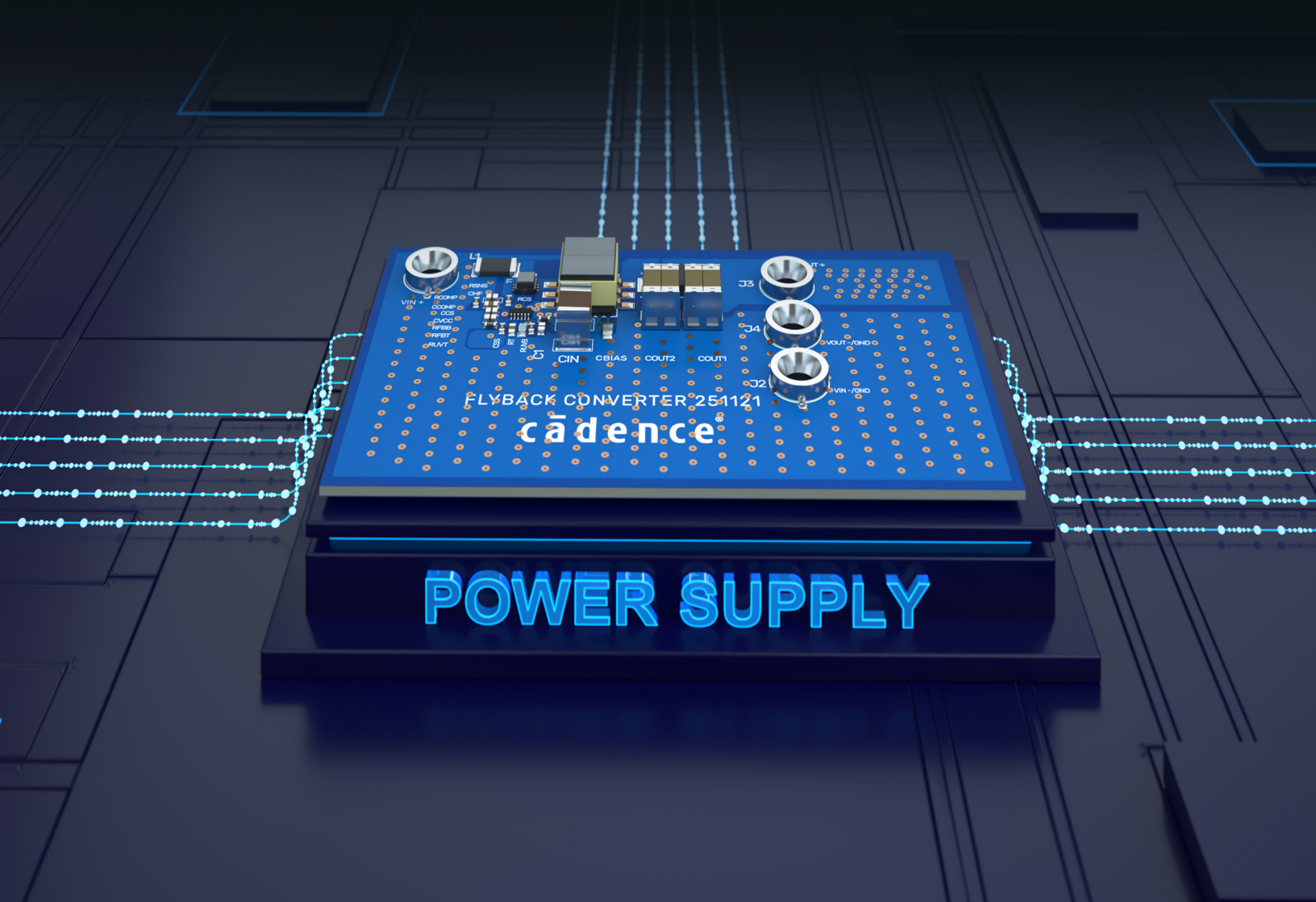
DESIGN **GUIDE**

cadence®

# Power Supply Design Guide 1: DC-DC Non-Isolated Flyback

LM5156-Q1 | 12 V  5 V / 2 A | Non-Isolated



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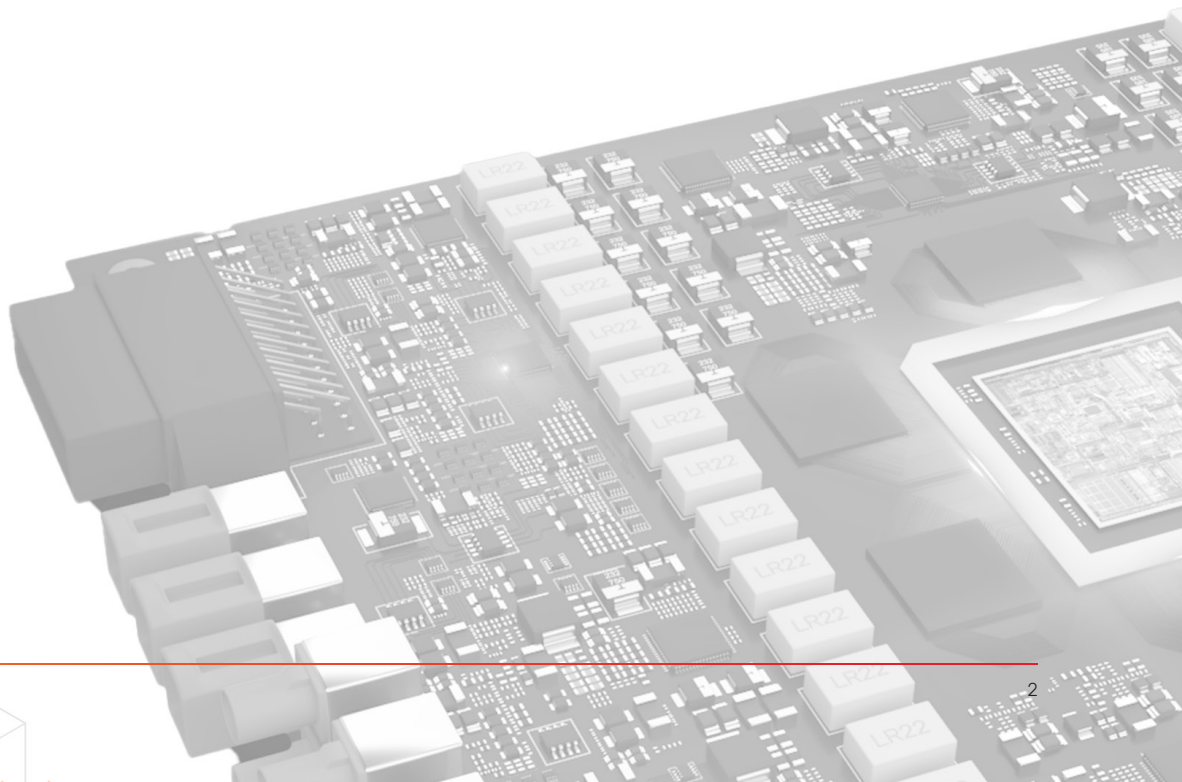


## Introduction

This guide breaks down the four phases of creating a working flyback converter: electrical design, transient simulation, loop stability, and PCB layout. We'll focus on the decisions that matter and the mistakes that can cost you a dead or noisy board.

Our target specifications:

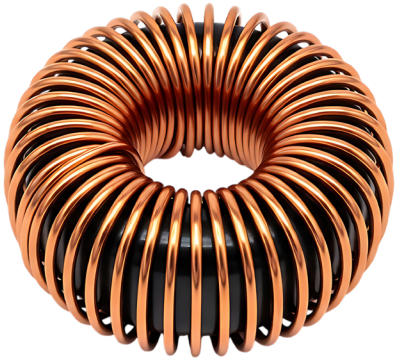
- **Input:** 9–36 V (nominal 12 V)
- **Output:** 5.00 V / 2 A
- **Controller:** LM5156-Q1
- **Switching frequency:** ~250 kHz
- **Topology:** Non-isolated flyback

**Note:** For human-touch applications, use an isolated flyback. The methods shown here transfer directly.

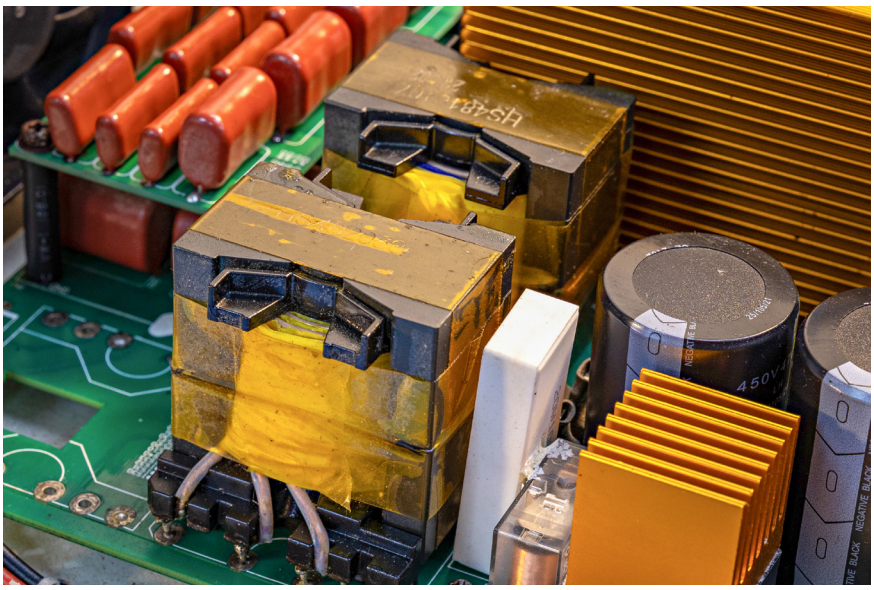
## Phase 1: Electrical Design

### The Physics You Can't Ignore

A flyback isn't a transformer in the classical sense. It's a coupled inductor that stores energy when the switch is ON and dumps it to the output when the switch is OFF.



*Inductor*

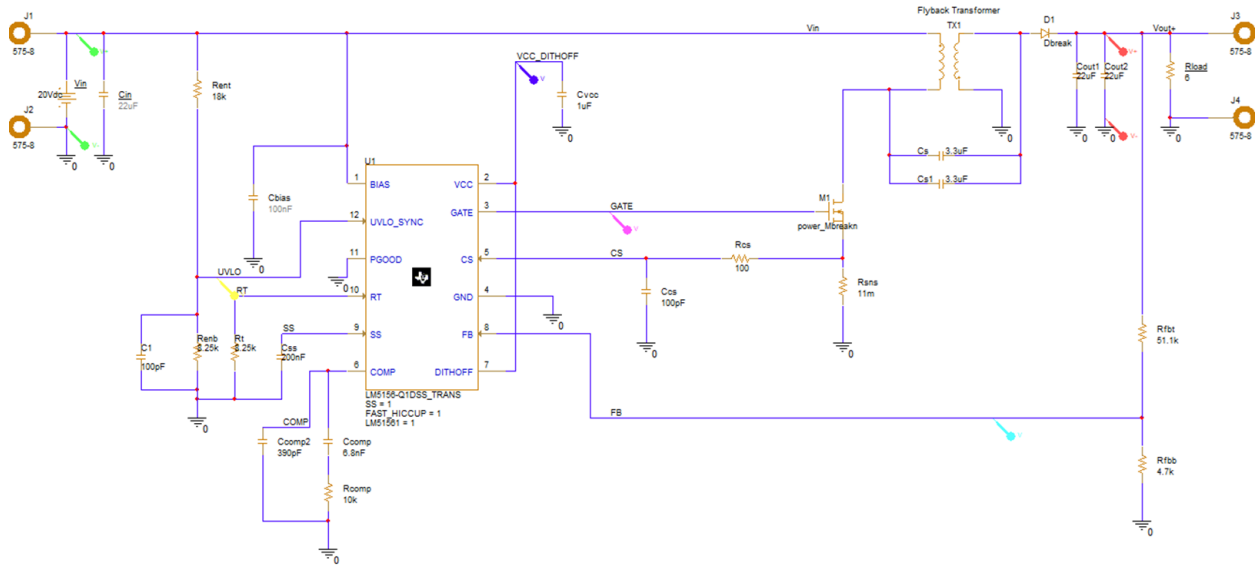


*Transformer*

Two current loops dominate your EMI performance:

- **Primary hot loop:** VIN cap → MOSFET → transformer primary → back to cap
- **Secondary hot loop:** Transformer secondary → Schottky → output caps → back

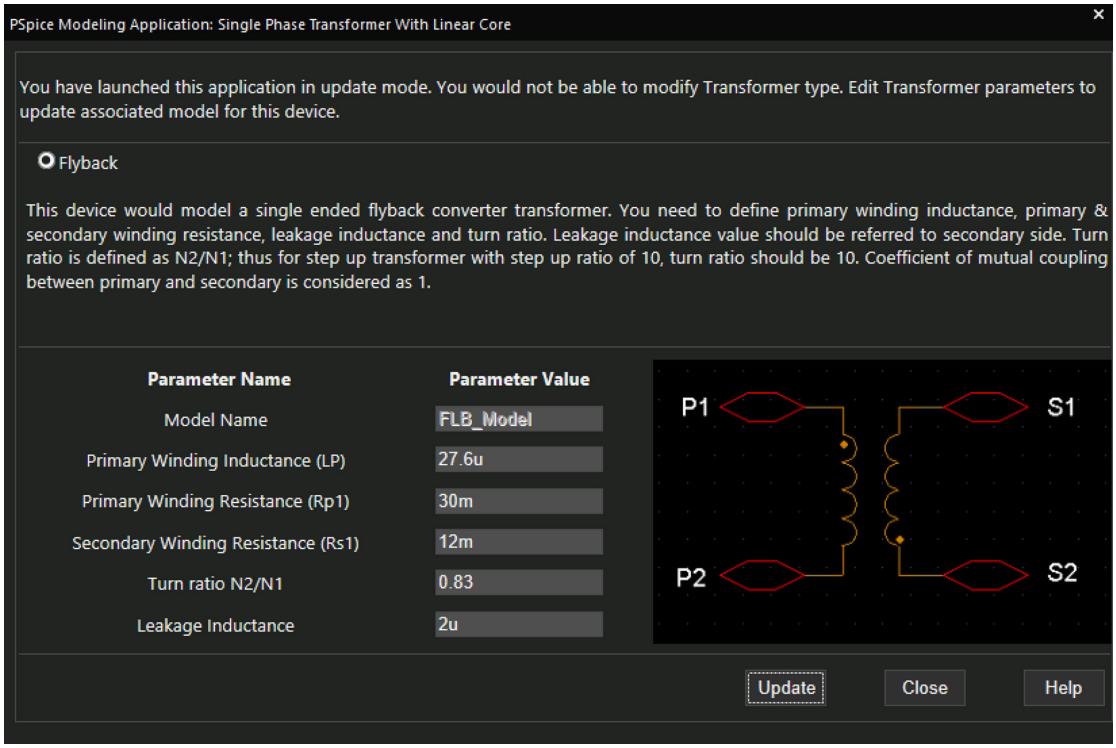
Make these loops tiny. Everything else is secondary.




*Flyback Converter (Non-isolated) Schematic in Allegro X*

## Key Sizing Decisions

**Switching frequency (~250 kHz):** Higher frequency means smaller magnetics but more switching loss. 250 kHz is the sweet spot for this power level (10 Watts).




*PSpice Modeling Application - Single Phase Transformer with Linear Core*

We're designing the transformer using the following specifications:

Primary Inductance *Lm ≈ 27.6 µH with Secondary Turns over Primary turns ratio (Ns/Np) ≈ 0.83 to 1.10 range.*

Leakage inductance modeled at 1–2 µH. These values were derived from design resources and manual calculations. You can then iterate in simulation. Expect the first set of conditions not to be right.

FB divider: 30 kΩ / 7.50 kΩ gives us the 5.00 V setpoint by dropping the 5V down to 1.0V. Double-check this math; a wrong divider is the #1 cause of "it regulates to the wrong voltage."

Soft-start cap: We use 22 nF for fast simulation (~5 ms ramp). Real applications often need 100+ nF for proper inrush control.

Rsns (current sense): 20 mΩ in this design. Must be Kelvin-sensed, more on that in Phase 4.

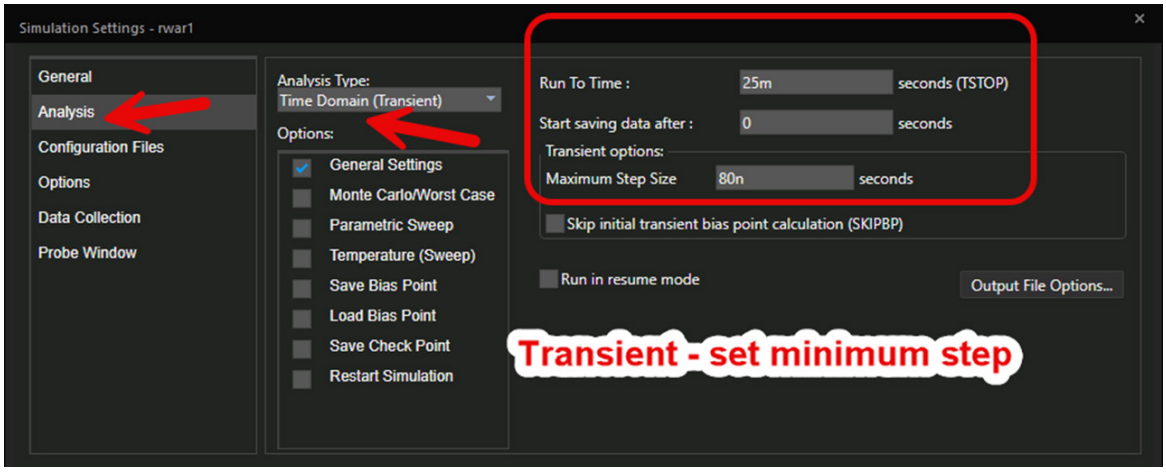
### What Can Go Wrong Here

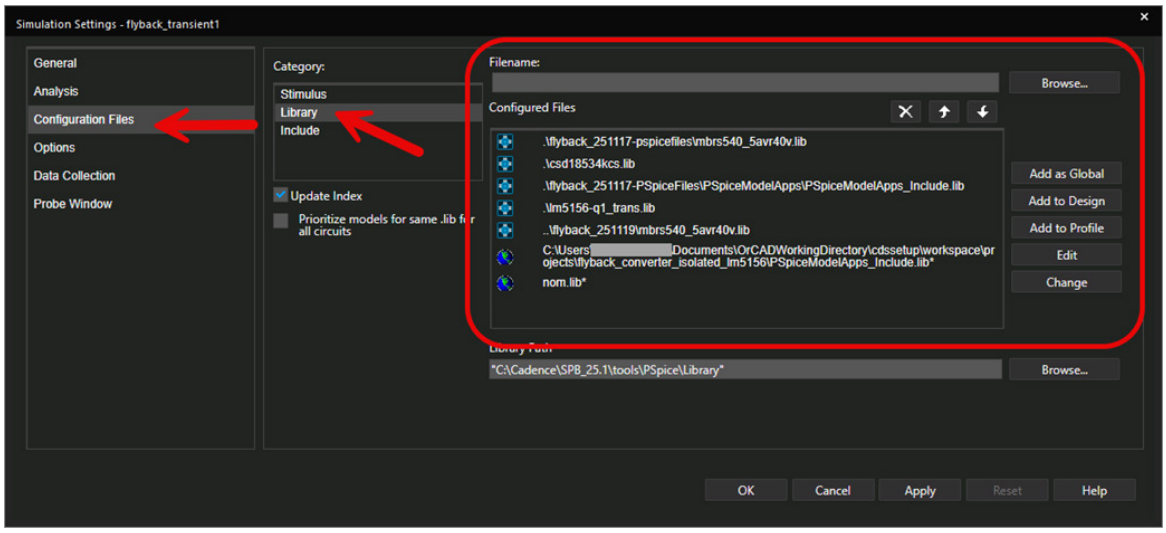
- Transformer saturation: If Lm is too low or the peak current too high, the core saturates. You'll see the current runaway in the simulation.
- Wrong output voltage: Almost always the FB divider. Recalculate it.
- MOSFET stress: VDS sees input voltage plus reflected secondary voltage. Add a 30% margin to your rating.

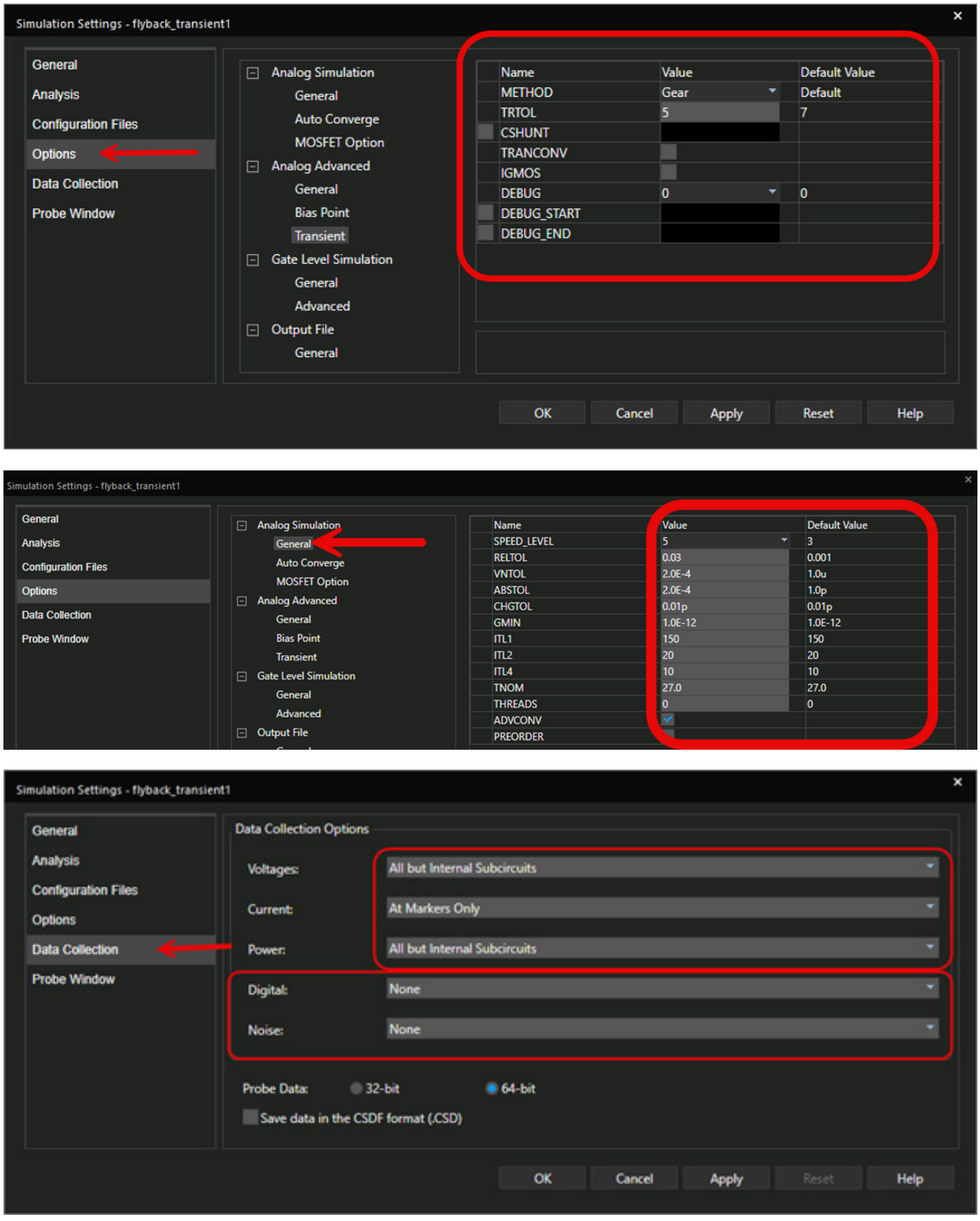
## Phase 2: Transient Simulation

### Settings That Actually Matter

Bad settings yield smooth, visually appealing waveforms that mask actual issues. Here's what to use:






*SPICE Simulation Settings for faster simulation*

| Parameter | Value | Why |
|---|---|---|
| TSTOP | 12-20ms | Covers startup + settling |
| TSTART | 0 | Cold start, no cheating |
| MAXSTEP | ≤50-80 ns | Critical. Catches switching edges |

**MAXSTEP is the one people get wrong.** At 250 kHz, your switching edges happen in tens of nanoseconds. Set MAXSTEP too large and the simulator steps right over the interesting stuff—you'll see wrong peak stresses and unrealistic ripple.

### What "Good" Looks Like

During startup (0–5 ms):

- VOUT rises with soft-start, slight overshoot OK if it damps in <1 ms
- FB voltage glides to ~1.000 V and locks there
- Gate duty cycle ramps up, then stabilizes
- CS (current sense) shows clean triangular ramps, no saturation

At steady state (8+ ms):

- VOUT ripple: tens of mV (we're using 2× 220 µF output caps)
- FB flat at 1.000 V
- Duty cycle stable, no hunting

Primary stress check:

- Look at the DRAIN voltage during the first few switching cycles
- Spikes should be <80% of MOSFET rating
- Some ringing is normal; heavy ringing means your snubber needs work

### The Mistake That Wastes Hours

Earlier iterations of this design were regulated to ~4 V instead of 5 V. The root cause was two-fold. Reason 2 bigger than the first.

Reason 1: The output caps were 220 nF instead of 220 µF (1000× too small). The loop couldn't compensate for the massive ripple.

Reason 2: Incorrect calculation of the feedback resistors (Rfbt and Rfbb). They were originally forcing voltage to reference 4 V instead of 5V.

Lesson: Verify your component values match the schematic, especially when copying and pasting components for quick schematic capture. Also double check that feedback voltage divider circuit three times.

## Phase 3: Loop Stability (AC Analysis)

### Skip the Math, Focus on the Result

You need to know two things from your Bode plot:

1. Bandwidth (crossover frequency): How fast can the loop correct errors? This happens at the frequency where gain crosses 0 dB.
2. Phase margin: Your safety buffer against oscillation. Measure the phase at the crossover frequency and add 180°. Aim for a margin of 50–60° to ensure stability. If the phase shifts 180° out of sync, the system could increase duty cycle when it should decrease, or vice versa, potentially causing device failure in a few milliseconds.

### In simple terms:

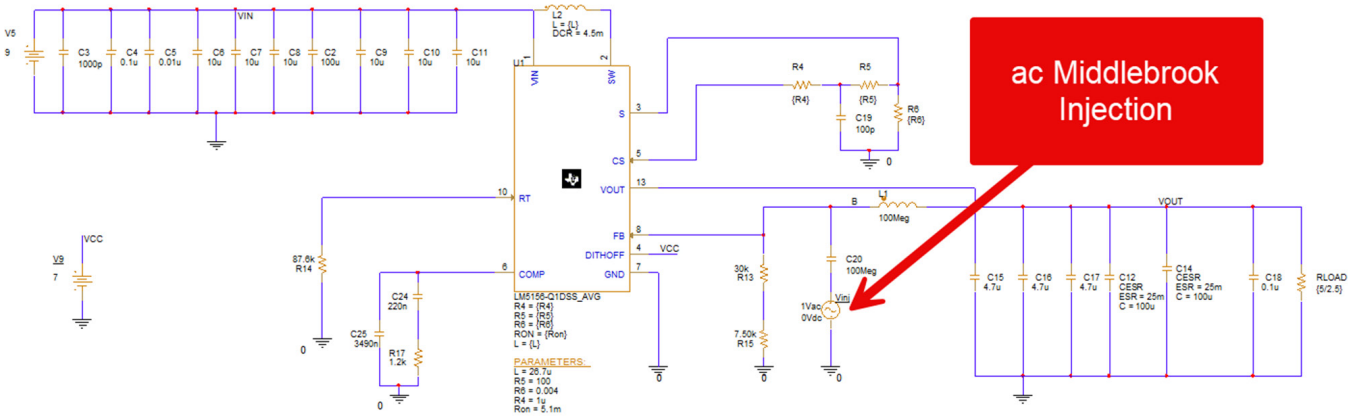
- Bandwidth = responsiveness. Higher = faster recovery from load steps.
- Phase margin = stability buffer. Below 30° and you'll see ringing. Negative means oscillation.

## The Middlebrook Injection Trick

To measure loop gain without disturbing DC operation:

First the setup:

Use the AC averaged PSpice model of the device if you can grab it (Manufacturer's website). Set up the circuit to handle that model. You don't need to model direct switching. Your circuit will look different from the transient version.

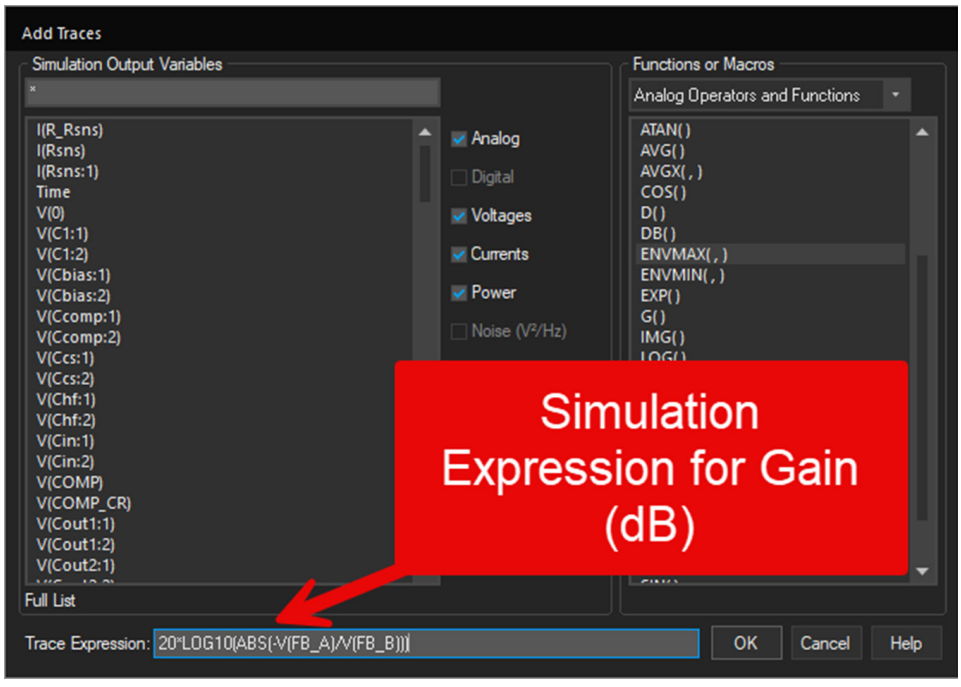


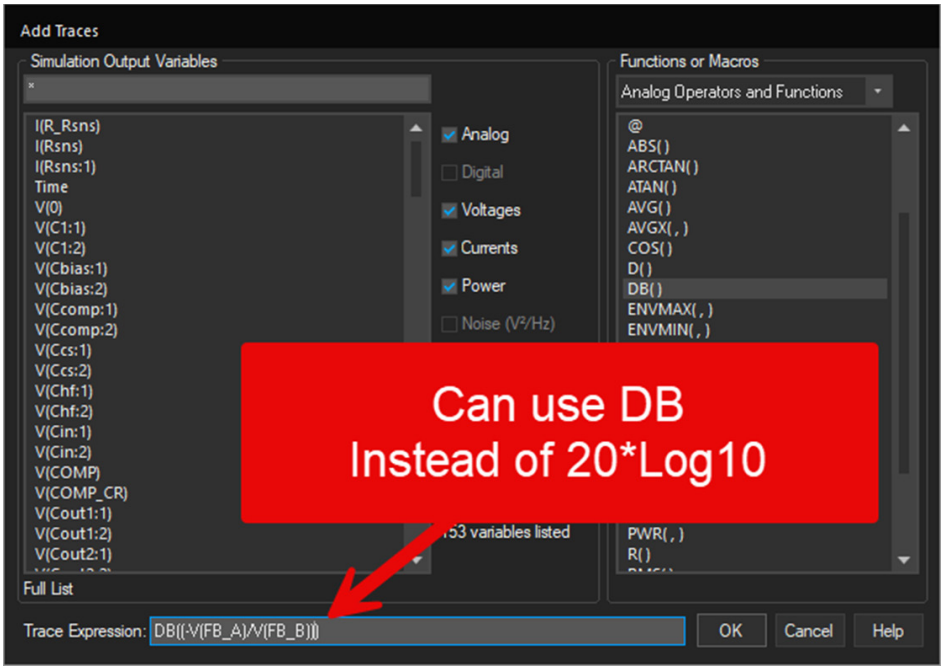

*PSpice ac averaged Model Circuit Schematic of Flyback*

With the circuit set up using the averaged model, we do the following:

1. Insert a small AC source in the FB path
2. Add a huge inductor in series (1 Meg) between the FB pin and Vout, to pass DC
3. Add a huge resistor in parallel (1 Giga) as backup OR
4. Add a huge capacitor in series with the ac injection (100Meg)
5. Sweep 10 Hz to 1 MHz, measure return signal vs. injection

The expressions in PSpice:



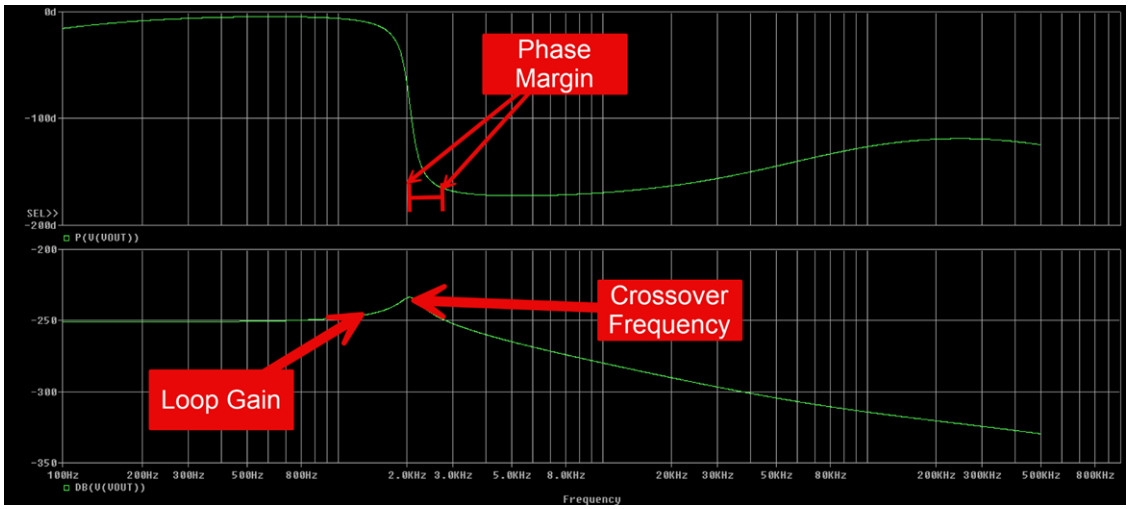



*PSpice expression input for Gain and Phase*

Gain (dB): 20*LOG10(ABS(-V(FB_A)/V(FB_B)))

Phase (deg): P(-V(FB_A)/V(FB_B))

## What You're Looking For




- **Phase margin ≥ 45°** — gives you a clean load step response (one or two lobes, then settles)
- **Gain margin ≥ 10 dB** — headroom against parameter variation
- **Crossover well below switching frequency** — rule of thumb: fc < fsw/5

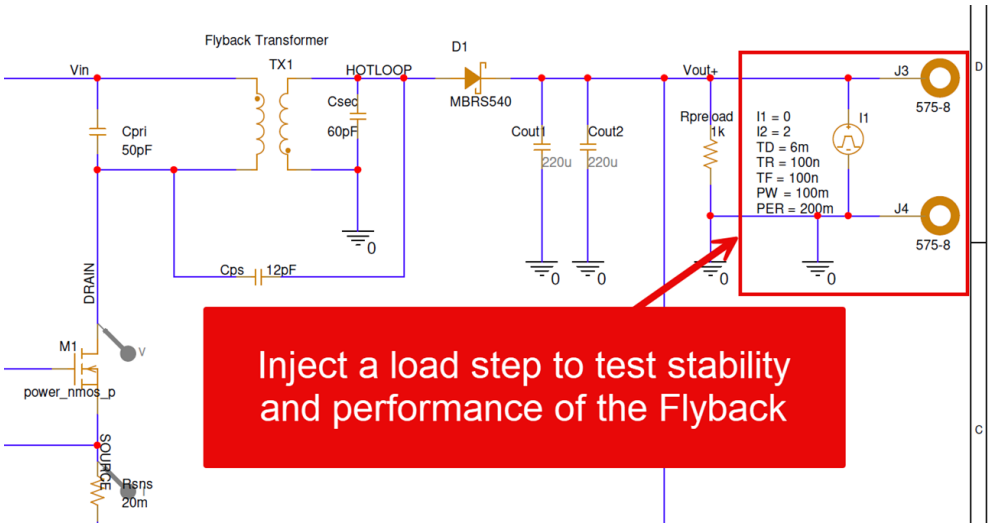
### The Flyback's "Wrong-Way" Problem (RHP Zero)

Here's something unique to flybacks: when the duty cycle increases, output voltage can initially dip before rising. Why? Energy only transfers to the secondary when the switch is OFF. More ON-time means less OFF-time right now, even though you're storing more energy.

This "wrong-way" response shows up as a right-half-plane zero in your transfer function. The practical fix: keep your crossover frequency well below where this zero lives. For this design, that's not a problem at our relatively narrow bandwidth of a few kHz.

### Design Review

After AC analysis, run a load step (0.2 A → 2 A). A good margin is characterized by a small dip and quick settling. A bad margin is indicated by ringing that lasts for milliseconds.



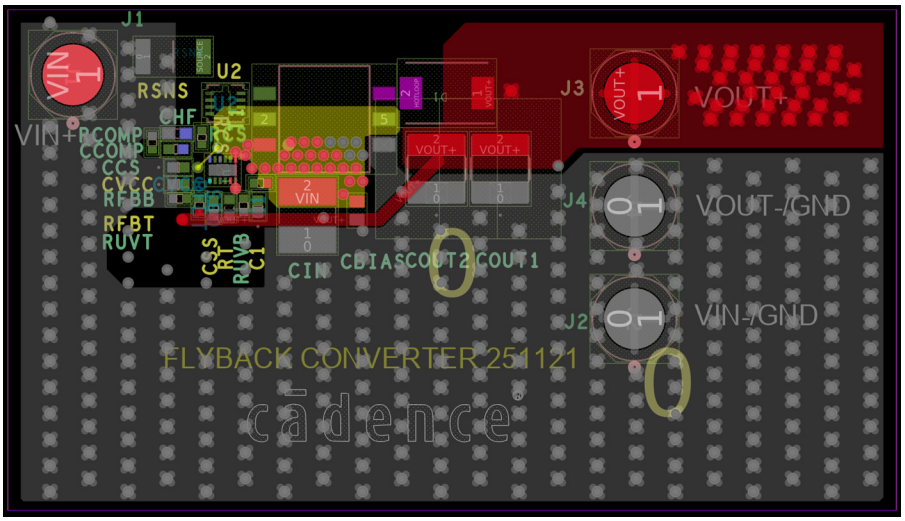

*Ringing for the circuit in response to a 2 Amp load step. Shaky Stability/Underdamped*

## Phase 4: PCB Layout

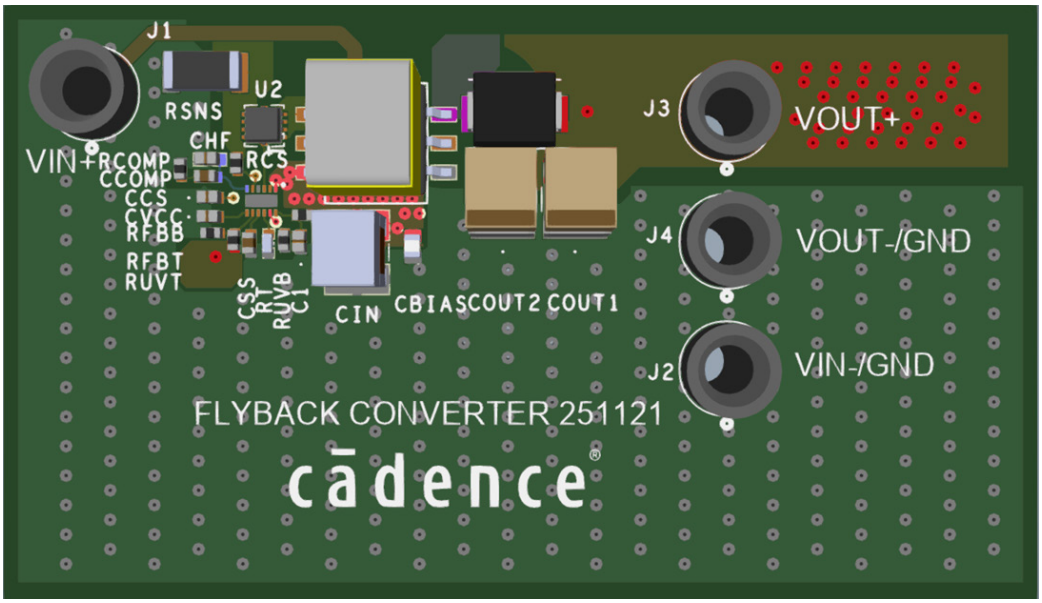
This is where theory meets copper. A perfect schematic with a bad layout will fail EMI, run hot, and maybe not even regulate.

### Hot Loop #1: Primary Side

**Goal:** Minimize the area of: VIN cap → MOSFET drain → transformer primary → back to cap.




*PCB Layout of Flyback Converter (Non-Isolated)*




*PCB Layout (corrected)*

How to get it right:

- Place input ceramic caps (not just bulk electrolytic) right at the MOSFET
- Orient transformers so the primary pins are close to the MOSFET drain
- Use copper pours, not skinny traces
- Snubber goes right at the drain node, not inches away

What happens if you don't: Voltage spikes on DRAIN exceed rating. High-frequency ringing radiates EMI. Snubber doesn't snub.

## Hot Loop #2: Secondary Side

Goal: Keep transformer secondary → Schottky → HF output caps → back as tight as possible. Aim for <10 mm total loop perimeter.

How to get it right:

- Schottky immediately adjacent to transformer secondary pins
- Small ceramics (100 nF, 1 µF) form the HF return path
- Bulk caps (220 µF) come after the HF caps
- Use a local copper island, stitch it to the ground with vias

What happens if you don't: Diode voltage overshoot. Reverse recovery ringing. Output noise.

## Kelvin Sensing: The #1 Layout Mistake

Your 20 mΩ Rsns is measuring current by its voltage drop. If power return current flows through your sense traces, you're measuring trace drop + Rsns drop—and your current limit is now wrong.

The fix:

- Two separate trace pairs: power path vs. sense path
- Sense traces go directly from the Rsns pads to the CS and GND pins on the IC
- No shared copper between power and sense
- Keep sense trace lengths matched within 2 mm

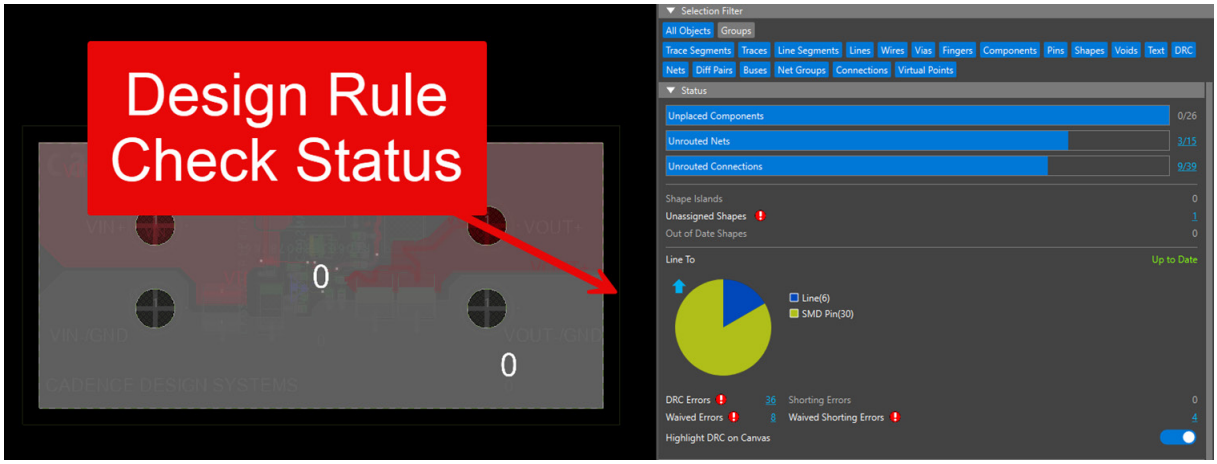
### FB/COMP Section: Keep It Quiet

The FB and COMP nodes are high-impedance analog. They'll pick up every bit of noise you let them hear.

- Keep FB/COMP/RT components ≥0.8 mm from any SW (switching noise) copper
- Don't route FB over plane voids or splits
- Guard with ground copper
- Use single-point returns to the IC's GND pin (i.e., don't share ground vias)

## Creepage and Clearance

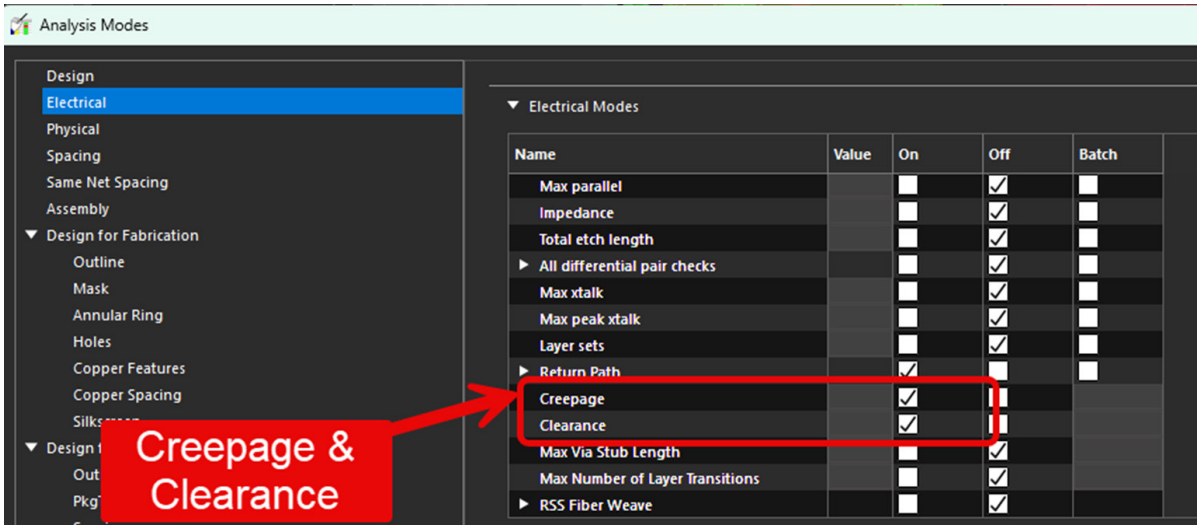
Even though this is non-isolated, you still need spacing rules for noise immunity and (if applicable) safety.




*PCB with DRC violations*

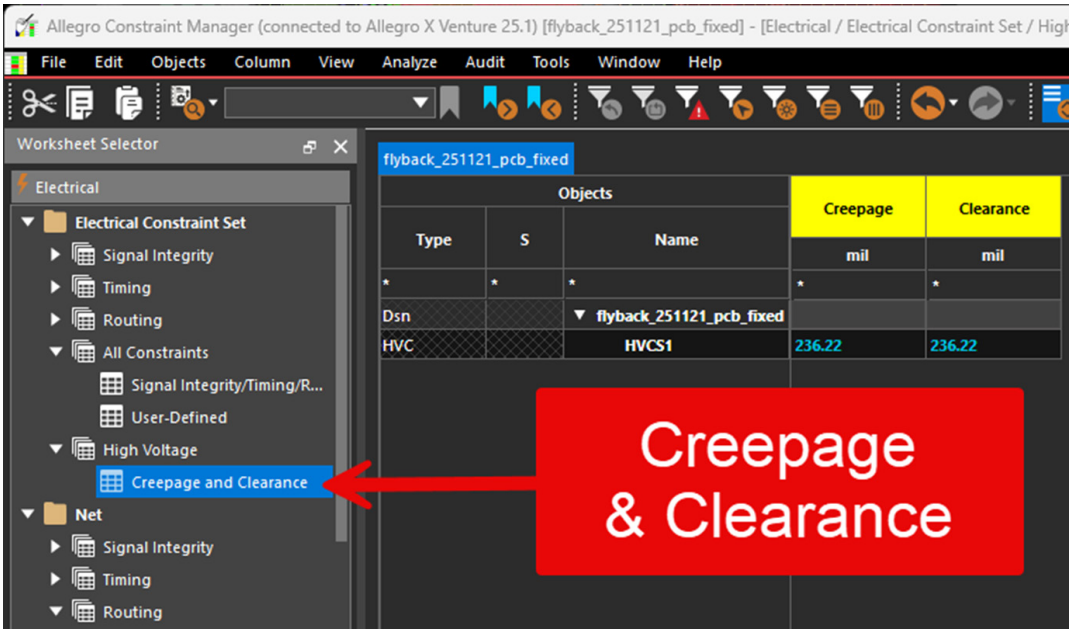
Our example uses 6 mm as a demo threshold. In Allegro X Venture:

1. Setup → Constraints → Constraint Modes — find Creepage and Clearance options
2. Set your values (e.g., 6 mm creepage, 6.5 mm clearance)
3. Create a voltage constraint set under Electrical → Creepage and Clearance



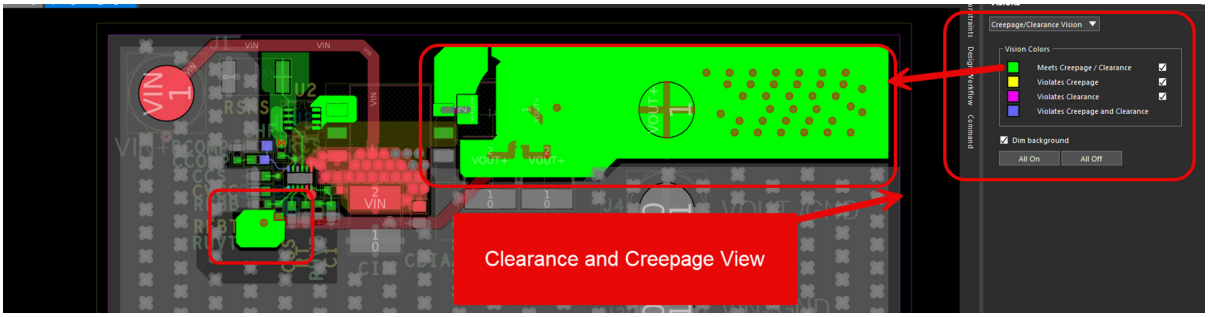

*Turn on Creepage and Clearance First in Constraint Modes*

4. Assign your hot loop nets to this constraint set
5. Run DRC — violations show up immediately




*Constraint Manager dialog*

The Vision Manager in Allegro X enables you to visualize what meets or violates your rules at a glance. Green indicates compliance, while highlighted areas signal the need for fixes.




*Creepage and Clearance Vision*

If you need more creepage, add a routed slot (board cutout) between primary and secondary. A 2 mm slot effectively doubles your creepage distance.

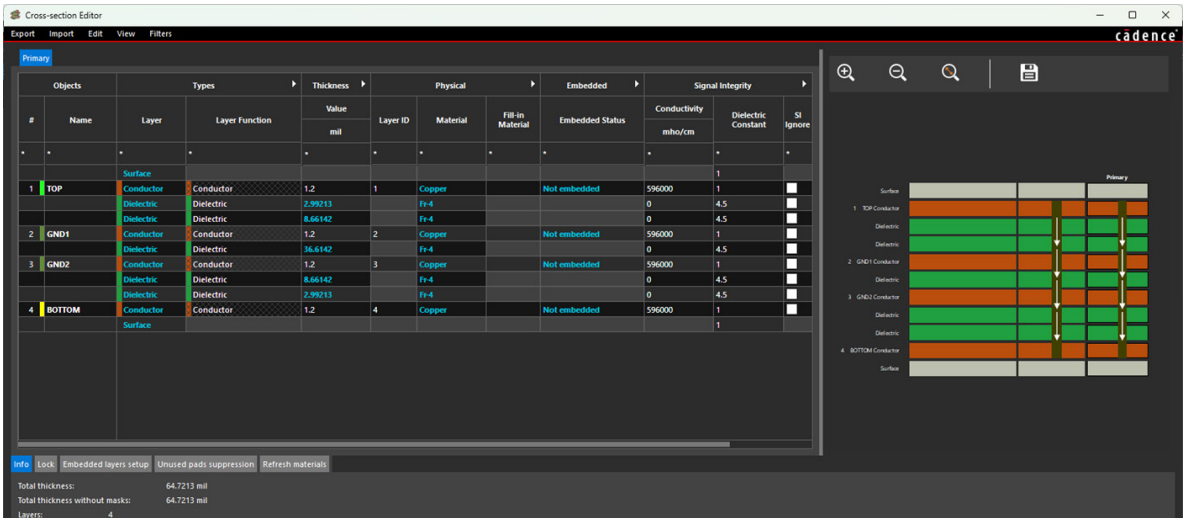
**Important:** 6 mm is an example. Follow your actual safety standard (IEC 62368-1, UL, etc.).

## Layer Stackup (4-Layer)

Let's use a good stack up for EMC (below).

| Layer | Use |
|---|---|
| L1 (Top) | Components, hot loop copper islands |
| L2 | Solid GND plane (no splits under analog) |
| L3 | Solid GND plane (no splits anywhere) |
| L4 (Bottom) | Remaining Traces, hot loop copper |

We want the inner layers to both be ground so we maximize capacitive coupling, minimize copper inductance and sink maximum current and maximize heat removal where needed.




*PCB stackup for reference design PCB layout in Allegro X*

Keep L2 and L3 solid under the LM5156 and FB network. If you split or void any areas of the GND planes, you're at risk of creating noise underneath sensitive nodes and components.

## Quick Checklist

Before You Simulate the Schematic, check the following:

- [ ] FB divider gives correct VOUT (30k/7.5k  5.00 V)
- [ ] Output caps are µF, not nF
- [ ] MAXSTEP ≤ 80 ns
- [ ] Transformer model has realistic leakage

### Before You Send to Fabrication

- [ ] Both hot loops are visibly small on the layout
- [ ] Rsns is Kelvin-sensed (check trace routing)
- [ ] Snubber is at the drain node, not remote
- [ ] FB/COMP traces don't cross SW or plane voids
- [ ] Creepage/clearance rules are set, and DRC is clean
- [ ] Thermal vias under MOSFET, diode, and Rsns

## Common Failure Modes

| Symptom | Likely Cause | Fix |
|---|---|---|
| Regulates to the wrong voltage | FB divider values | Recalculate 30k/7.5k ratio |
| Random overcurrent trips | Rsns not Kelvin-sensed | Fix sense trace routing |
| Excessive DRAIN spikes | Hot loop too large | Tighten primary loop, add/tune snubber |
| Oscillation or ringing | Low phase margin | Adjust Ccomp/Rcomp, verify layout |
| Runs hot | Insufficient vias, poor thermal path | Add thermal via field |

## Reference

### Probe expressions for AC analysis:

Gain: 20*LOG10(ABS(-V(FB_A)/V(FB_B)))

Phase: P(-V(FB_A)/V(FB_B))

### Net classes to define:

- HOT_LOOP_PRI — primary switching loop
- HOT_LOOP_SEC — secondary switching loop
- FEEDBACK — FB, COMP, RT network
- SENSE — Rsns Kelvin traces

### Key component values:

- Lm: 27.6 µH
- Ns/Np: 1.10
- Rsns: 20 mΩ
- FB divider: 30 kΩ / 7.50 kΩ
- Ccomp: 220 nF
- Chf: 3490 pF
- Rcomp: 1.2 kΩ

*LM5156-Q1 flyback reference design. PSpice project and PCB database available in supplemental files.*

## Frequently Asked Questions -

### Can I use a buck converter with isolation?

No—buck converters are inherently non-isolated. If you require isolation with step-down behavior, use a forward converter, which is essentially a transformer-isolated buck converter. For lower power (<150W) and lower current (<10A), flyback is often a more straightforward and cost-effective solution.

### When should I use a SEPIC instead of a buck-boost converter?

Use SEPIC when you need a non-inverted output and your input voltage crosses above and below your output voltage. Buck-boost inverts the output polarity, which can complicate system design. SEPIC adds complexity (two inductors or a coupled inductor plus a coupling capacitor) but eliminates the polarity problem.

### Why is flyback so popular for USB-C chargers?

USB-C chargers typically need: (1) isolation from mains, (2) power levels of 20–100W, and (3) output currents well under 10A. Flyback hits all three requirements while being the simplest and most cost-effective isolated topology. No separate output inductor is needed since the transformer stores energy, and the circuit supports multiple output voltages (important for USB-PD negotiation).

### What's the difference between flyback and forward converter transformers?

The fundamental difference is **where energy is stored:**

- **Flyback:** The transformer itself stores energy (requires an air gap in the core).
- **Forward:** The transformer only transfers energy (no air gap); a separate output inductor stores energy.

This is why forward converters have a higher part count but can achieve higher efficiency and handle higher output currents.

### Why did desktop PC power supplies move to LLC resonant?

Efficiency regulations (80 Plus certification) and thermal constraints drove the shift. LLC resonant achieves zero-voltage switching, which dramatically reduces switching losses at the high power levels (300W–1000W+) that modern desktop PSUs deliver. The complexity and cost are justified by the efficiency gains and reduced cooling requirements. Note that the 5V standby rail still typically uses a flyback, as it's always on at low power.

### How do I know if my design needs simulation?

Short answer: It always does. Even for "simple" buck converters, simulation identifies problems that calculations may miss, including transient response, worst-case efficiency, switch stress at startup, and thermal behavior. For isolated topologies—especially flyback and LLC resonant—simulation is essential for magnetics design, snubber optimization, and control loop stability. Build time on the bench is expensive; simulation time in PSpice is cheap.