DESIGN **GUIDE**

cadence®

Designing HDI in Allegro X

The Complete Workflow Guide from Stackup to Signoff

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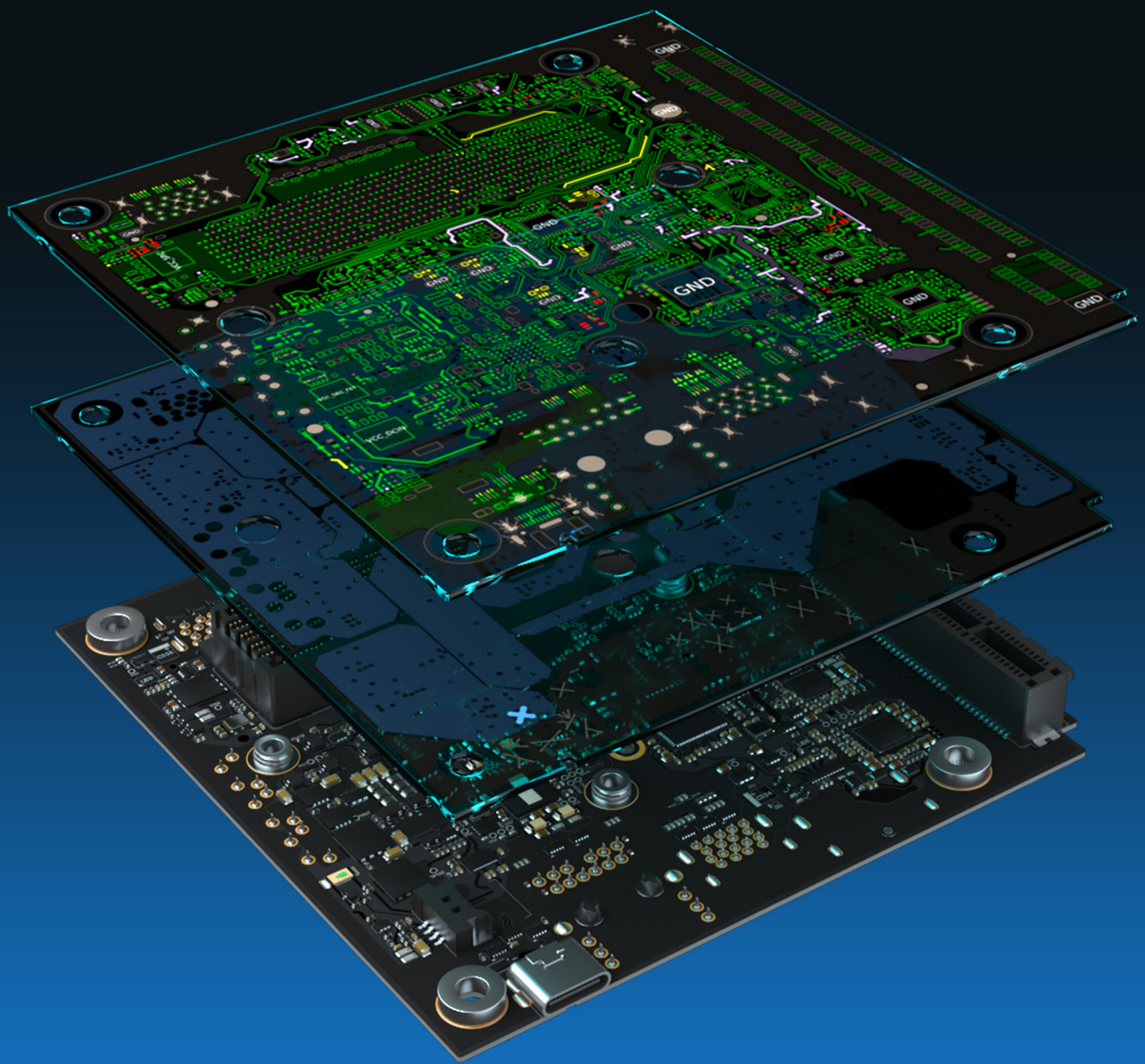
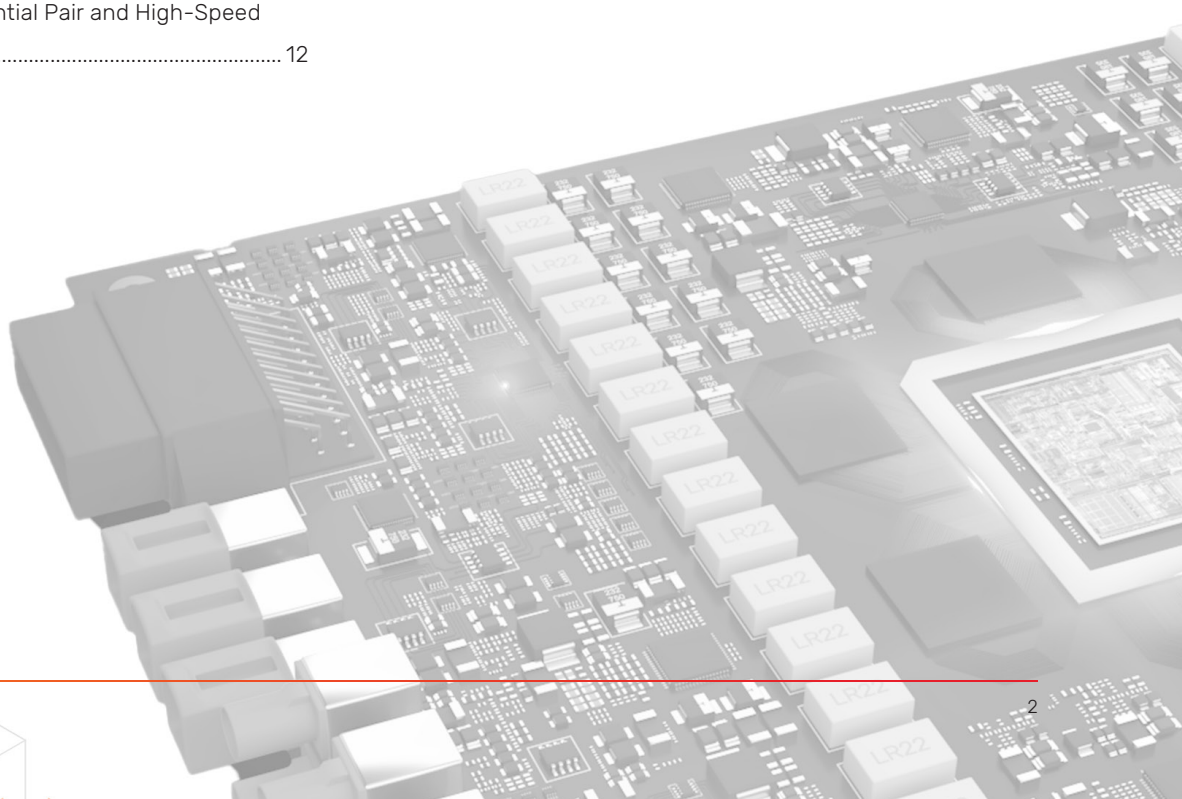


Contents



1. Project Setup for HDI in Allegro X

HDI design success begins before the first component is placed. It starts with proper project setup, which involves establishing the right constraint environment, preparing HDI-capable libraries, and configuring via structures. These actions prevent the constraint violations and DRC errors that plague designs where HDI was retrofitted rather than being planned.

This section walks through the project setup workflow for HDI designs in Allegro X, establishing the foundation that subsequent chapters build upon.

1.1 HDI-Specific Constraint Environments

The Constraint Manager in Allegro X provides the framework for defining design rules that govern HDI layouts. Before beginning layout, establish constraint classes that reflect your HDI capabilities and requirements.

Physical Constraint Sets for HDI

Create physical constraint sets that define the trace width, spacing, and via rules appropriate for each routing region:

- BGA_FINE_PITCH: For routing directly beneath fine-pitch BGAs (0.4-0.5mm). Minimum trace width (e.g., 3 mil), minimum spacing (e.g., 3 mil), microvia-only via list.
- BGA_ULTRA_FINE: For 0.35mm and finer pitch regions. Sub-3-mil geometries if your fabricator supports them.
- HDI_STANDARD: For general HDI routing outside BGA footprints. Relaxed width/spacing (4-5 mil) with HDI via options.
- CONVENTIONAL: For board regions using through-hole vias. Standard fabrication rules.

Assign these constraint sets to appropriate regions or net classes. BGA escape routes use the fine-pitch constraints; signals transition to standard HDI or conventional constraints as they route away from dense regions.

Spacing Constraints for HDI Geometries

HDI designs require attention to spacing rules that conventional designs may overlook:

- Via-to-via spacing: Minimum distance between microvia pads. Fabricator-dependent; typically 6-8 mils for standard HDI capability.
- Via-to-trace spacing: Often tighter than via-to-via due to the smaller cross-section of traces.
- Drill-to-copper: Critical for mechanical via registration. Laser-drilled microvias allow tighter drill-to-copper than mechanically-drilled vias due to better positional accuracy.
- Pad-to-pad spacing: Soldermask web requirements between pads, particularly for via-in-pad configurations where BGA pads and via pads overlap.

1.2 Library Preparation for Microvia Padstacks and VIP

HDI designs require padstack definitions that conventional libraries may not include. Before beginning layout, verify that your padstack library contains the microvia, blind via, and via-in-pad structures your design requires.

Microvia Padstack Structure

A microvia padstack definition includes:

- Drill diameter: Typically 4-6 mils for production HDI. Verify against fabricator capability and aspect ratio limits.
- Capture pad (top): Pad on the entry layer. Size depends on drill diameter plus required annular ring (typically drill + 4-6 mils diameter).
- Target pad (bottom): Pad on the landing layer. May be the same size as the capture pad or slightly smaller depending on the laser drilling process.
- Layer span: Defines which layers the microvia connects. A Layer 1-2 microvia only exists on layers 1 and 2.
- Plating type: Filled (for stacked configurations or via-in-pad) or conformal (for staggered configurations).

Via-in-Pad (VIP) Considerations

Via-in-pad configurations place vias directly within BGA or component pads, eliminating the fan-out trace that would otherwise consume routing space. VIP padstacks require:

- **Filled via specification:** VIP vias must be filled and planarized to provide a flat surface for solder joint formation.
- **Pad size matching:** The via's capture pad must fit within the BGA pad. For fine-pitch BGAs, this may require smaller via and pad sizes than standard microvia definitions.
- **Fill and cap attributes:** Fabrication notes should specify fill material (typically copper or conductive epoxy) and cap plating requirements.

Create a complete set of microvia padstacks covering all layer pairs in your stackup before beginning layout. Attempting to create padstacks mid-design leads to inconsistencies and potential DRC issues.

2. Building a HDI Stackup

The Cross-Section Editor is the central location for defining your board's physical structure. For HDI designs, this tool controls not just layer sequence and materials but also the via structures permitted between each layer pair, which are the rules that make HDI possible.

2.1 Defining Dielectric Layers, Materials, and Copper Weights

Begin by defining the complete layer structure from top to bottom. For each layer, specify:

Objects		Types		Thickness	Physical	
#	Name	Layer	Layer Function	Value mm	Layer ID	Material
*	*	*	*	*	*	*
		Surface				
		Dielectric	Dielectric	0.018		Soldermask
1	TOP	Conductor	Conductor	0.038	1	COPPER 38UM...
		Dielectric	Dielectric	0.069		EM-370(Z)-15 ...
2	L2	Plane	Plane	0.023	2	COPPER 23UM...
		Dielectric	Dielectric	0.076		EM-370(Z)-15 ...
3	L3	Conductor	Conductor	0.023	3	COPPER 23UM...
		Dielectric	Dielectric	0.076		EM-370(Z)-15 ...
4	L4	Plane	Plane	0.038	4	COPPER 38UM...
		Dielectric	Dielectric	0.06		EM-370(Z)-15 ...
5	L5	Conductor	Conductor	0.03	5	COPPER 1OZ
		Dielectric	Dielectric	0.711		EM-370(Z)-15 ...
6	L6	Conductor	Conductor	0.03	6	COPPER 1OZ
		Dielectric	Dielectric	0.06		EM-370(Z)-15 ...
7	L7	Plane	Plane	0.038	7	COPPER 38UM...
		Dielectric	Dielectric	0.076		EM-370(Z)-15 ...
8	L8	Conductor	Conductor	0.023	8	COPPER 23UM...
		Dielectric	Dielectric	0.076		EM-370(Z)-15 ...
9	L9	Plane	Plane	0.023	9	COPPER 23UM...
		Dielectric	Dielectric	0.069		EM-370(Z)-15 ...
10	BOTTOM	Conductor	Conductor	0.038	10	COPPER 38UM...
		Dielectric	Dielectric	0.018		Soldermask
		Surface				

Figure 2.1: PCB stackup cross-section settings and dielectric properties for NVIDIA Jetson AGX Orin 64GB Carrier board shown in Allegro X PCB Layout

Conductor Layers

- Layer type: Signal, plane or mixed in real life (your software may adhere to signal or plane). HDI designs typically use a mix of signal and power where you use both routing and reference plane areas.
- Copper weight: Copper weight is expressed as oz/ft² (½ oz, 1 oz, 2 oz, etc.). Internal layers often use ½ oz copper for fine-feature capability; core layers may use 1 oz for power distribution. Outer layers typically use ½ oz or 1 oz copper. 2 oz or heavier copper for higher current carrying capacity.
- Start copper: The base copper foil thickness before plating. It affects the minimum achievable trace width.

Dielectric Layers

- Material type: Prepreg (for bonding layers) or core (rigid laminate). HDI buildup layers use prepreg; the central core uses rigid laminate.
- Thickness: The press-out thickness after lamination. HDI buildup dielectrics are typically 2-4 mils (0.051 - 0.102 mm). Verify the thickness against microvia aspect ratio limits.
- Material name: The specific laminate or prepreg material (e.g., Isola 370HR, Panasonic Megtron 6). Enables accurate electrical property modeling.
- Dielectric constant (Dk): The relative permittivity at your signal frequency. Used for impedance calculations.
- Loss tangent (Df): Dissipation factor for loss calculations at high frequencies.

2.2 Creating Layer Pairs and Sequential Lamination Cycles

Manufacturers use the concept of “substack” or “lamination cycle” to define how the board is manufactured. Each lamination cycle represents a press operation that bonds layers together.

For a 1-N-1 stackup:

1. Core lamination: The inner layers are laminated first, forming the structural core of the board.
2. First sequential lamination: Buildup layers are added to both surfaces of the core. After this press, microvias connecting outer buildup layers to the core can be drilled and plated.

For a 2-N-2 stackup, add a third lamination cycle that adds the outermost layers after the first buildup layers are drilled and plated.

Define these lamination cycles explicitly in your software or fabrication notes if needed. The tool uses this information to determine which via structures are legal between which layer pairs. A microvia can only span layers within the same lamination cycle or between a lamination cycle and its immediate predecessor.

2.3 Assigning Via Transitions Based on Lamination

The Cross-Section Editor enforces via legality based on the lamination structure you define. Understanding these rules prevents frustrating DRC violations during routing.

Legal Via Transitions

- Microvias: Can only span adjacent layers within a buildup cycle. A Layer 1-2 microvia is drilled after the buildup layer is laminated to the core.
- Buried vias: Span layers within the core lamination. Must be drilled and plated before sequential buildup begins.
- Blind vias: Start on an outer surface and end on an inner layer. May span multiple layers if drilled after all lamination cycles are complete.
- Through vias: Span all layers. Drilled after final lamination.

Via Stack Definitions

For stacked microvia configurations, define via stacks that specify the complete path from surface to target layer. A stacked via from Layer 1 to Layer 4 might consist of:

- Microvia 1-2 (drilled after second sequential lamination)
- Microvia 2-3 (drilled after first sequential lamination)
- Microvia 3-4 (drilled after core lamination if Layer 3 is a buildup layer)

The Cross-Section Editor validates that the defined stack is physically manufacturable given the lamination sequence.

3. Defining Via Structures

Via definition in Allegro X for HDI designs goes beyond simple padstack creation. The tool must understand via type, layer span, fill requirements, and how vias combine to form legal transition paths through the stackup.

3.1 Microvia, Blind, Buried, and Via-in-Pad Definitions

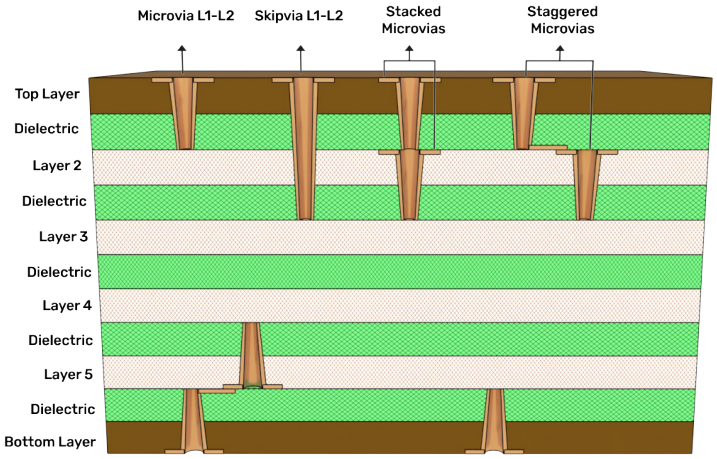


Figure 3.1: BGA escape routing cross-section view

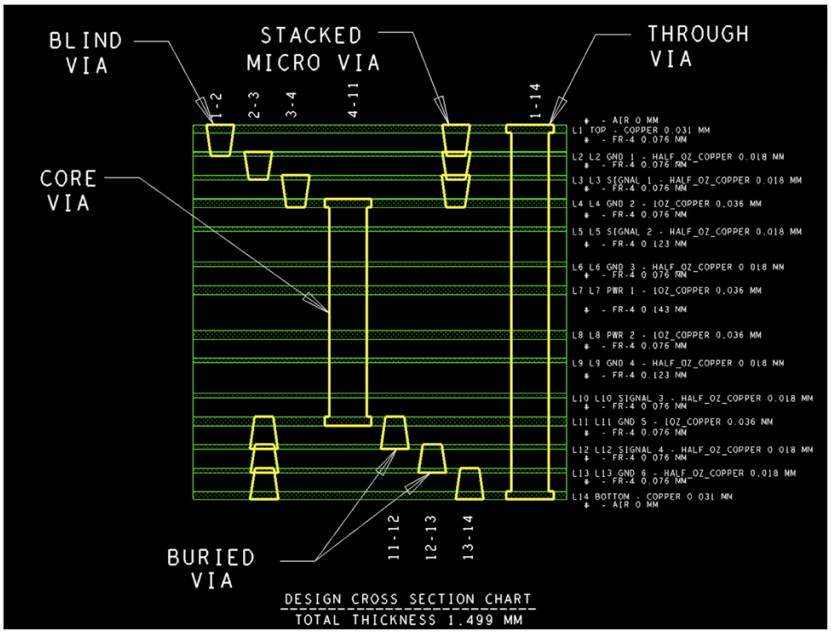


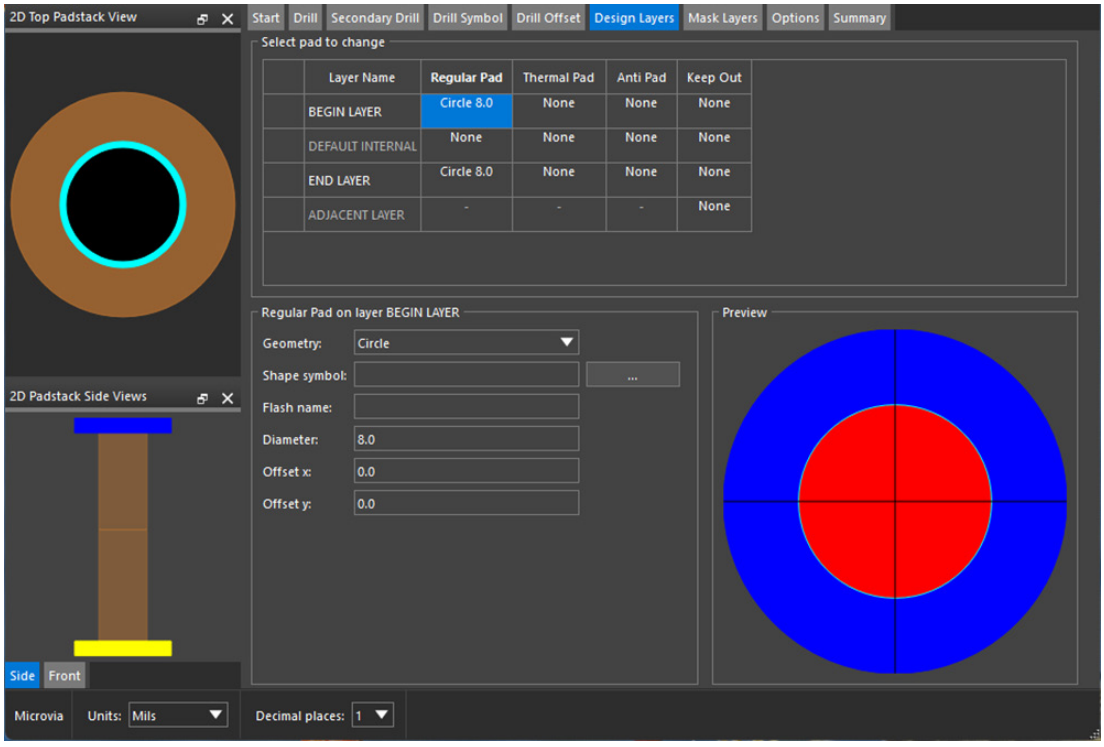
Figure 3.2: More examples of via types in Cadence Allegro X Layout

Create distinct via definitions for each via type used in your design:

Microvia Definitions

For each microvia layer pair (1-2, 2-3, N-1 to N, etc.), define a padstack with:

- **Drill size (Hole Diameter above):** 4-6 mils typical. Smaller requires tighter fabrication capability.
- **Capture pad diameter:** Drill + minimum annular ring × 2. For 4-mil drill with 2-mil annular ring: 8-mil pad minimum.
- **Target pad diameter:** Same as capture pad or per fabricator specification.



- **Layer span:** Exactly two adjacent layers.
- **Fill type:** Copper filled for stacked or VIP; conformal for staggered.

Buried Via Definitions

Buried vias in the core typically use mechanical drilling with larger geometry than microvias:

- **Drill size:** 8-12 mils typical for core buried vias.
- **Pad diameter:** Drill + minimum annular ring × 2. Larger annular ring than microvias due to mechanical drill tolerance.
- **Layer span:** Any layers within the core lamination.
- **Fill type:** Filled if microvias will stack on top; otherwise resin-filled during subsequent lamination.

Via-in-Pad Definitions

VIP requires special attributes to ensure manufacturability:

- **Via size:** Must fit within the component pad. For a 10-mil BGA pad, the via must be ≤10 mils including capture pad.
- **Fill requirement:** Always filled and capped/planarized.
- **Surface finish:** Cap plating must be compatible with the appropriate soldering process (ENIG, ENEPIG, or OSP over planarized fill).

3.2 Creating Via Stacks Tied to Lamination Cycles

Via stacks in Allegro X PCB Layout define the sequence of vias that form a complete vertical connection. The tool validates that each via in the stack can be manufactured at the appropriate point in the lamination sequence.

To create a stacked microvia from Layer 1 to Layer 4 in a 2-N-2 design:

1. Define individual microvia padstacks for each layer pair (1-2, 2-3, 3-4)
2. Create a via stack that sequences these padstacks in the correct drilling order
3. Associate the via stack with the appropriate net class or physical constraint set

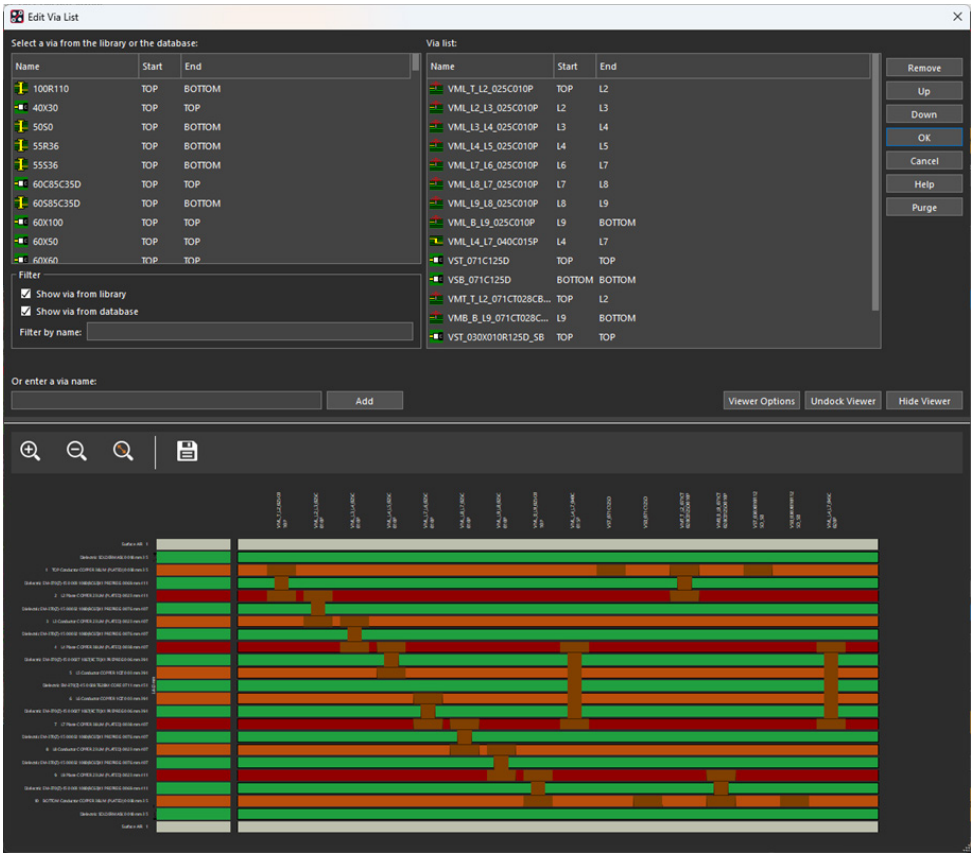


Figure 3.3: Allegro X PCB Layout Constraint Manager via list

The router can then use this via stack when transitioning signals between layers 1 and 4, automatically placing the complete stacked structure.

3.3 VIP Fill/Cap Configuration and Metallization Settings

Via-in-pad configurations require specific fabrication attributes that inform both DFM checking and fabrication documentation:

- **Fill type:** Conductive (copper) or non-conductive (epoxy). Copper fill is preferred for thermal and electrical performance.

- **Cap requirement:** Plated cap over fill material to provide solderable surface.
- **Planarization:** Surface must be flat to within specification (typically ≤0.5 mil deviation) for reliable solder joint formation.
- **Final finish:** Surface metallization compatible with assembly process (ENIG, ENEPIG, immersion silver, etc.).

Document these attributes in the padstack properties and ensure they propagate to fabrication outputs.

3.4 Validation of Legal/Illegal Transitions

Allegro X validates via transitions against the stackup definition. A transition is illegal if:

- The via spans layers that cannot be connected with a single drilling operation
- The via requires drilling through a layer that already contains filled vias (for non-stacked configurations)
- The via stack includes vias that would be drilled after layers they connect have already been buried

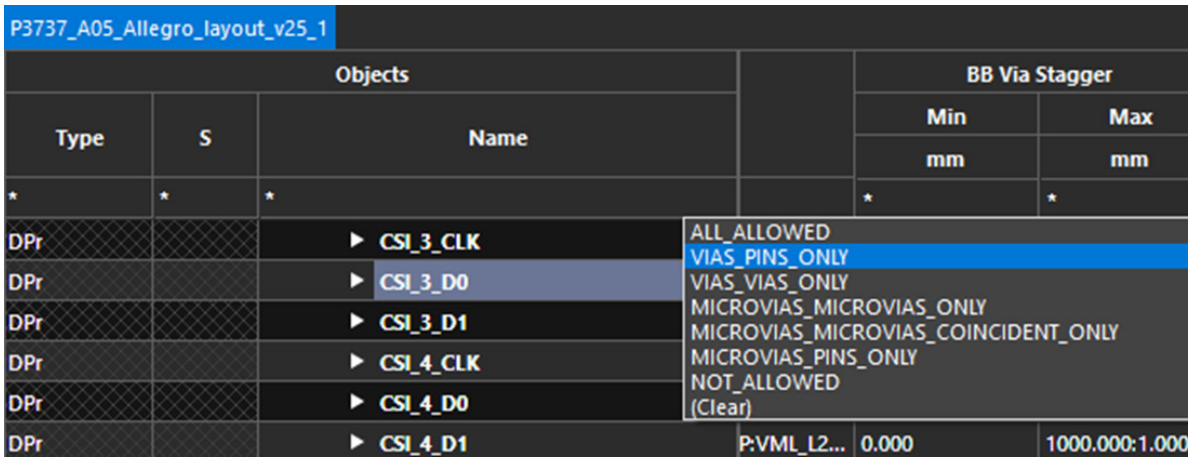


Figure 3.4: Allegro X PCB Layout Via connection constraints for routing

Run design rule checks early and often during layout. Via legality violations discovered late in the design cycle require significant rework to resolve.

4. BGA Breakout & Fanout Using HDI

BGA escape routing is often the most density-constrained region of an HDI design. Fine-pitch BGAs (0.35-0.5mm) present thousands of pins in a compact footprint where every mil of space is contested. This section describes systematic approaches for BGA breakout in Allegro X using HDI techniques.

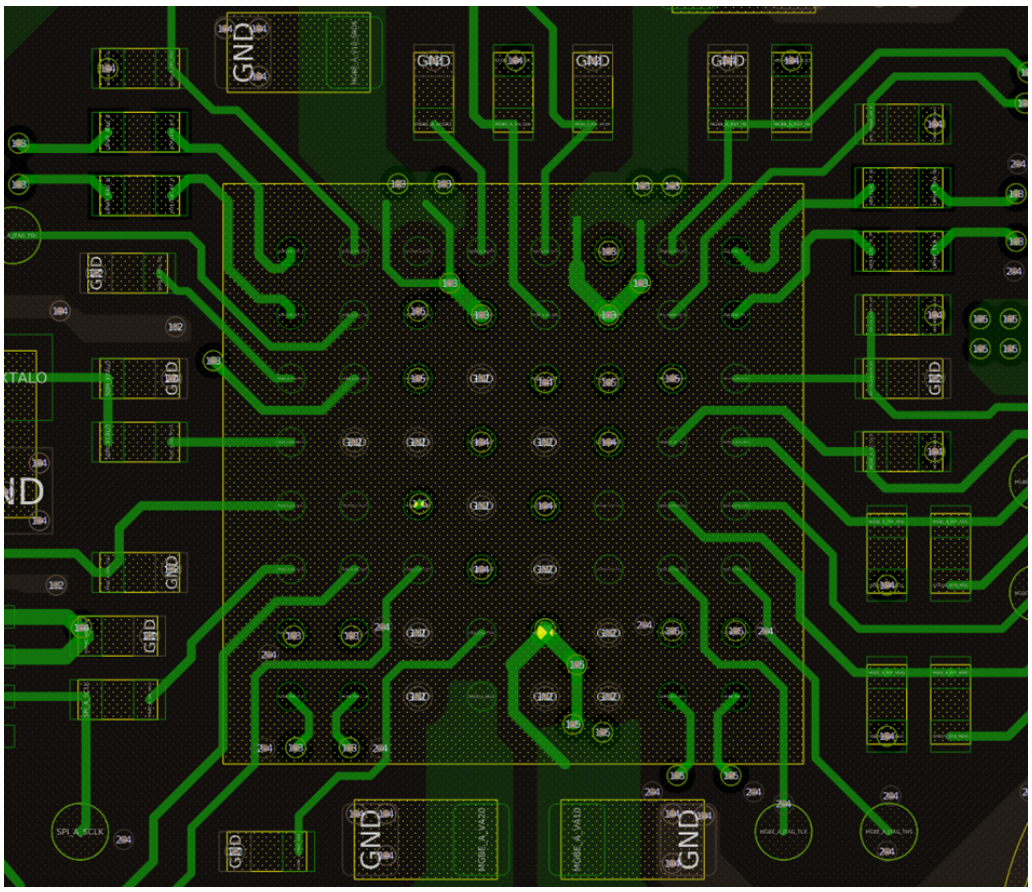


Figure 4: BGA Breakout example on NVIDIA AGX Orin Carrier Board

4.1 Microvia-First Fanout Strategy

The microvia-first strategy places via-in-pad structures as the first step, before any horizontal routing. Every signal exits its BGA pad vertically through a microvia to the first inner layer.

Implementation Steps

1. **Assign vias to all signal pads:** Place filled microvias in every signal pad. Power and ground pads may connect to planes on immediate inner layers.
2. **Route on Layer 2:** Begin escape routing from the Layer-2 via landing pads. The outer ring of signals routes directly outward on Layer 2.
3. **Transition inner signals deeper:** Signals from inner BGA rows that cannot escape on Layer 2 transition via additional microvias to Layer 3 or beyond.
4. **Complete escape routing:** Each routing layer carries signals outward from the BGA footprint until all signals have escaped to general routing channels.

This approach maximizes Layer-1 utilization for power delivery (large copper pours with thermal vias) while distributing signal routing across multiple inner layers.

4.2 Pitch-Aware Escape Strategies

The BGA pitch determines how many traces, if any, can route between pins on each layer. Plan escape strategies based on pitch:

0.5mm Pitch

At 0.5mm pitch (19.7 mils), there is approximately 10 mils between pad edges (assuming 10-mil pads). With 3/3 trace/space rules, one trace can route between pads. This allows some dog-bone fanout on Layer 1, but via-in-pad is more efficient for dense BGAs.

0.4mm Pitch

At 0.4mm pitch (15.7 mils), approximately 6 mils between pad edges. No traces route between pads with standard design rules. Via-in-pad is mandatory; all horizontal routing occurs on inner layers.

0.35mm Pitch and Below

At 0.35mm pitch (13.8 mils), geometry becomes extremely constrained. Pad sizes shrink to maintain minimum spacing; via diameters approach fabrication limits. Sub-3-mil trace/space rules may be required. Engage your fabricator early to verify capability.

4.3 Maintaining Reference Plane Integrity

Dense microvia fields beneath BGAs can fragment reference planes if not managed carefully. Signal integrity depends on continuous reference planes beneath routing layers.

- **Antipad management:** Microvia antipads (clearances in planes) accumulate to create Swiss-cheese patterns. Use minimum antipad sizes that meet fabrication rules.
- **Power/ground via placement:** Distribute power and ground vias throughout the BGA field, not just at the periphery. These vias connect to planes without creating additional clearances.
- **Ground stitching:** Include ground stitching microvias adjacent to signal vias to maintain return path integrity through layer transitions.
- **Plane layer allocation:** Consider dedicating certain layers to reference planes only (no routing) in the BGA region to ensure continuous reference for adjacent signal layers.

5. Board-Level HDI Routing Strategies

Beyond BGA escape, HDI routing throughout the board requires strategies that leverage microvia flexibility while respecting electromagnetic constraints. This section addresses routing channel planning, layer optimization, and high-speed routing considerations for HDI designs.

5.1 Routing Channel Planning

Effective HDI routing begins with channel planning by identifying the paths signals will take between source and destination before detailed routing begins.

- Layer assignment by function: Assign layers to signal groups based on their routing requirements. High-speed differential pairs may warrant dedicated layers; general-purpose I/O can share layers more densely.
- Vertical zoning: In HDI stackups, signals that need to route together should be assigned to layers accessible via the same via structures. A signal that must connect to a component on Layer 1 and another on Layer 8 needs a via path through the entire stackup.
- Channel width estimation: Estimate the number of traces that must pass through critical routing channels. HDI may allow wider channels and more signals per routing layer, but requires more layer transitions.

5.2 Microvia Path Optimization Across Layers

HDI provides flexibility in layer transitions that conventional designs lack. Use this flexibility strategically:

- **Minimize stack depth:** Prefer shallow via transitions (1-2 layers) over deep stacks when routing permits. Each stacked level adds inductance and reliability risk.

- **Balance layer loading:** Distribute routing across available layers rather than concentrating on a few. This improves copper balance and reduces crosstalk density.
- **Use staggered vias when space permits:** Outside dense regions, staggered configurations may offer better reliability than stacked vias with minimal routing penalty.

5.3 Avoiding Cavity Resonances and Return-Path Discontinuities

HDI stackups can exhibit unexpected electromagnetic behavior if plane management is neglected:

- **Plane-pair stitching:** Add ground stitching vias throughout the board (not just at edges) to short plane pairs and suppress cavity resonances. Use via types appropriate for each plane pair.
- **Reference plane selection:** When possible, route signals on layers that reference the same ground plane or planes connected by nearby stitching vias. Avoid references to split planes or isolated plane regions.
- **Transition stitching:** Every signal via transition should have an adjacent ground stitching via. This is non-negotiable for high-speed signals and strongly recommended for all signals in dense designs.

5.4 HDI-Aware Differential Pair and High-Speed Routing

High-speed differential pairs in HDI designs require special attention to maintain signal integrity through microvia transitions:

- **Via symmetry:** Both legs of a differential pair must traverse identical via structures. If P uses a two-level stack, N must use the same two-level stack, not a three-level stack or different via type.
- **Matched via placement:** P and N vias should be placed at equal distances from their respective traces, with equal length stubs (if any).
- **Ground via patterns:** Use symmetric ground stitching patterns around differential pairs such as GSG or GSSG through via transitions.
- **Length matching through vias:** Via transitions should occur at matched points in the P and N paths. Avoid transitioning one leg while the other remains on the original layer.

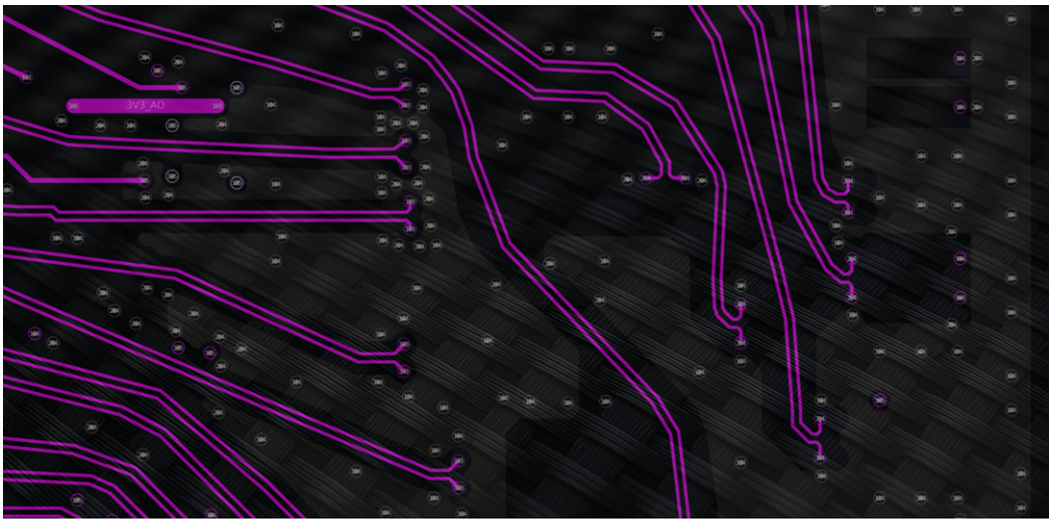


Figure 5: PCB PCIe differential pair traces routed over fiber weave dielectric (greyed out) underneath as seen in the NVIDIA Jetson AGX Orin 64GB Carrier PCB demo design

6. Thermal & Power Considerations

HDI designs must address thermal management within the constraints of microvia technology and thin dielectrics. This section covers thermal via field design, heat spreading strategies, and copper balancing for warpage control in Allegro X.

6.1 Designing Thermal Via Fields in HDI

Thermal vias transfer heat from hot components to inner copper layers and ultimately to heat sinks or the ambient environment. In HDI designs, thermal via fields must work within microvia geometry constraints.

Via Array Sizing

Calculate thermal via count based on thermal resistance requirements:

1. Determine required thermal conductance from component thermal specification and target temperature rise.
2. Calculate individual via thermal conductance based on diameter, fill material, and span length.
3. Divide required conductance by individual via conductance to determine minimum via count.
4. Add margin for manufacturing variation and verify via array fits within available area.

For high-power components, consider hybrid approaches: microvias in signal-routing regions, larger through-vias or buried vias in dedicated thermal zones.

6.2 Managing Heat Spread Through Thin Dielectrics

Thin HDI dielectrics transfer heat vertically more efficiently than thicker conventional dielectrics, but they also concentrate thermal loading on inner copper layers.

- **Copper pour sizing:** Ensure copper pours on plane layers extend beyond the thermal source footprint to allow lateral heat spreading.
- **Layer stack optimization:** Place ground or power planes adjacent to thermal via fields to maximize heat spreading area.
- **Avoid routing obstructions:** In thermal critical regions, avoid routing that fragments copper pours needed for heat spreading.

6.3 Copper Balancing Tools

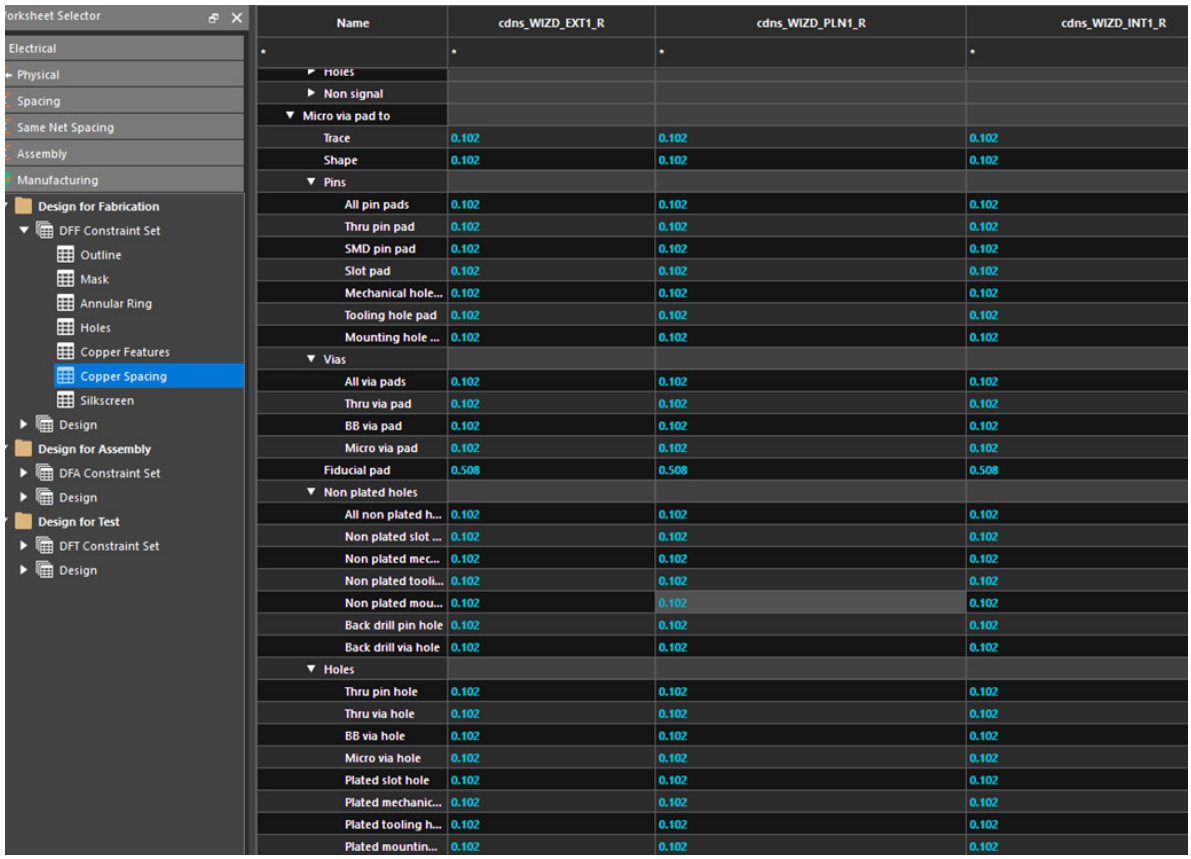
Allegro X provides copper analysis features to evaluate and optimize copper distribution for warpage control:

- **Copper percentage display:** View copper density by layer and region to identify imbalances.
- **Copper thieving generation:** Automatically add dummy copper fills to sparse regions to balance density.
- **Layer-pair comparison:** Compare copper percentages between corresponding layers (1 vs. N, 2 vs. N-1) to verify symmetry.

Target copper balance within 10-15% between corresponding layers. Run copper analysis iteratively during layout and adjust fills as needed.

7. In-Design DFM Checks

Design for manufacturability (DFM) analysis should be integrated throughout the HDI design process, not relegated to a final check before release. Allegro X provides DFM capabilities that flag manufacturing risks early when they can be addressed without major rework.



Name	cdns_WIZD_EXT1_R	cdns_WIZD_PLN1_R	cdns_WIZD_INT1_R
*	*	*	*
Holes			
Non signal			
Micro via pad to			
Trace	0.102	0.102	0.102
Shape	0.102	0.102	0.102
Pins			
All pin pads	0.102	0.102	0.102
Thru pin pad	0.102	0.102	0.102
SMD pin pad	0.102	0.102	0.102
Slot pad	0.102	0.102	0.102
Mechanical hole...	0.102	0.102	0.102
Tooling hole pad	0.102	0.102	0.102
Mounting hole ...	0.102	0.102	0.102
Vias			
All via pads	0.102	0.102	0.102
Thru via pad	0.102	0.102	0.102
BB via pad	0.102	0.102	0.102
Micro via pad	0.102	0.102	0.102
Fiducial pad	0.508	0.508	0.508
Non plated holes			
All non plated h...	0.102	0.102	0.102
Non plated slot ...	0.102	0.102	0.102
Non plated mec...	0.102	0.102	0.102
Non plated tooli...	0.102	0.102	0.102
Non plated mou...	0.102	0.102	0.102
Back drill pin hole	0.102	0.102	0.102
Back drill via hole	0.102	0.102	0.102
Holes			
Thru pin hole	0.102	0.102	0.102
Thru via hole	0.102	0.102	0.102
BB via hole	0.102	0.102	0.102
Micro via hole	0.102	0.102	0.102
Plated slot hole	0.102	0.102	0.102
Plated mechanic...	0.102	0.102	0.102
Plated tooling h...	0.102	0.102	0.102
Plated mountin...	0.102	0.102	0.102

Figure 7: Extensive Design for Fabrication constraints for micovias shown above

7.1 Resin Starvation Checks

Resin starvation occurs when dense copper regions displace too much prepreg resin during lamination, leaving voids. DFM analysis identifies high-risk regions:

- **Copper density analysis:** Flag regions where copper density exceeds fabricator limits (typically 70-80% maximum).

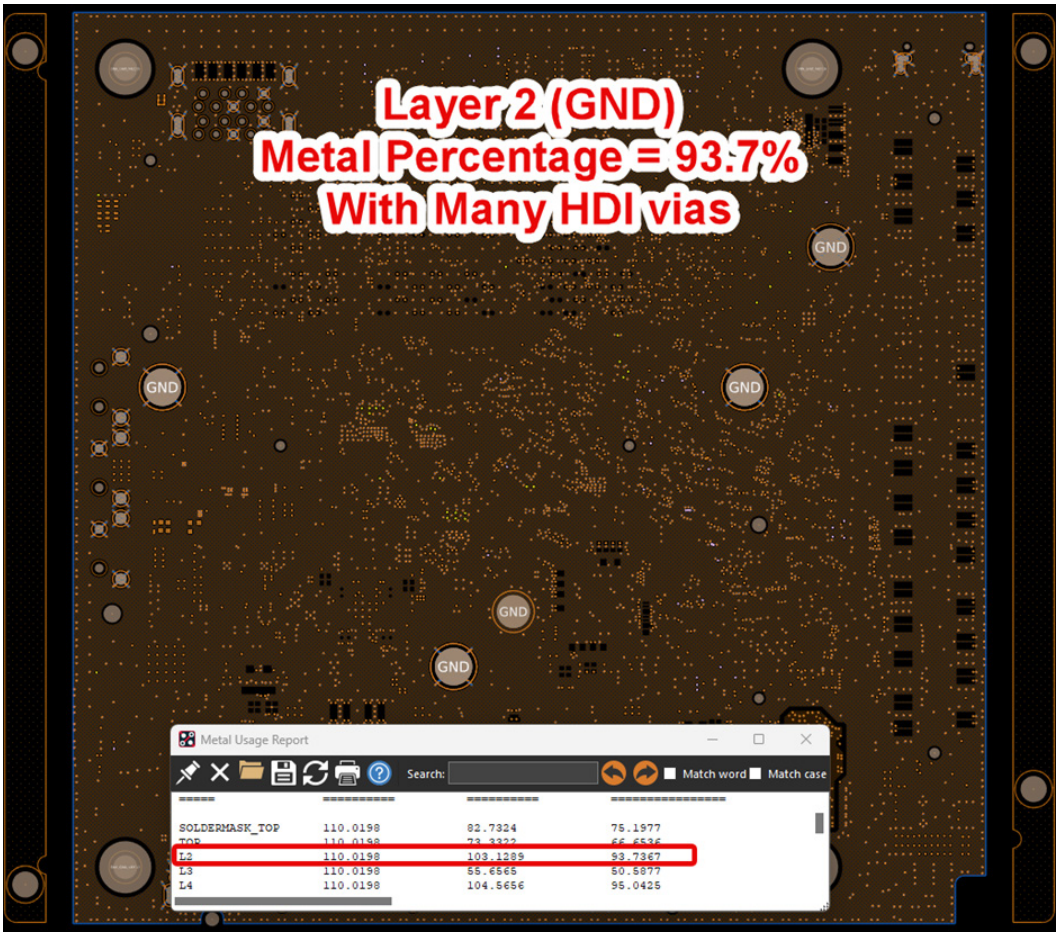


Figure 7.1: Copper Metal Percentage (density analysis)

7.2 Via Field Alignment and Spacing

Dense microvia fields require verification of spacing rules that may be more stringent than general via rules:

- **Minimum via-to-via spacing:** Verify all vias meet minimum spacing requirements, including stacked via offsets for staggered configurations.
- **Stacked via alignment:** For stacked configurations, verify that via centers align within tolerance to prevent offset stacking that stresses interfaces.
- **Via pattern regularity:** Irregular via patterns can create resin flow problems; DFM may flag patterns that deviate significantly from uniform grids.

7.3 Copper Density and Warpage Risk

Copper imbalance contributes to board warpage. DFM checks should verify:

- **Global copper balance:** Overall copper percentage on top-half layers vs. bottom-half layers.
- **Regional copper balance:** Copper distribution across different board regions (center vs. edge, component-dense vs. sparse areas).
- **Layer-pair symmetry:** Copper percentage comparison between layer 1 and layer N, layer 2 and layer N-1, etc.

7.4 Lamination-Aware Manufacturability Checks

HDI-specific DFM checks validate designs against sequential lamination constraints:

- **Via legality:** Verify all vias can be manufactured given the defined lamination sequence.
- **Stack height limits:** Flag stacked via configurations that exceed fabricator capability or reliability guidelines.
- **Aspect ratio compliance:** Verify microvia aspect ratios against maximum limits (typically 0.75:1 or per fabricator specification).
- **Annular ring verification:** Confirm all vias maintain minimum annular ring after accounting for drill tolerance and registration.

8. SI/PI Validation for HDI Using Sigrity X Aurora

Signal integrity and power integrity analysis for HDI designs requires extraction and simulation tools capable of modeling the three-dimensional electromagnetic behavior of microvia structures, thin dielectrics, and dense routing. Sigrity X Aurora provides these capabilities integrated with the Allegro X design environment.

8.1 Microvia Stub Analysis

While microvias eliminate the stub problem that plagues through-vias, stub-like behavior can still occur in certain HDI configurations:

- **Unused via pads:** Intermediate pads in stacked via structures that don't connect to routing can create minor stub effects at very high frequencies.
- **Buried via stubs:** If buried vias in the core extend beyond the layers actually used, stub effects occur just as with through-vias.

Use Sigrity X extraction to model via structures and identify any stub resonances within your signal bandwidth. For signals above 10 GHz, even minor stub effects warrant investigation.

8.2 PDN Impedance Checks

Power delivery network impedance through HDI structures determines power supply noise and transient response. Key analysis points:

- **Via inductance extraction:** Extract the inductance of microvia connections from planes to component power pins. Compared to through-via equivalents to quantify HDI PDN benefits.
- **Plane resonance identification:** Identify resonant frequencies of plane pairs and verify that stitching via placement adequately suppresses resonances.
- **Decoupling effectiveness:** Simulate decoupling capacitor connection paths to verify that microvia inductance doesn't negate capacitor effectiveness at target frequencies.

8.3 Return Path Disruption Modeling

Return path integrity analysis verifies that ground stitching strategies provide adequate return current paths:

- **Layer transition analysis:** Extract the additional inductance from signal via transitions and adjacent ground stitching. Quantify the benefit of closer stitching placement.
- **Plane split crossing:** Model signals that must cross plane splits or reference voids. Identify return path discontinuities and their impact on signal integrity.
- **Current density visualization:** View return current distribution on reference planes to identify bottlenecks or regions where return current is forced to take long paths.

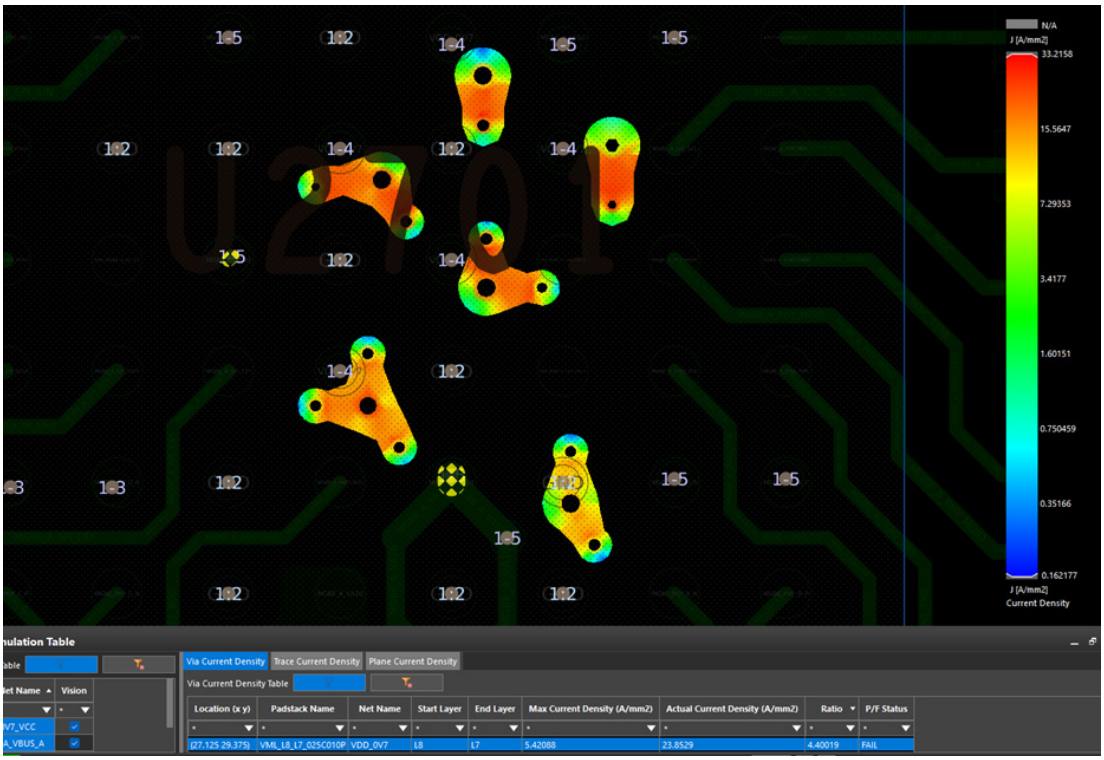


Figure 8.3.1: Higher current density spots for blind, buried and microvias in the NVIDIA AGX Orin Carrier Board

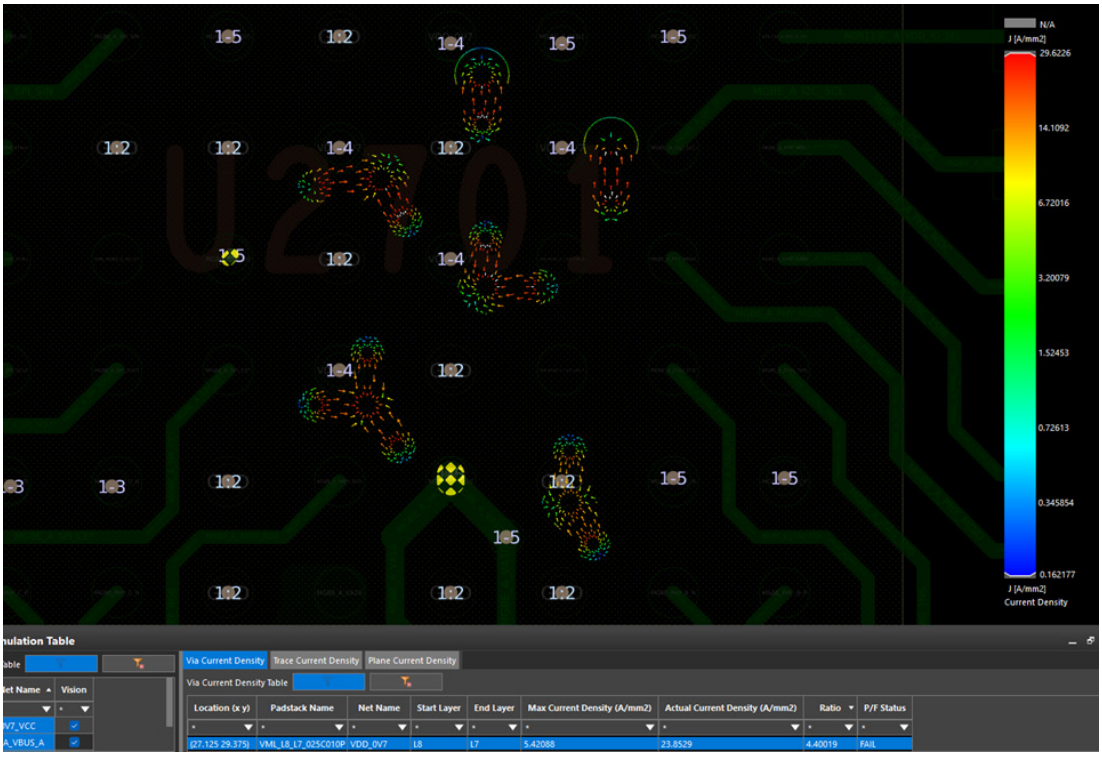


Figure 8.3.2: Current flow for blind, buried and microvias in the NVIDIA AGX Orin Carrier Board

8.4 EM Solver Flows for HDI Verification

Full-wave electromagnetic simulation captures effects that simpler models miss, particularly in dense HDI regions:

- **BGA region extraction:** Extract the complete electromagnetic model of the BGA escape region, including all signal vias, ground vias, and plane interactions.
- **Via-to-via coupling:** Quantify crosstalk between adjacent vias in dense fields, which doesn't appear in schematic-level analysis.
- **S-parameter extraction:** Generate S-parameter models of critical via transitions for use in channel simulation.
- **Correlation to measurement:** Compare extracted models to measurements from test vehicles to validate modeling accuracy for your specific HDI process.

9. Final Fabrication Outputs & HDI Handoff

HDI fabrication requires more detailed documentation than conventional PCB manufacturing. The fabricator must understand not just the final geometry but the complete lamination sequence, via structure definitions, and process requirements at each manufacturing step.

9.1 HDI Stackup Documentation

Export comprehensive stackup documentation including:

- **Complete layer table:** All layers with material types, thicknesses, copper weights, and dielectric properties.
- **Lamination sequence:** Clear indication of which layers are laminated at each cycle (core lamination, first sequential, second sequential, etc.).
- **Material specifications:** Exact material names, manufacturers, and acceptable substitutes for each material in the stackup.
- **Controlled impedance requirements:** Target impedance values, tolerance, and reference layers for each controlled impedance net class.

9.2 Via Stack Tables

Document all via structures with:

- **Via type identification:** Unique identifier for each via type (microvia, buried, blind, through).
- **Layer span:** Start and end layers for each via type.
- **Geometry:** Drill diameter, pad sizes on each layer, antipad sizes on plane layers.
- **Process requirements:** Fill type, plating thickness, planarization requirements.
- **Drilling sequence:** When each via type is drilled relative to lamination cycles.

9.3 Fabrication Notes for Microvia Construction

Include explicit fabrication notes covering:

- **Laser drilling parameters:** Laser type expectations (CO_2, UV), depth control requirements, target pad requirements.
- **Fill requirements:** Fill material (copper electrolytic, conductive epoxy, non-conductive epoxy), fill coverage percentage, void acceptance criteria.
- **Planarization requirements:** Surface flatness tolerance, cap plating thickness.
- **Reliability requirements:** IPC class, thermal cycling requirements, acceptance criteria for cross-section inspection.

9.4 VIP and Lamination Callouts

Via-in-pad designs require specific callouts:

- **VIP identification:** Clear indication of which pads contain vias and require fill/planarization.
- **Fill and cap specification:** Detailed requirements for via fill under solderable pads.
- **Surface finish compatibility:** Verification that specified surface finish is compatible with planarized via fill.
- **Inspection requirements:** Cross-section or X-ray inspection requirements for VIP quality verification.

Consider creating a fabrication drawing that visually shows the lamination sequence, via drilling order, and key process steps. This drawing supplements the digital data and ensures fabricators understand the complete manufacturing flow.

10. Conclusion

Successful HDI design in Allegro X requires a systematic workflow that addresses stackup definition, via structure configuration, constraint management, routing strategy, DFM verification, and SI/PI validation. This guide has walked through each phase of that workflow, from initial project setup to final fabrication handoff.

Key workflow principles:

1. **Plan HDI from the start.** Establish stackup, via structures, and constraints before component placement begins.
2. **Use the Cross-Section Editor as the source of truth.** Define lamination cycles and via legality in the Cross-Section Editor; let the tool enforce manufacturability.
3. **Run DFM continuously.** Check manufacturability throughout layout, not just before release.
4. **Validate SI/PI early.** Use Sigrity extraction and simulation to verify critical paths before routing is complete.
5. **Document thoroughly.** HDI fabrication requires more detailed documentation than conventional designs. Invest time in clear, complete fabrication handoff.

With proper workflow discipline and the capabilities of Allegro X, designers can leverage HDI technology to meet the most demanding density, signal integrity, and form factor requirements of modern electronic systems.