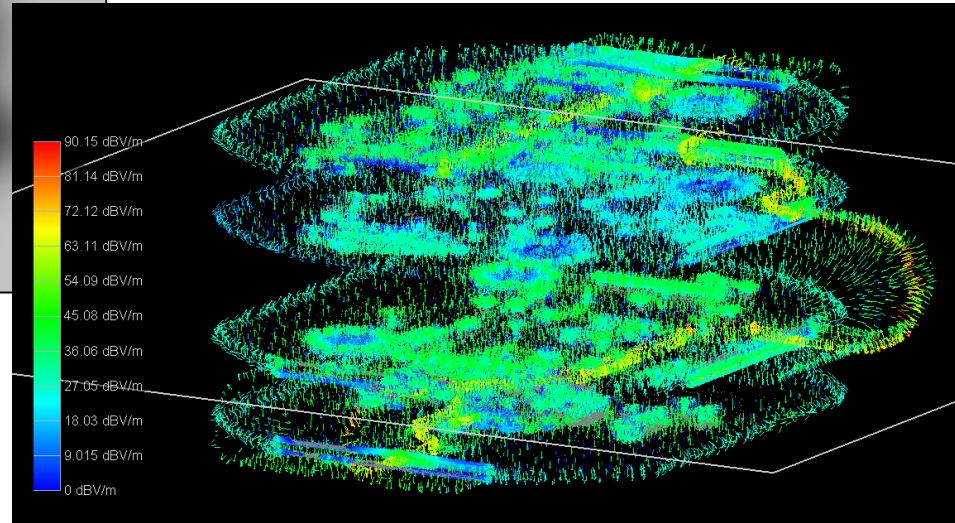
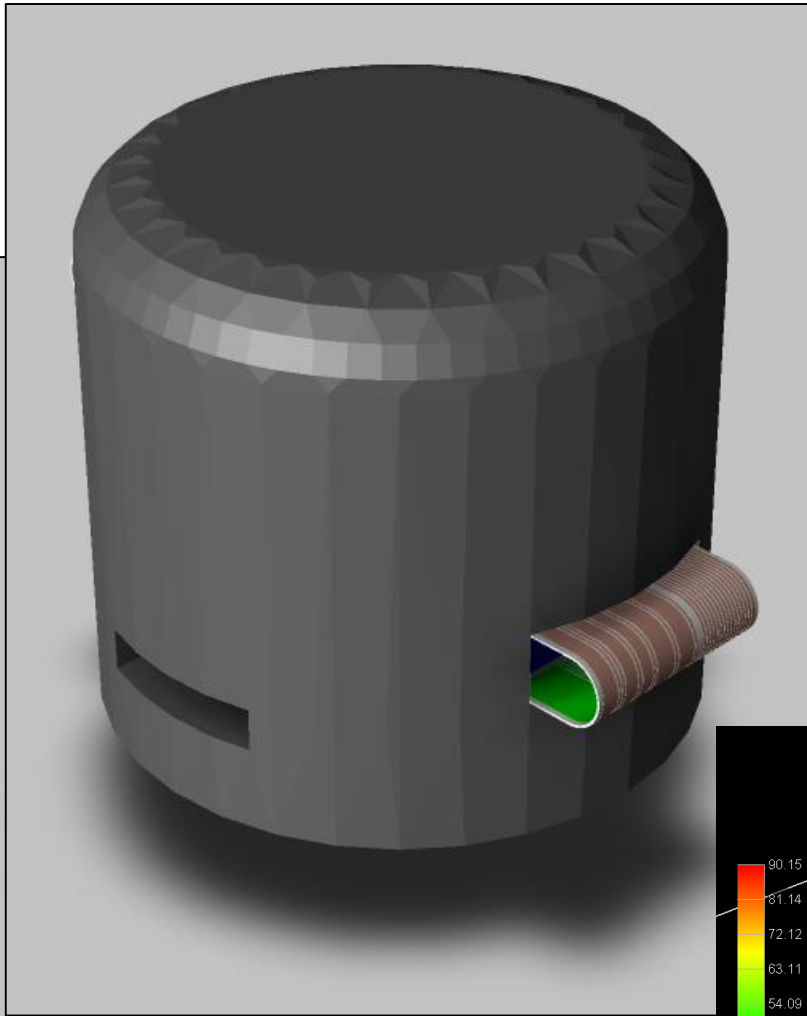
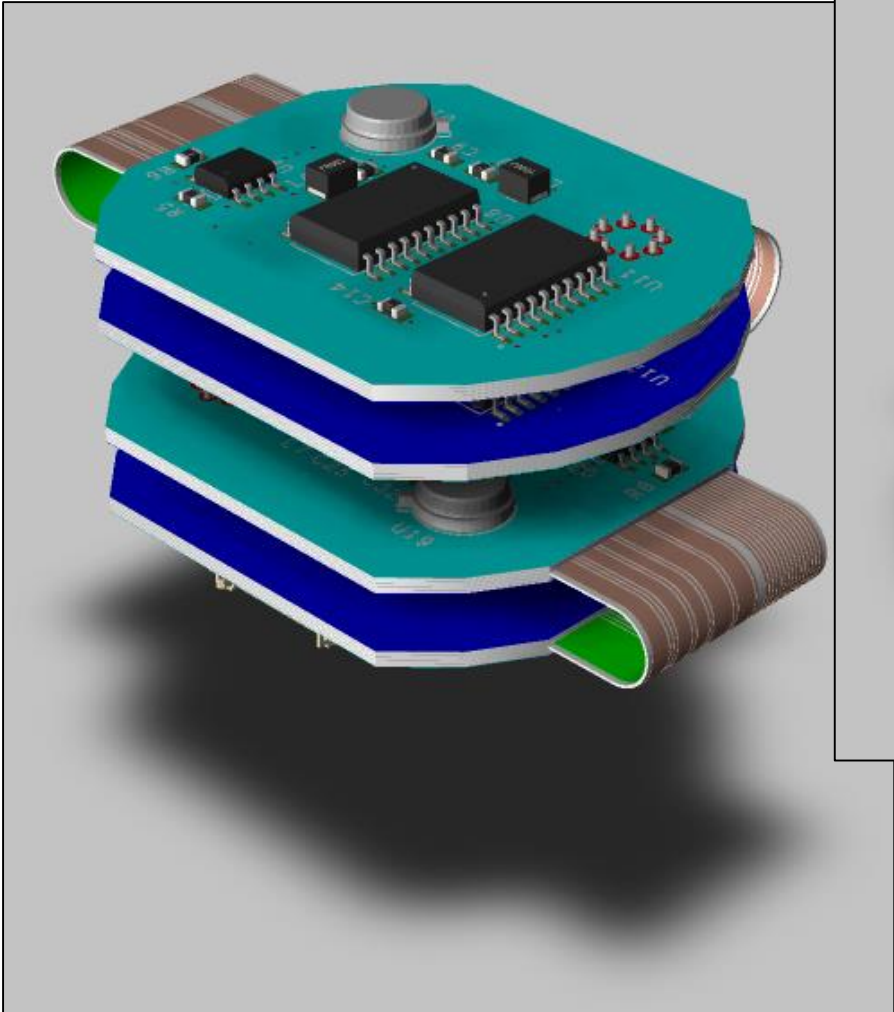


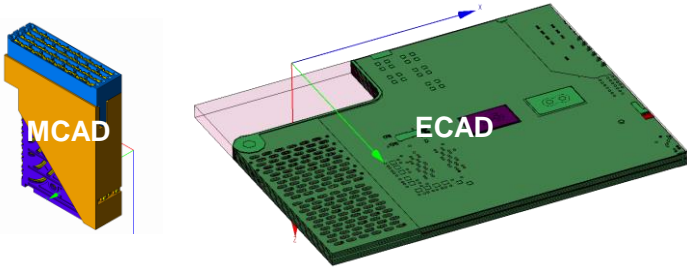


Bridging the Gap Between Electrical and Mechanical, and More

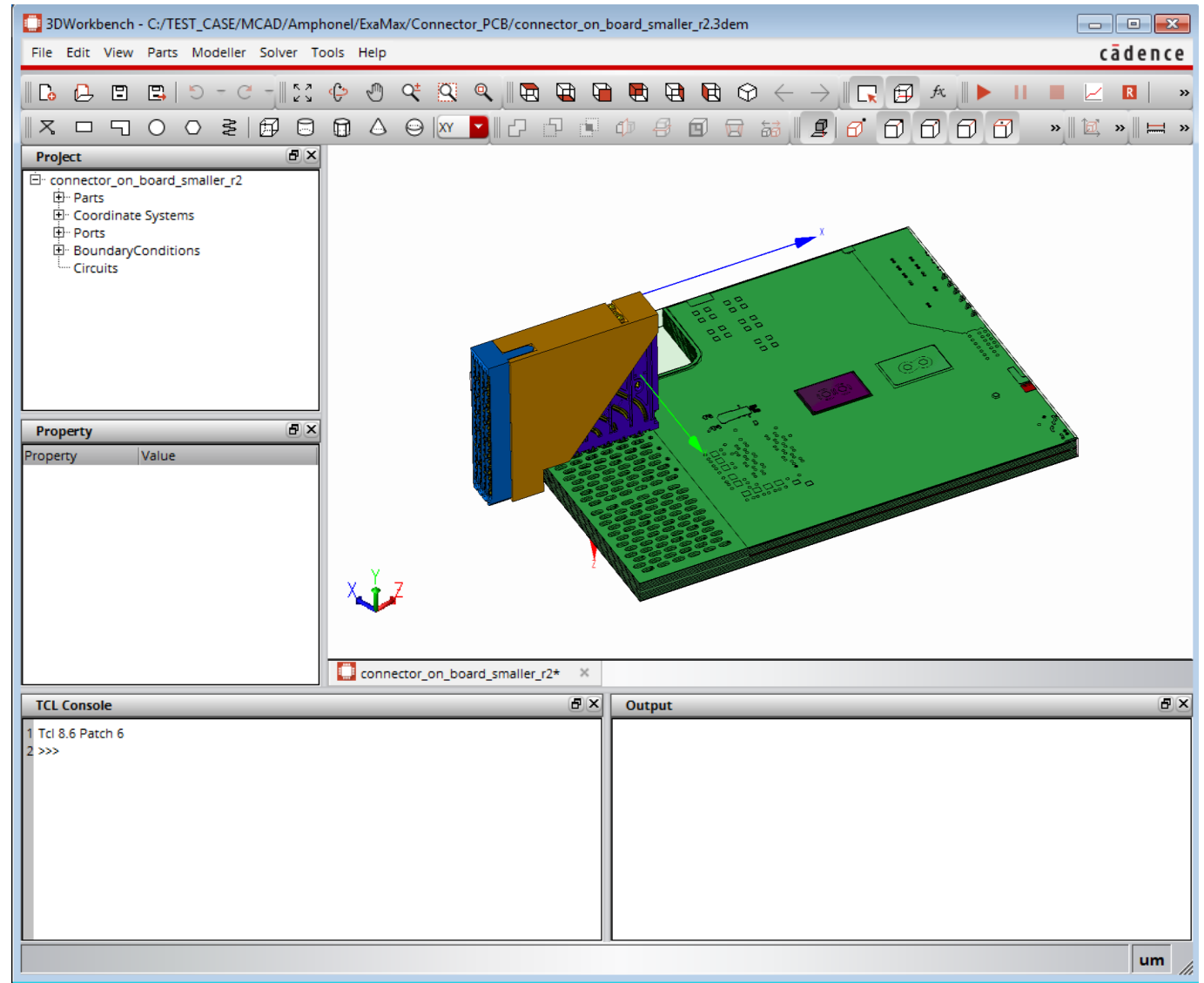
An-Yu Kuo, PhD
Sr. Group Director
October 2018



Three Challenges for Modern System Design Tools



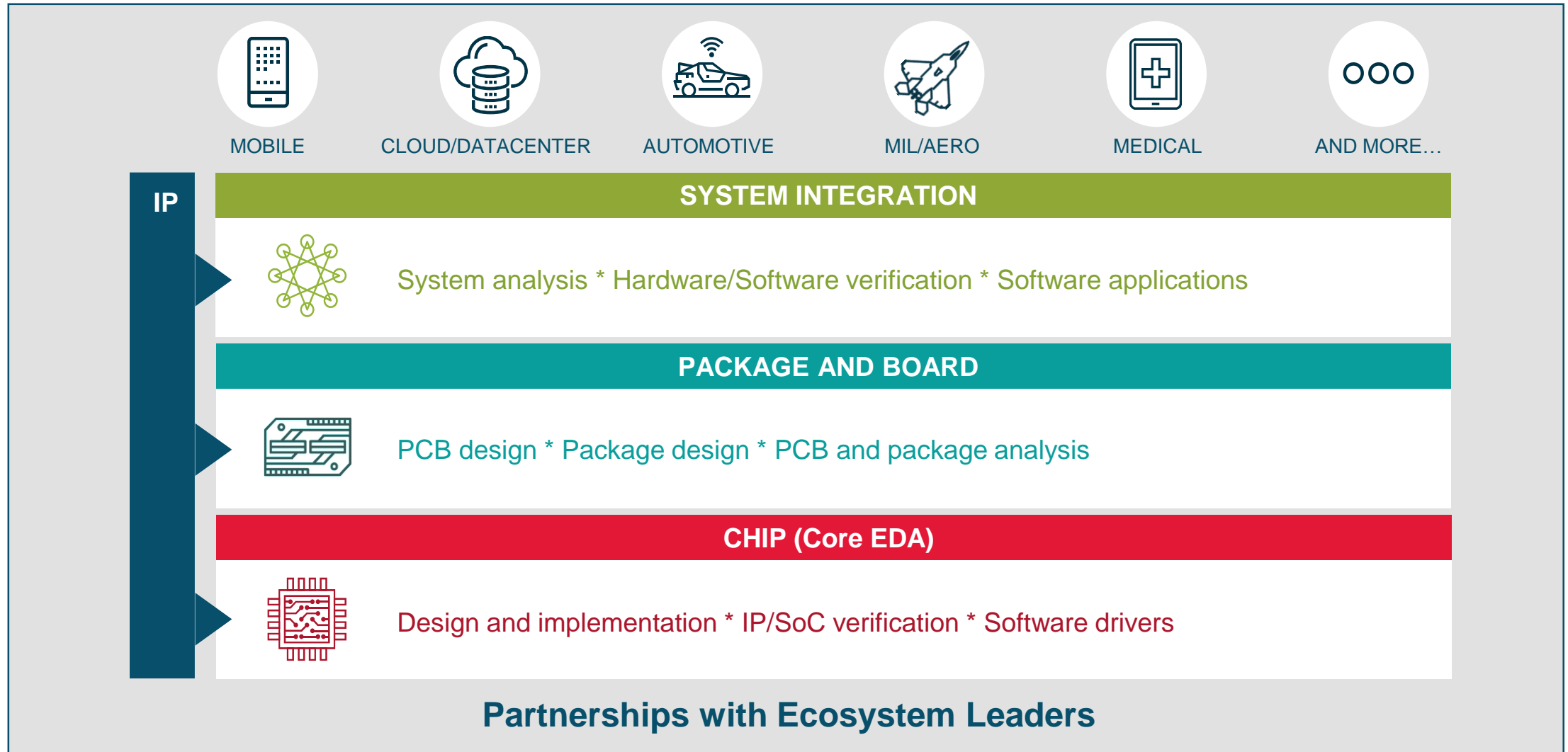
- Connect MCAD designs and ECAD designs together for engineers of all disciplines
- Enable engineers of all disciplines to meet multi-physics design requirements
- Automation, automation, automation



Outline

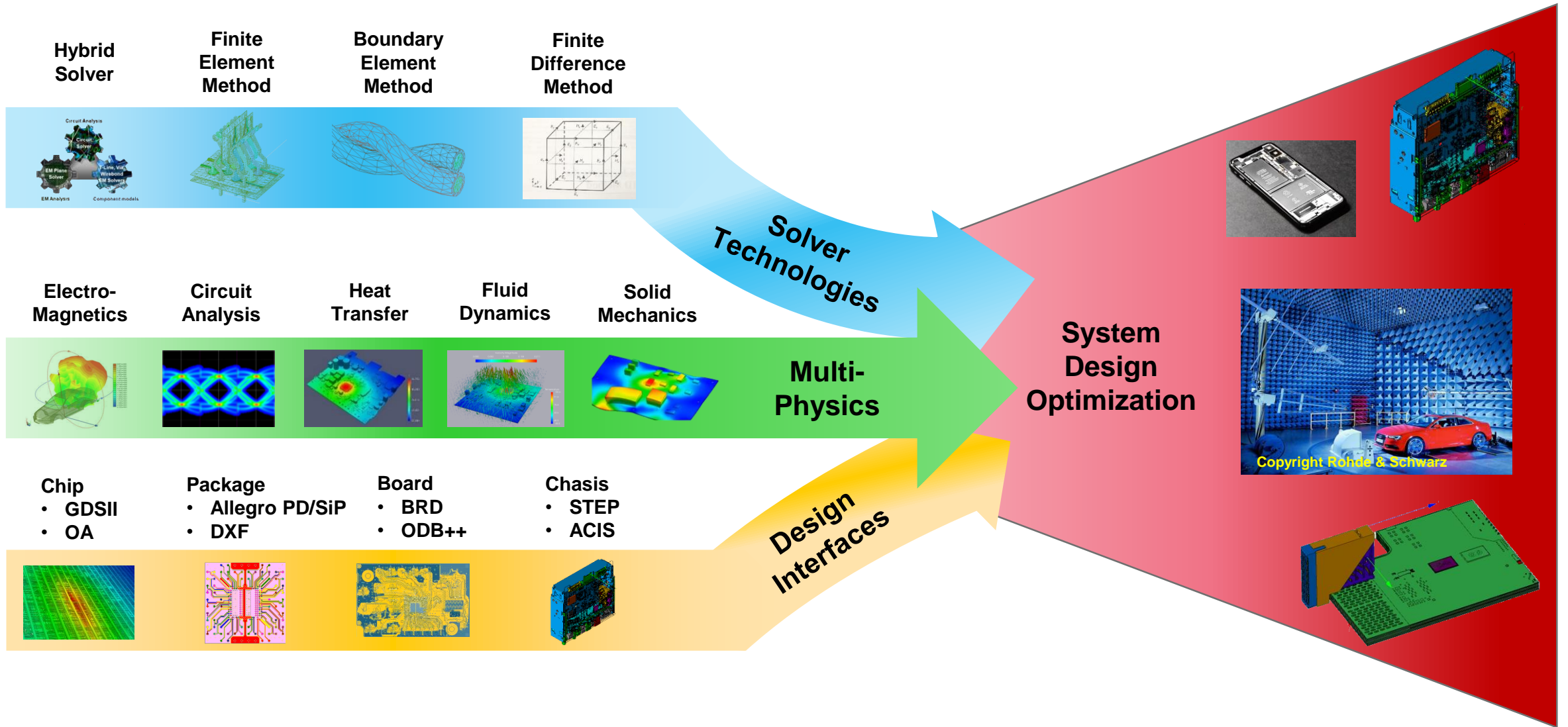
- System Design Enablement
- Integrated ECAD/MCAD for System Design Optimization
- Multi-Physics Co-Simulation
 - Novel System-Level Thermal Solution
 - Efficient and Accurate System Level-Level EMI Solution
- Tight Integration of Design/Simulation Tools

System Design Enablement: Connection, Interaction, Integration



System Design Enablement

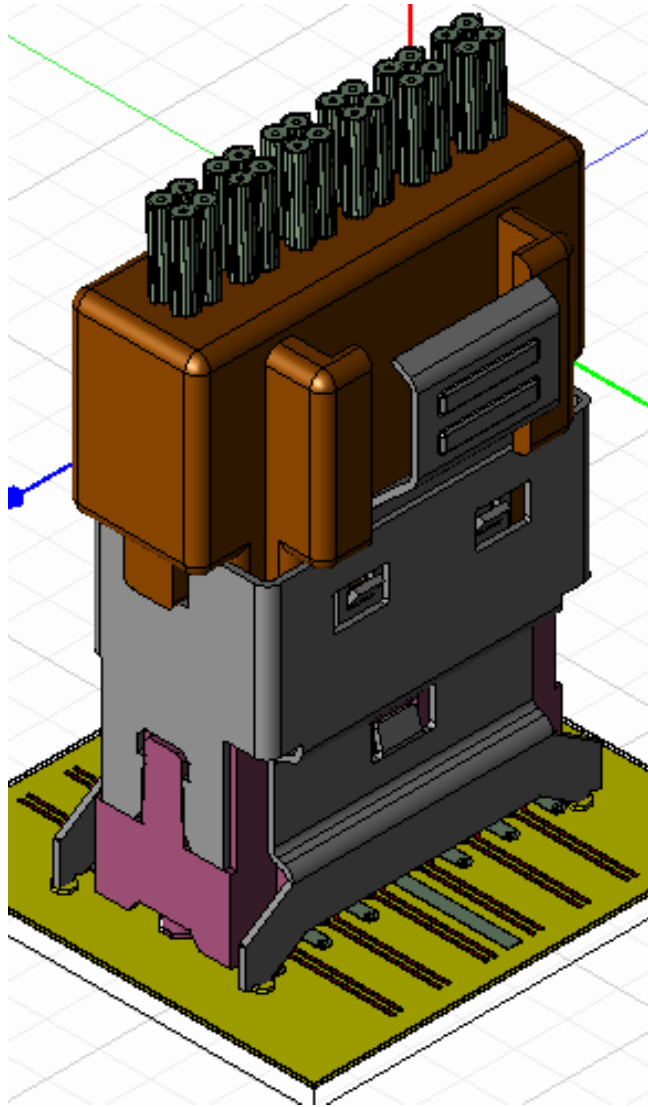
Convergence of technologies



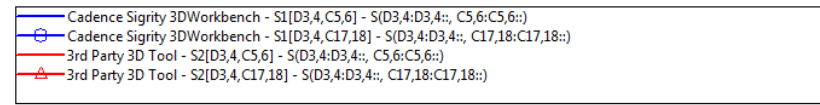
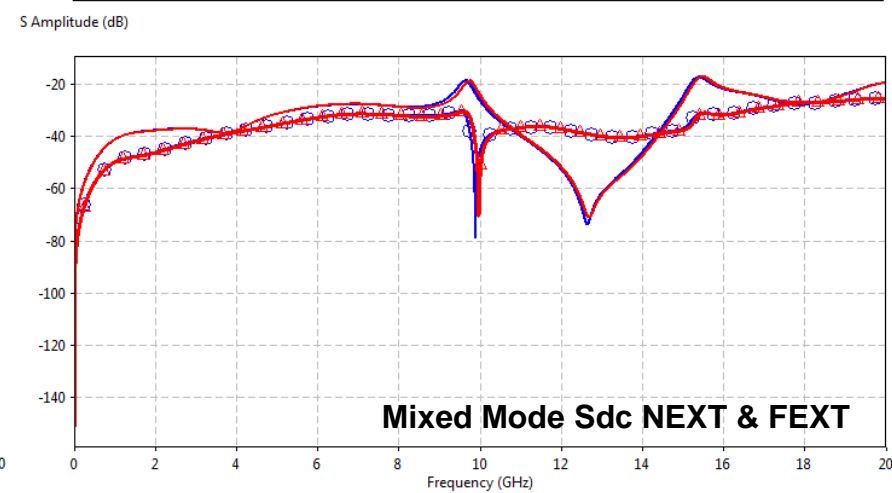
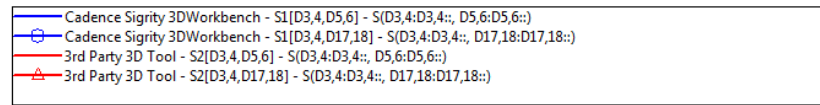
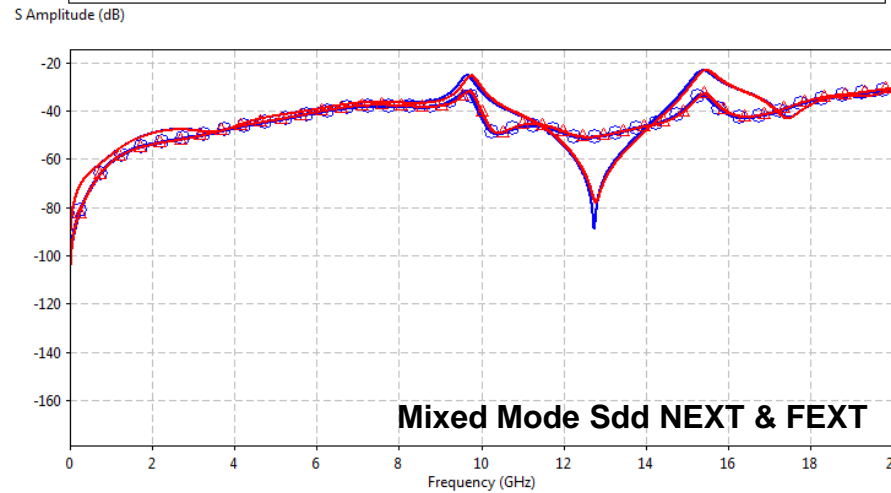
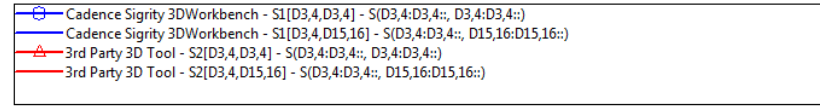
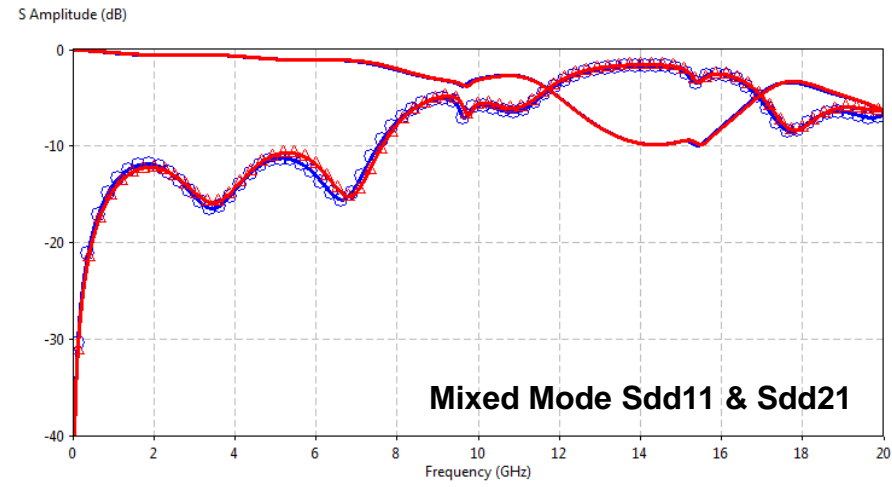
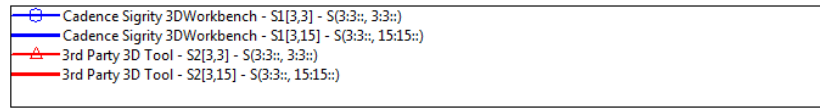
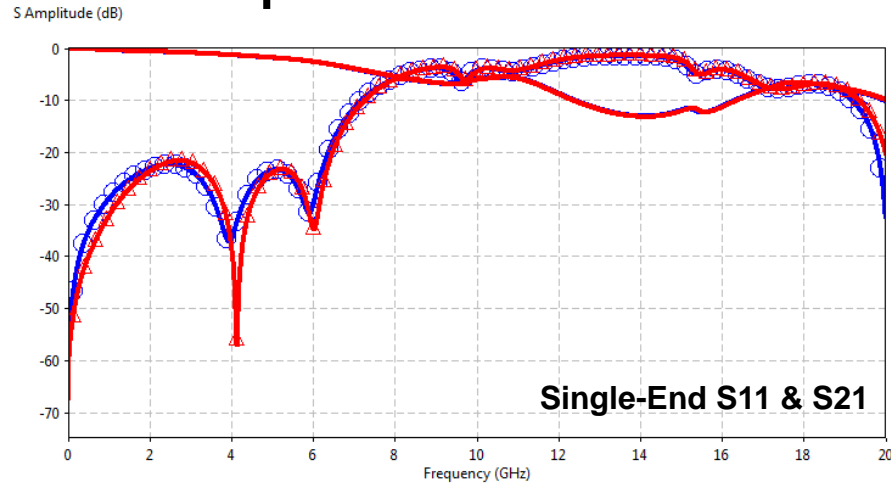
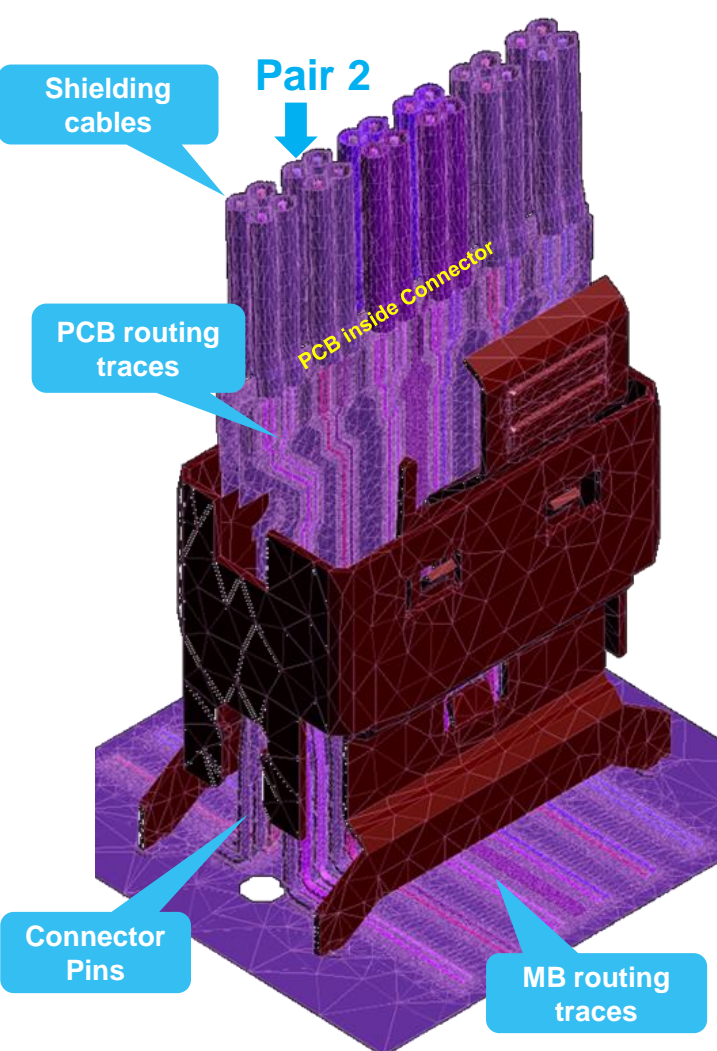
Outline

- System Design Enablement
- Integrated ECAD/MCAD for System Design Optimization
- Multi-Physics Co-Simulation
 - Novel System-Level Thermal Solution
 - Efficient and Accurate System Level-Level EMI Solution
- Tight Integration of Design/Simulation Tools

PCIe 8Gbps or SAS 12Gbps

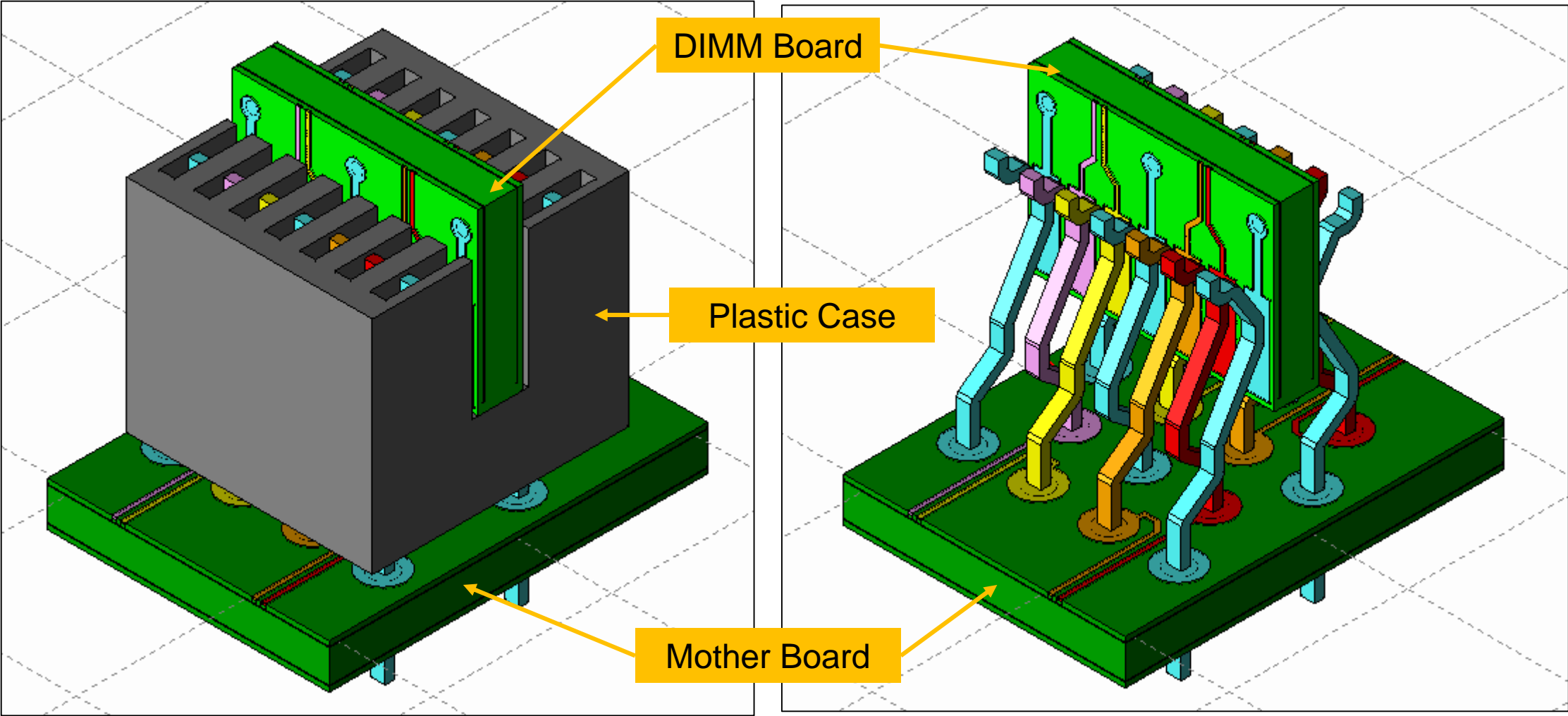


PCIe 8Gbps or SAS 12Gbps Correlation



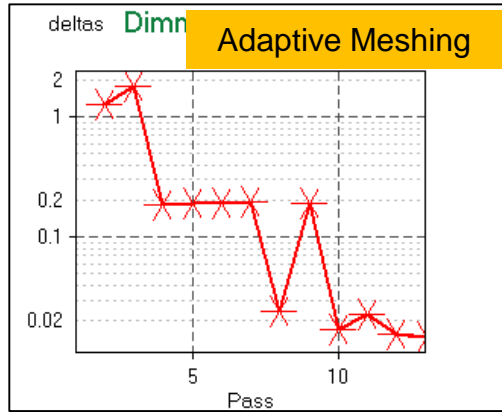
DIMM Connector plus Boards

Geometry



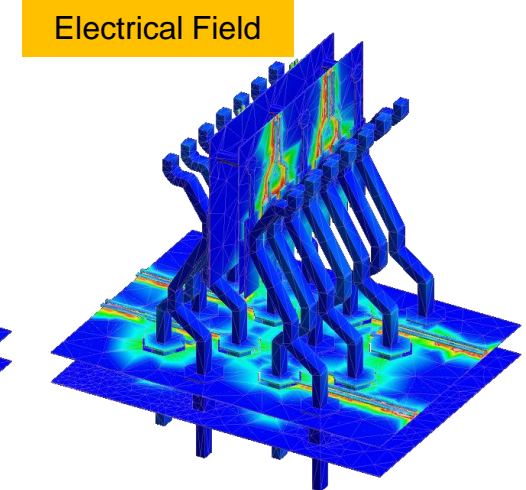
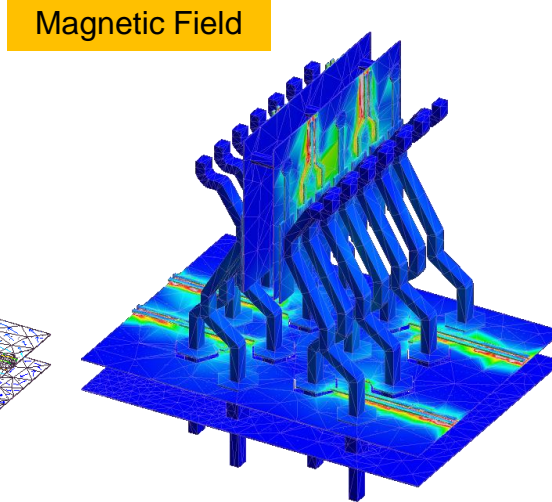
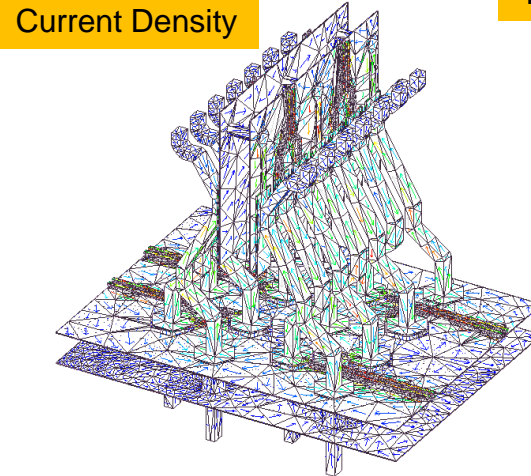
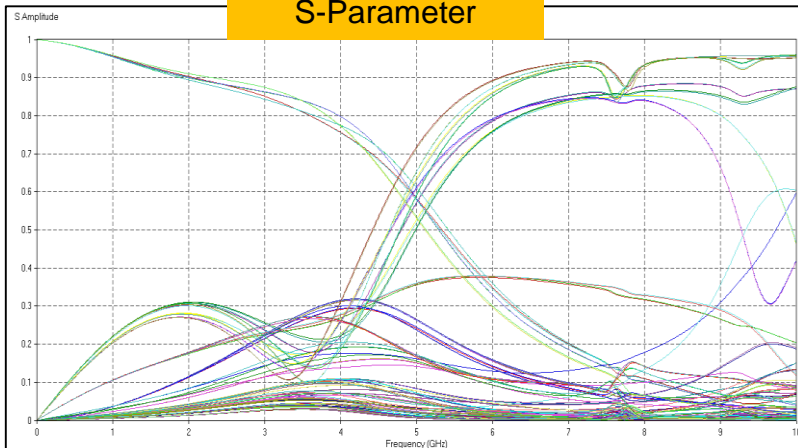
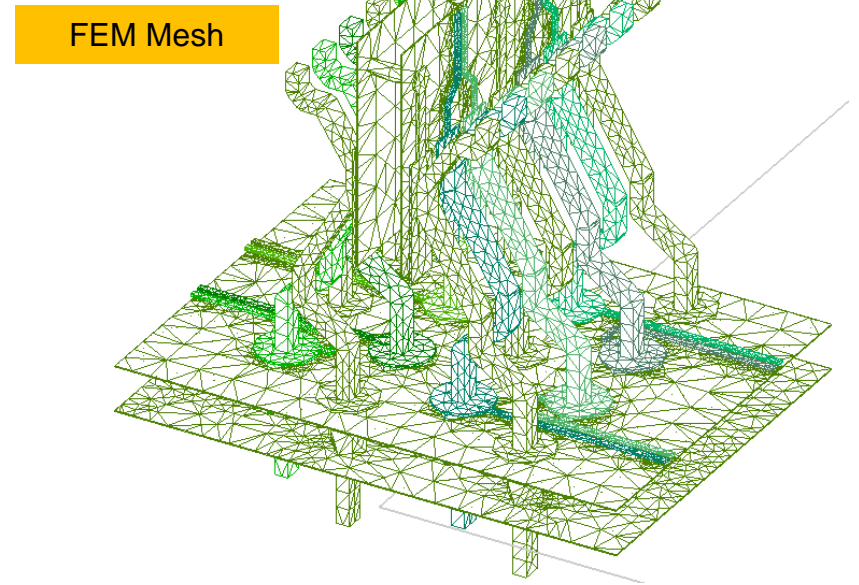
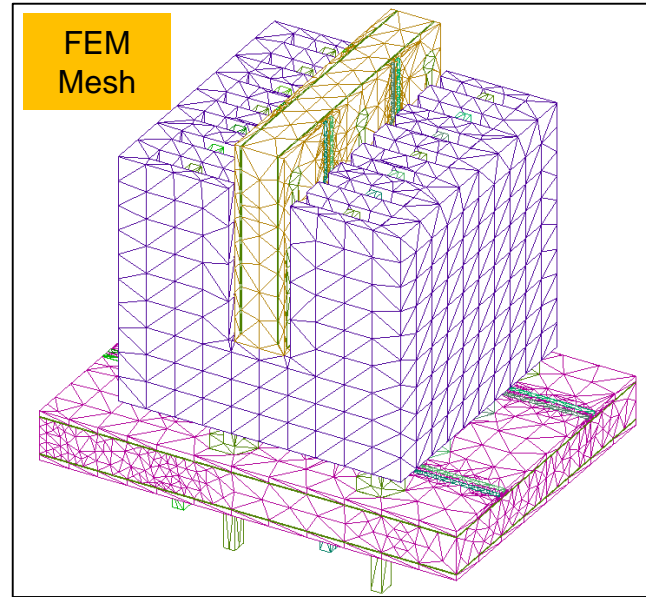
DIMM Connector plus Boards

Results and performance

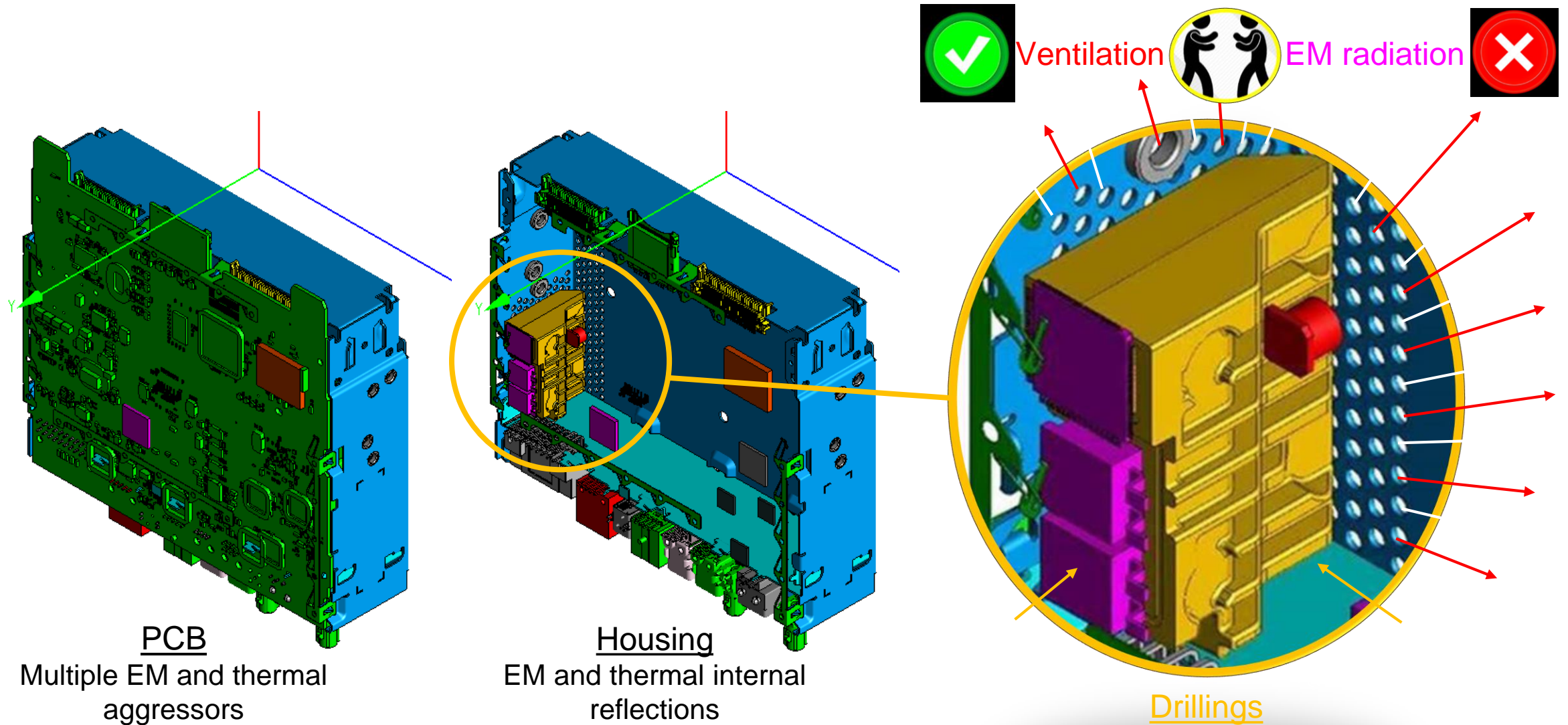


- Lenovo T560
- 31 min 6 sec
- 13.35 GB peak memory

Performance



EMI/Thermal Co-Design of an ECU Design

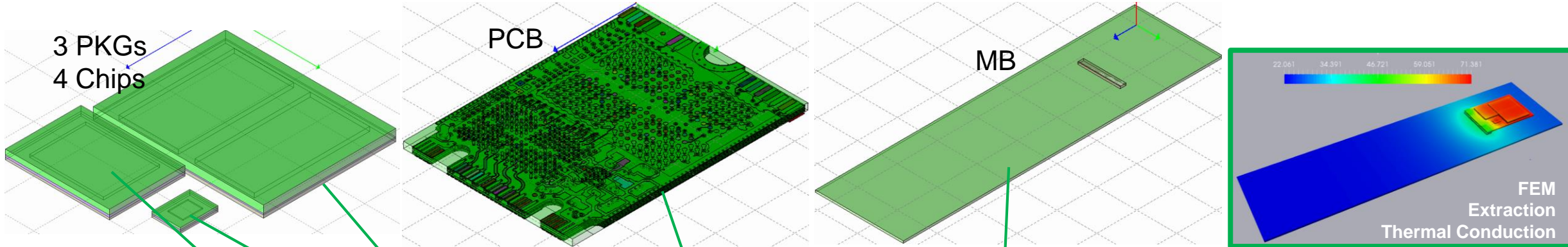


Outline

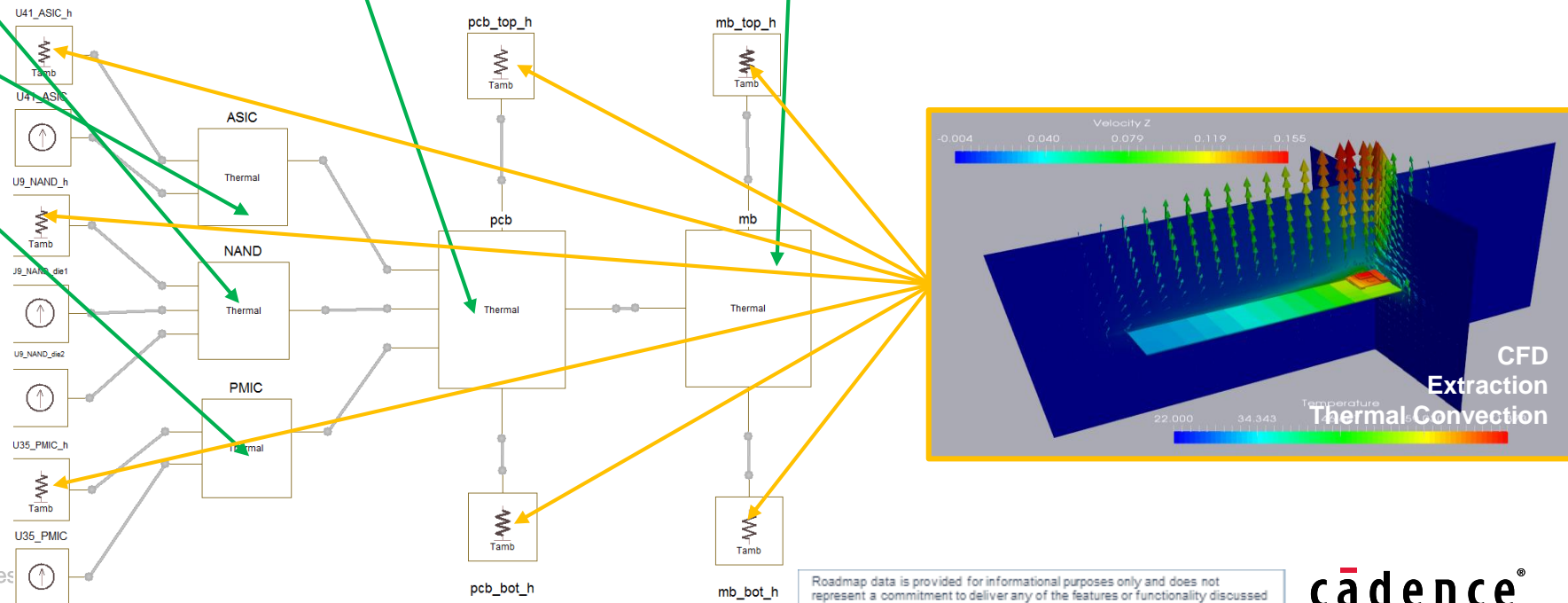
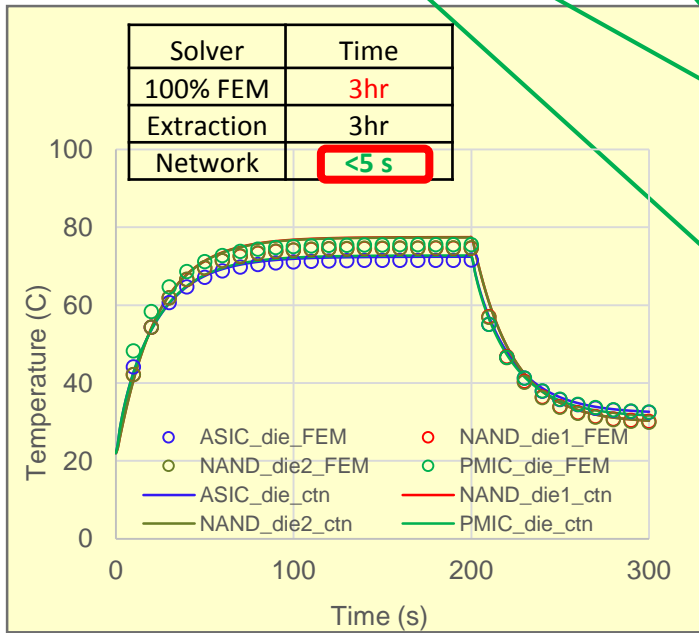
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- Tight Integration of Design/Simulation Tools

System-Level Transient Thermal

- Extract thermal models of three PKGs, PCB, and motherboard



- Assemble and run a network (3 PKGs + PCB + MB)



A Joint Paper with TI Presented in the 33rd Semi-Therm (March, 2017)

System-Level Electro-Thermal Analysis of $R_{DS(ON)}$ for Power MOSFET

Rajen Murugan¹, Nathan Ai², and C.T. Kao²

Texas Instruments, Inc. Dallas, Texas, 75044, USA

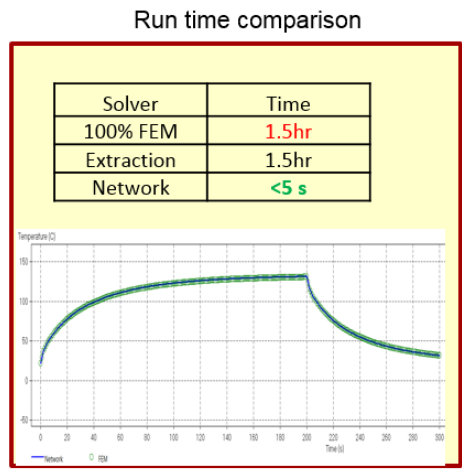
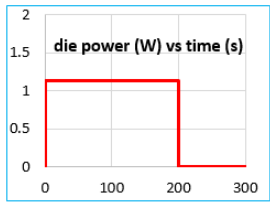
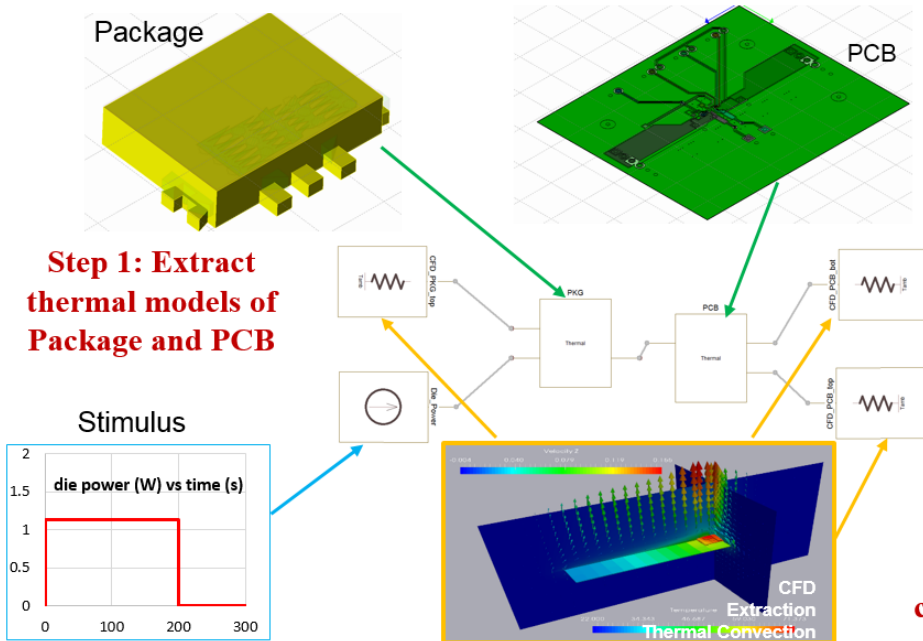
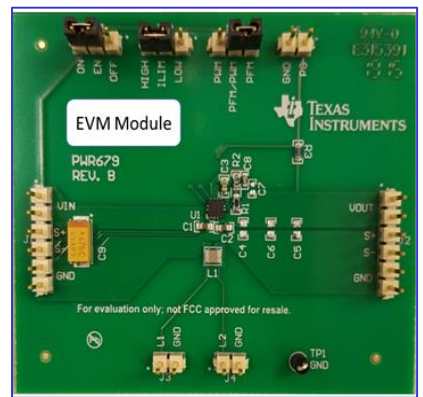
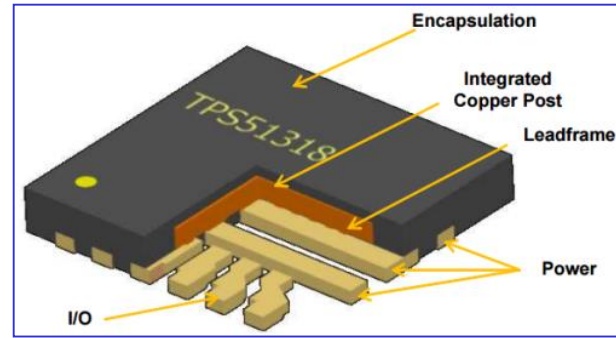
² Cadence Design Systems, Santa Clara, California, USA

*r-murugan@ti.com, +1 214-567-6377



Abstract

A coupled-electro-thermal $R_{DS(ON)}$ (drain to source ON resistance) co-analysis methodology for Power MOSFET is proposed. The methodology contains two functional modules: 1) physical field solvers and 2) equivalent circuit/network solver. The field solver resolves the electrical and thermal field variables by the conventional 3D finite-element method, while the network solver can achieve accurate and efficient results by connecting the equivalent electrical, thermal and flow circuits that are extracted from the system through advanced numerical computational schemes. The integrated equivalent network can then be solved by a generic circuit solver for steady state and transient responses. The methodology is demonstrated, via simulation and measurement, on a 2.5MHz DCDC buck-boost converter. Good correlation between co-analysis methodology and laboratory measurements is achieved.



Step 2: Assemble and run the combined system thermal network

Thermal Innovation: Thermal Model

Modularized, reusable, two orders of magnitude faster

Notebook Computer

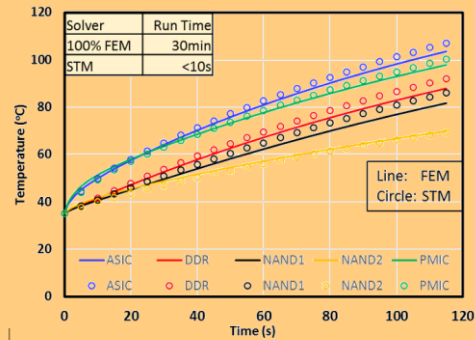
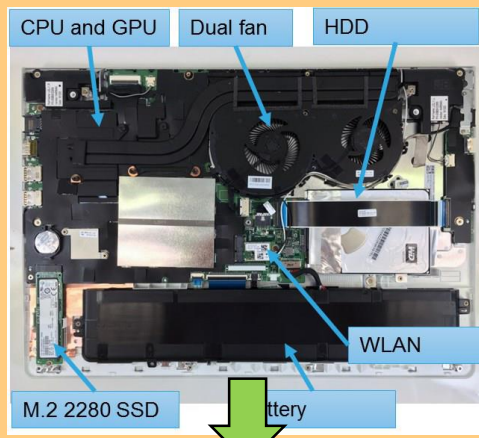
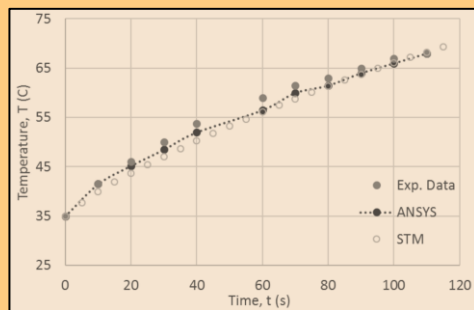
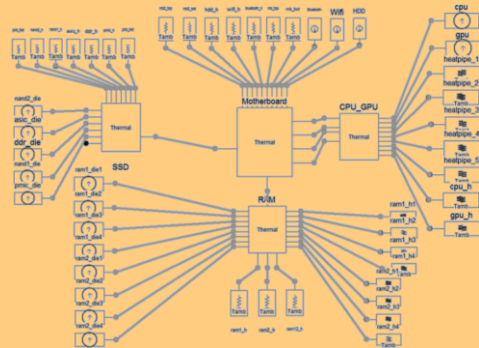


Fig. 11 Transient temperature trends of key SSD components: comparison of network thermal model vs FEM solutions



Server Box

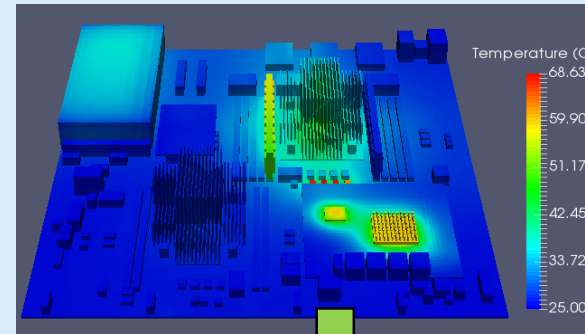
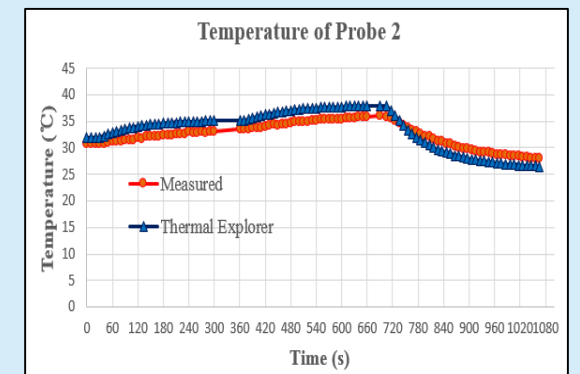
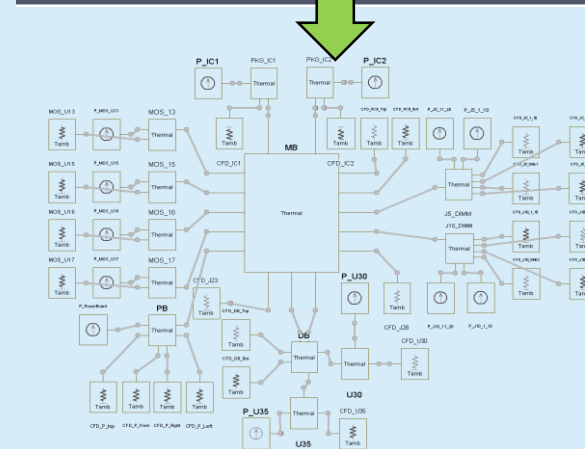
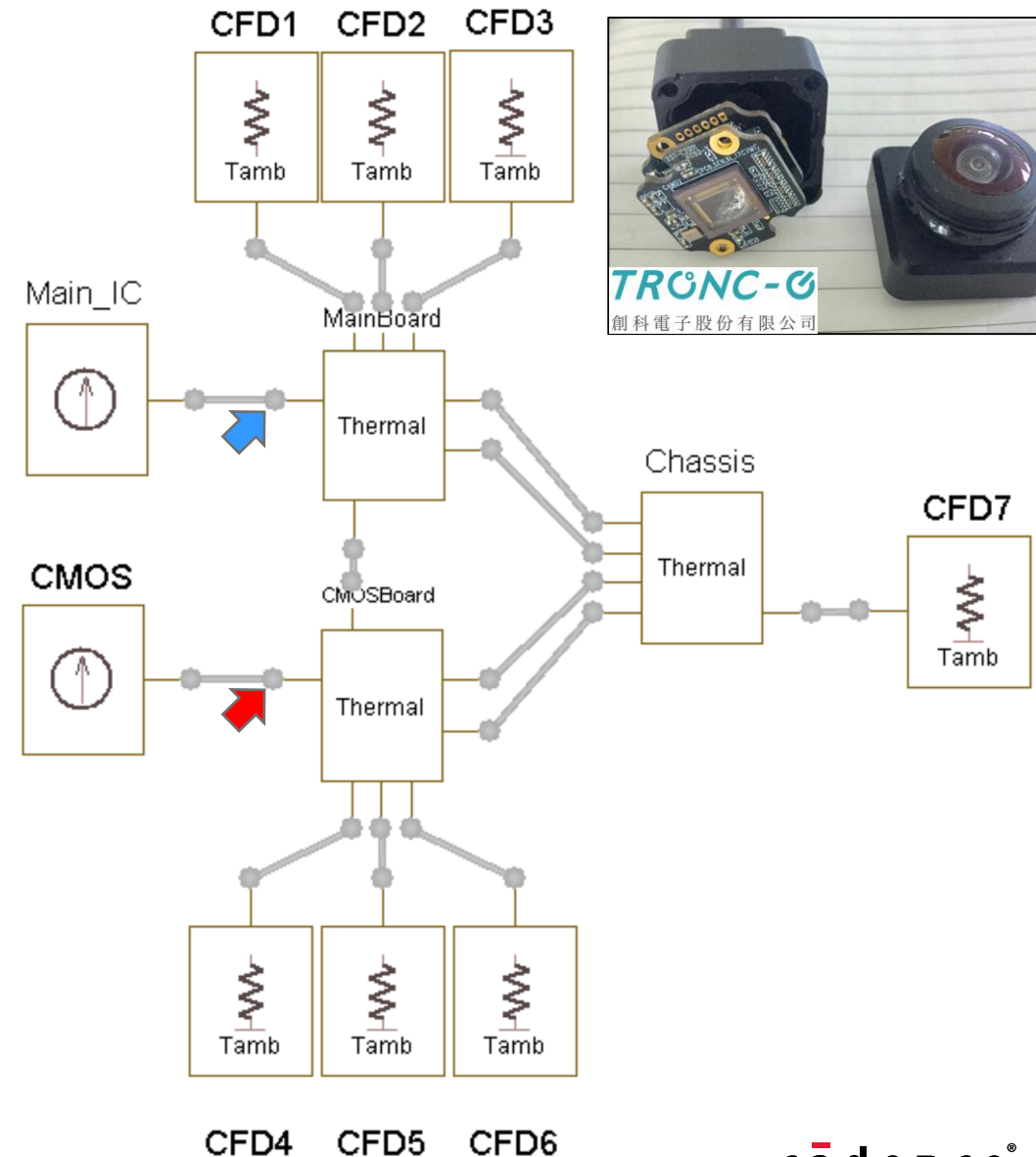
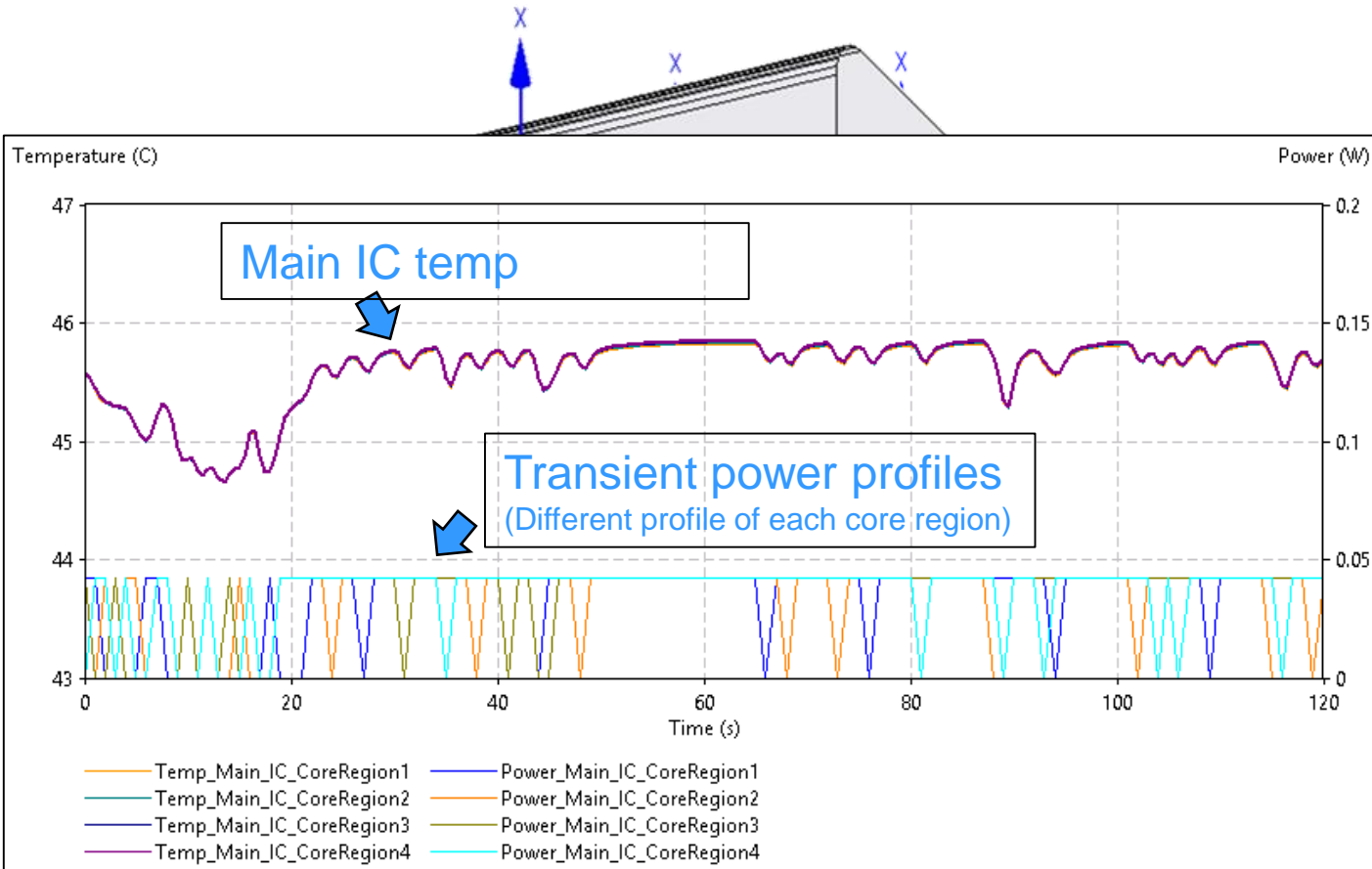
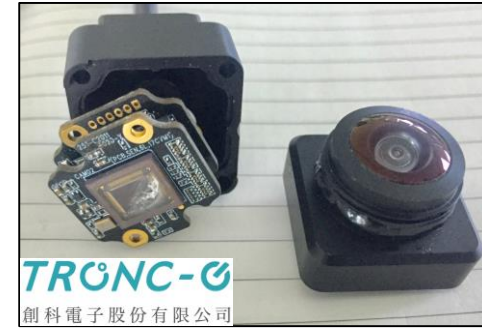


Table 6: Measured and thermal model simulated temperature of different power dissipation.

Temp	P1-31W	P2-41.8W	P3-64.5W	P4-82.4W
Probe1				
Measurement	35.02 °C	39.10 °C	46.86 °C	53.00 °C
Thermal Model	36.40 °C	40.39 °C	47.94 °C	54.31 °C
ΔT_Probe1	-1.38 °C	-1.29 °C	-1.08 °C	-1.31 °C
Probe2				
Measurement	30.60 °C	30.70 °C	34.55 °C	35.75 °C
Thermal Model	30.11 °C	31.74 °C	35.18 °C	37.89 °C
ΔT_Probe2	0.49 °C	-1.04 °C	-0.63 °C	-2.14 °C



Thermal Simulation of a Camera Module (TRONC-E)

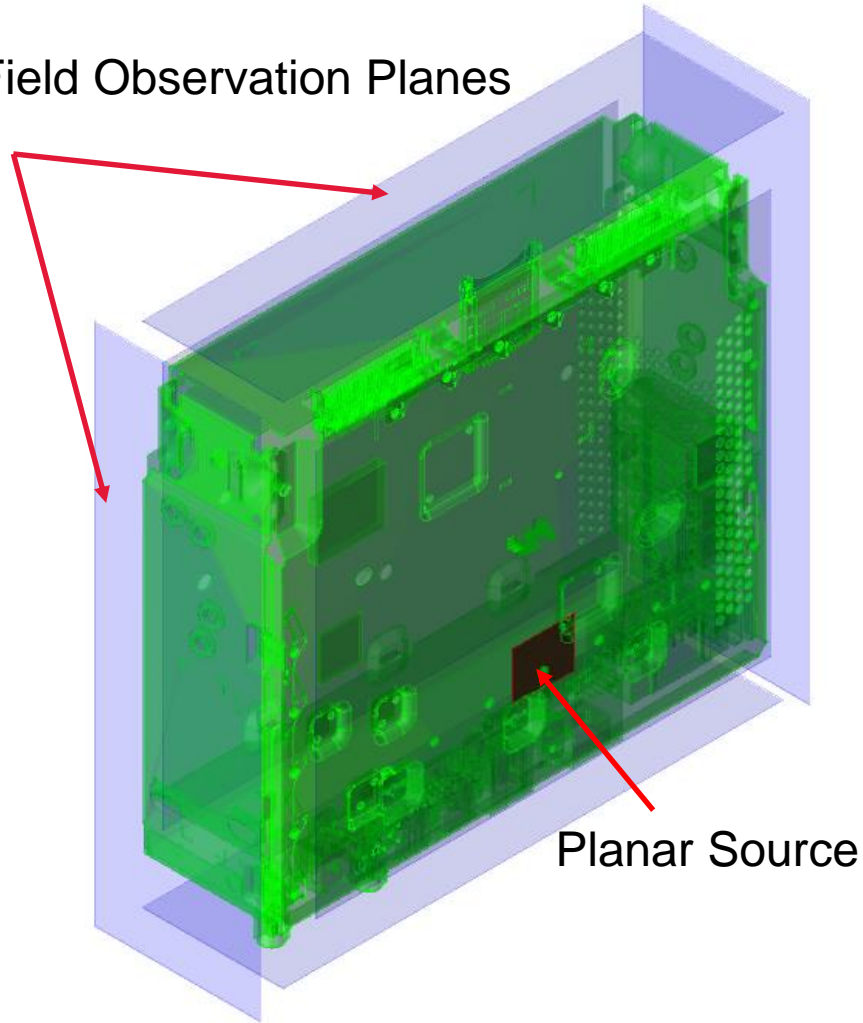


Outline

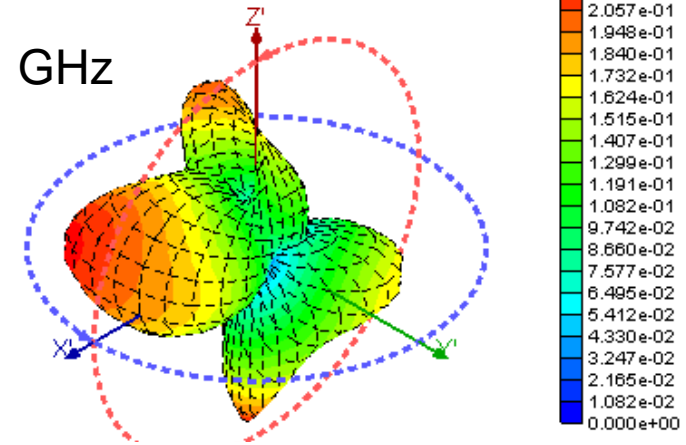
- System Design Enablement
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Housing with Red Plane Source (Far Field)

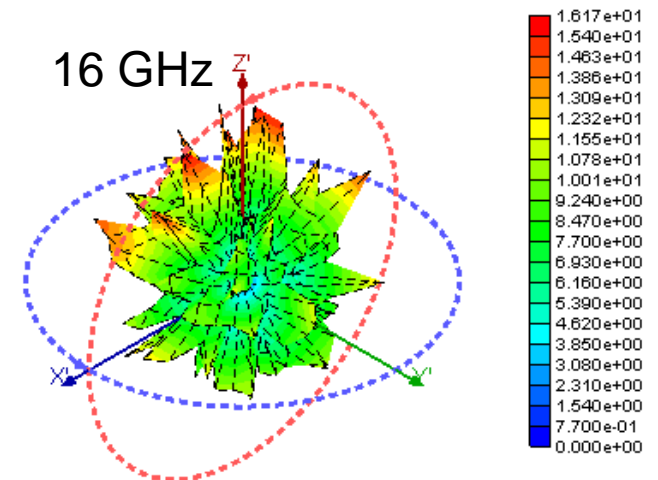
Six Near-Field Observation Planes



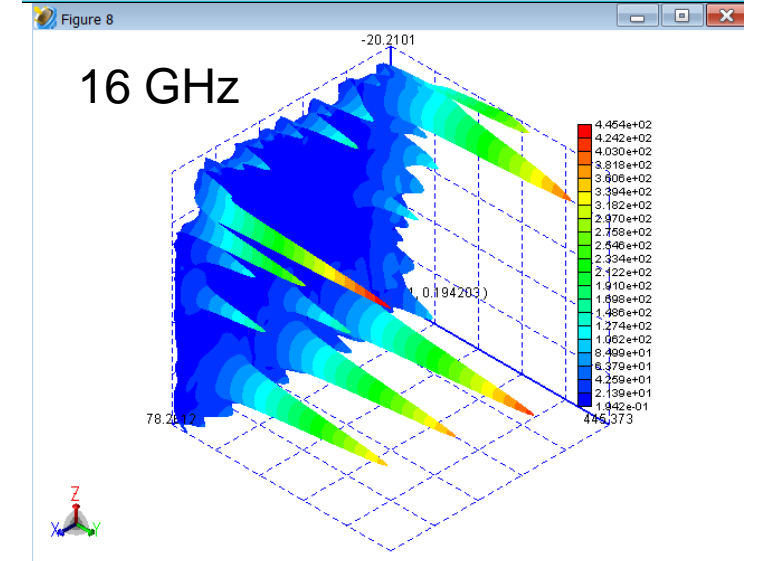
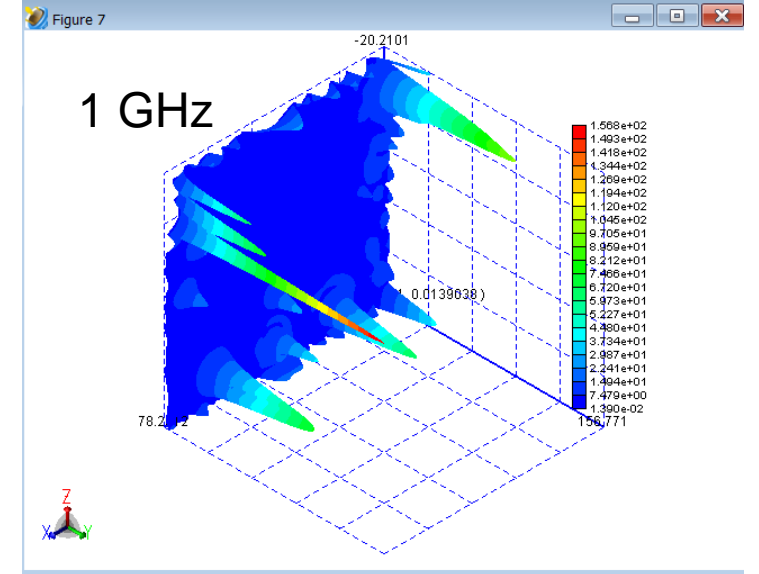
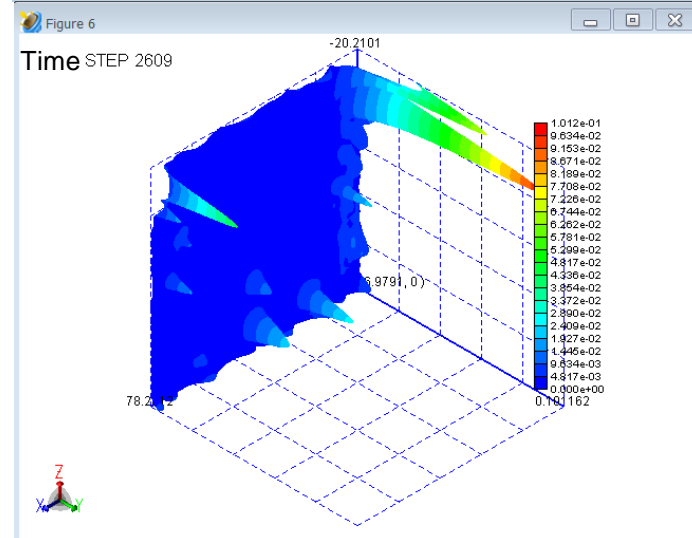
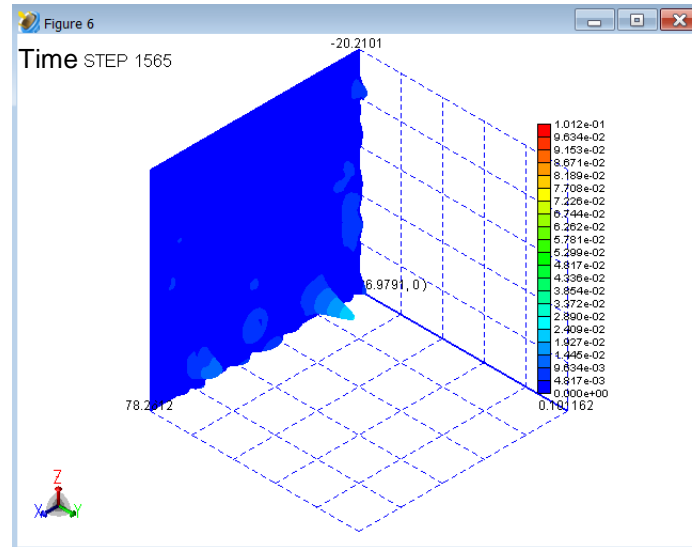
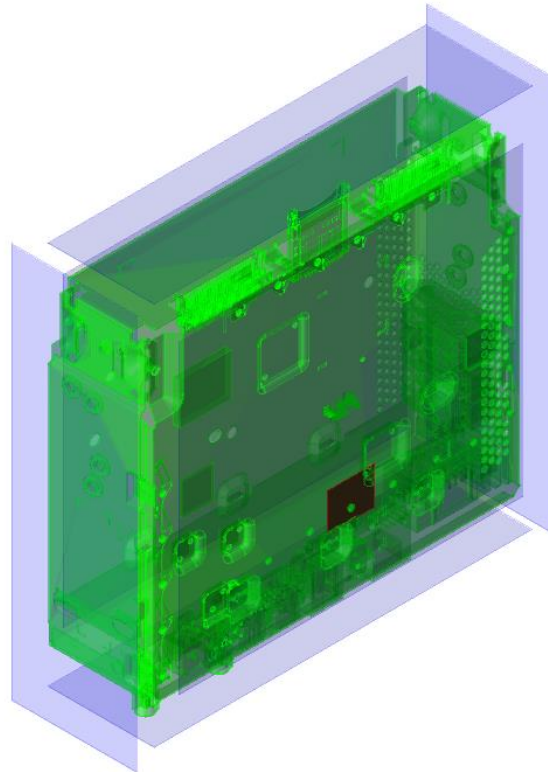
1 GHz



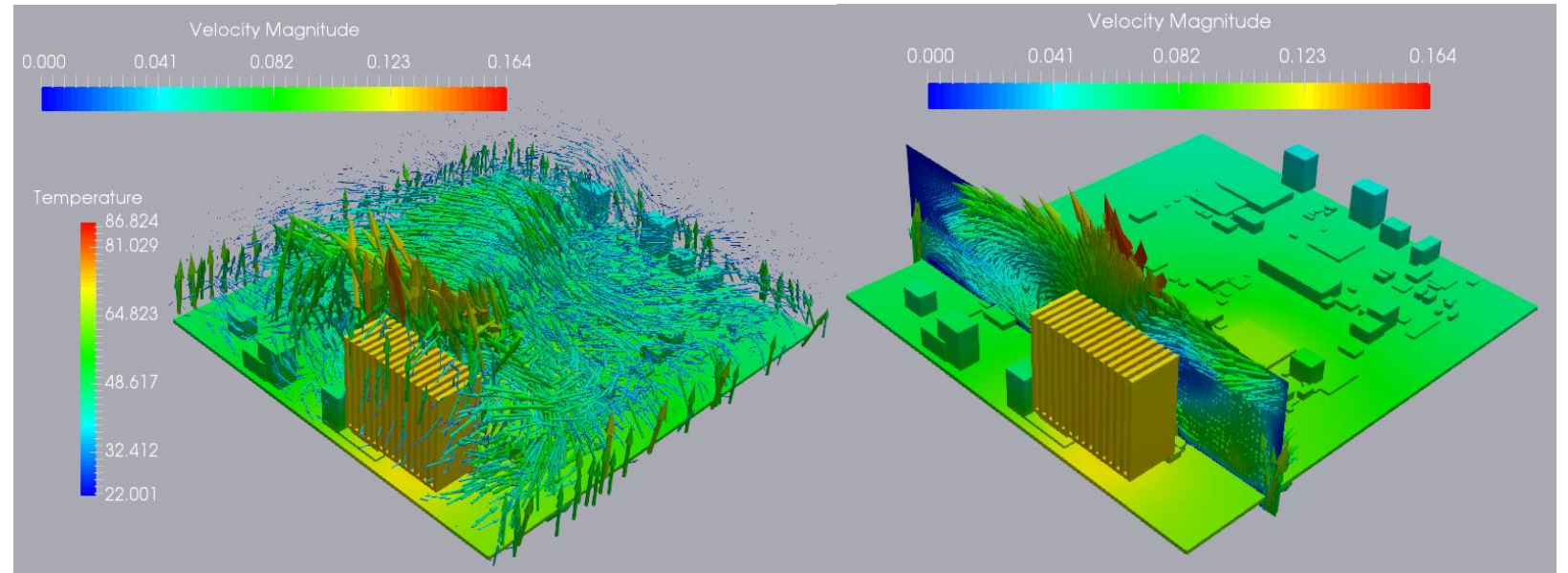
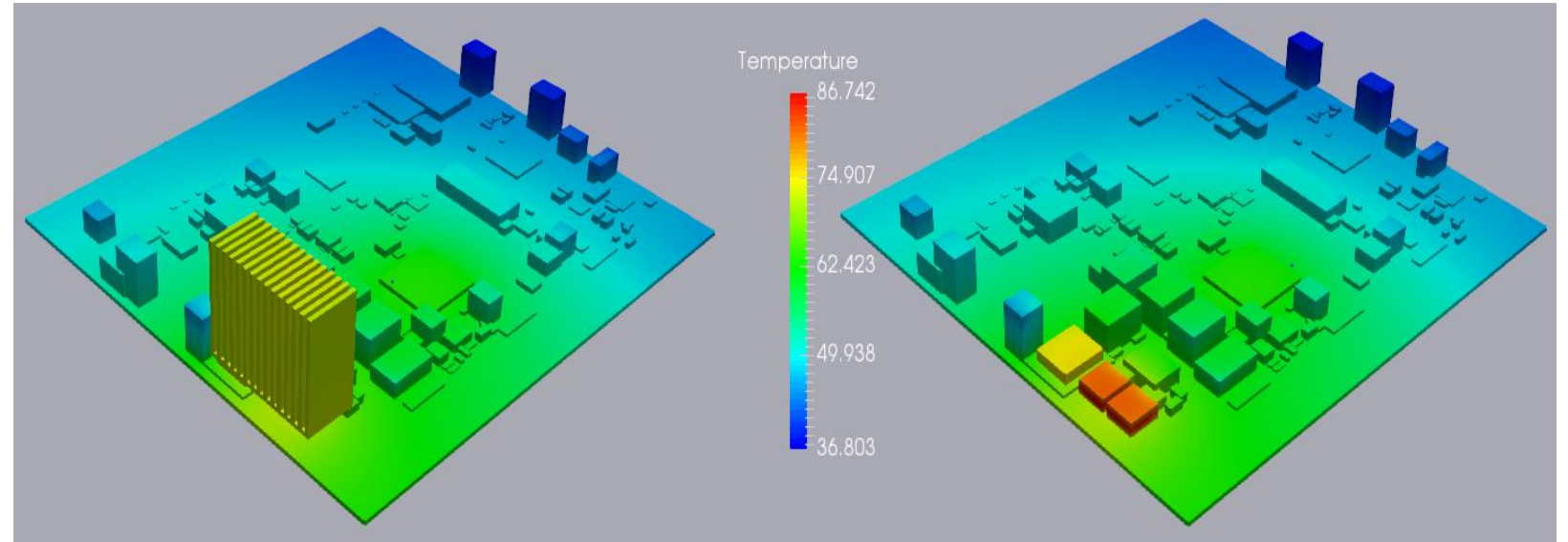
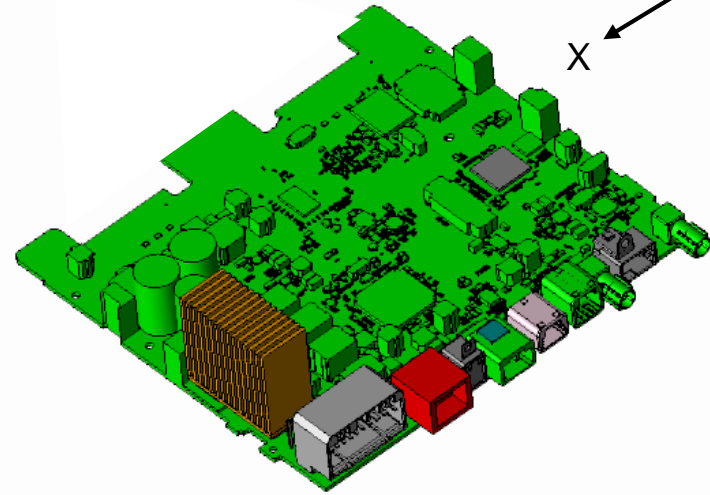
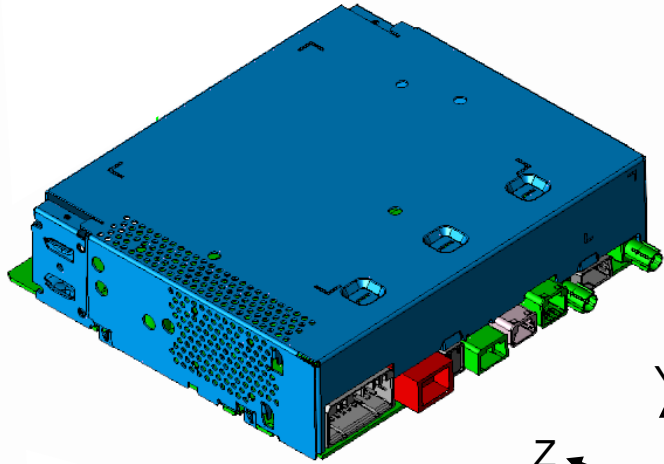
16 GHz



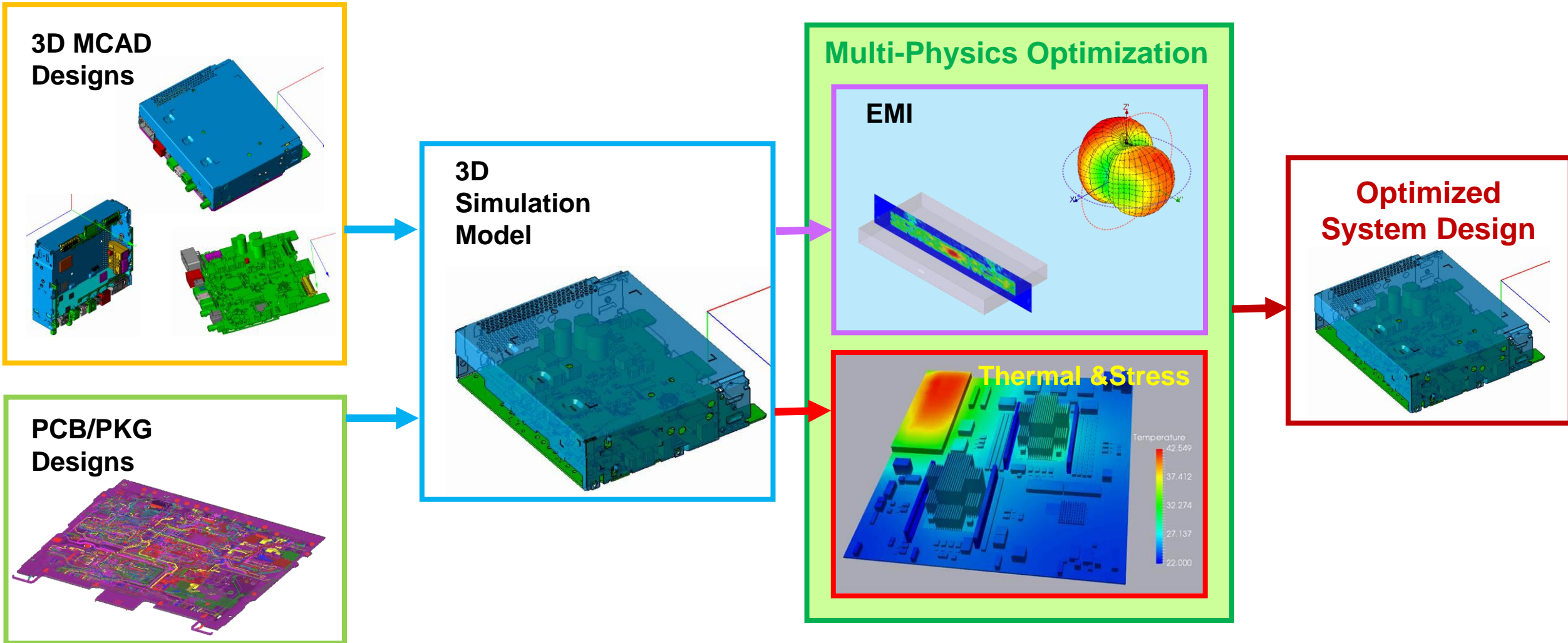
Near-Field Radiation at the XZ Back Plane



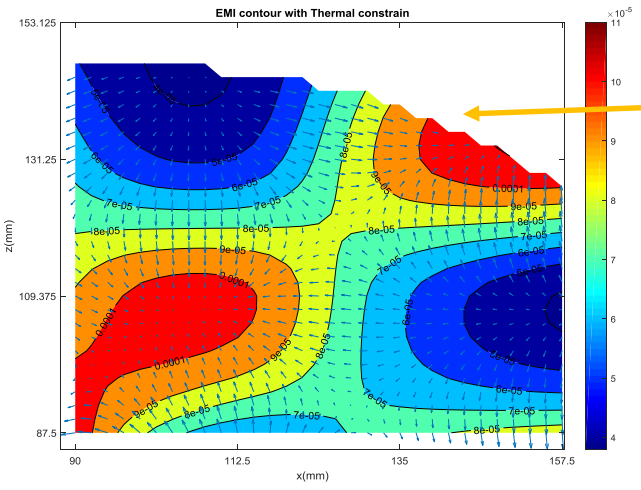
Thermal Simulation of ECU



Complete System Thermal and EMI Optimization Flow

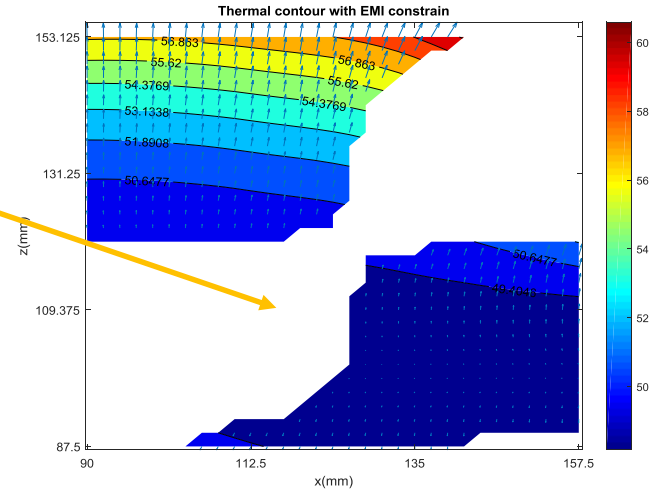


EMI and Thermal Optimization Example

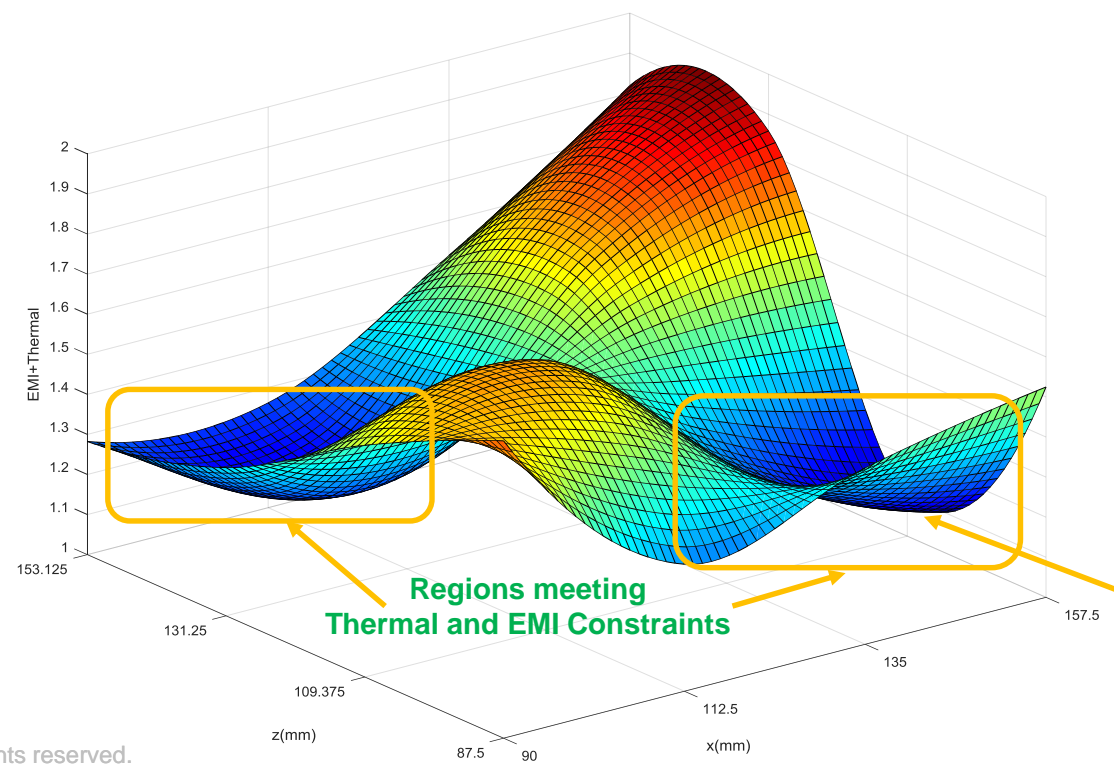


Bad Thermal Region

Bad EMI Region



Normalized Thermal + Normalized EMI



Regions meeting Thermal and EMI Constraints

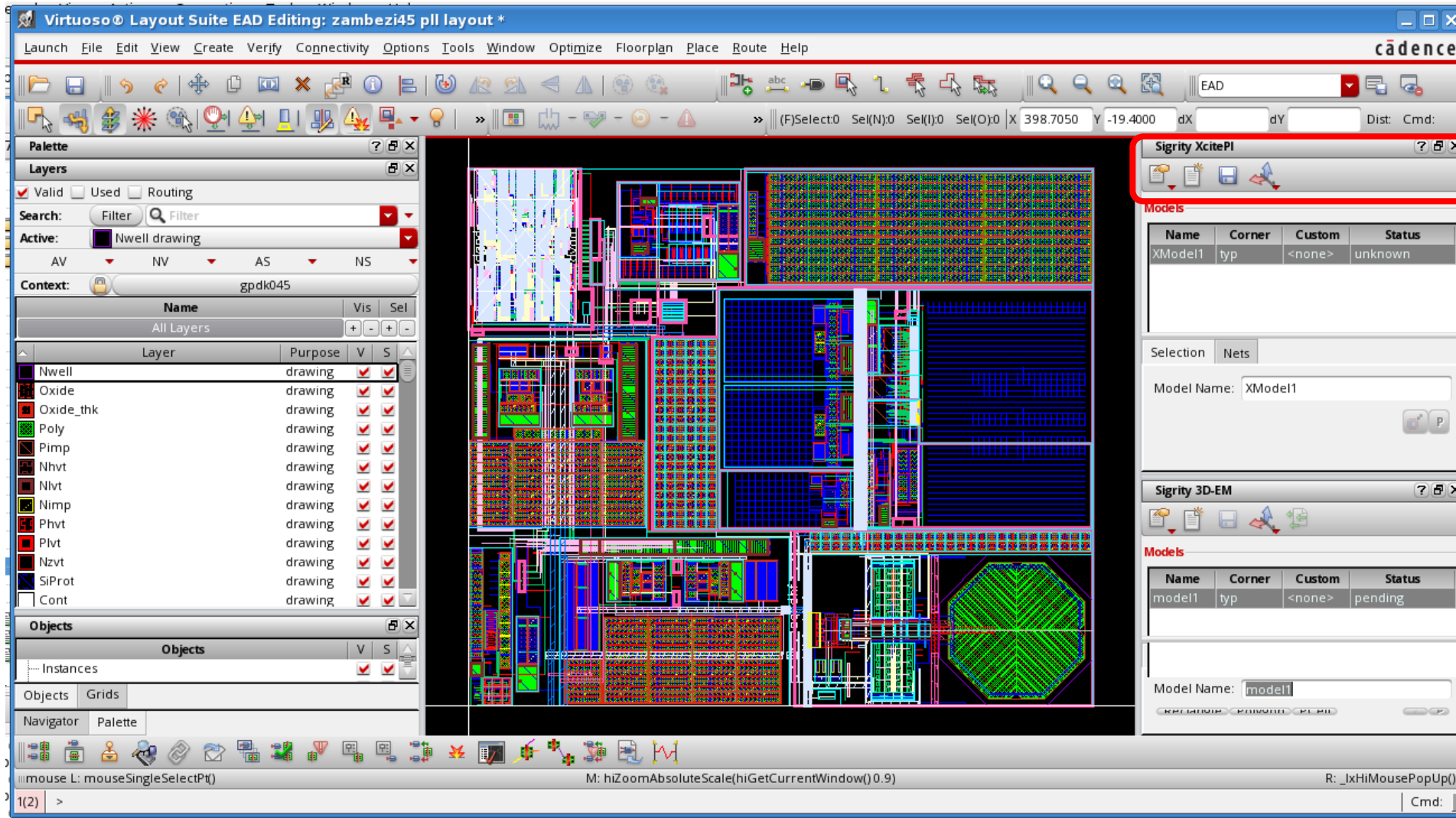
Optimum Thermal and EMI position

Outline

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Sigrity EM/SI/PI Solvers Inside Virtuoso Layout Suite EAD

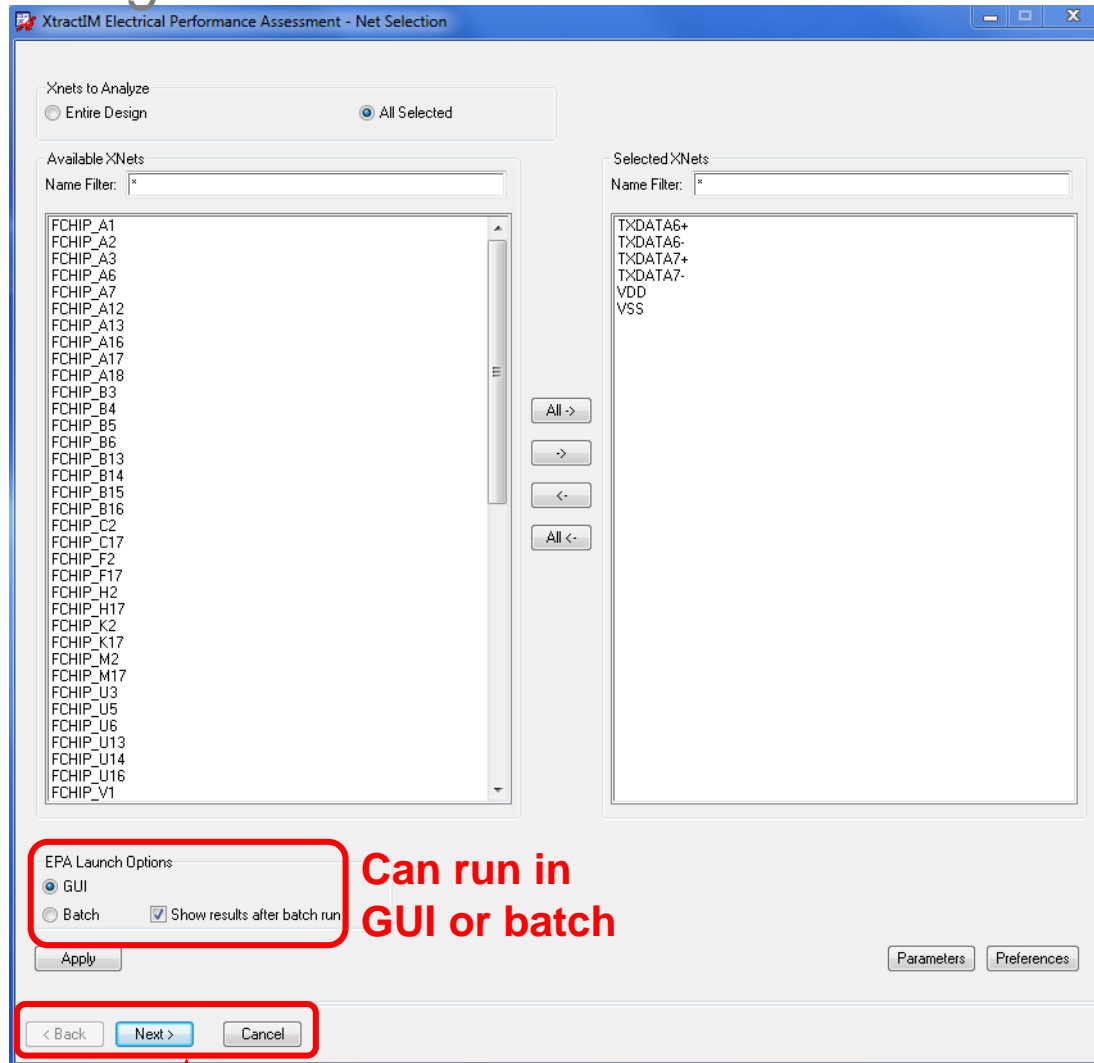
Chip-Level Integration



Sigrity XtractIM Inside Allegro Package Designer/Cadence SiP Layout

Package extraction and assessment

Package-Level Integration

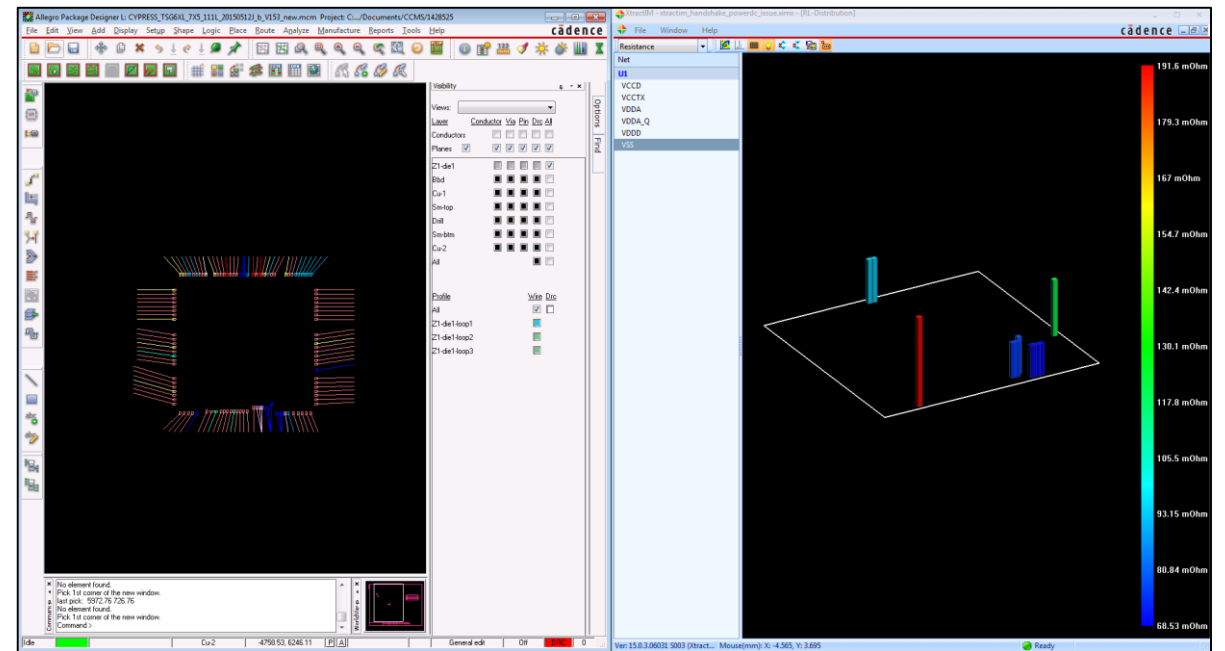


Can run in GUI or batch

Step-by-step Sigrity™ XtractIM™ technology setup wizard inside Cadence® SiP Layout



Access to 4 solvers

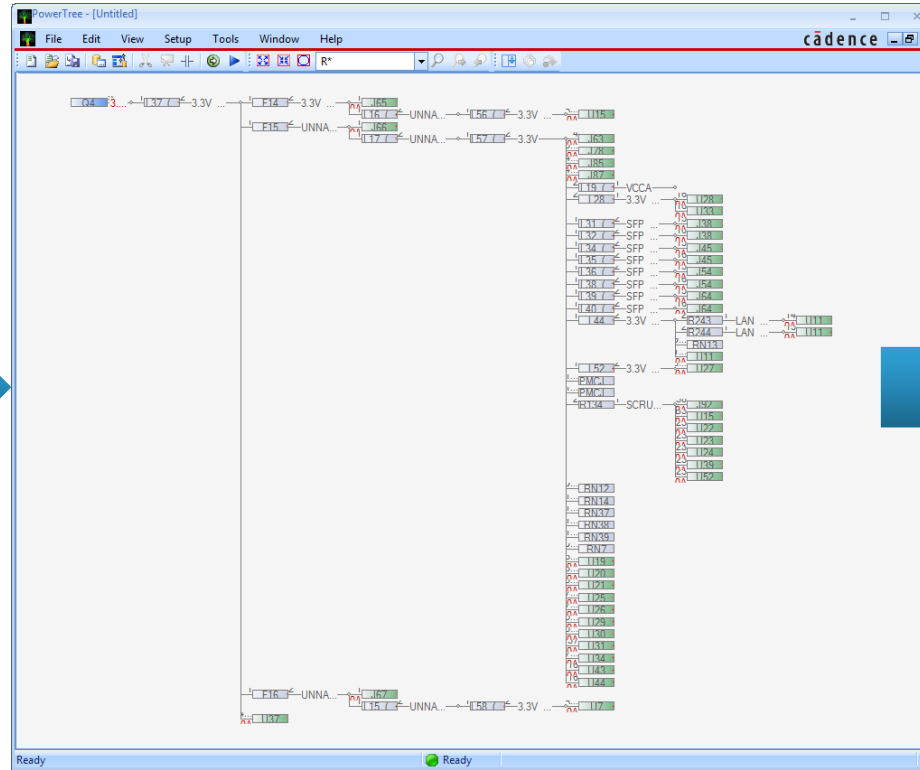


Allegro PowerTree Technology for PI Analysis Automation

Connection between Allegro/OrCAD schematic and Sigrity PowerDC/OptimizePI technology

Allegro® netlist data

AMM library data



Simulation setup
for Sigrity™
PowerDC™ or
Sigrity
OptimizePI™
technologies

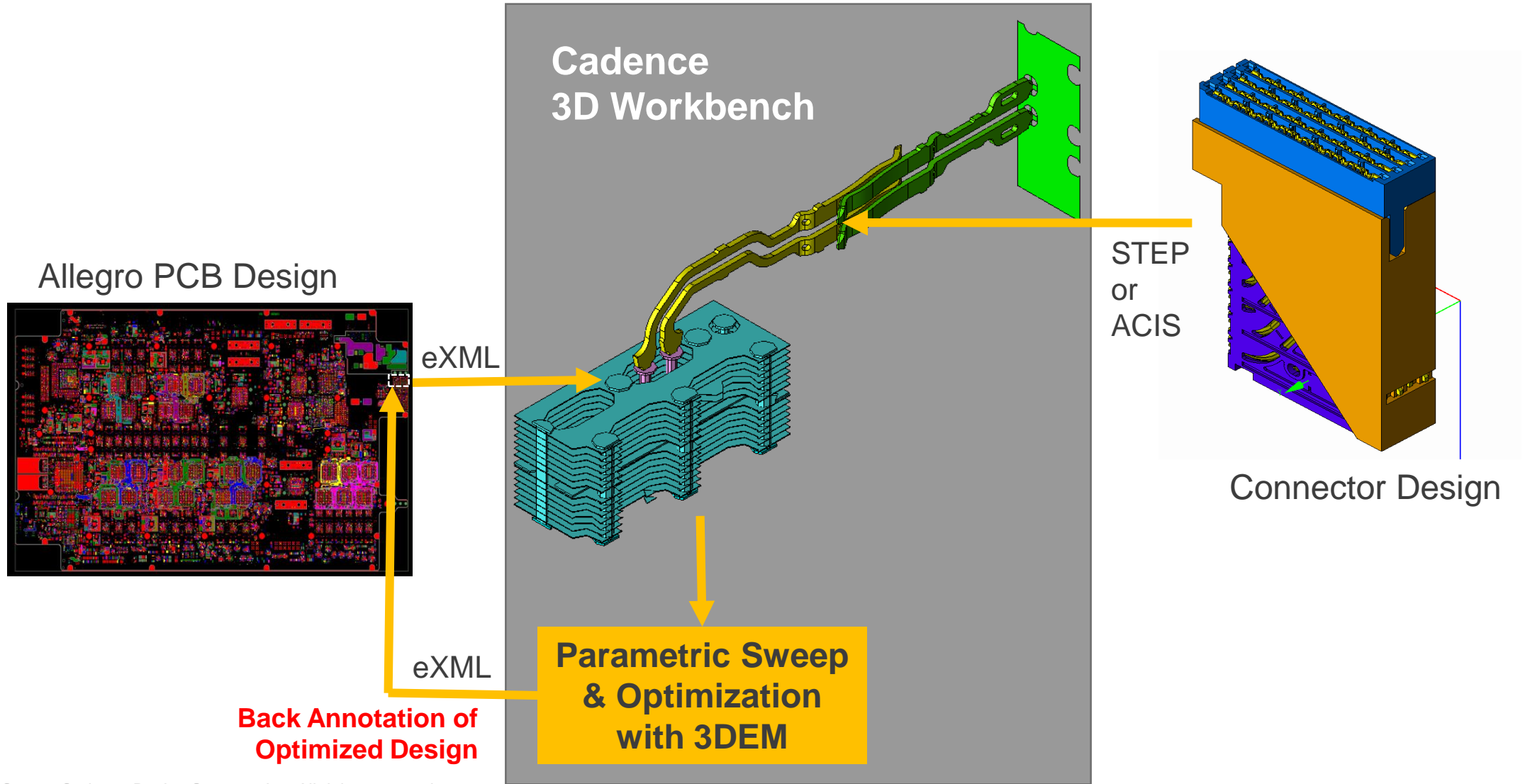
Settings for reuse

Allegro PowerTree™ Technology creates and edits schematics of PDN

High-Speed Structure Optimization (HSSO) Flow

Cadence Palladium Board and Amphenol Connector

PCB-Level
Integration

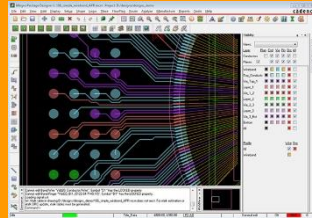


System Design Enablement

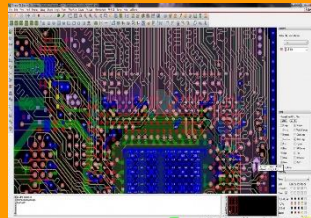
The Cadence Advantage

Tightly Integrated

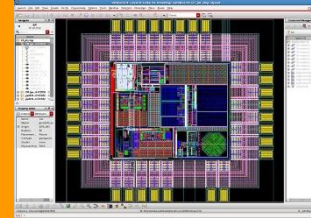
Allegro® Technology



Allegro Package Designer/Cadence® SiP



Virtuoso® Technology



Voltus™ Technology

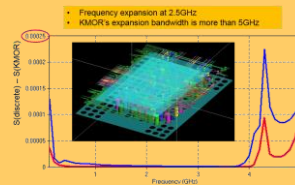


Quantus™ Technology

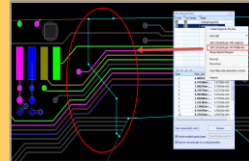


Innovative

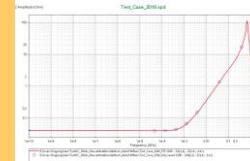
Fast KMOR Frequency Expansion



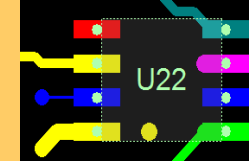
Cut-and-Stitch for Long Nets



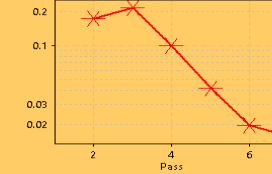
Low Frequency Solution Stability



Co-Sim of EM and Multi-Node Circuit

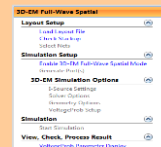


Adaptive Meshing for Accuracy

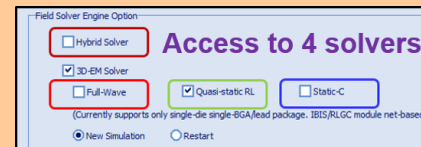


User Friendly

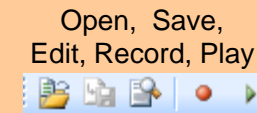
User Configurable Workflow



All Solvers in One Canvas

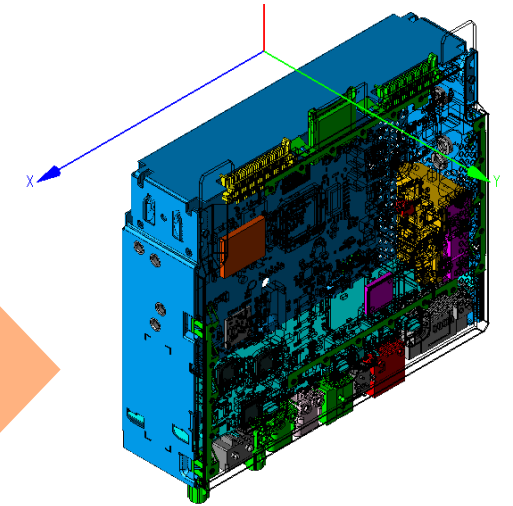
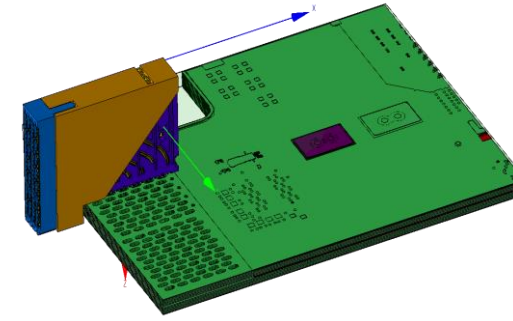


TCL Commands for Automated Batch Runs



Outline

- System Design Enablement
- Integrated ECAD/MCAD for System Design Optimization
- Multi-Physics Co-Simulation
 - Novel System-Level Thermal Solution
 - Efficient and Accurate System Level-Level EMI Solution
- Tight Integration of Design/Simulation Tools



*Thank
You*



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